Semiconductors for Telecom Systems

DATA HANDBOOK

BOOK IC03 1993

Philips Semiconductors

PHILIPS

QUALITY ASSURED

Our quality system focuses on the continuing high quality of our components and the best possible service for our customers. We have a three-sided quality strategy: we apply a system of total quality control and assurance; we operate customer-oriented dynamic improvement programmes; and we promote a partnering relationship with our customers and suppliers.

PRODUCT SAFETY

In striving for state-of-the-art perfection, we continuously improve components and processes with respect to environmental demands. Our components offer no hazard to the environment in normal use when operated or stored within the limits specified in the data sheet.

Some components unavoidably contain substances that, if exposed by accident or misuse, are potentially hazardous to health. Users of these components are informed of the danger by warning notices in the data sheets supporting the components. Where necessary the warning notices also indicate safety precautions to be taken and disposal instructions to be followed. Obviously users of these components, in general the set-making industry, assume responsibility towards the consumer with respect to safety matters and environmental demands.

All used or obsolete components should be disposed of according to the regulations applying at the disposal location. Depending on the location, electronic components are considered to be 'chemical', 'special' or sometimes 'industrial' waste. Disposal as domestic waste is usually not permitted.

Semiconductors for Telecom systems

Contents

Semiconductors for Telecom systems — Contents

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

SELECTION GUIDE

Semiconductors for Telecom systems — Functional index

General

For further information, refer to Data Handbook SC14, 1993; "RF Wideband Transistors", except otherwise specified.

RF wideband transistors

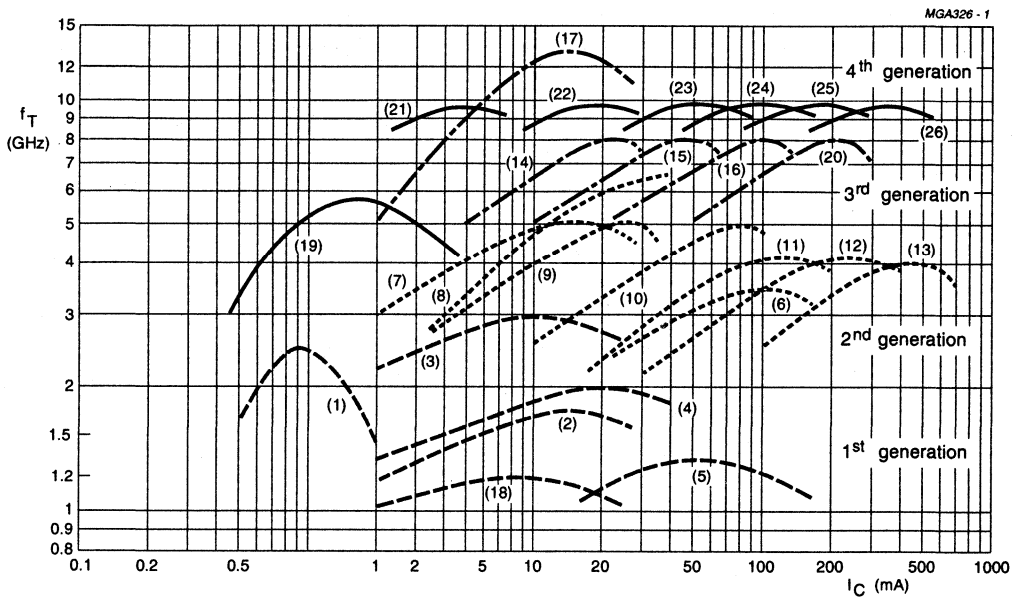


Fig.1 Transition frequency (f_T) characteristics as a function of collector current (I_C) for the four generations of RF bipolar wideband transistors.

Table 1 First generation npn wideband transistors (f_T up to 3.5 GHz).

ENVELOPE		TRANSITION FREQUENCY (f_T) CHARACTERISTICS numbers in parenthesis refer to curve profiles detailed in Fig.1						
		(1)	(2)	(3)	(4)	(5)	(6)	(18)
METAL CAN	SOT5 (TO-39)					BFW16A BFW17A	BFR95	
	TO-72		BFY90		BFW30			
PLASTIC	SOT54 (TO-92)		BF689K BF763					BF748
	SOT37	BFT24	BFW92	BFW92A	BFW93			
CERAMIC	SOT122						BFR94A	
SURFACE MOUNTED	SOT23	BFT25	BFS17	BFS17A	BFR53			BF547 BF747
	SOT89					BFQ17		
	SOT143			BFG17A				
	SOT223					BFG16A		
	SOT323		BFS17W					BF547W BF747W

Table 2 Second generation npn wideband transistors (f_T up to 6 GHz).

ENVELOPE		TRANSITION FREQUENCY (f_T) CHARACTERISTICS numbers in parenthesis refer to curve profiles detailed in Fig.1					
		(7)	(8)	(10)	(11)	(12)	(13)
METAL CAN	TO-72	BFQ53	BFQ22S	BFQ63			
PLASTIC	SOT37	BFR90 BFR90A	BFR91 BFR91A	BFR96 BFR96S	BFQ34T		
	SOT103	BFG90A	BFG91A	BFG96	BFG34		
CERAMIC	SOT122				BFQ34	BFQ68	BFQ136
	SOT173 SOT173X	BFP90A	BFP91A	BFP96			
SURFACE MOUNTED	SOT23	BFR92 BFR92A	BFR93 BFR93A	BFR106			
	SOT89			BFQ19	BFQ18A		
	SOT143 SOT143R	BFG92A BFG92A/X BFG92A/XR	BFG93A BFG93A/X BFG93A/XR				
	SOT223		BFG94	BFG97	BFG35		
	SOT323	BFR92AW	BFR93AW				

Table 3 Second generation pnp wideband transistors (f_T up to 6 GHz).

ENVELOPE		TRANSITION FREQUENCY (f_T) CHARACTERISTICS numbers in parenthesis refer to curve profiles detailed in Fig.1				
		(7)	(9)	(10)	(11)	(12)
METAL CAN	TO-72	BFQ52	BFQ24	BFQ32M		
PLASTIC	SOT37	BFQ51	BFQ23	BFQ32 BFQ32S	BFQ54T	
	SOT103			BFG32		
CERAMIC	SOT122					BFQ108
	SOT173 SOT173X		BFQ23C	BFQ32C		
SURFACE MOUNTED	SOT23	BFT92	BFT93			
	SOT89			BFQ149		
	SOT223			BFG31	BFG55	
	SOT323	BFT92AW	BFT93AW			

Table 4 Third generation npn wideband transistors (f_T up to 8 GHz).

ENVELOPE		TRANSITION FREQUENCY (f_T) CHARACTERISTICS numbers in parenthesis refer to curve profiles detailed in Fig.1				
		(14)	(15)	(16)	(17)	(20)
PLASTIC	SOT37	BFQ65		BFR134		
	SOT103	BFG65	BFG195	BFG134		
CERAMIC	SOT172			BFQ135		BFQ270
	SOT173 SOT173X	BFQ66			BFQ33C	
SURFACE MOUNTED	SOT23	BFQ67				
	SOT143 SOT143R	BFG67 BFG67/X BFG67/XR	BFG197 BFG197/X BFG197/XR		BFG33 BFG33/X BFG33/XR	
	SOT223		BFG198	BFG135		
	SOT323	BFQ67W				

Table 5 Fourth generation npn wideband transistors (f_T up to 10 GHz).

ENVELOPE		TRANSITION FREQUENCY (f_T) CHARACTERISTICS numbers in parenthesis refer to curve profiles detailed in Fig.1						
		(19)	(21)	(22)	(23)	(24)	(25)	(26)
PLASTIC	SOT103			BFR521 (note 1)	BFR541 (note 1)	BFR591 (note 1)		
CERAMIC	SOT172						BFQ621 (note 1)	BFQ741 (note 1)
	SOT173 SOT173X		BFP505 (note 1)	BFP520 (note 1)	BFP540 (note 1)			
SURFACE MOUNTED	SOT23	BFT25A	BFR505	BFR520	BFR540			
	SOT143 SOT143R	BFG25A/X	BFG505 BFG505/X BFG505/XR	BFG520 BFG520/X BFG520/XR	BFG540 BFG540/X BFG540/XR	BFG590 BFG590/X BFG590/XR		
	SOT223				BFG541	BFG591	BFG621 (note 1)	BFG741 (note 1)
	SOT323	BFS25A	BFS505	BFS520	BFS540			

Note

1. In development.

Table 6 Competitor name equivalents for surface mounted packages.

PHILIPS	MOTOROLA	NEC	TOSHIBA	SIEMENS
SOT23	318-07 (SOT23)	mini-mold (3-pin)	SM (SOT23)	SOT23
SOT103	317-01 (macro-x)	disk mold	μX (24F1C)	SOT103
SOT143	–	–	–	–
SOT143 (cross-emitter pinning)	318-A-05 (SOT143)	–	–	SOT143
SOT143R (cross-emitter pinning)	–	mini-mold (4-pin)	SMQ (SC61) (SOT143)	–
SOT173	358-01 (micro-x)	μX	–	–
SOT173X	–	–	–	CEREC-x
SOT223	318E-04 (SOT223)	–	–	SOT223
SOT323	SC70	super mini-mold (3-pin)	USM (SC70)	–

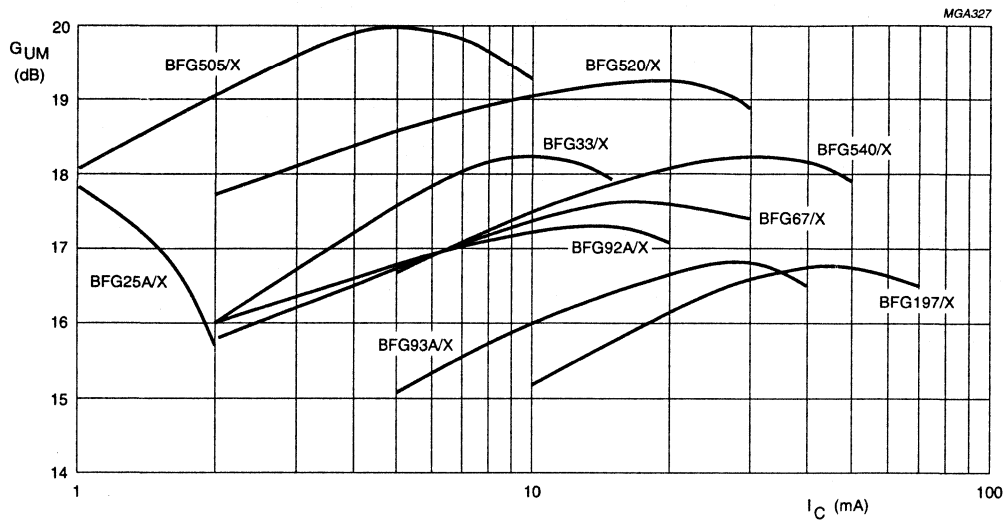
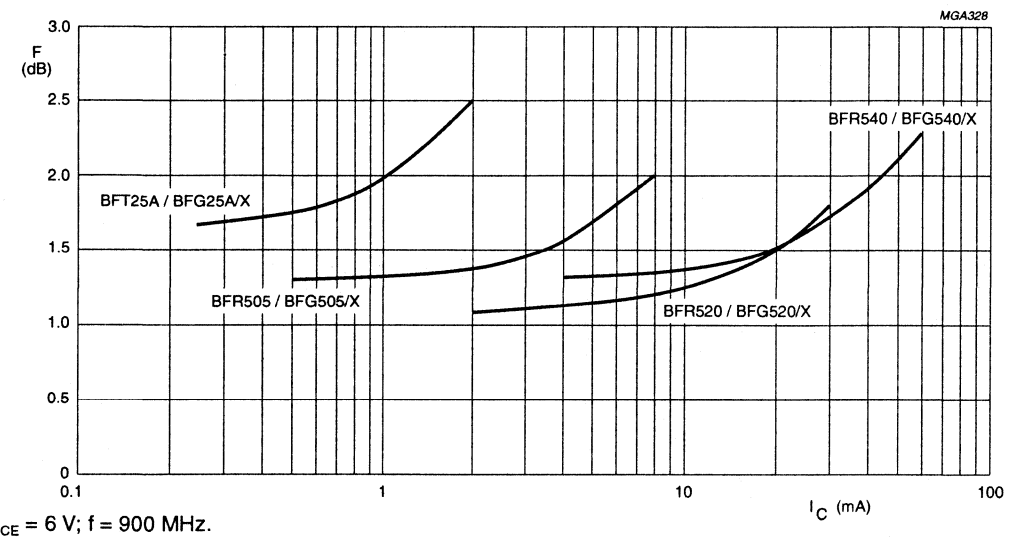
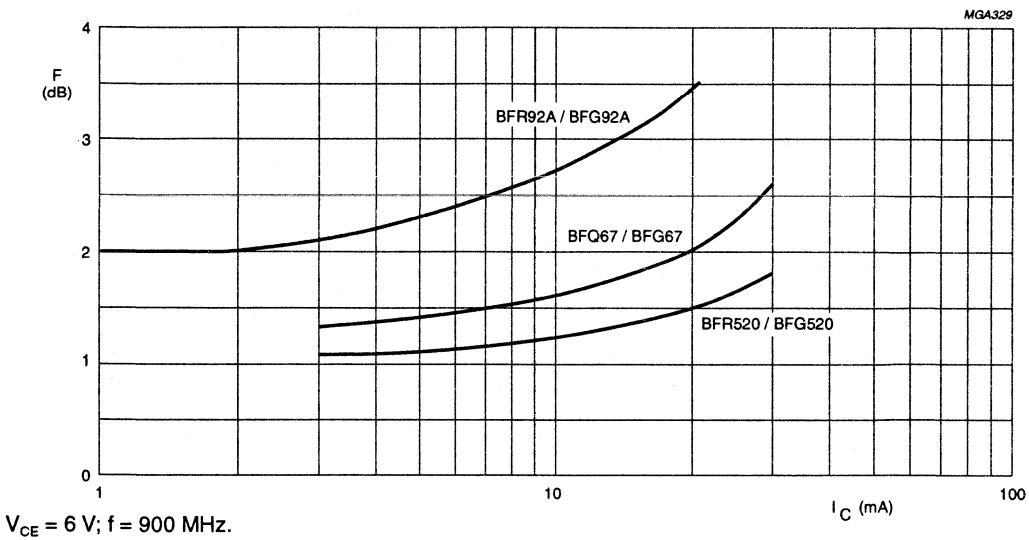


Fig.2 Maximum unilateral power gain (G_{UM}) as a function of collector current (I_C) for various types in SOT143 envelopes.



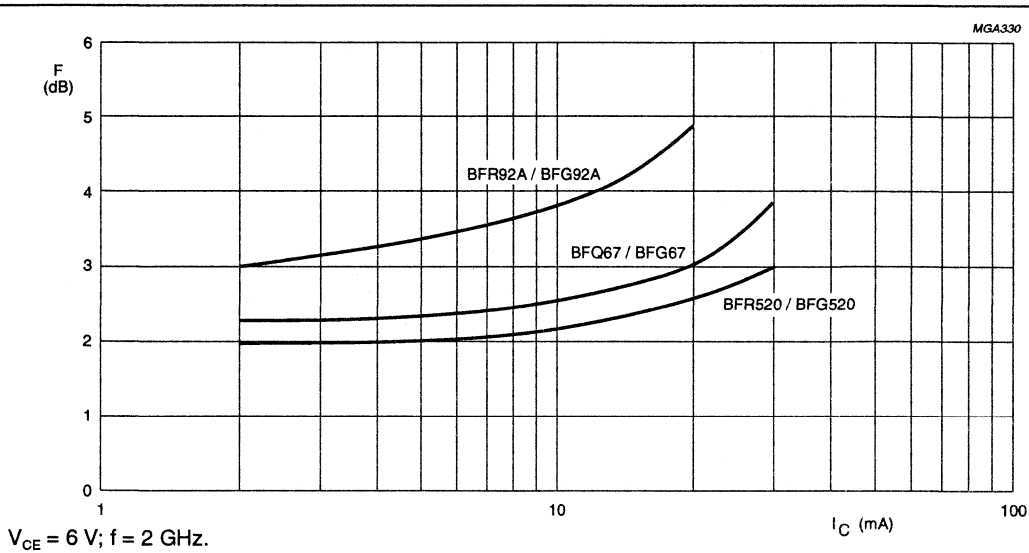
V_{CE} = 6 V; f = 900 MHz.

Fig.3 Noise figure (F) as a function of collector current (I_C) for 4th generation devices in SOT23 and SOT143 envelopes.



V_{CE} = 6 V; f = 900 MHz.

Fig.4 Noise figure (F) as a function of collector current (I_C) for three comparable crystals (nominal 20 mA) in SOT23 and SOT143 envelopes.



V_{CE} = 6 V; f = 2 GHz.

Fig.5 Noise figure (F) as a function of collector current (I_C) for three comparable crystals (nominal 20 mA) in SOT23 and SOT143 envelopes.

Table 7 Plastic RF power transistors (Class-AB) for cellular and cordless telephones.

TYPE NUMBER	ENVELOPE	f (MHz)	V_{CE} (V)	P_L (W)	G_p (dB)	η_C (%)
BLT50 (note 1)	SOT223	470	7.5	1.2	> 10.5 typ. 11.2	> 55 typ. 65
		900	7.5	0.8	> 4.5 typ. 5	> 65 typ.70
BLT80 (note 1)	SOT223	900	7.5	0.8	> 6.0 typ. 7.5	> 60 typ. 67
BLT81 (note 1)	SOT223	900	7.5	1.2	> 6.0	> 65
BLT10	SOT103	1900	6.0	0.3	> 6.0	> 50
BLT11	SOT103	1900	6.0	0.6	> 6.0	> 50
BFG10; BFG10/X	SOT143; SOT143R	1900	3.6	0.2	> 5.0	> 50
BFG11; BFG11/X	SOT143; SOT143R	1900	3.6	0.4	> 4.0	> 50

Note

1. For further information, refer to Data Handbook SC08a, 1993; "RF Power Bipolar Transistors", available February 1993.

Table 8 RF wideband transistors for pagers; see Fig.6.

SOCKET	SOT323	SOT23	SOT143 (note 1)	GENERATION
RF amplifier	BFR92AW	BFR92A	BFG92A/X	2nd
	BFS25A	BFT25A	BFG25A/X	4th
	BFS505	BFR505	BFG505/X	4th
	BFS520	BFR520	BFG520/X	4th
MIX	see RF amplifier			
OSC	see RF amplifier			

Note

1. European and Japanese pinning versions are also available.

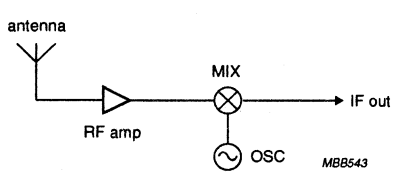


Fig.6 Pager RF input circuit.

Table 9 RF wideband transistors for cellular phones; see Figs 7 and 8.

SOCKET		SOT323	SOT23	SOT143 (note 1)	SOT223	GENERATION
Receiver	Input amplifier and MIX1	BFQ67W	BFQ67	BFG67/X		3rd
		BFS25A	BFT25A	BFG25A/X		4th
		BFS505	BFR505	BFG505/X		4th
		BFS520	BFR520	BFG520/X		4th
	B1 amplifier	BFR92AW	BFR92A	BFG92A/X		2nd
		BFR93AW	BFR93A	BFG93A/X		2nd
		BFS505	BFR505	BFG505/X		4th
		BFS520	BFR520	BFG520/X		4th
	IF amplifier	BFS25A	BFT25A	BFG25A/X		4th
		BFS505	BFR505	BFG505/X		4th
VCO1 and VCO2	OSC	BFR92AW	BFR92A	BFG92A/X		2nd
		BFR93AW	BFR93A	BFG93A/X		2nd
		BFS505	BFR505	BFG505/X		4th
		BFS520	BFR520	BFG520/X		4th
	B2 amplifier: as OSC, plus:	BFQ67W	BFQ67	BFG67/X		3rd
Transmitter	Pre-amplifier	BFQ67W	BFQ67	BFG67/X		3rd
		BFS505	BFR505	BFG505/X		4th
		BFS520	BFR520	BFG520/X		4th
	MIX2 and B1 amplifier:	see OSC	see OSC	see OSC		
	Driver amplifier		BFQ67	BFG67/X		3rd
			BFR520	BFG520/X		4th
	PA1				BFG35	2nd
					BFG198	3rd
				BFG540/X	BFG541	4th
				BFG590/X	BFG591	4th
	PA2				BLT50 (note 2)	3rd
					BFG135	3rd
					BFG621 (note 3)	4th
	PA3				BLT80 (note 2)	3rd
					BLT81 (note 2)	3rd

Notes

1. European and Japanese pinning versions are also available.
2. For further information, refer to Data Handbook SC08a, 1993; "RF Power Bipolar Transistors", available February 1993.
3. In development.

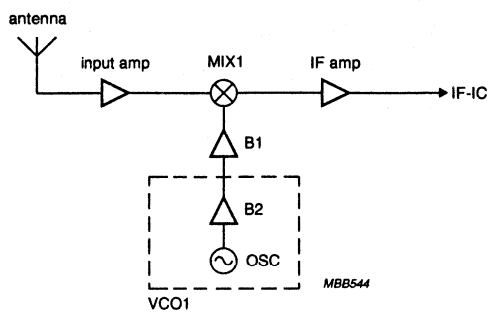


Fig.7 Cellular phone receiver circuit.

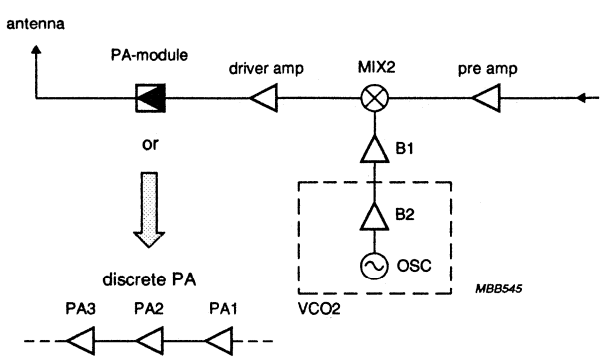


Fig.8 Cellular phone transmitter circuit.

Table 10 RF wideband transistors for cordless phones; see Fig.9.

SOCKET		SOT323	SOT23	SOT143 (note 1)	SOT223	SOT103	GENERATION
Receiver		see selection guide for cellular phones					
VCO1 and VCO2		see selection guide for cellular phones					
Transmitter	Pre-amplifier	BFQ67W	BFQ67	BFG67/X			3rd
		BFS505	BFR505	BFG505/X			4th
		BFS520	BFR520	BFG520/X			4th
	MIX2 and B1 amplifier: as pre-amplifier, plus:	BFR92AW	BFR92A	BFG92A/X			2nd
		BFR93AW	BFR93A	BFG93A/X			2nd
	PA1	BFQ67W	BFQ67	BFG67/X			3rd
		BFS505	BFR505	BFG505/X			4th
		BFS520	BFR520	BFG520/X			4th
	PA2 and PC1			BFG67/X			3rd
				BFG520/X			4th
				BFG540/X			4th
	PB1			BFG540/X			4th
	PB2				BFG541		4th
				BFG590/X	BFG591		4th
				BFG10/X		BLT10	4th
	PB3				BFG135		3rd
				BFG11/X	BFG621 (note 2)	BLT11	4th
					BFG741 (note 2)		4th

Notes

1. European and Japanese pinning versions are also available.
2. In development.
3. For further information, refer to Data Handbook SC08a, 1993; "RF Power Bi-polar Transistors", available April 1993.

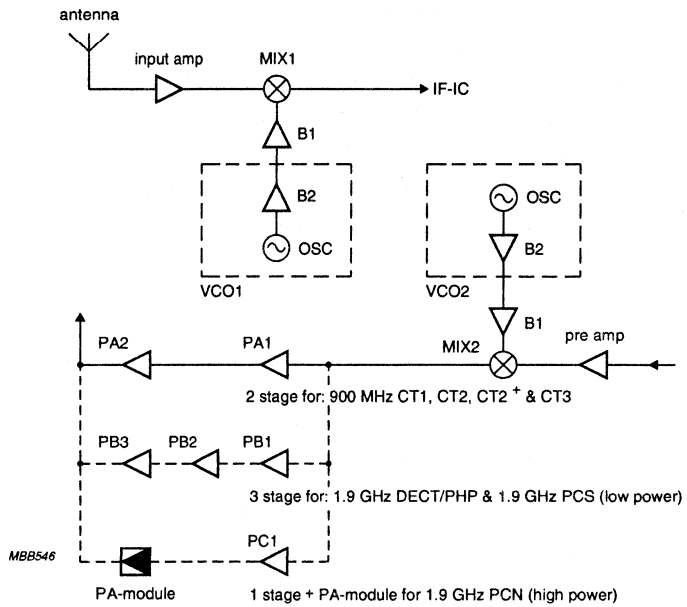


Fig.9 Cordless phone circuit.

DIALLERS

Table 11 Dialler feature reference matrix.

TYPE NUMBER	PULSE	DTMF	REDIAL	REP. DIAL	RINGER
PCD3310 Family	x	x	x	.	.
PCD3315/512, PCD3315/513	x (note 1)	x	x	.	.
PCD332X Family	x	.	x	.	.
PCD3330-1	x	x	x	x	x
PCD3331-1	x	x	x	.	x
PCD3332-1	x	x	x	x	x
PCD3344/004 PCD3344/011 PCD3344/047	x	x	x	x	.
PCD3347/001 PCD3347/020	x	x	x	x	x
PCD3349/017	x	x	x	x	.
PCD3349/018	x	x	x	x	.
PCD4420	.	x	x	.	.
PCD4421	.	x	x	.	.

Note

1. With optional PCD3312 DTMF generator.

MICROCONTROLLERS

Table 12 Preferred telephone set microcontroller selection matrix.

TYPE NUMBER	TEL. SETS	ANSW. MACH.	CORDL CT0/CT1	DIG. CORDL	DIG. CELL. RADIO	ANAL. CELL. RADIO	PAGERS	PERIP. CONT.
PCD3315A	x	.	.	.	.	.	.	x
PCD3343A	x	.	.	.	.	.	.	x
PCD3344A	x	x	.	.	.	.	.	.
PCD3346	x	.	.	.	.	.	.	.
PCD3347A	x	.	.	.	.	.	.	.
PCD3348A	x	x	.	.	.	.	.	x
PCD3349A	x	x	x	.	.	.	.	.
PCD3350A	x	x	x	.	.	.	.	x
PCD3351A	x	.	.	.	.	.	.	x
PCD3352A	x	.	.	.	.	.	.	x
PCD3353A	x	x	x	.	.	.	.	x
PCD3354A	x	x	x	.	.	.	.	x
PCA83C552-4	.	.	.	.	.	x	.	.
PCF83C562	.	.	.	.	.	.	.	.
PCF83C652	.	.	x	.	.	.	.	.
PCF83C654	.	.	x	x	.	x	.	.
PCF83C851	.	.	.	.	.	x	.	.
PCF84CXX/XXX	x	x	x	.	.	.	.	x
P80CL31/51	x	x	x	.	.	.	x	x
P80CL32/52	x	x	x	.	.	.	x	x
P83CL410	x	x	x	.	.	.	x	x
P83CL411	x	x	x	.	.	.	x	x
P83C550	.	.	.	.	.	x	.	.
P83CL580	.	.	x	.	.	x	x	x
P83CL781	x	x	x	x	.	.	x	x
P83CL782	x	x	x	x	.	.	x	x
P93C101	.	.	.	.	x	.	.	.

GENERAL

QUALITY

Total Quality Management

Philips Semiconductors are a Quality Company, renowned for the high quality of our products and service. We keep alive this tradition by constantly aiming towards one ultimate standard, that of zero defects. This aim is guided by our Total Quality Management (TQM) system, the basis of which is:

quality assurance

based on ISO 9000 standards, customer standards such as Ford Q1 and IBM MDQ, and the CECC system of conformity. Our factories are certified to ISO 9000 and CECC by external inspectorates

partnerships with customers

PPM co-operations, design-in agreements, and ship-to-stock, just-in-time and self-qualification programmes

partnerships with suppliers

ship-to-stock, statistical process control and ISO 9000 audits

quality improvement programme

continuous process and system improvement, design improvement, complete use of statistical process control, realization of our final objective of zero defects, and logistics improvement by ship-to-stock and just-in-time agreements.

Advanced quality planning

During the design and development of new products and processes, quality is built-in by advanced quality planning. Through failure-mode-and-effect analysis the critical parameters are detected and measures taken to ensure good performance on these parameters. The capability of process steps is also planned in this phase.

Product conformance

The assurance of product conformance is an integral part of our quality assurance (QA) practice. This is achieved by:

- incoming material management through partnerships with suppliers
- in-line quality assurance to monitor process reproducibility during manufacture and initiate any necessary corrective action. Critical process steps are 100% under statistical process control
- acceptance tests on finished products to verify conformance with the device specification. The test results are used for quality feedback and corrective actions. The inspection and test requirements are detailed in the general quality specifications
- periodic inspections to monitor and measure the conformance of products.

Product reliability

With the increasing complexity of OEM (original equipment manufacturer) equipment, component reliability must be extremely high. Our research laboratories and development departments study the failure mechanisms of semiconductors. Their studies have resulted in design rules and process optimization for the highest built-in product reliability. Highly accelerated tests are applied to the products reliability evaluation. Rejects from reliability tests and from customer complaints are submitted to failure analysis, to result in corrective action.

Customer responses

Our quality improvement depends on joint action with our customer. We need our customer's inputs and we invite constructive comments on all aspects of our performance. Please contact our local sales representative.

PRO ELECTRON TYPE NUMBERING SYSTEM FOR DISCRETE SEMICONDUCTORS

Basic type number

This type designation code applies to discrete semiconductor devices (not integrated circuits), multiples of such devices, semiconductor chips and Darlington transistors.

FIRST LETTER

The first letter gives information about the material for the active part of the device.

A germanium or other material with a band gap of 0.6 to 1 eV

B silicon or other material with a band gap of 1 to 1.3 eV

C gallium arsenide (GaAs) or other material with a band gap of 1.3 eV or more

R compound materials, e.g. cadmium sulphide.

SECOND LETTER

The second letter indicates the function for which the device is primarily designed. The same letter can be used for multi-chip devices with similar elements. In the following list low power types are defined by $R_{th\ j\text{-}mb} > 15$ K/W and power types by $R_{th\ j\text{-}mb} \leq 15$ K/W.

A diode; signal, low power

B diode; variable capacitance

C transistor; low power, audio frequency

D transistor; power, audio frequency

E diode; tunnel

F transistor; low power, high frequency

G multiple of dissimilar devices/miscellaneous devices; e.g. oscillators. Also with special third letter, see under '*Serial number*'

H diode; magnetic sensitive

L transistor; power, high frequency

N photocoupler

P radiation detector; e.g. high sensitivity photo-transistor; with special third letter

Q radiation generator; e.g. LED, laser; with special third letter

R control or switching device; e.g. thyristor, low power; with special third letter

S transistor; low power, switching

T control and switching device; e.g. thyristor, power; with special third letter

U transistor; power, switching

W surface acoustic wave device

X diode; multiplier, e.g. varactor, step recovery

Y diode; rectifying, booster

Z diode; voltage reference or regulator, transient suppressor diode; with special third letter.

SERIAL NUMBER/SPECIAL THIRD LETTER

The number comprises three figures running from 100 to 999 for devices primarily intended for consumer equipment, or one letter (Z, Y, X, etc.) and two figures running from 10 to 99 for devices primarily intended for industrial or professional equipment.(1) The letter has no fixed meaning, except in the following cases:

A for triacs, after second letter 'R' or 'T'

F for emitters and receivers in fibre-optic communication, after second letter 'G', 'P' or 'Q'. When the second letter is 'G', the first letter should be defined in accordance with the material of the main optical device.

L for lasers in non-fibre-optic applications, after second letter 'G' or 'Q'. When the second letter is 'G', the first letter should be defined in accordance with the material of the main optical device.

O for opto-triacs, after second letter 'R'

T for 3-state bicolour LEDs, after second letter 'Q'

W for transient voltage suppressor diodes, after second letter 'Z'.

EXAMPLES OF BASIC TYPE NUMBERS

AA112: germanium, low power signal diode (consumer type)

ACY32: germanium, low power AF transistor (industrial type)

BD232: silicon, power AF transistor (consumer type)

CQY17: GaAs, light-emitting diode (industrial type)

RPY84: CdS, photo-conductive cell (industrial type).

Version letter(s)

One or two letters may be added to the basic type number to indicate minor electrical or mechanical variants of the basic type. The letters never have a fixed meaning, except that the letter 'R' indicates reverse polarity and the letter 'W' indicates a surface mounted device (SMD).

(1) When the supply of these serial numbers is exhausted, the serial number may be expanded to three figures for industrial types and four figures for consumer types.

Suffix

Sub-classification can be used for devices supplied in a wide range of variants, called associated types. The following sub-coding suffixes are in use:

VOLTAGE REFERENCE AND VOLTAGE REGULATOR DIODES

One letter and one number, preceded by a hyphen (-). The letter, if required, indicates the nominal tolerance of the Zener voltage.

A 1%
B 2%
C 5%
D 10%
E 20%

In the case of a 3% tolerance, the letter 'F' is used.

The number denotes the typical operating (Zener) voltage, related to the nominal current rating for the entire range. The letter 'V' is used in place of the decimal point.

Example: BZY74-C6V3 or -C10.

TRANSIENT VOLTAGE SUPPRESSOR DIODES

One number, preceded by a hyphen (-). The number indicates the maximum recommended continuous reversed (stand-off) voltage, V_R. The letter 'V' is used in place of the decimal point.

Example: BZW70-9V1 or –39.

The letter 'B' may be used immediately after the last number, to indicate a bidirectional suppressor diode.

Example: BZW10-15B.

CONVENTIONAL AND CONTROLLED AVALANCHE RECTIFIER DIODES AND THYRISTORS

One number, preceded by a hyphen (-). The number indicates the rated maximum repetitive peak reverse voltage, V_{RRM}, or the rated repetitive peak off-state voltage, V_{DRM}, whichever is the lower. Reversed polarity with respect to the case is indicated by the letter 'R' immediately after the number.

Example: BYT-100 or -100R.

RADIATION DETECTORS

One number, preceded by a hyphen (-). The number indicates the depletion layer in micrometres (μm). The resolution is indicated by a version letter.

Example: BPX10-2A.

ARRAY OF RADIATION DETECTORS AND GENERATORS

One number, preceded by a hyphen (-). The number indicates the number of basic devices assembled into the array.

Examples: BPW50-6, BPW50-9, BPW50-12.

HIGH FREQUENCY POWER TRANSISTORS

One number, preceded by a hyphen (-). The number indicates the supply voltage.

Example: BLU80-24.

PRO ELECTRON TYPE NUMBERING SYSTEM FOR INTEGRATED CIRCUITS

Basic type number

This type designation code applies to semiconductor monolithic, semiconductor multi-chip, thin film, thick film and hybrid integrated circuits. The basic type number comprises three letters followed by a serial number.

FIRST AND SECOND LETTERS

Digital family circuits

The first two letters identify the family.(1)

Solitary circuits

The first letter divides solitary circuits into:

S solitary digital circuits
T analog circuits

(1) A logic family is an assembly of digital circuits designed to be interconnected and defined by its base electrical characteristics, such as supply voltage, power consumption, propagation delay, noise immunity.

U mixed analog/digital circuits.

The second letter is a serial letter without any further significance except 'H' which stands for hybrid circuits.(1)

Microprocessors

The first two letters identify microprocessors and related circuits:

MA microcomputer or central processing unit

MB slice processor (functional slice of microprocessor)

MD related memories

ME other related circuits such as interfaces, clocks, peripheral controllers, etc.

Charge-transfer devices and switched capacitors

The first two letters identify:

NH hybrid circuits

NL logic circuits

NM memories

NS analog signal processing using switched capacitors

NT analog signal processing using charge-transfer devices

NX imaging devices

NY other related circuits

THIRD LETTER

The third letter indicates the operating ambient temperature range:

A temperature range not specified below

B 0 to + 70 °C

C −55 to +125 °C

D −25 to + 70 °C

E −25 to + 85 °C

F −40 to + 85 °C

G −55 to + 85 °C.

If a device has another temperature range, the letter 'A' or a letter indicating a narrower temperature may be used, for example, the range of 0 to +75 °C can be indicated by 'A' or 'B'. Should two devices with the same basic type number both have temperature ranges other than those specified, one would use the letter 'A' and the other the letter 'X'.

Serial number

This may be a four-digit number assigned by Pro Electron, or the serial number (which may be a combination of figures and letters) of an existing company type designation of the manufacturer.

Version letter

A single version letter may be added to the basic type number. This indicates a minor variant of the basic type or the package. The version letter has no fixed meaning except for 'Z' which means customized wiring. The following letters are recommended for package variants:

C cylindrical

D ceramic dual in-line (CERDIL, CERDIP)

F flat pack (two leads)

G flat pack (four leads)

H quad flat pack (QFP)

L chip on tape (foil)

P plastic dual in-line (DIL)

Q quad in-line (QUIL)

T mini pack (SOL, SO, VSO)

U uncased chip

Two-letter suffix

A two-letter suffix may be used instead of a single package version letter to give more information. To avoid confusion with serial numbers that end with a letter, a hyphen should precede the suffix.

FIRST LETTER (GENERAL SHAPE)

C cylindrical

D dual in-line (DIL)

E power DIL (with external heatsink)

F flat pack (leads on two sides)

G flat pack (leads on four sides)

H quad flat pack (QFP)

(1) The first letter 'S' should be used for all solitary memories, to which, in the event of hybrids, the second letter 'H' should be added, for example, SH for bubble memories.

K diamond (TO-3 family)
M multiple in-line (except dual, triple and quad)
Q quad in-line (QUIL)
R power QUIL (with external heatsink)
S single in-line (SIL)
T triple in-line
W leaded chip carrier (LCC)
X leadless chip carrier (LLCC)
Y pin grid array (PGA)

SECOND LETTER (MATERIAL)

C metal-ceramic
G glass-ceramic
M metal
P plastic

Examples

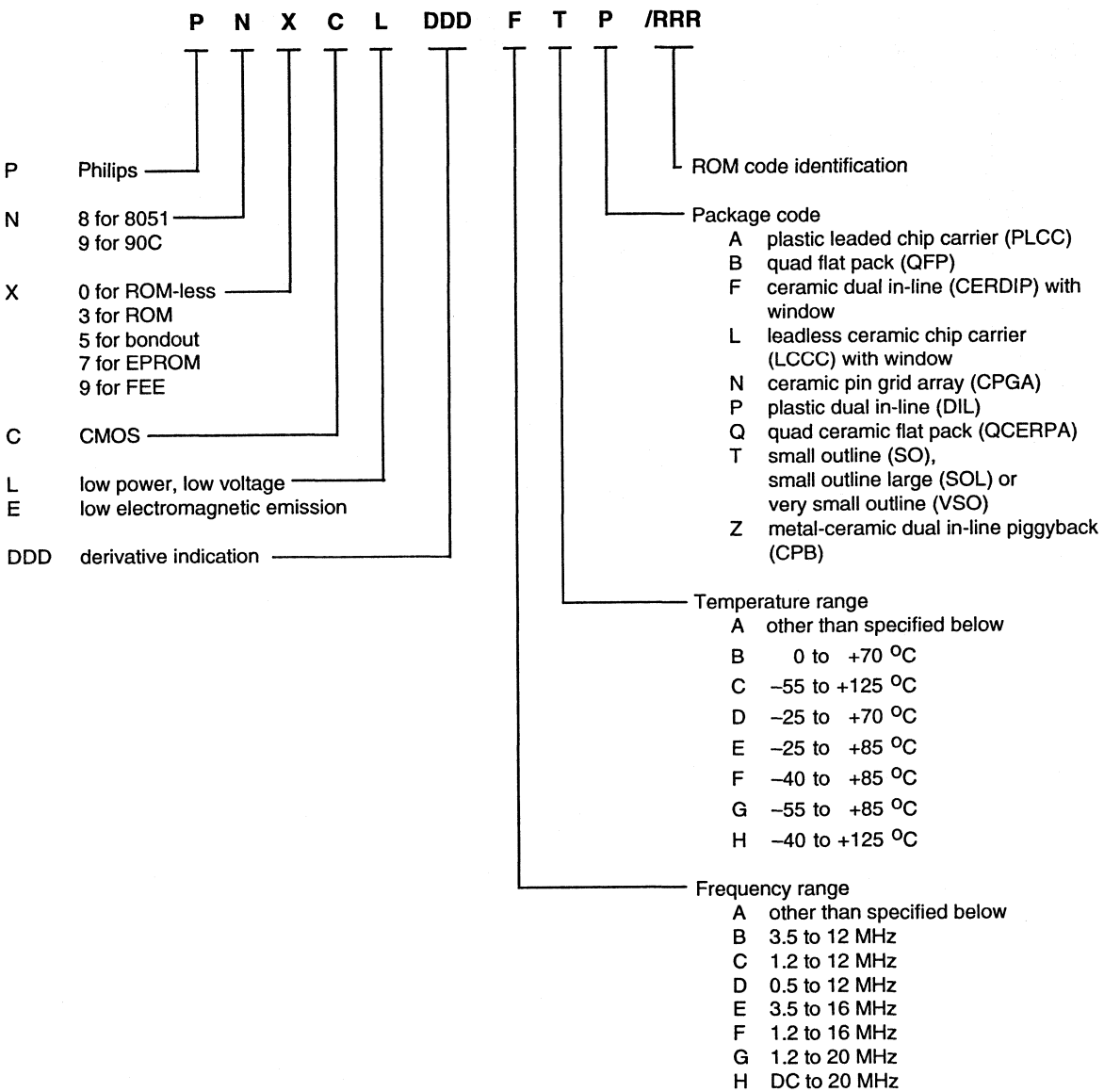
PCF1105WP: digital IC; PC family; operating temperature range –40 to +85 °C; serial number 1105; plastic leaded chip carrier.

GMB74LS00A-DC: digital IC; GM family; operating temperature range 0 to +70 °C; company number 74LS00A; ceramic DIL package.

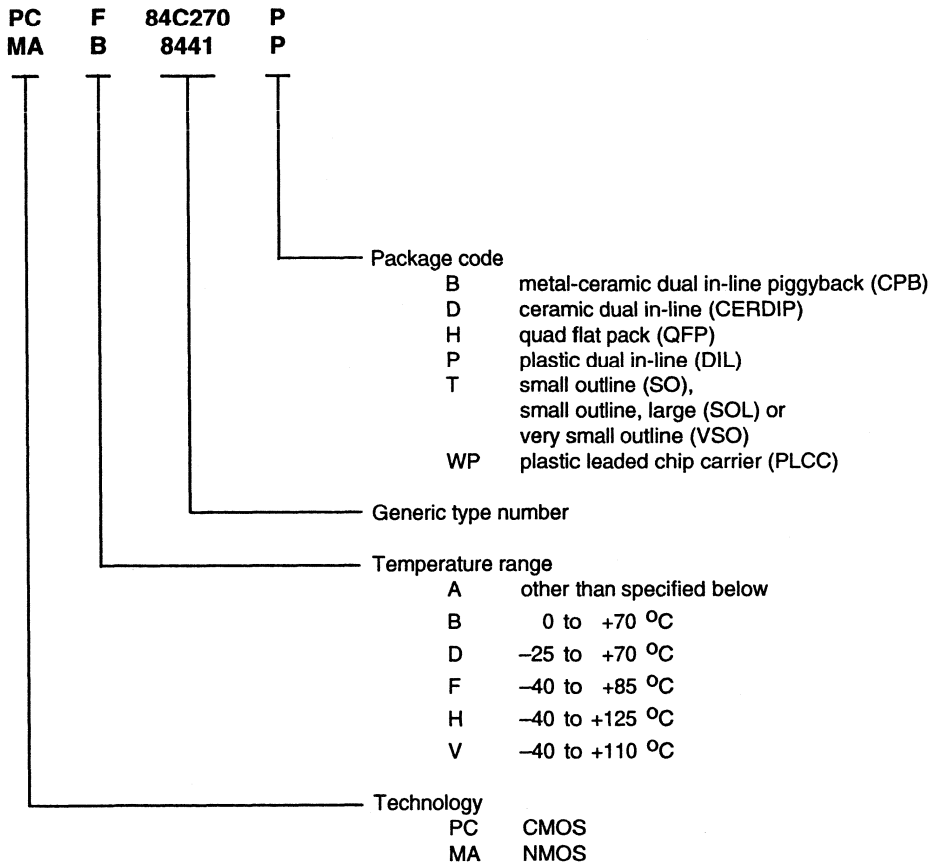
TDA1000P: analog IC; operating temperature range non-standard; serial number 1000; plastic DIL package.

SAC2000: solitary digital circuit; operating temperature range –55 to +125 °C; serial number 2000.

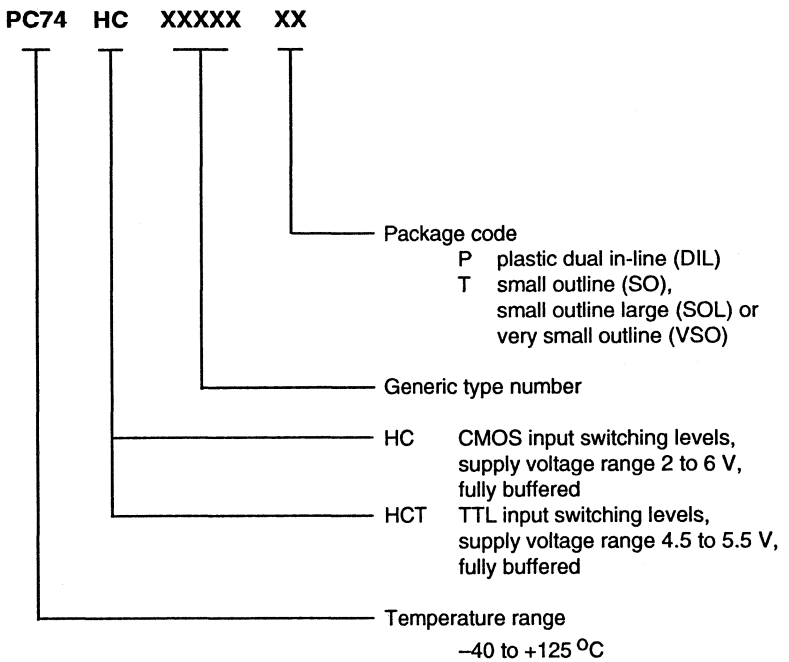
TYPE NUMBERING of 8051 and 90C MICROCONTROLLER DERIVATIVES



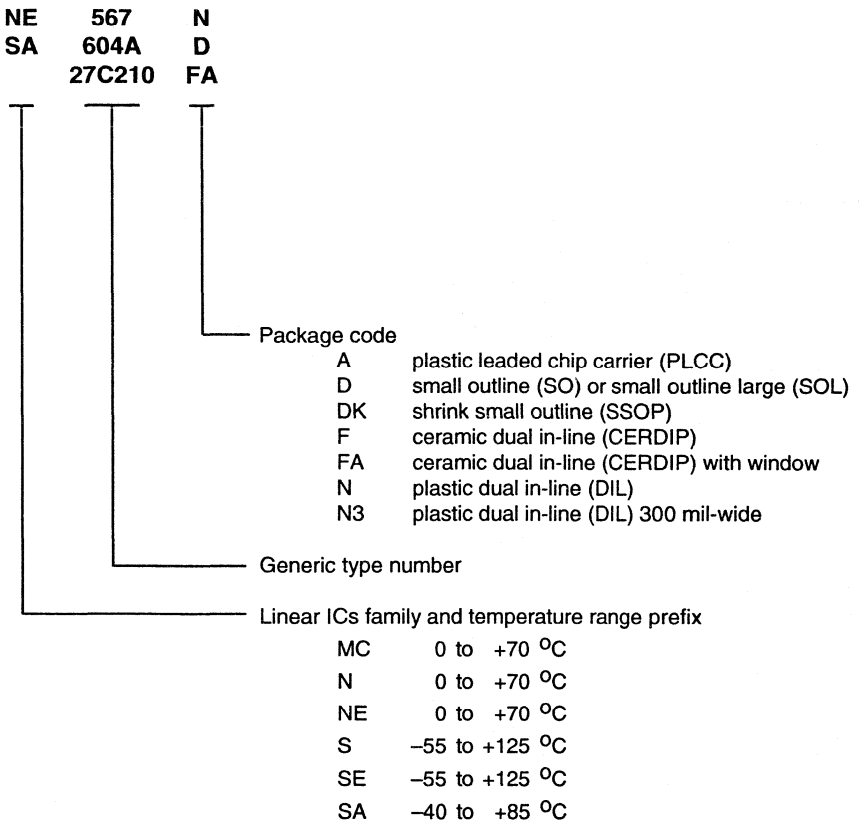
TYPE NUMBERING of 8048 MICROCONTROLLER DERIVATIVES



TYPE NUMBERING of HCMOS INTEGRATED CIRCUITS



TYPE NUMBERING of SIGNETICS LINEAR AND MEMORY DEVICES



RATING SYSTEMS

The rating systems described are those recommended by the IEC in its publication number 134.

Definitions of terms used

ELECTRONIC DEVICE

An electronic tube or valve, transistor or other semiconductor device. This definition excludes inductors, capacitors, resistors and similar components.

CHARACTERISTIC

A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

BOGEY ELECTRONIC DEVICE

An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics that are directly related to the application.

RATING

A value that establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms. Limiting conditions may be either maxima or minima.

RATING SYSTEM

The set of principles upon which ratings are established and which determine their interpretation. The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

Absolute maximum rating system

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type, as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout the life of the device, no absolute maximum value for the intended service is exceeded with any device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

Design maximum rating system

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout the life of the device, no design maximum value for the intended service is exceeded with a bogey electronic device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

Design centre rating system

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage

variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

HANDLING MOS DEVICES

Electrostatic charges

Electrostatic charges can exist in many things; for example, man-made-fibre clothing, moving machinery, objects with air blowing across them, plastic storage bins, sheets of paper stored in plastic envelopes, paper from electrostatic copying machines, and people. The charges are caused by friction between two surfaces, at least one of which is non-conductive. The magnitude and polarity of the charges depend on the different affinities for electrons of the two materials rubbing together, the friction force and the humidity of the surrounding air.

Electrostatic discharge is the transfer of an electrostatic charge between bodies at different potentials and occurs with direct contact or when induced by an electrostatic field. All of our MOS devices are internally protected against electrostatic discharge but they **can** be damaged if the following precautions are not taken.

Work station

Figure 1 shows a working area suitable for safely handling electrostatic sensitive devices. It has a work bench, the surface of which is conductive or covered by an antistatic sheet. Typical resistivity for the bench surface is between 1 and 500 kΩ per cm^2. The floor should also be covered with antistatic material. The following precautions should be observed:

- persons at a work bench should be earthed via a wrist strap and a resistor
- all mains-powered electrical equipment should be connected via an earth leakage switch
- equipment cases should be earthed
- relative humidity should be maintained between 50 and 65%
- an ionizer should be used to neutralize objects with immobile static charges.

Receipt and storage

MOS devices are packed for dispatch in antistatic/conductive containers, usually boxes, tubes or blister tape. The fact that the contents are sensitive to electrostatic discharge is shown by warning labels on both primary and secondary packing.

The devices should be kept in their original packing whilst in storage. If a bulk container is partially unpacked, the unpacking should be performed at a protected work station. Any MOS devices that are stored temporarily should be packed in conductive or antistatic packing or carriers.

Assembly

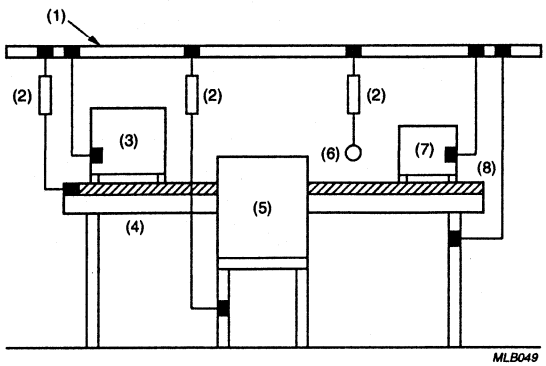
MOS devices must be removed from their protective packing with earthed component pincers or short-circuit clips. Short-circuit clips must remain in place during mounting, soldering and cleansing/drying processes. Do not remove more devices from the storage packing than are needed at any one time. Production/assembly documents should state that the product contains electrostatic sensitive devices and that special precautions need to be taken.

During assembly, ensure that the MOS devices are the last of the components to be mounted and that this is done at a protected work station.

All tools used during assembly, including soldering tools and solder baths, must be earthed. All hand tools should be of conductive or antistatic material and, where possible, should not be insulated.

Measuring and testing of completed circuit boards must be done at a protected work station. Place the soldered side of the circuit board on conductive or antistatic foam and remove the short-circuit clips. Remove the circuit board from the foam, holding the board only at the edges. Make sure the circuit board does not touch the conductive surface of the work bench. After testing, replace the circuit board on the conductive foam to await packing.

Assembled circuit boards containing MOS devices should be handled in the same way as unmounted MOS devices. They should also carry warning labels and be packed in conductive or antistatic packing.



(1) Earthing rail.
(2) Resistor (500 kΩ ± 10%, 0.5 W).
(3) Ionizer.
(4) Work bench.
(5) Chair.
(6) Wrist strap.
(7) Electrical equipment.
(8) Conductive surface/antistatic sheet.

Fig.1 Protected work station.

DEVICE DATA

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC09 OR DATA SHEET

UHF POWER AMPLIFIER MODULE

UHF broadband amplifier module designed for use in mobile communication equipment operating directly from a 9.6 V electrical supply. The module will produce a minimum of 1.4 W into a 50 Ω load over the frequency range 400 to 440 MHz.

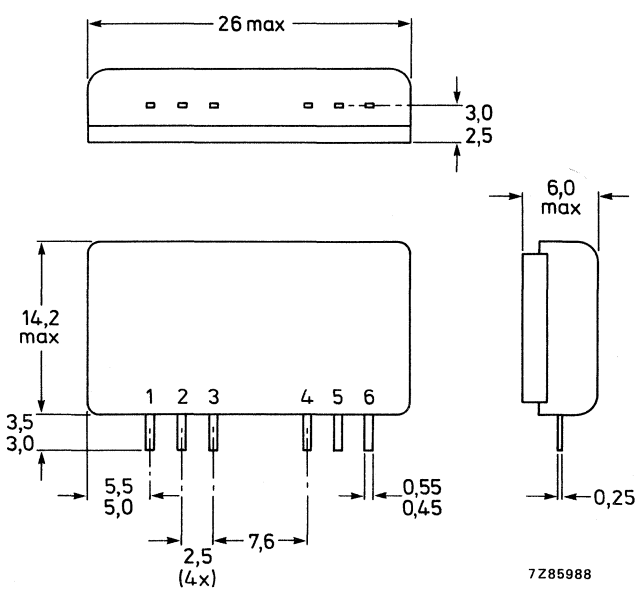
The module consists of a two-stage RF amplifier using npn transistor chips with lumped element matching components in a SOT-181 plastic encapsulation. The negative supply is internally connected to the flange.

QUICK REFERENCE DATA

Mode of operation		continuous wave	
Frequency range		400 to 440	MHz
DC supply voltage (terminal 3)	V_{S1}	nom. 7.5	V
DC supply voltage (terminal 4)	V_{S2}	nom. 9.6	V
RF drive power	P_D	< 45	mW
RF load power	P_L	min. 1.4	W
Efficiency	η	typ. 42	%

MECHANICAL DATA

Dimensions in mm



Lead reference

1. RF input
2. Earth
3. V_{S1}
4. V_{S2}
5. Earth
6. RF output

Flange connected to earth.

Fig. 1 SOT-181.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC09 OR DATA SHEET

UHF POWER AMPLIFIER MODULE

UHF broadband amplifier module designed for use in mobile communication equipment operating directly from a 9.6 V electrical supply. The module will produce a minimum of 1.4 W into a 50 Ω load over the frequency range of 430 to 470 MHz.

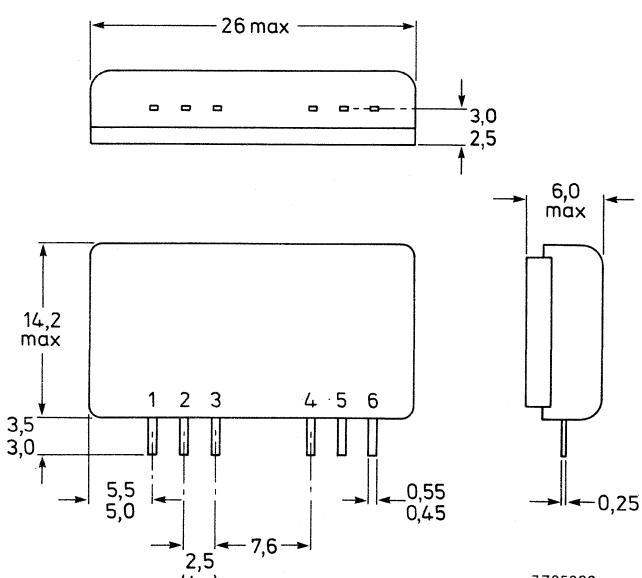
The module consists of a two-stage RF amplifier using npn transistor chips with lumped element matching components in a SOT-181 plastic encapsulation. The negative supply is internally connected to the flange.

QUICK REFERENCE DATA

Mode of operation			continuous wave	
Frequency range			430 to 470	MHz
DC supply voltage (terminal 3)	V_{S1}	nom.	7.5	V
DC supply voltage (terminal 4)	V_{S2}	nom.	9.6	V
RF drive power	P_D	<	45	mW
RF load power	P_L	min.	1.4	W
Efficiency	η	typ.	45	%

MECHANICAL DATA

Dimensions in mm



Lead reference

1. RF input
2. Earth
3. V_{S1}
4. V_{S2}
5. Earth
6. RF output

Flange connected to earth.

Fig. 1 SOT-181.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC09 OR DATA SHEET

UHF POWER AMPLIFIER MODULE

A broadband UHF amplifier module primarily designed for mobile communications equipment, operating directly from 7.5 V or 9.6 V electrical systems. The module will produce a minimum output of 2.0 W or 3.2 W into a 50 Ω load over the frequency range 400 to 470 MHz.

The module consists of a two-stage RF amplifier, using npn transistor chips with lumped-element matching components in a plastic stripline encapsulation (SOT181). The negative supply is internally connected to the flange.

QUICK REFERENCE DATA

Mode of operation			CW
Frequency range			400 to 470 MHz
DC supply voltage (terminal 3)	V_{S1}		7.5 or 9.6 V
DC supply voltage (terminal 4)	V_{S2}		7.5 or 9.6 V
RF drive power	P_D	max.	50 mW
RF load power	P_L	min.	2.0 or 3.2 W
Efficiency	η	typ.	44 %

MECHANICAL DATA

Dimensions in mm

Lead reference

1 = RF input
2 = Earth
3 = V_{S1}
4 = V_{S2}
5 = Earth
6 = RF output
Flange = earth

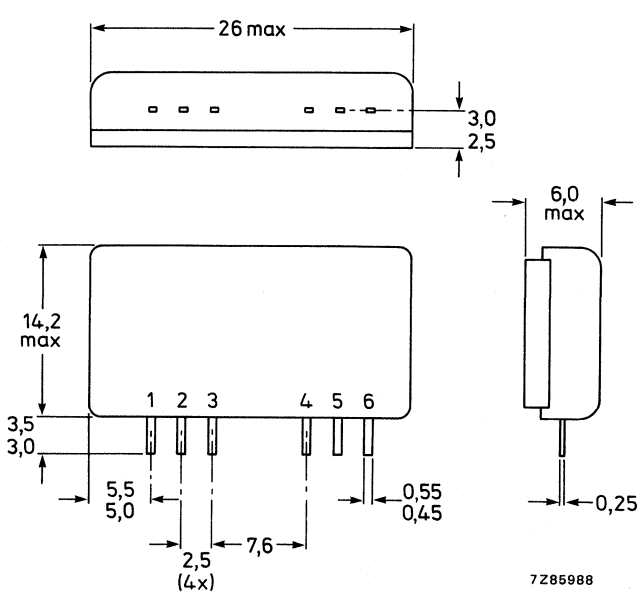


Fig.1 SOT181.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC09 OR DATA SHEET

UHF AMPLIFIER MODULE

The BGY95 is a three-stage UHF amplifier module designed primarily for mobile transmitting equipment operating from a nominal 7.5 V power supply.

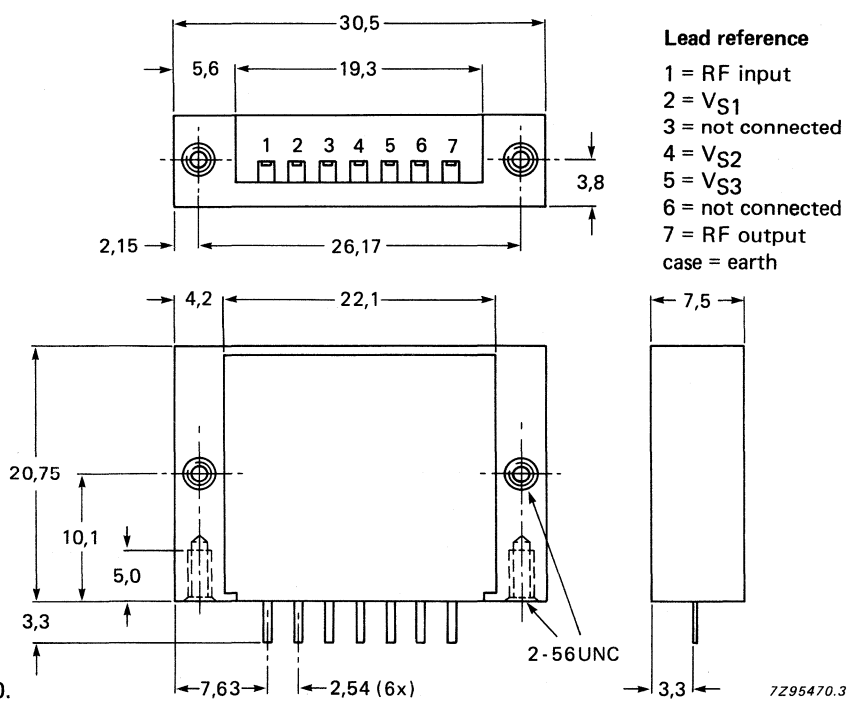
The module consists of three npn silicon planar transistors mounted on a metallized ceramic substrate, together with matching and bias circuitry. The BGY95A and BGY95B produce an output power of 2.2 W into a 50 Ω load over the frequency band of 824-851 MHz and 890-915 MHz respectively. The output power can be controlled by means of a DC voltage (V_{S1}).

QUICK REFERENCE DATA

Mode of operation				CW
Frequency range	BGY95A	f		824 to 851 MHz
	BGY95B	f		890 to 915 MHz
RF load power V_{S1} = 6 V; V_{S2} = V_{S3} = 7.5 V; P_D = 20 mW		P_L	min.	2.2 W
RF drive power V_{S1} = 6 V; V_{S2} = V_{S3} = 7.5 V; P_L = 2.2 W		P_D	⩽	20 mW
Output load impedance		Z_L	nom.	50 Ω

MECHANICAL DATA

Dimensions in mm



Lead reference

1 = RF input
2 = V_{S1}
3 = not connected
4 = V_{S2}
5 = V_{S3}
6 = not connected
7 = RF output
case = earth

Fig.1 SOT200.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC09 OR DATA SHEET

UHF AMPLIFIER MODULE

The BGY96 is a three-stage UHF amplifier module designed primarily for mobile transmitting equipment operating from a nominal 9.6 V power supply.

The module consists of three npn silicon planar transistors mounted on a metallized ceramic substrate, together with matching and bias circuitry. The BGY96A and BGY96B produce an output power of 2.5 W into a 50 Ω load over the frequency band of 824-851 MHz and 890-915 MHz respectively. The output power can be controlled by means of a DC voltage (V_{S1}).

QUICK REFERENCE DATA

Mode of operation				CW
Frequency range	BGY96A	f		824 to 851 MHz
	BGY96B	f		890 to 915 MHz
RF power output V_{S1} = 6 V; V_{S2} = V_{S3} = 9.6 V; P_D = 20 mW		P_L	min.	2.5 W
RF input drive power P_L = 2.5 W		P_D	⩽	20 mW
Output load impedance		Z_L	nom.	50 Ω

MECHANICAL DATA

Dimensions in mm

Lead reference

1 = RF input
2 = V_{S1}
3 = not connected
4 = V_{S2}
5 = V_{S3}
6 = not connected
7 = RF output
case = earth

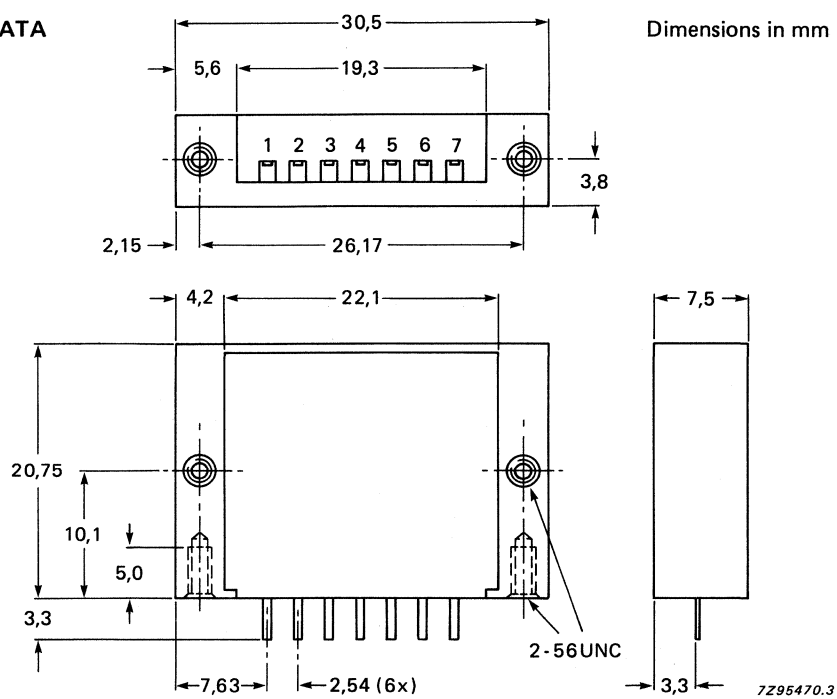


Fig. 1 SOT-200.

UHF amplifier modules

BGY110D; BGY110E; BGY110F; BGY110G

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC09 OR DATA SHEET

DESCRIPTION

The BGY110 is a four-stage UHF amplifier module, primarily designed for hand-held transmitting equipment operating from a nominal 7.2 V power supply.

The module consists of four npn silicon planar transistor chips, mounted on a metallized ceramic substrate, together with matching and bias circuitry.

The BGY110D, 110E, 110F and 110G produce an output power of 1.7 W into a 50 Ω load over the frequency bands 824 - 849 MHz, 872 - 905 MHz, 890 - 915 MHz and 902 - 928 MHz, respectively. The output power can be controlled by means of a DC voltage (V_C).

PINNING - SOT246

PIN	DESCRIPTION
1	RF input/V_C
2	V_{S1}
3	V_{S2}
4	V_{S3}
5	RF output
flange	earth

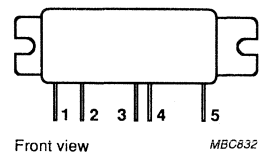


Fig.1 Simplified outline.

QUICK REFERENCE DATA

RF performance at T_{mb} = 25 °C.

TYPE NUMBER	MODE OF OPERATION	f (MHz)	V_S (V)	V_C (V)	P_L (W)	G_p (dB)	η (%)	Z_i/Z_L (Ω)
BGY110D	c.w.	824 - 849	7.2	4.5	1.7	> 32.3	> 39	50
BGY110E	c.w.	872 - 905	7.2	4.5	1.7	> 32.3	> 39	50
BGY110F	c.w.	890 - 915	7.2	4.5	1.7	> 32.3	> 39	50
BGY110G	c.w.	902 - 928	7.2	4.5	1.7	> 32.3	> 39	50

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{S1}; V_{S2}; V_{S3}	DC supply voltage	–	10	V
V_C	DC control voltage	–	4.5	V
$+V_O$	RF output terminal voltage	–	25	V
P_L	load power	–	2.25	W
P_D	drive power	–	3	mW
T_{stg}	storage temperature range	–40	100	°C
T_{mb}	mounting base temperature	–	90	°C

DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC02 OR DATA SHEET

BREAKOVER DIODES

A range of bidirectional diodes in hermetically sealed axial-leaded implosion-diode glass outlines with a +/– 12% tolerance of breakover voltage. These devices feature controlled breakover voltage and high holding current together with a good peak current handling capability. Typical applications include transient overvoltage in telephony equipment, data transmission and remote instrumentation lines.

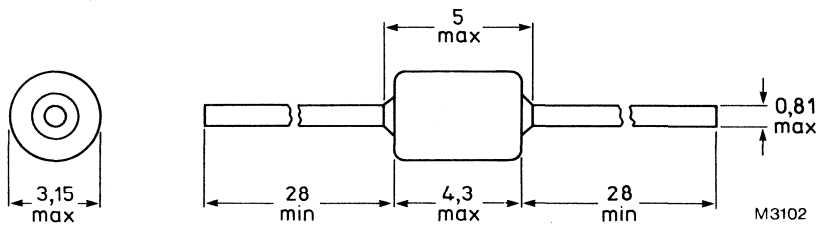
QUICK REFERENCE DATA

			BR211–100 to 280	
Breakover voltage	$V_{(BO)}$	nom.	100 to 280	V
Holding current	I_H	>	150	mA
Transient peak current (10/320 μs impulse)	I_{TSM}	max.	40	A

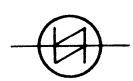
MECHANICAL DATA

Dimensions in mm

Fig.1 SOD-84.



Circuit symbol:



Net mass: 0.35 g.

For packing details see data sheet Bandolier and reel specification for axial-leaded devices.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	February 1991

BS107

N-channel enhancement mode vertical D-MOS transistor

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High speed switching
- No secondary breakdown

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope and intended for use as a line current interruptor in telephone sets and for applications in relay, high speed and line transformer drivers.

PIN CONFIGURATION

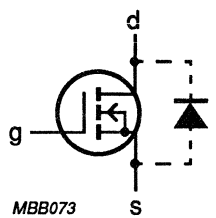


Fig.1 Symbol.

PINNING - TO-92 variant

PIN	DESCRIPTION
1	source
2	gate
3	drain

Note: Other pinnings are available on request.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	200	V
I_D	drain current	150	mA
$R_{DS(on)}$	drain-source on-resistance	28	Ω
$V_{GS(th)}$	gate threshold voltage	2.4	V

N-channel enhancement mode vertical D-MOS transistor

BS108

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

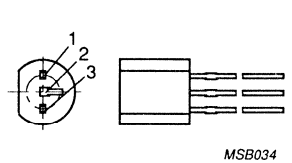
N-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope, intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

PINNING

PIN	DESCRIPTION
1	source
2	gate
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	200	V
I_D	DC drain current	250	mA
$R_{DS(on)}$	drain-source on-resistance	8	Ω
$V_{GS(th)}$	gate-source threshold voltage	1.8	V



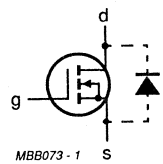


Fig.1 Simplified outline (TO-92 variant) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	200	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	DC drain current		–	250	mA
I_{DM}	peak drain current		–	1	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	125 K/W

Note

1. Device mounted on a printed-circuit board, maximum lead length 4 mm; mounting pad for the drain lead minimum 10 mm².

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and intended for use in relay, high-speed and line-transformer drivers.

Features

- Low R_{DSon}.
- Direct interface to C-MOS, TTL, etc.
- High-speed switching.
- No secondary breakdown.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	60 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	15 V
Drain current (DC)	I_D	max.	500 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	830 mW
Junction temperature	T_j	max.	150 °C
Drain-source ON-resistance V_{GS} = 10 V; I_D = 200 mA	R_{DSon}	max.	5 Ω

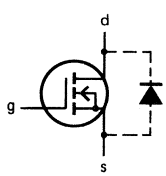
MECHANICAL DATA

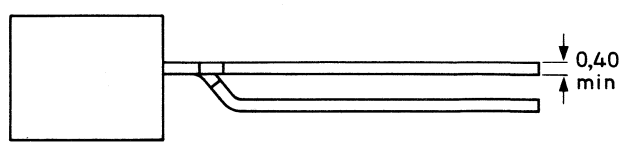
Dimensions in mm

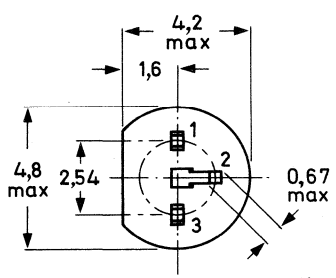
Fig. 1 TO-92 variant.

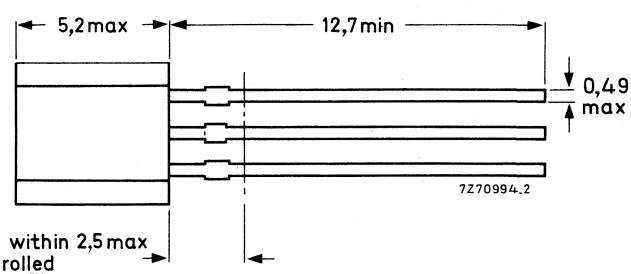
Pinning:

1 = source
2 = gate
3 = drain









Note: Various pin configurations available.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTORS

N-channel enhancement mode vertical D-MOS transistors in TO-92 variant envelope and designed for use as line current interrupters in telephone sets and for application in relay, high-speed and line-transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown
- Low $R_{DS(on)}$

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	250 V
Drain current (DC)	I_D	max.	300 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Drain-source on-resistance I_D = 300 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ. max.	5.0 Ω 7.0 Ω
Gate-source threshold voltage	$V_{GS(th)}$	max.	2 V

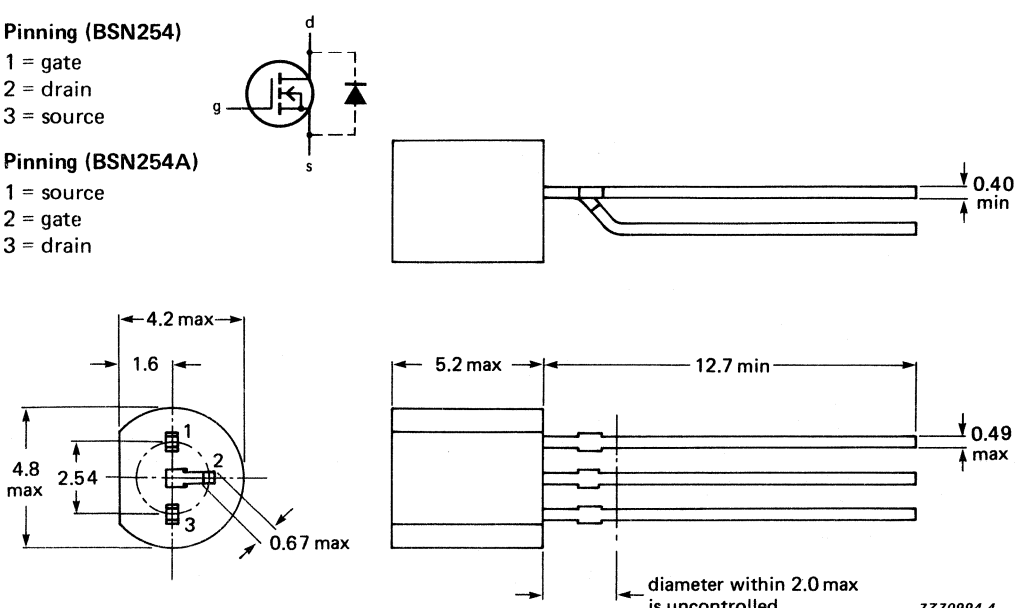
MECHANICAL DATA

Dimensions in mm

Fig.1 TO-92 variant.

Pinning (BSN254)
1 = gate
2 = drain
3 = source

Pinning (BSN254A)
1 = source
2 = gate
3 = drain



Note: Various pinnings are available on request.

N-channel enhancement mode vertical D-MOS transistor

BSP89

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT223 envelope, intended for use as a surface-mounted device in line current interruptors in telephone sets and for application in relay, high speed and line transformer drivers.

PINNING

PIN	DESCRIPTION
Code: BSP89	
1	gate
2	drain
3	source
4	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	240	V
I_D	DC drain current	350	mA
$R_{DS(on)}$	drain-source on-resistance	6	Ω
$V_{GS(th)}$	gate-source threshold voltage	2	V

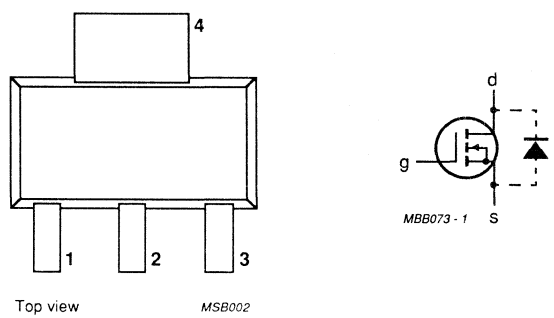


Fig.1 Simplified outline (SOT223) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	240	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	DC drain current		–	350	mA
I_{DM}	peak drain current		–	1.4	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1.5	W
T_{stg}	storage temperature range		-65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	83.3 K/W

Note

1. Transistor mounted on an epoxy printed circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain tab minimum 6 cm^2.

P-channel enhancement mode vertical D-MOS transistor

BSP92

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

FEATURES

- Low threshold voltage $V_{GS(th)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
$-V_{DS}$	drain-source voltage	240	V
$-I_D$	DC drain current	180	mA
$R_{DS(on)}$	drain-source on-resistance	20	Ω
$-V_{GS(th)}$	gate-source threshold voltage	1.8	V

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a SOT223 envelope, intended for use as a surface-mounted device in line current interruptor in telephone sets and for application in relay, high speed and line transformer drivers.

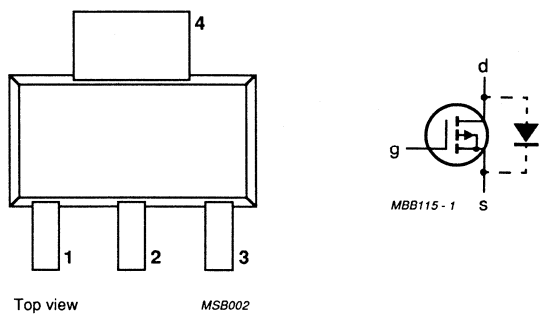


Fig.1 Simplified outline (SOT223) and symbol.

PINNING

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$-V_{DS}$	drain-source voltage		–	240	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
$-I_D$	DC drain current		–	180	mA
$-I_{DM}$	peak drain current		–	720	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1.5	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	83.3 K/W

Note

1. Transistor mounted on an epoxy printed circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain tab minimum 6 cm².

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and designed for use as a line interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching.
- No secondary breakdown.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	250 V
Drain current (DC)	I_D	max.	350 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1.5 W
Drain-source on-resistance I_D = 300 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ. max.	5.0 Ω 7.0 Ω
Gate-source threshold voltage	$V_{GS(th)}$	max.	2 V

MECHANICAL DATA

Dimensions in mm

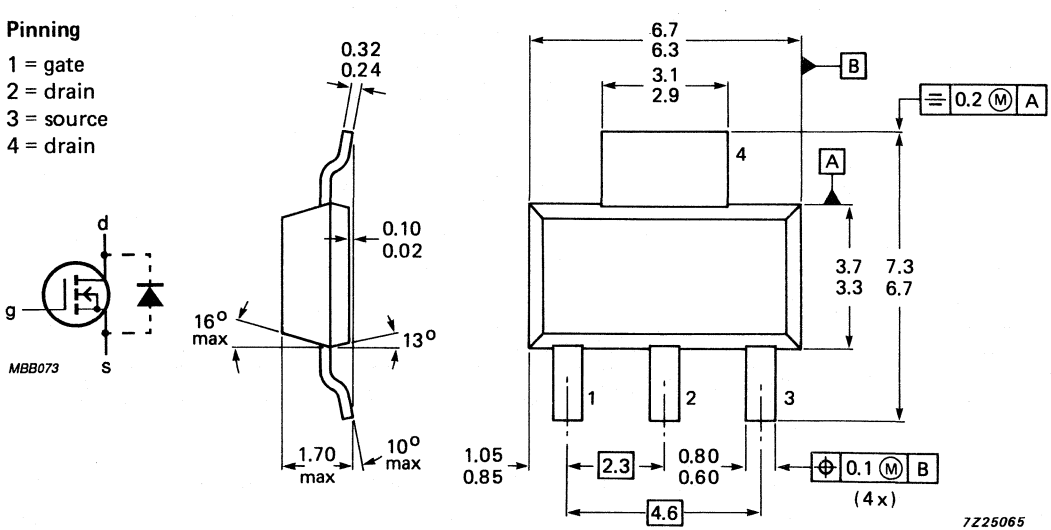
Fig.1 SOT223.

Marking code

BSP126

Pinning

1 = gate
2 = drain
3 = source
4 = drain



Philips Semiconductors

Data sheet	
status	Product specification
date of issue	November 1990

BSP225

P-channel enhancement mode vertical D-MOS transistor

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

FEATURES

- Low $R_{DS(on)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope, intended for use in relay, high-speed and line transformer drivers.

PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$-V_{DS}$	drain-source voltage		250	V
$-I_D$	drain current	DC value	225	mA
$R_{DS(on)}$	drain-source on-resistance	$-I_D$ = 200 mA $-V_{GS}$ = 10 V	15	Ω
$-V_{GS(th)}$	gate-source threshold voltage	$-I_D$ = 1 mA $V_{GS} = V_{DS}$	2.8	V

PIN CONFIGURATION

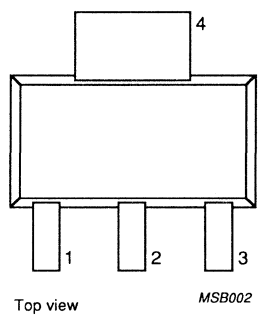


Fig.1 Simplified outline and symbol.

Data sheet	
status	Product specification
date of issue	February 1991

BSP254/BSP254A

P-channel enhancement mode vertical D-MOS transistor

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

P-channel vertical D-MOS transistor in TO-92 variant envelope and intended for use in relay, high-speed and line transformer drivers.

PIN CONFIGURATION

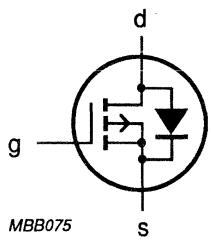


Fig.1 Symbol.

PINNING - TO-92 variant (BSP254)

PIN	DESCRIPTION
1	gate
2	drain
3	source

PINNING - TO-92 variant (BSP254A)

PIN	DESCRIPTION
1	source
2	gate
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{DS}$	drain-source voltage		-	-	250	V
$\pm V_{GSO}$	gate-source voltage	open drain	-	-	20	V
$-I_D$	drain-current	DC	-	-	0.2	A
P_{tot}	total power dissipation	T_{amb} = 25 °C	-	-	1	W
$R_{DS(on)}$	drain-source on-resistance	$-V_{GS}$ = 10 V $-I_D$ = 200 mA	-	10	15	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	$-I_D$ = 200 mA $-V_{DS}$ = 25 V	100	200	-	mS

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope. Designed primarily as a line current interrupter in telephone sets, it can also be applied in other applications such as in relays, line and highspeed transformer drivers etc.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

QUICK REFERENCE DATA

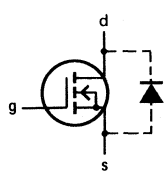
Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	300 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Drain-source ON-resistance I_D = 400 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	4.5 Ω 6 Ω
Transfer admittance I_D = 400 mA; V_{DS} = 25 V	$\|y_{fs}\|$	min. typ.	140 mS 350 mS

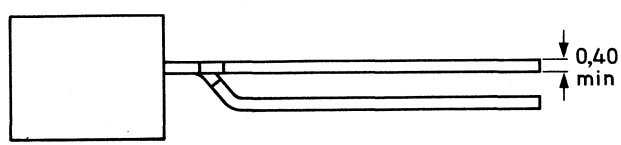
MECHANICAL DATA

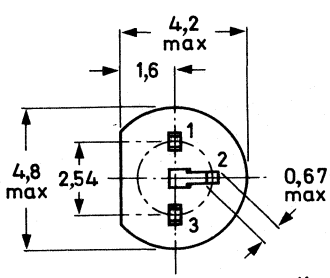
Dimensions in mm

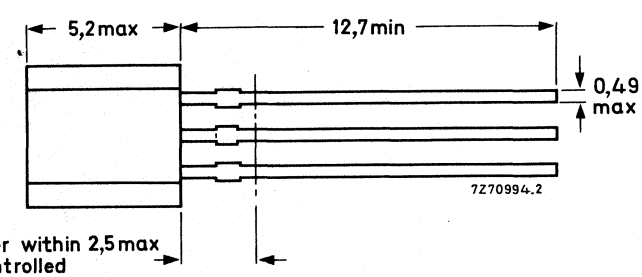
Fig. 1 TO-92 variant.

Pinning:
1 = gate
2 = drain
3 = source









FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

P-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

P-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope, intended for use in relay, high-speed and line-transformer drivers, and as a line current interruptor in telephony applications.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

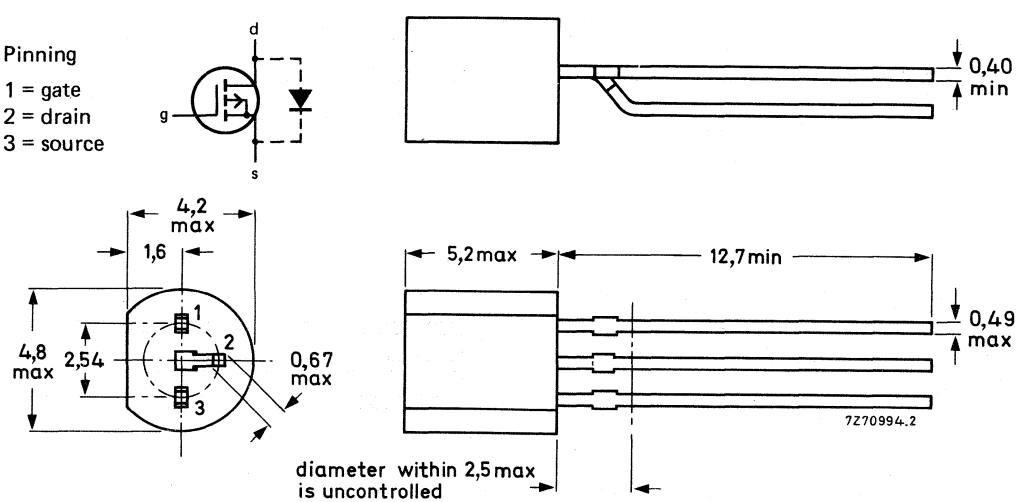
QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$-I_D$	max.	0.15 A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Drain-source ON-resistance $-I_D$ = 100 mA; $-V_{GS}$ = 10 V	R_{DSon}	typ. max.	10 Ω 20 Ω
Transfer admittance $-I_D$ = 100 mA; $-V_{DS}$ = 25 V	$\|y_{fs}\|$	min. typ.	60 mS 200 mS

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.



FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and designed for use as line current interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	250 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Drain-source ON-resistance I_D = 250 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	6 Ω 12 Ω
Transfer admittance I_D = 250 mA; V_{DS} = 15 V	$\lvert y_{fs} \rvert$	typ.	250 mS

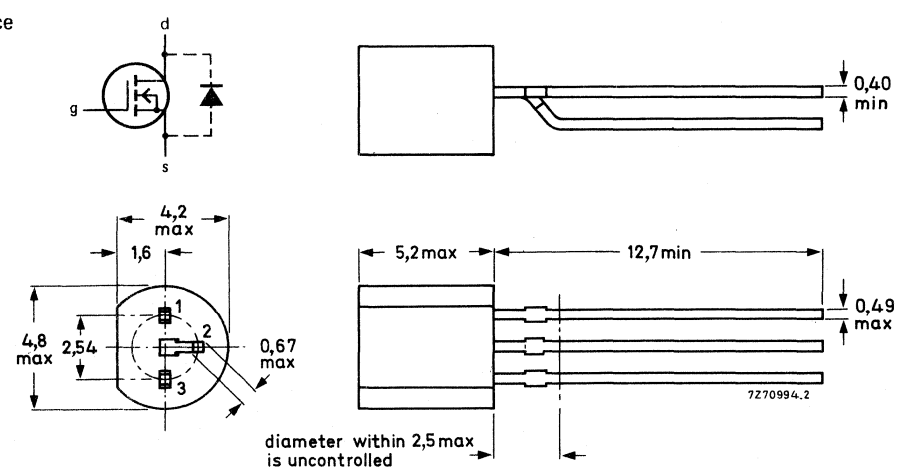
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning:

1 = source
2 = gate
3 = drain



Note: Various pinout configurations available.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

N-CHANNEL ENHANCEMENT MODE VERTICAL D-MOS TRANSISTOR

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and designed for use as line current interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

Features

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	180 V
Drain-source voltage (non-repetitive peak; $t_p \leqslant 2$ ms)	$V_{DS(SM)}$	max.	200 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	300 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1 W
Drain-source ON-resistance I_D = 15 mA; V_{GS} = 3 V	R_{DSon}	typ. max.	7 Ω 10 Ω
Transfer admittance I_D = 300 mA; V_{DS} = 15 V	$\lvert y_{fs} \rvert$	typ.	250 mS

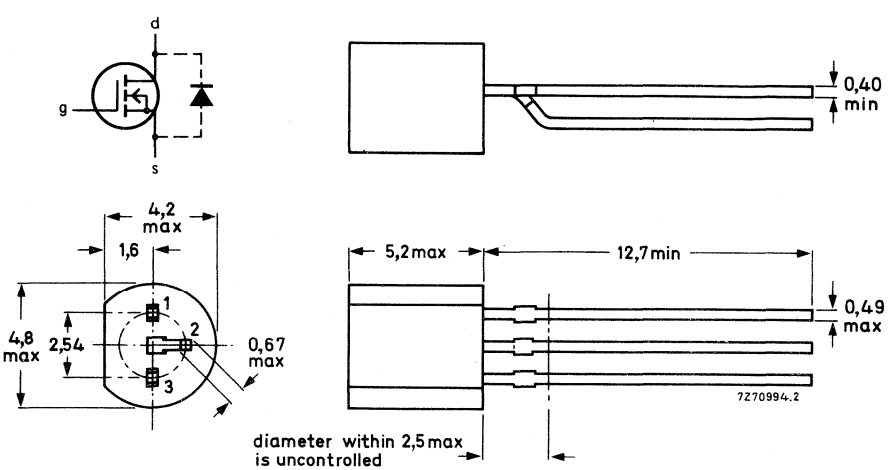
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning:

1 = source
2 = gate
3 = drain



Note: Various pinout configurations available.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATA SHEET

REGULATOR DIODES

Glass passivated diodes in hermetically sealed axial-leaded glass envelopes. They are intended for use as voltage regulator and transient suppressor diode in medium power regulation and transient suppression circuits.

The series consists of BZW03-C7V5 to BZW03-C510 in the normalized E24 range.

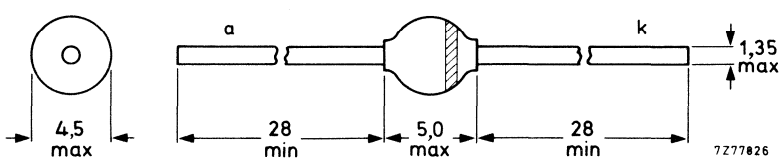
QUICK REFERENCE DATA

			voltage regulator	transient suppressor	
Working voltage range	V_Z	nom.	7,5 to 270		V
Stand-off voltage	V_R			6,2 to 430	V
Total power dissipation	P_{tot}	max.	6		W
Non-repetitive peak reverse power dissipation T_j = 25 °C; t_p = 100 μs	P_{RSM}			1000	W

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOD-64.



The marking band indicates the cathode.

Products approved to CECC 50 005-019.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC01 OR DATA SHEET

TRANSIENT SUPPRESSOR DIODE

A double-diffused silicon glass passivated diode in a hermetically sealed axial-leaded glass envelope intended for transient suppression in telephony equipment.

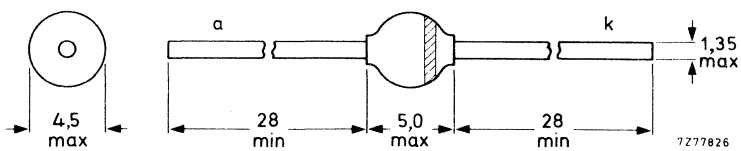
QUICK REFERENCE DATA

Stand-off voltage	V_R	max.	12 V
Non-repetitive peak reverse current	I_{RSM}	max.	50 A
Clamping voltage	$V_{(CL)R}$	<	28 V

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOD-64.



The marking band indicates the cathode.

MC3361
Low Power FM IF

Objective Specification

Linear Products

DESCRIPTION

The MC3361 is a monolithic low-power FM IF signal processing system consisting of an oscillator, mixer, limiting amplifier, quadrature detector, filter amplifier, squelch, scan control and mute switch. It is intended for use in narrow band FM dual conversion communications equipment. The MC3361 is available in a 16-lead, dual-in-line plastic package and 16-lead SO (surface-mounted miniature package).

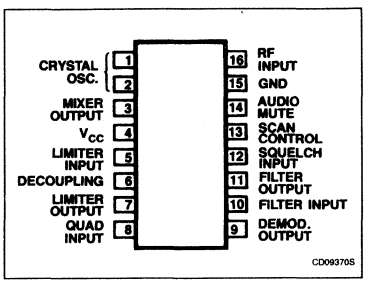
FEATURES

- **2.0V to 8.0V operation**
- **Low current: 4.2mA typ at V_{CC} = 4.0V_{DC}**
- **Excellent sensitivity: 2.0μV for -3dB limiting typ**
- **Low external parts count**
- **Operation to 60MHz**

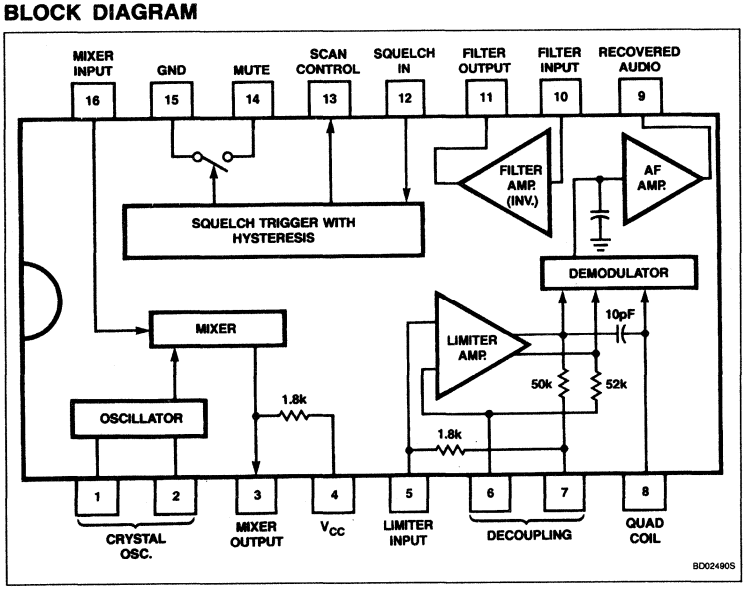
APPLICATIONS

- **Cordless telephone**
- **Narrow band receivers**
- **Remote control**

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0 to +70°C	MC3361N
16-Pin Plastic; SO (surface-mounted miniature package)	0 to +70°C	MC3361D

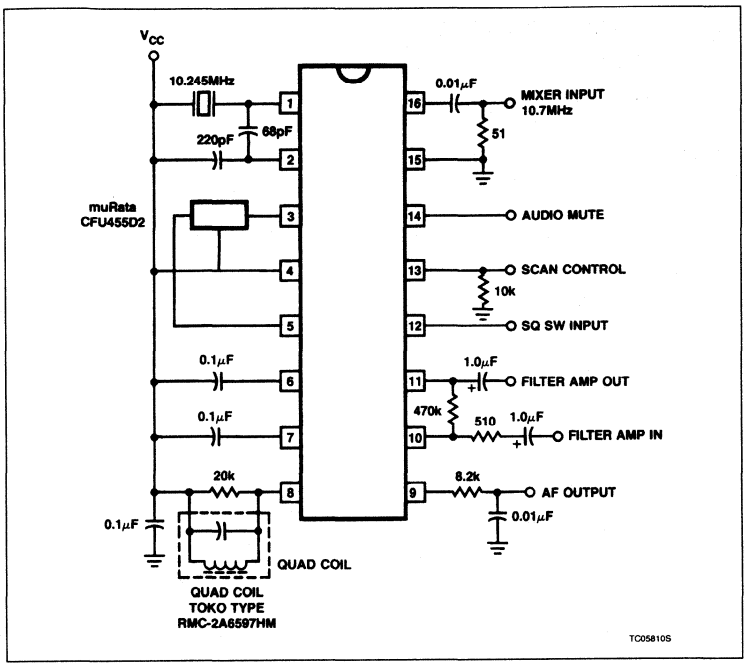
ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

SYMBOL	PARAMETER	PIN	RATING	UNIT
V_{CC} (Max)	Power supply voltage	4	10	V_{DC}
V_{CC}	Generating supply voltage range	4	2.0 to 8.0	V_{DC}
	Detector input voltage	8	1.0	V_{P-P}
V_{16}	Input voltage (V_{CC}≥4.0V)	16	1.0	V_{RMS}
V_{14}	Mute function	14	−0.5 to 5.0	V_{PK}
T_J	Junction temperature		150	°C
T_A	Operating ambient temperature range		−30 to +75	°C
T_{STG}	Storage temperature range		−65 to +150	°C

AC AND DC ELECTRICAL CHARACTERISTICS (V_{CC} = 4.0V_{DC}, f_O = 10.7MHz, Δf = ±3.0kHz, f_{MOD} = 1.0kHz, T_A = 25°C unless otherwise noted.)

PARAMETER	PIN	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Drain current (no signal) squelch off squelch on	4			 4.2 5.4	 7.0 9.0	mA
Input limiting voltage	16	−3.0dB limiting		2.0	6.0	μV
Detector output voltage	9			2.0		V_{DC}
Detector output impedance				450		Ω
Recovered audio output voltage	9	V_{IN} = 10mV_{RMS}	100	150	270	mV_{RMS}
Filter gain (10kHz)		V_{IN} = 1.0mV_{RMS}	40	46		dB
Filter output voltage	11			1.7		V_{DC}
Trigger hysteresis				50		mV
Mute function low	14			10		Ω
Mute function high	14			10		MΩ
Scan function low (mute off)	13	V_{12} = 1.0V_{DC}			0.5	V_{DC}
Scan function high (mute on)	13	V_{12} = GND	3.5			V_{DC}
Mixer conversion gain	3			27		dB
Mixer input resistance	16			3.6		kΩ
Mixer input capacitance	16			2.2		pF

TEST CIRCUIT



Compandor — NE570/571/SA571

DESCRIPTION

The NE570/571 is a versatile low cost dual gain control circuit in which either channel may be used as a dynamic range compressor or expandor. Each channel has a full-wave rectifier to detect the average value of the signal, a linerarized temperature-compensated variable gain cell, and an operational amplifier.

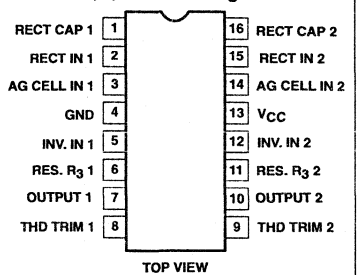
The NE570/571 is well suited for use in cellular radio and radio communications systems, modems, telephone, and satellite broadcast/receive audio systems.

FEATURES

- Complete compressor and expandor in one IChip
- Temperature compensated
- Greater than 110dB dynamic range
- Operates down to 6VDC
- System levels adjustable with external components
- Distortion may be trimmed out
- Dynamic noise reduction systems
- Voltage-controlled amplifier

PIN CONFIGURATION

D, F, and N Packages[1]



TOP VIEW

NOTE:
1. SOL - Released in Large SO Package Only.

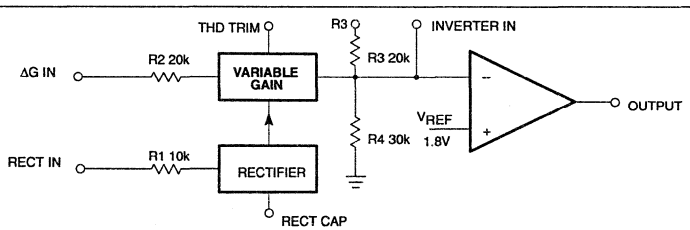
APPLICATIONS

- Cellular radio
- Telephone trunk compandor—570
- Telephone subscriber compandor—571
- High level limiter
- Low level expandor—noise gate
- Dynamic filters
- CD Player

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic SOL	0 to +70°C	NE570D
16-Pin Cerdip	0 to +70°C	NE570F
16-Pin Plastic DIP	0 to +70°C	NE570N
16-Pin Plastic SOL	0 to +70°C	NE571D
16-Pin Cerdip	0 to +70°C	NE571F
16-Pin Plastic DIP	0 to +70°C	NE571N
16-Pin Plastic SOL	-40 to +85°C	SA571D
16-Pin Cerdip	-40 to +85°C	SA571F
16-Pin Plastic DIP	-40 to +85°C	SA571N

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Maximum operating voltage 570 571	 24 18	VDC
T_A	Operating ambient temperature range NE SA	 0 to 70 -40 to +85	°C
P_D	Power dissipation	400	mW

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS NE570			LIMITS NE/SA571[5]			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		6		24	6		18	V
I_{CC}	Supply current	No signal		3.2	4.8		3.2	4.8	mA
I_{OUT}	Output current capability		±20			±20			mA
SR	Output slew rate			±.5			±.5		V/µs
	Gain cell distortion[2]	Untrimmed Trimmed		0.3 0.05	1.0		0.5 0.1	2.0	%
	Resistor tolerance			±5	±15		±5	±15	%
	Internal reference voltage		1.7	1.8	1.9	1.65	1.8	1.95	V
	Output DC shift[3]	Untrimmed		±20	±100		±30	±150	mV
	Expandor output noise	No signal, 15Hz-20kHz[1]		20	45		20	60	µV
	Unity gain level[6]	1kHz	-1	0	+1	-1.5	0	+1.5	dBm
	Gain change[2, 4]			±0.1	±0.2		±0.1		dB
	Reference drift[4]			±5	±10		+2, -25	+20, -50	mV
	Resistor drift[4]			+1, -0			+8, -0		%
	Tracking error (measured relative to value at unity gain) equals [V_O - V_O (unity gain)] dB - V_2dBm	Rectifier input, V_2 = +6dBm, V_1 = 0dB V_2 = -30dBm, V_1 = 0dB		+0.2 +0.2	 -0.5, +1		+0.2 +0.2	 -1, +1.5	dB
	Channel separation			60			60		dB

NOTES:
1. Input to V_1 and V_2 grounded.
2. Measured at 0dBm, 1kHz.
3. Expandor AC input change from no signal to 0dBm.
4. Relative to value at T_A = 25°C.
5. Electrical characteristics for the SA571 only are specified over -40 to +85°C temperature range.
6. 0dBm = 775mV_{RMS}.

CIRCUIT DESCRIPTION

The NE570/571 compandor building blocks, as shown in the block diagram, are a full-wave rectifier, a variable gain cell, an operational amplifier and a bias system. The arrangement of these blocks in the IC result in a circuit which can perform well with few external components, yet can be adapted to many diverse applications.

The full-wave rectifier rectifies the input current which flows from the rectifier input, to an internal summing node which is biased at V_{REF}. The rectified current is averaged on an external filter capacitor tied to the C_{RECT} terminal, and the average value of the input current controls the gain of the variable gain cell. The gain will thus be proportional to the average value of the input signal for capacitively-coupled voltage inputs as shown in the following equation. Note that for capacitively-coupled inputs there is no offset voltage capable of producing a gain error. The only error will come from the bias current of the rectifier (supplied internally) which is less than 0.1μA.

$$G \propto \frac{|V_{IN} - V_{REF}|_{avg}}{R_1}$$

or

$$G \propto \frac{|V_{IN}|_{avg}}{R_1}$$

The speed with which gain changes to follow changes in input signal levels is determined by the rectifier filter capacitor. A small capacitor will yield rapid response but will not fully filter low frequency signals. Any ripple on the gain control signal will modulate the signal passing through the variable gain cell. In an expander or compressor application, this would lead to third harmonic distortion, so there is a trade-off to be made between fast attack and decay times and distortion. For step changes in amplitude, the change in gain with time is shown by this equation.

$$G(t) = (G_{initial} - G_{final})_e^{-t/\tau} + G_{final} \; ; \; \tau = 10k \times C_{RECT}$$

The variable gain cell is a current-in, current-out device with the ratio I_{OUT}/I_{IN} controlled by the rectifier. I_{IN} is the current which flows from the ΔG input to an internal summing node biased at V_{REF}. The following equation applies for capacitively-coupled inputs. The output current, I_{OUT}, is fed to the summing node of the op amp.

$$I_{IN} = \frac{V_{IN} - V_{REF}}{R_2} = \frac{V_{IN}}{R_2}$$

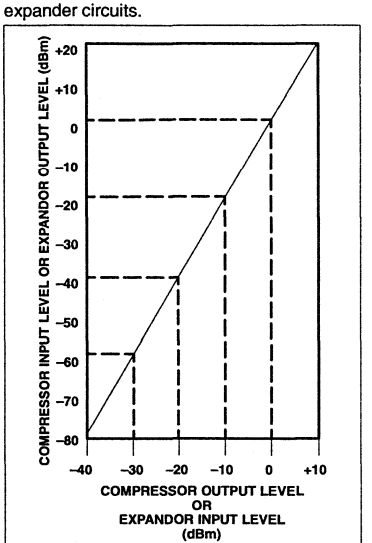
A compensation scheme built into the ΔG cell compensates for temperature and cancels out odd harmonic distortion. The only distortion which remains is even harmonics, and they exist only because of internal offset voltages. The THD trim terminal provides a means for nulling the internal offsets for low distortion operation.

The operational amplifier (which is internally compensated) has the non-inverting input tied to V_{REF}, and the inverting input connected to the ΔG cell output as well as brought out externally. A resistor, R_3, is brought out from the summing node and allows compressor or expander gain to be determined only by internal components.

The output stage is capable of ±20mA output current. This allows a +13dBm ($3.5V_{RMS}$) output into a 300Ω load which, with a series resistor and proper transformer, can result in +13dBm with a 600Ω output impedance.

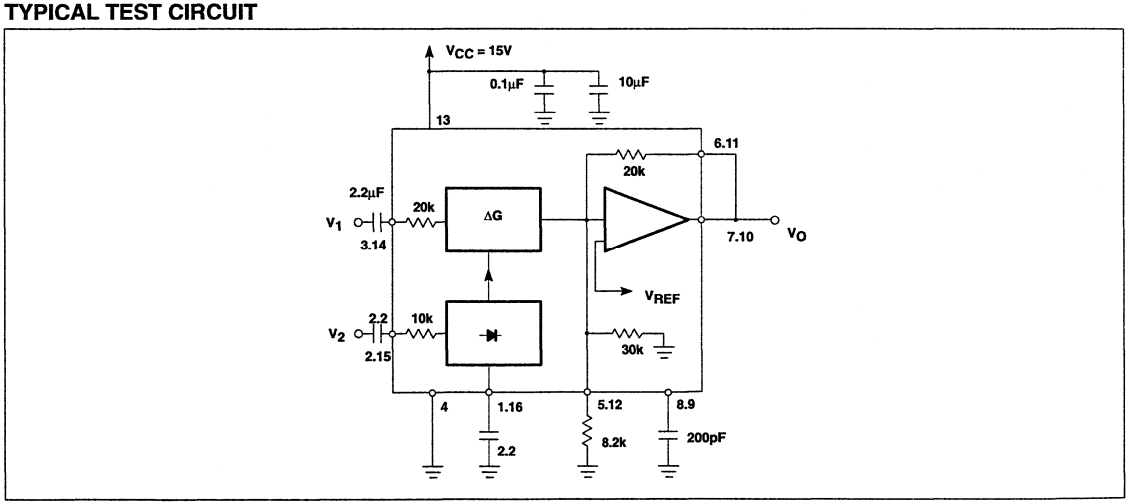
A bandgap reference provides the reference voltage for all summing nodes, a regulated supply voltage for the rectifier and ΔG cell, and a bias current for the ΔG cell. The low tempco of this type of reference provides very stable biasing over a wide temperature range.

The typical performance characteristics illustration shows the basic input-output transfer curve for basic compressor or expander circuits.



Basic Input-Output Transfer Curve

TYPICAL TEST CIRCUIT



INTRODUCTION

Much interest has been expressed in high performance electronic gain control circuits. For non-critical applications, an integrated circuit operational transconductance amplifier can be used, but when high-performance is required, one has to resort to complex discrete circuitry with many expensive, well-matched components. This paper describes an inexpensive integrated circuit, the NE570 Compandor, which offers a pair of high performance gain control circuits featuring low distortion (<0.1%), high signal-to-noise ratio (90dB), and wide dynamic range (110dB).

CIRCUIT BACKGROUND

The NE570 Compandor was originally designed to satisfy the requirements of the telephone system. When several telephone channels are multiplexed onto a common line, the resulting signal-to-noise ratio is poor and companding is used to allow a wider dynamic range to be passed through the channel. Figure 1 graphically shows what a compandor can do for the signal-to-noise ratio of a restricted dynamic range channel. The input level range of +20 to -80dB is shown undergoing a 2-to-1 compression where a 2dB input level change is compressed into a 1dB output level change by the compressor. The original 100dB of dynamic range is thus compressed to a 50dB range for transmission through a restricted dynamic range channel. A complementary expansion on the receiving end restores the original signal levels and reduces the channel noise by as much as 45dB.

The significant circuits in a compressor or expander are the rectifier and the gain control element. The phone system requires a simple full-wave averaging rectifier with good accuracy, since the rectifier accuracy determines the (input) output level tracking accuracy. The gain cell determines the distortion and noise characteristics, and the phone system specifications here are very loose. These specs could have been met with a simple operational transconductance multiplier, or OTA, but the gain of an OTA is proportional to temperature and this is very undesirable. Therefore, a linearized transconductance multiplier was designed which is insensitive to temperature and offers low noise and low distortion performance. These features make the circuit useful in audio and data systems as well as in telecommunications systems.

BASIC CIRCUIT HOOK-UP AND OPERATION

Figure 2 shows the block diagram of one half of the chip, (there are two identical channels on the IC). The full-wave averaging rectifier provides a gain control current, I_G, for the variable gain (ΔG) cell. The output of the ΔG cell is a current which is fed to the summing node of the operational amplifier. Resistors are provided to establish circuit gain and set the output DC bias.

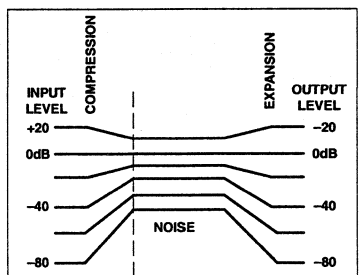


Figure 1. Restricted Dynamic Range Channel

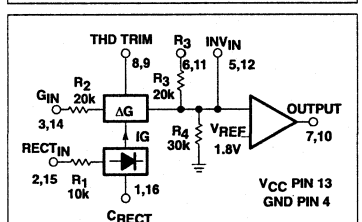


Figure 2. Chip Block Diagram (1 of 2 Channels)

The circuit is intended for use in single power supply systems, so the internal summing nodes must be biased at some voltage above ground. An internal band gap voltage reference provides a very stable, low noise 1.8V reference denoted V_{REF}. The non-inverting input of the op amp is tied to V_{REF}, and the summing nodes of the rectifier and ΔG cell (located at the right of R_1 and R_2) have the same potential. The THD trim pin is also at the V_{REF} potential.

Figure 3 shows how the circuit is hooked up to realize an expandor. The input signal, V_{IN}, is applied to the inputs of both the rectifier and the ΔG cell. When the input signal drops by 6dB, the gain control current will drop by a factor of 2, and so the gain will drop 6dB. The output level at V_{OUT} will thus drop 12dB, giving us the desired 2-to-1 expansion.

Figure 4 shows the hook-up for a compressor. This is essentially an expandor placed in the feedback loop of the op amp. The ΔG cell is setup to provide AC feedback only, so a separate DC feedback loop is provided by the two R_{DC} and C_{DC}. The values of R_{DC} will determine the DC bias at the output of the op amp. The output will bias to:

$$V_{OUT}\ DC = 1 + \frac{R_{DC1} + R_{DC2}}{R_4}$$

$$V_{REF} = \left(1 + \frac{R_{DCTOT}}{30k}\right) 1.8V$$

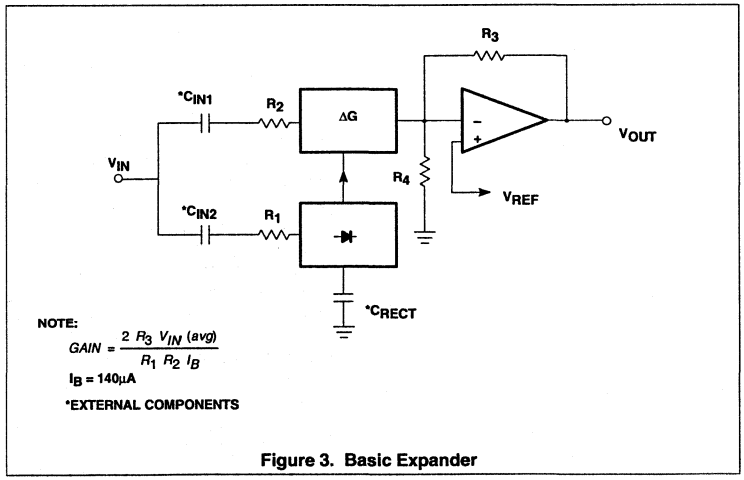


Figure 3. Basic Expander

The output of the expander will bias up to:

$$V_{OUT}\ DC = 1 + \frac{R_3}{R_4}\ V_{REF}$$

$$V_{REF} = \left(1 + \frac{20k}{30k}\right) 1.8V = 3.0V$$

The output will bias to 3.0V when the internal resistors are used. External resistors may be placed in series with R_3, (which will affect the gain), or in parallel with R_4 to raise the DC bias to any desired value.

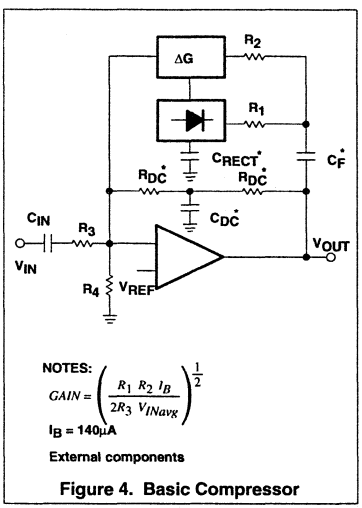


Figure 4. Basic Compressor

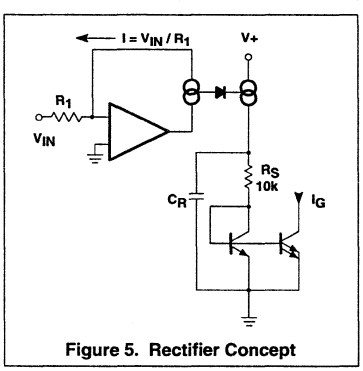


Figure 5. Rectifier Concept

CIRCUIT DETAILS—RECTIFIER

Figure 5 shows the concept behind the full-wave averaging rectifier. The input current to the summing node of the op amp, $V_{IN}R_1$, is supplied by the output of the op amp. If we can mirror the op amp output current into a unipolar current, we will have an ideal rectifier. The output current is averaged by R_5, CR, which set the averaging time constant, and then mirrored with a gain of 2 to become I_G, the gain control current.

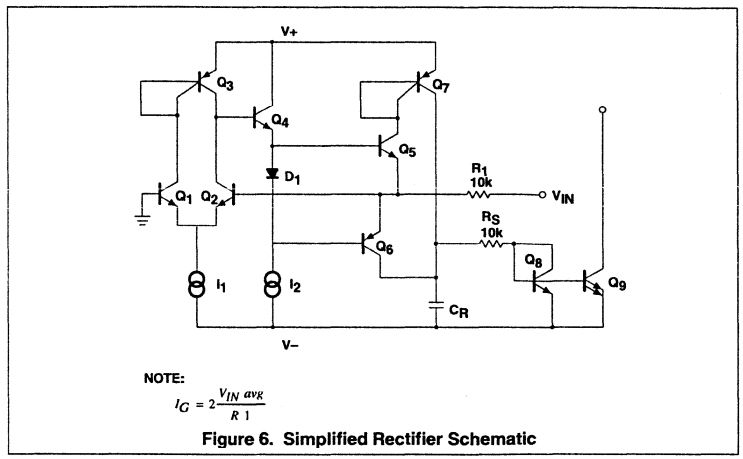


Figure 6. Simplified Rectifier Schematic

Figure 6 shows the rectifier circuit in more detail. The op amp is a one-stage op amp, biased so that only one output device is on at a time. The non-inverting input, (the base of Q_1), which is shown grounded, is actually tied to the internal 1.8V V_{REF}. The inverting input is tied to the op amp output, (the emitters of Q_5 and Q_6), and the input summing resistor R_1. The single diode between the bases of Q_5 and Q_6 assures that only one device is on at a time. To detect the output current of the op amp, we simply use the collector currents of the output devices Q_5 and Q_6. Q_6 will conduct when the input swings positive and Q_5 conducts when the input swings negative. The collector currents will be in error by the *a* of Q_5 or Q_6 on negative or positive signal swings, respectively. ICs such as this have typical NPN βs of 200 and PNP βs of 40. The *a*'s of 0.995 and 0.975 will produce errors of 0.5% on negative swings and 2.5% on positive swings. The 1.5% average of these errors yields a mere 0.13dB gain error.

At very low input signal levels the bias current of Q_2, (typically 50nA), will become significant as it must be supplied by Q_5. Another low level error can be caused by DC coupling into the rectifier. If an offset voltage exists between the V_{IN} input pin and the base of Q_2, an error current of V_{OS}/R_1 will be generated. A mere 1mV of offset will cause an input current of 100nA which will produce twice the error of the input bias current. For highest accuracy, the rectifier should be coupled into capacitively. At high input levels the β of the PNP Q_6 will begin to suffer, and there will be an increasing error until the circuit saturates. Saturation can be avoided by limiting the current into the rectifier input to 250μA. If necessary, an external resistor may be placed in series with R_1 to limit the current to this value. Figure 7 shows the rectifier accuracy vs input level at a frequency of 1kHz.

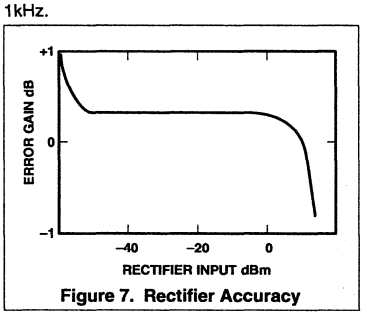


Figure 7. Rectifier Accuracy

At very high frequencies, the response of the rectifier will fall off. The roll-off will be more pronounced at lower input levels due to the increasing amount of gain required to switch between Q_5 or Q_6 conducting. The rectifier frequency response for input levels of 0dBm, -20dBm, and -40dBm is shown in Figure 8. The response at all three levels is flat to well above the audio range.

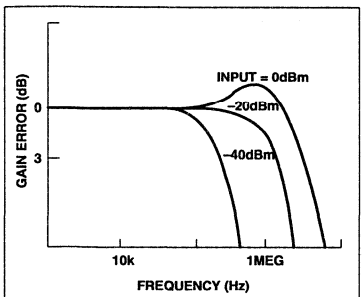


Figure 8. Rectifier Frequency Response vs Input Level

VARIABLE GAIN CELL

Figure 9 is a diagram of the variable gain cell. This is a linearized two-quadrant transconductance multiplier. Q_1, Q_2 and the op amp provide a predistorted drive signal for the gain control pair, Q_3 and Q_4. The gain is controlled by I_G and a current mirror provides the output current.

The op amp maintains the base and collector of Q_1 at ground potential (V_{REF}) by controlling the base of Q_2. The input current I_{IN} ($=V_{IN}/R_2$) is thus forced to flow through Q_1 along with the current I_1, so $I_{C1}=I_1+I_{IN}$. Since I_2 has been set at twice the value of I_1, the current through Q_2 is:

$I_2-(I_1+I_{IN})=I_1-I_{IN}=I_{C2}$.

The op amp has thus forced a linear current swing between Q_1 and Q_2 by providing the proper drive to the base of Q_2. This drive signal will be linear for small signals, but very non-linear for large signals, since it is compensating for the non-linearity of the differential pair, Q_1 and Q_2, under large signal conditions.

The key to the circuit is that this same predistorted drive signal is applied to the gain control pair, Q_3 and Q_4. When two differential pairs of transistors have the same signal applied, their collector current ratios will be identical regardless of the magnitude of the currents. This gives us:

$$\frac{I_{C1}}{I_{C2}} = \frac{I_{C4}}{I_{C3}} = \frac{I_1 + I_{IN}}{I_1 - I_{IN}}$$

plus the relationships $I_G=I_{C3}+I_{C4}$ and $I_{OUT}=I_{C4}-I_{C3}$ will yield the multiplier transfer function,

$$I_{OUT} = \frac{I_G}{I_1} I_{IN} = \frac{V_{IN}}{R_2}\frac{I_G}{I_1}$$

This equation is linear and temperature-insensitive, but it assumes ideal transistors.

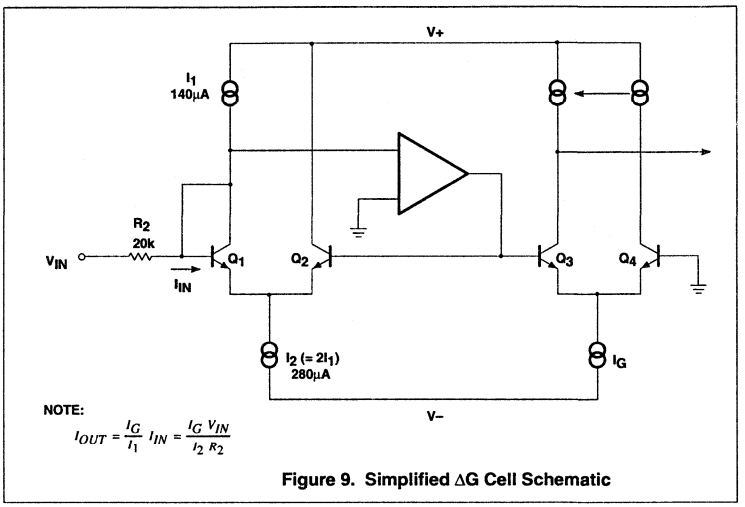


Figure 9. Simplified ΔG Cell Schematic

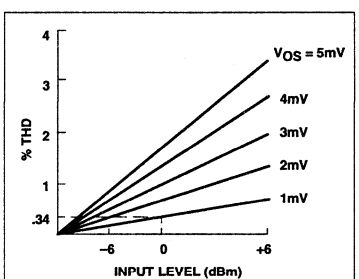


Figure 10. ΔG Cell Distortion vs Offset Voltage

If the transistors are not perfectly matched, a parabolic, non-linearity is generated, which results in second harmonic distortion. Figure 10 gives an indication of the magnitude of the distortion caused by a given input level and offset voltage. The distortion is linearly proportional to the magnitude of the offset and the input level. Saturation of the gain cell occurs at a +8dBm level. At a nominal operating level of 0dBm, a 1mV offset will yield 0.34% of second harmonic distortion. Most circuits are somewhat better than this, which means our overall offsets are typically about mV. The distortion is not affected by the magnitude of the gain control current, and it does not increase as the gain is changed. This second harmonic distortion could be eliminated by making perfect transistors, but since that would be difficult, we have had to resort to other methods. A trim pin has been provided to allow trimming of the internal offsets to zero, which effectively eliminated second harmonic distortion. Figure 11 shows the simple trim network required.

Figure 12 shows the noise performance of the ΔG cell. The maximum output level before clipping occurs in the gain cell is plotted along with the output noise in a 20kHz bandwidth. Note that the noise drops as the gain is reduced for the first 20dB of gain reduction. At high gains, the signal to noise ratio is 90dB, and the total dynamic range from maximum signal to minimum noise is 110dB.

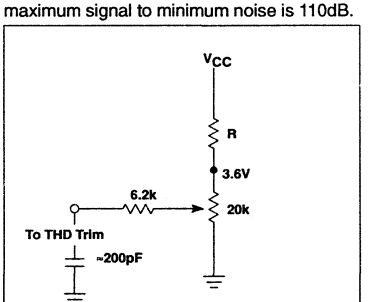


Figure 11. THD Trim Network

Control signal feedthrough is generated in the gain cell by imperfect device matching and mismatches in the current sources, I_1 and I_2. When no input signal is present, changing I_G will cause a small output signal. The distortion trim is effective in nulling out any control signal feedthrough, but in general, the null for minimum feedthrough will be different than the null in distortion. The control signal feedthrough can be trimmed independently of distortion by tying a current source to the ΔG

input pin. This effectively trims I_1. Figure 13 shows such a trim network.

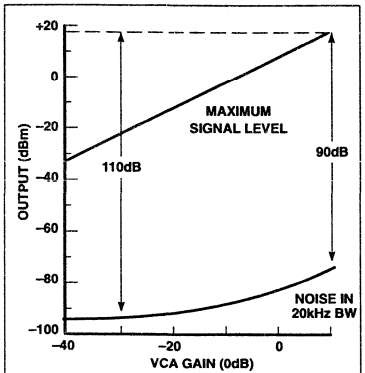


Figure 12. Dynamic Range of NE570

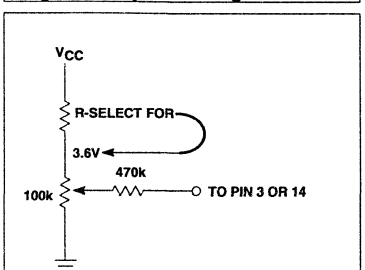


Figure 13. Control Signal Feedthrough Trim

OPERATIONAL AMPLIFIER

The main op amp shown in the chip block diagram is equivalent to a 741 with a 1MHz bandwidth. Figure 14 shows the basic circuit. Split collectors are used in the input pair to reduce g_M, so that a small compensation capacitor of just 10pF may be used. The output stage, although capable of output currents in excess of 20mA, is biased for a low quiescent current to conserve power. When driving heavy loads, this leads to a small amount of crossover distortion.

RESISTORS

Inspection of the gain equations in Figures 3 and 4 will show that the basic compressor and expander circuit gains may be set entirely by resistor ratios and the internal voltage reference. Thus, any form of resistors that match well would suffice for these simple hook-ups, and absolute accuracy and temperature coefficient would be of no importance. However, as one starts to modify the gain equation with external resistors, the internal resistor accuracy and tempco become very significant. Figure 15 shows the effects of temperature on the diffused resistors which are normally used in integrated circuits, and the ion-implanted resistors which are used in this circuit. Over the critical 0°C to +70°C temperature range, there is a 10-to-1 improvement in drift from a 5% change for the diffused resistors, to a 0.5% change for the implemented resistors. The implanted resistors have another advantage in that they can be made the size of the diffused resistors due to the higher resistivity. This saves a significant amount of chip area.

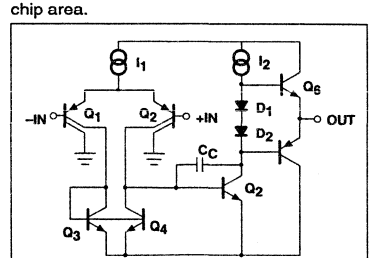


Figure 14. Operational Amplifier

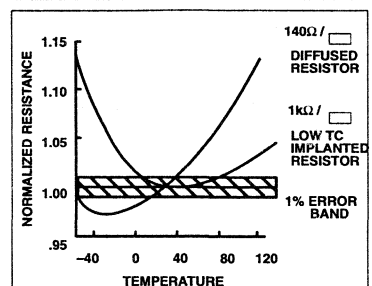


Figure 15. Resistance vs Temperature

NE/SA572
Programmable Analog Compandor

Product Specification

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATA SHEET

DESCRIPTION

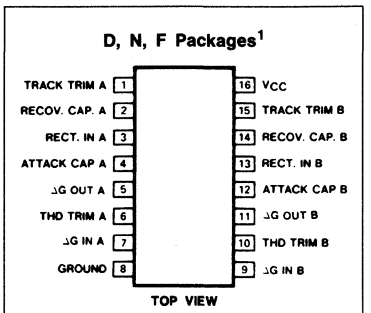
The NE572 is a dual-channel, high-performance gain control circuit in which either channel may be used for dynamic range compression or expansion. Each channel has a full-wave rectifier to detect the average value of input signal, a linearized, temperature-compensated variable gain cell (ΔG) and a dynamic time constant buffer. The buffer permits independent control of dynamic attack and recovery time with minimum external components and improved low frequency gain control ripple distortion over previous compandors.

The NE572 is intended for noise reduction in high-performance audio systems. It can also be used in a wide range of communication systems and video recording applications.

FEATURES

- **Independent control of attack and recovery time**
- **Improved low frequency gain control ripple**
- **Complementary gain compression and expansion with external op amp**
- **Wide dynamic range — greater than 110dB**
- **Temperature-compensated gain control**
- **Low distortion gain cell**
- **Low noise — 6μV typical**
- **Wide supply voltage range — 6V – 22V**
- **System level adjustable with external components**

PIN CONFIGURATION



NOTE:
1. D package released in large SO (SOL) package only.

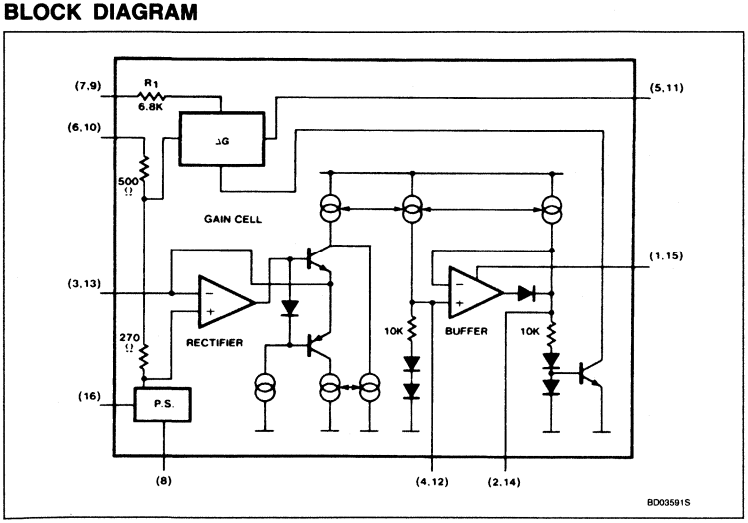
APPLICATIONS

- **Dynamic noise reduction system**
- **Voltage control amplifier**
- **Stereo expandor**
- **Automatic level control**
- **High-level limiter**
- **Low-level noise gate**
- **State variable filter**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic SO	0 to +70°C	NE572D
16-Pin Plastic DIP	0 to +70°C	NE572N
16-Pin Plastic SO	-40°C to +85°C	SA572D
16-Pin Cerdip	-40°C to +85°C	SA572F
16-Pin Plastic DIP	-40°C to +85°C	SA572N

BLOCK DIAGRAM



Low voltage compandor — NE/SA575A

DESCRIPTION

The NE/SA575A is a precision dual gain control circuit designed for low voltage applications. The NE/SA575A's channel 1 is an expandor, while channel 2 can be configured either for expandor, compressor, or automatic level controller (ALC) application.

The NE/SA575A replaces the NE/SA575 and offers improved performance such as 1mA less supply current, low voltage operation down to 2V and 3000V ESD protection.

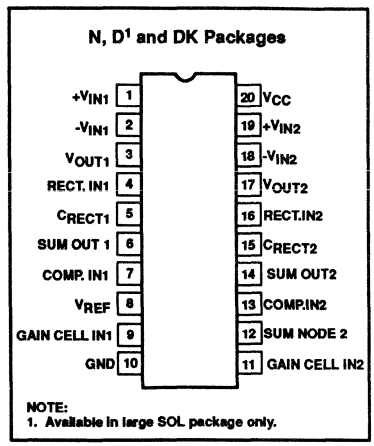
FEATURES

- Operating voltage range from 2V to 7V
- Reference voltage of $100mV_{RMS}$ = 0dB
- One dedicated summing op amp per channel and two extra uncommitted op amps
- 600Ω drive capability
- Single or split supply operation
- Wide input/output swing capability
- 3000V ESD protection

APPLICATIONS

- Portable communications
- Cellular radio
- Cordless telephone
- Consumer audio
- Portable broadcast mixers
- Wireless microphones
- Modems
- Electric organs
- Hearing aids

PIN CONFIGURATION



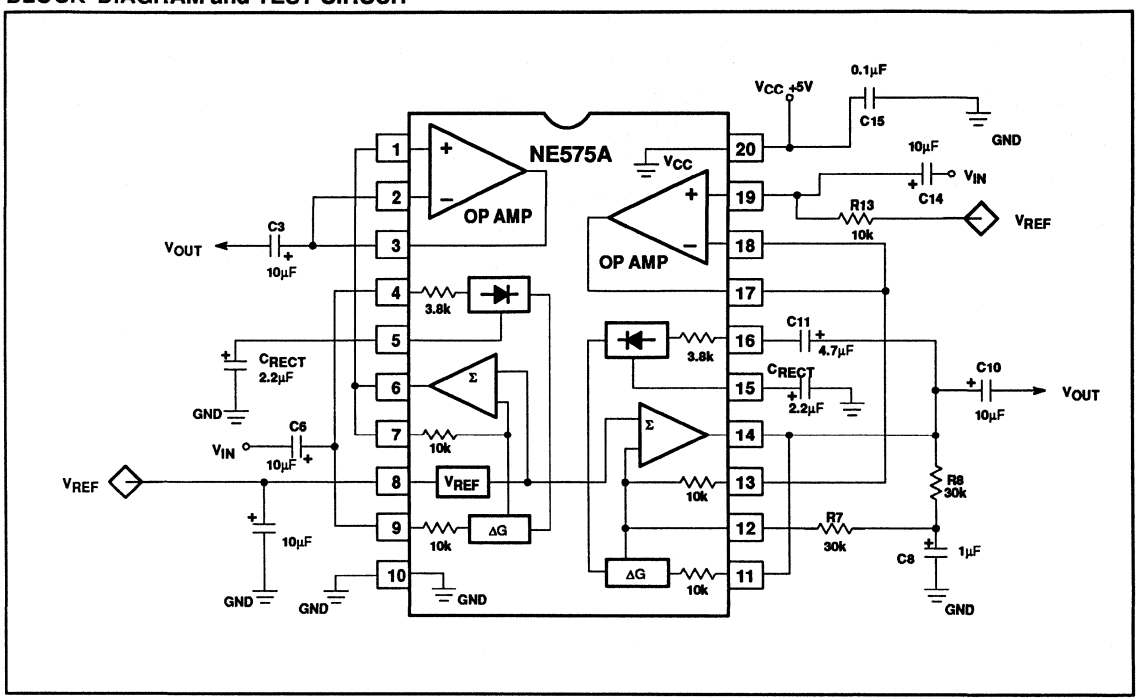
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG
20-Pin Plastic DIP	0 to +70°C	NE575AN	0408
20-Pin Plastic SOL	0 to +70°C	NE575AD	0172
20-Pin Plastic SSOP	0 to +70°C	NE575ADK	1563
20-Pin Plastic DIP	-40 to +85°C	SA575AN	0408
20-Pin Plastic SOL	-40 to +85°C	SA575AD	0172
20-Pin Plastic SSOP	-40 to +85°C	SA575ADK	1563

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		RATING		UNITS
			NE575A	SA575A	
V_{CC}	Single supply voltage		–0.3 to 8	–0.3 to 8	V
V_{IN}	Voltage applied to any other pin		–0.3 to (V_{CC}+0.3)	–0.3 to (V_{CC}+0.3)	V
T_A	Operating ambient temperature range		-40 to +85	-40 to +85	°C
T_{STG}	Storage temperature range		-65 to +150	-65 to +150	°C
θ_{JA}	Thermal impedance	DIP	68	68	°C/W
		SOL	112	112	°C/W
		SSOP	117	117	°C/W

BLOCK DIAGRAM and TEST CIRCUIT



DC ELECTRICAL CHARACTERISTICS

Typical values are at T_A = 25°C. Minimum and Maximum values are for the full operating temperature range: 0 to 70°C for NE575A, -40 to +85°C for SA575A, except SSOP package is tested at +25°C only. V_{CC} = 5V, unless otherwise stated. Both channels are tested in the Expandor mode (see Test Circuit)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE575A			SA575A			
			MIN	TYP	MAX	MIN	TYP	MAX	
For compandor, including summing amplifier									
V_{CC}	Supply voltage[1]		3	5	7	3	5	7	V
I_{CC}	Supply current	No signal		3.8	4.5		3.8	4.5	mA
V_{REF}	Reference voltage[2]	V_{CC} = 5V	2.4	2.5	2.6	2.4	2.5	2.6	V
R_L	Summing amp output load		10			10			kΩ
THD	Total harmonic distortion	1kHz, 0dB BW = 3.5kHz		0.12	1.0		0.12	1.5	%
E_{NO}	Output voltage noise	BW = 20kHz, R_S = 0Ω		6	20		6	30	µV
0dB	Unity gain level	1kHz	-1.0		1.0	-1.5		1.5	dB
V_{OS}	Output voltage offset	No signal	-100		100	-150		150	mV
	Output DC shift	No signal to 0dB	-50		50	-100		100	mV
	Tracking error relative to 0dB	Gain cell input = 0dB, 1kHz Rectifier input = 6dB, 1kHz	-0.5		0.5	-1.0		1.0	dB
		Gain cell input = 0dB, 1kHz Rectifier input = -30dB, 1kHz	-0.5		0.5	-1.0		1.0	dB

DC ELECTRICAL CHARACTERISTICS (cont.)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE575A			SA575A			
			MIN	TYP	MAX	MIN	TYP	MAX	
	Crosstalk	1kHz, 0dB, C_{REF} = 220µF		-80	-65		-80	-65	dB
For operational amplifier									
V_O	Output swing	R_L = 10kΩ	V_{CC}-0.4	V_{CC}		V_{CC}-0.4	V_{CC}		V
R_L	Output load	1kHz	600			600			Ω
CMR	Input common-mode range		0		V_{CC}	0		V_{CC}	V
CMRR	Common-mode rejection ratio		60	75		60	75		dB
I_B	Input bias current	V_{IN} = 0.5V to 4.5V	-0.5		0.5	-1		1	µA
V_{OS}	Input offset voltage			2.5			2.5		mV
A_{VOL}	Open-loop gain	R_L = 10kΩ		80			80		dB
SR	Slew rate	Unity gain		1			1		V/µs
GBW	Bandwidth	Unity gain		3			3		MHz
E_{NI}	Input voltage noise	BW = 20kHz		2.5			2.5		µV
PSRR	Power supply rejection ratio	1kHz, 250mV		60			60		dB

NOTES:
1. Operation down to V_{CC} = 2V is possible, but performance is reduced. See curves in Figure 5a and 5b.
2. Reference voltage, V_{REF}, is typically at 1/2V_{CC}.

FUNCTIONAL DESCRIPTION

This section describes the basic subsystems and applications of the NE/SA575A Compandor. More theory of operation on compandors can be found in AN174 and AN176. The typical applications of the NE/SA575A low voltage compandor in an Expandor (1:2), Compressor (2:1) and Automatic Level Control (ALC) function are explained. These three circuit configurations are shown in Figures 1, 2, 3 respectively.

The NE/SA575A has two channels for a complete companding system. The left channel, A, can be configured as a 1:2 Expandor while the right channel, B, can be configured as either a 2:1 Compressor, a 1:2 Expandor or an ALC. Each channel consists of the basic companding building blocks of rectifier cell, variable gain cell, summing amplifier and V_{REF} cell. In addition, the NE/SA575A has two additional high performance uncommitted op amps which can be utilized for application such as filtering, pre-emphasis/de-emphasis or buffering.

Figure 4 shows the complete schematic for the applications demo board. Channel A is configured as an expandor while channel B is configured so that it can be used either as a compressor or as an ALC circuit. The switch, S1, toggles the circuit between compressor and ALC mode. Jumpers J1 and J2 can be used to either include the additional op amps for signal conditioning or exclude them from the signal path. Bread boarding space is provided for R1, R2, C1, C2, R10, R11, C10 and C11 so that the response can be tailored for each individual need. The components as specified are suitable for the complete audio spectrum from 20Hz to 20kHz.

The most common configuration is as a unity gain non-inverting buffer where R1, C1, C2, R10, C10 and C11 are eliminated and R2 and R11 are shorted. Capacitors C3, C5, C8, and C12 are for DC blocking. In systems where the inputs and outputs are AC coupled, these capacitors and resistors can be eliminated. Capacitors C4 and C9 are for setting the attack and release time constant.

C6 is for decoupling and stabilizing the voltage reference circuit. The value of C6 should be such that it will offer a very low impedance to the lowest frequencies of interest. Too small a capacitor will allow supply ripple to modulate the audio path. The better filtered the power supply, the smaller this capacitor can be. R12 provides DC reference voltage to the amplifier of channel B. R6 and R7 provide a DC feedback path for the summing amp of channel B, while C7 is a short-circuit to ground for signals. C14 and C15 are for power supply decoupling. C14 can also be eliminated if the power supply is well regulated with very low noise and ripple.

DEMONSTRATED PERFORMANCE

The applications demo board was built and tested for a frequency range of 20Hz to 20kHz with the component values as shown in Figure 4 and V_{CC} = 5V. In the expandor mode, the typical input dynamic range was from -34dB to +12dB where 0dB is equal to 100mV_{RMS}. The typical unity gain level measured at 0dB @ 1kHz input was ±0.5dB and the typical tracking error was ±0.1dB for input range of -30 to +10dB.
In the compressor mode, the typical input dynamic range was from -42dB to ±18dB with a tracking error +0.1dB and the typical unity gain level was ±0.5dB.
In the ALC mode, the typical input dynamic range was from -42dB to +8dB with typical output deviation of ±0.2dB about the nominal output of 0dB. For input greater than +9dB in ALC configuration, the summing amplifier sometimes exhibits high frequency oscillations. There are several solutions to this problem. The first is to lower the values of R6 and R7 to 20kΩ each. The second is to add a current limiting resistor in series with C12 at Pin 13. The third is to add a compensating capacitor of about 22 to 30pF between the input and output of summing amplifier (Pins 12 and 14). With any one of the above recommendations, the typical ALC mode input range increased to +18dB yielding a dynamic range of over 60dB.

EXPANDOR

The typical expandor configuration is shown in Figure 1. The variable gain cell and the rectifier cell are in the signal input path. The V_{REF} is always 1/2 V_{CC} to provide the maximum headroom without clipping. The 0dB ref is 100mV_{RMS}. The input is AC coupled through C5, and the output is AC coupled through C3. If in a system the inputs and outputs are AC coupled, then C3 and C5 can be eliminated, thus requiring only one external component, C4. The variable gain

cell and rectifier cell are DC coupled so any offset voltage between Pins 4 and 9 will cause small offset error current in the rectifier cell. This will affect the accuracy of the gain cell. This can be improved by using an extra capacitor from the input to Pin 4 and eliminating the DC connection between Pins 4 and 9.

The expandor gain expression and the attack and release time constant is given by Equation 1 and Equation 2, respectively.

Equation 1.

$$\text{Expandor gain} = \frac{4V_{IN(avg)}}{3.8k \times 100\mu A}$$

where $V_{IN(avg)} = 0.95V_{IN(RMS)}$

Equation 2.

$$\tau_R = \tau_A = 10k \times C_{RECT} = 10k \times C4$$

COMPRESSOR

The typical compressor configuration is shown in Figure 2. In this mode, the rectifier cell and variable gain cell are in the feedback path. R6 and R7 provide the DC feedback to the summing amplifier. The input is AC coupled through C12 and output is AC coupled through C8. In a system with inputs and outputs AC coupled, C8 and C12 could be eliminated and only R6, R7, C7, and C13 would be required. If the external components R6, R7 and C7 are eliminated, then the output of the summing amplifier will motor-boat in absence of signals or at extremely low signals. This is because there is no DC feedback path from the output to input. In the presence of an AC signal this phenomenon is not observed and the circuit will appear to function properly.

The compressor gain expression and the attack and release time constant is given by Equation 3 and Equation 4, respectively.

Equation 3.

$$\text{Compressor gain} = \left[\frac{3.8k \times 100\mu A}{4V_{IN(avg)}}\right]^{1/2}$$

where $V_{IN(avg)} = 0.95V_{IN(RMS)}$

Equation 4.

$$\tau_R = \tau_A = 10k \times C_{RECT} = 10k \times C4$$

AUTOMATIC LEVEL CONTROL

The typical Automatic Level Control circuit configuration is shown in Figure 3. It can be seen that it is quite similar to the compressor schematic except that the input to the rectifier cell is from the input path and not from the feedback path. The input is AC coupled through C12 and C13 and the output is AC coupled through C8. Once again, as in the previous cases, if the system input and output signals are already AC coupled, then C12, C13 and C8 could be eliminated. Concerning the compressor, removing R6, R7 and C7 will cause motor-boating in absence of signals. C_{COMP} is necessary to stabilize the summing amplifier at higher input levels. This circuit provides an input dynamic range greater than 60dB with the output within ±0.5dB typical. The necessary design expressions are given by Equation 5 and Equation 6, respectively.

Equation 5.

$$\text{ALC gain} = \frac{3.8k \times 100\mu A}{4V_{IN(avg)}}$$

Equation 6.

$$\tau_R = \tau_A = 10k \times C_{RECT} = 10k \times C9$$

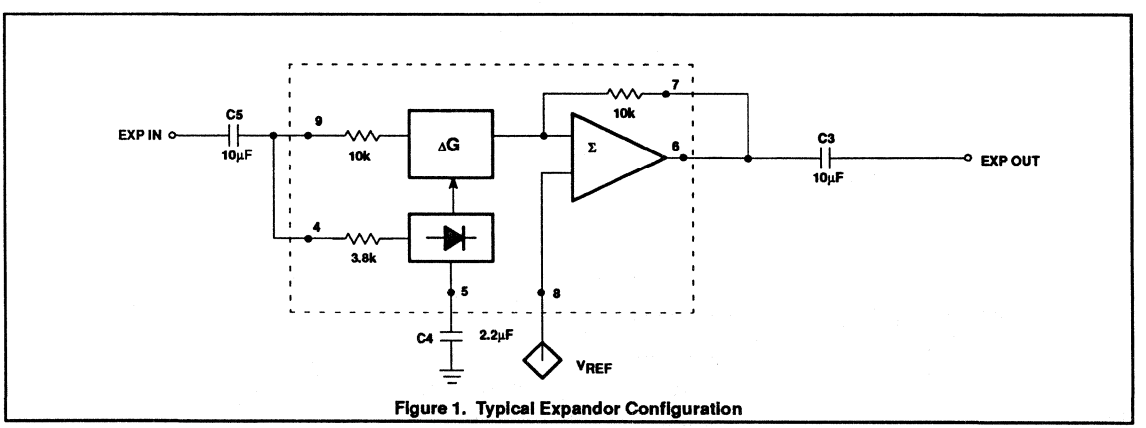


Figure 1. Typical Expandor Configuration

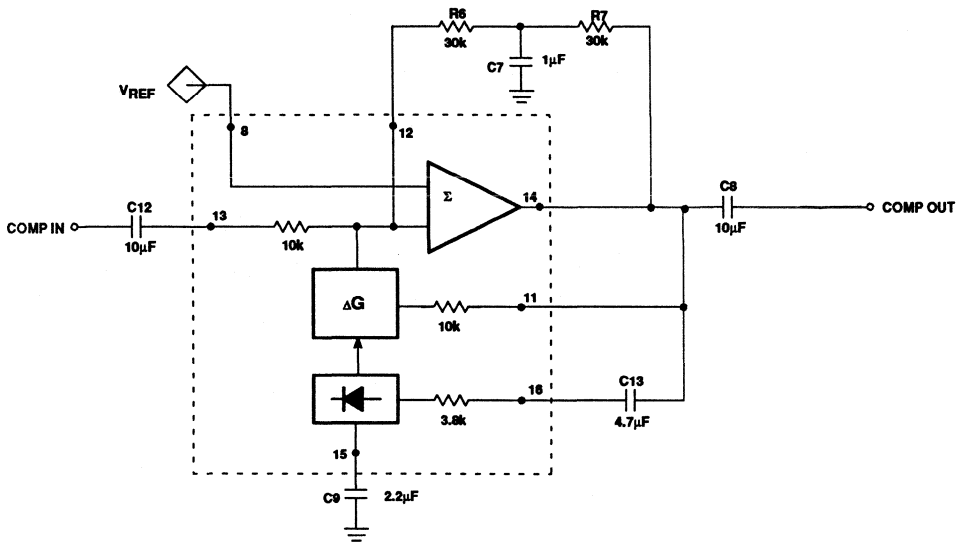


Figure 2. Typical Compressor Configuration

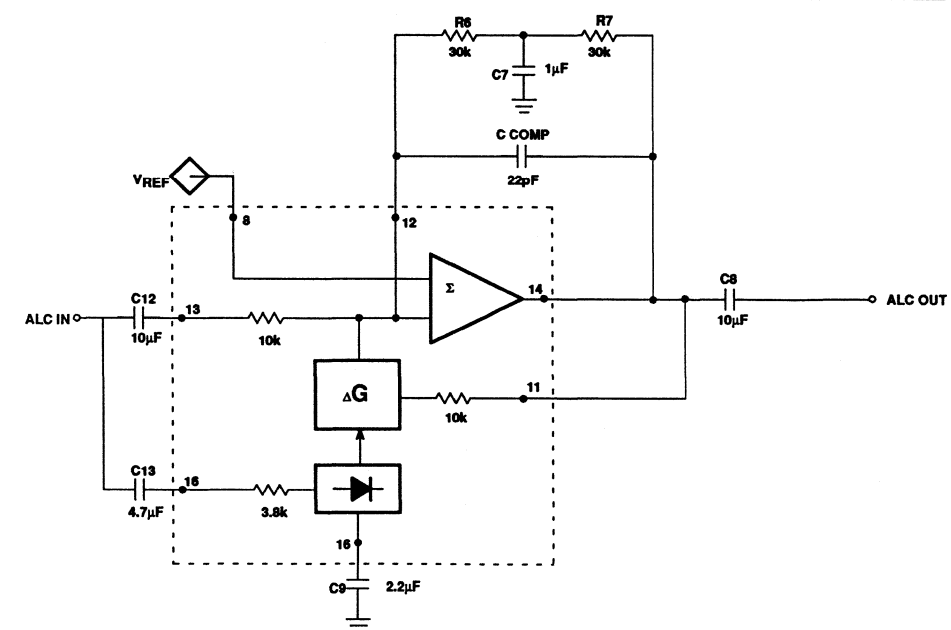


Figure 3. Typical ALC Configuration

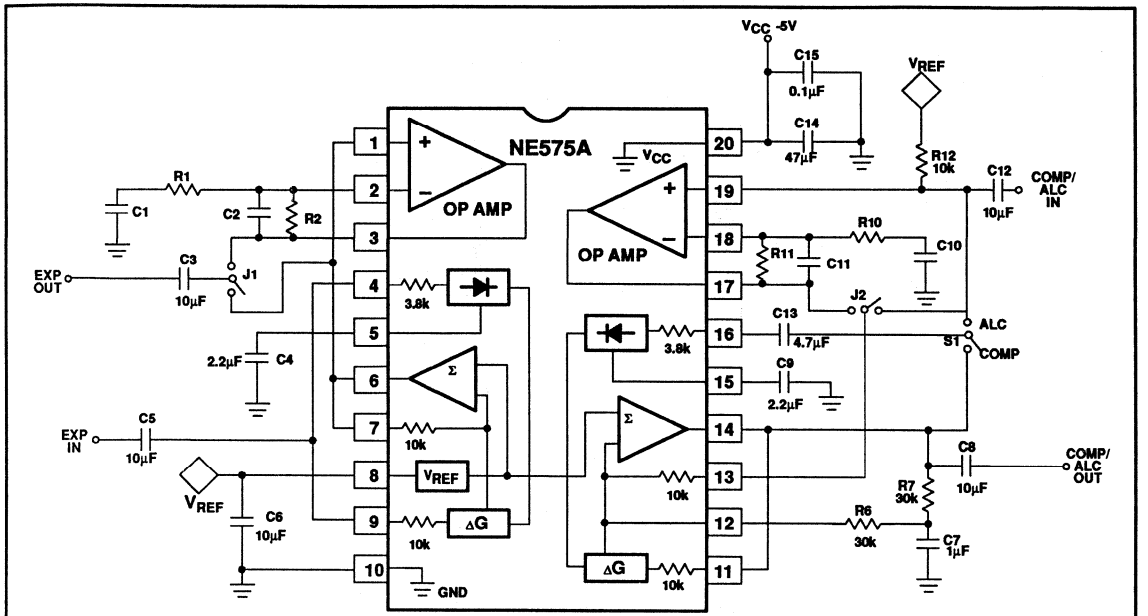
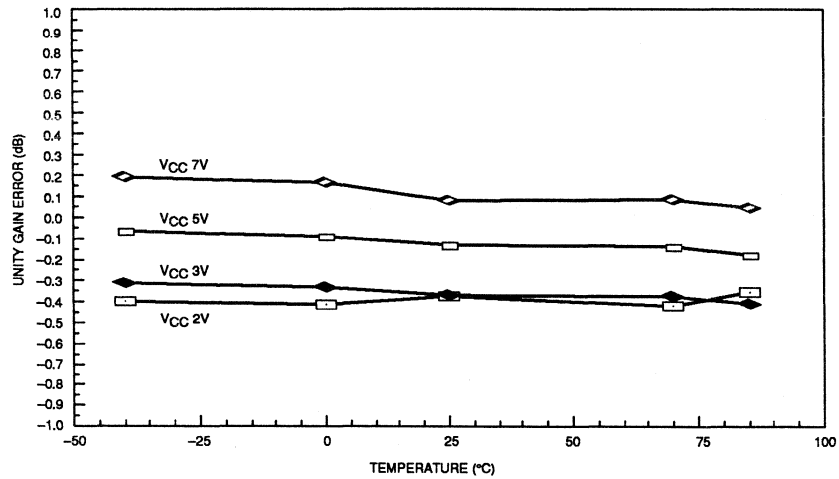
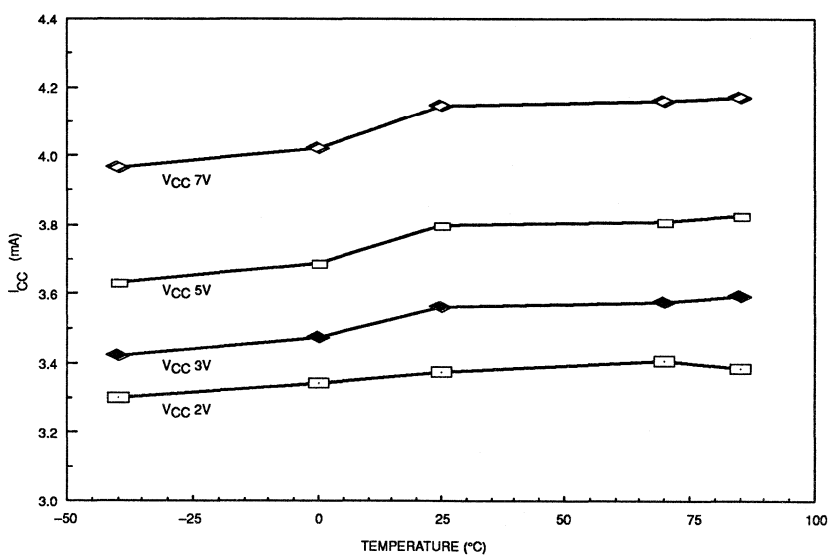


Figure 4. Signetics NE/SA575A Low Voltage Expandor/Compressor/ALC Demo Board



a. Unity Gain Error vs Temperature and V_{CC}



b. I_{CC} vs Temperature and V_{CC}

Figure 5. Temperature and V_{CC} Curves

TYPICAL PERFORMANCE CHARACTERISTICS

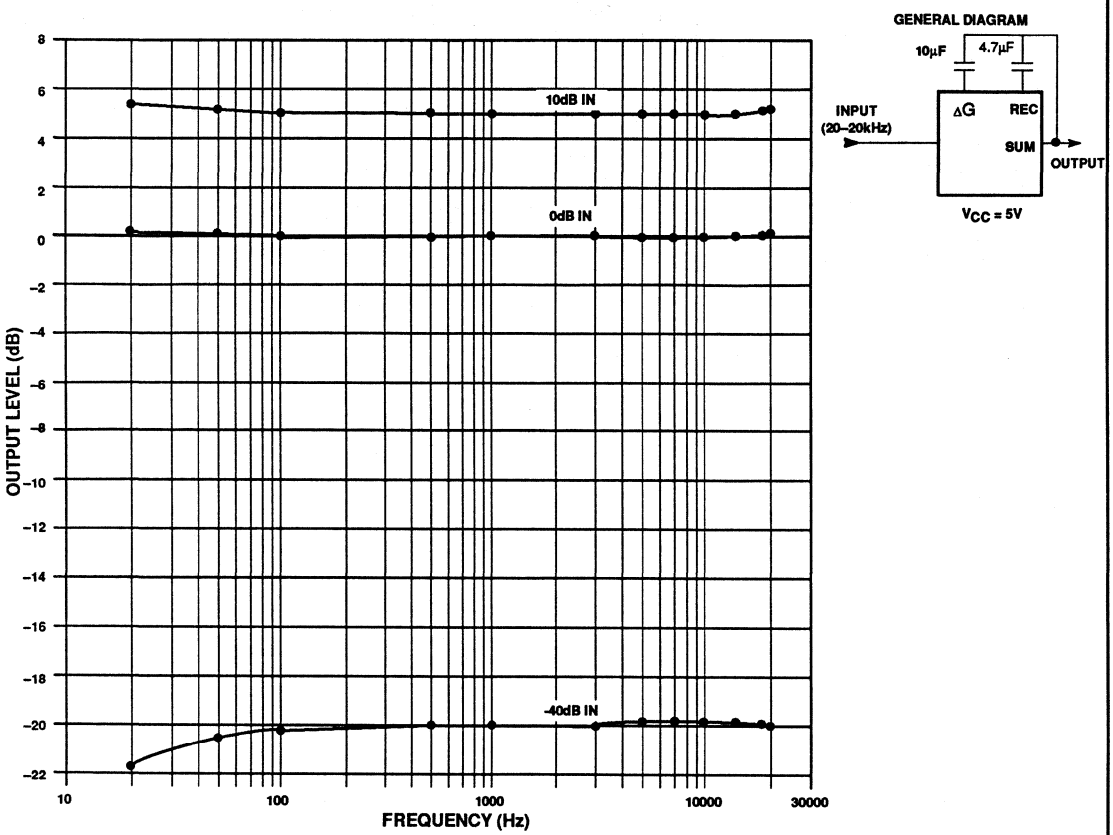


Figure 6. Compressor Output Frequency Response

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

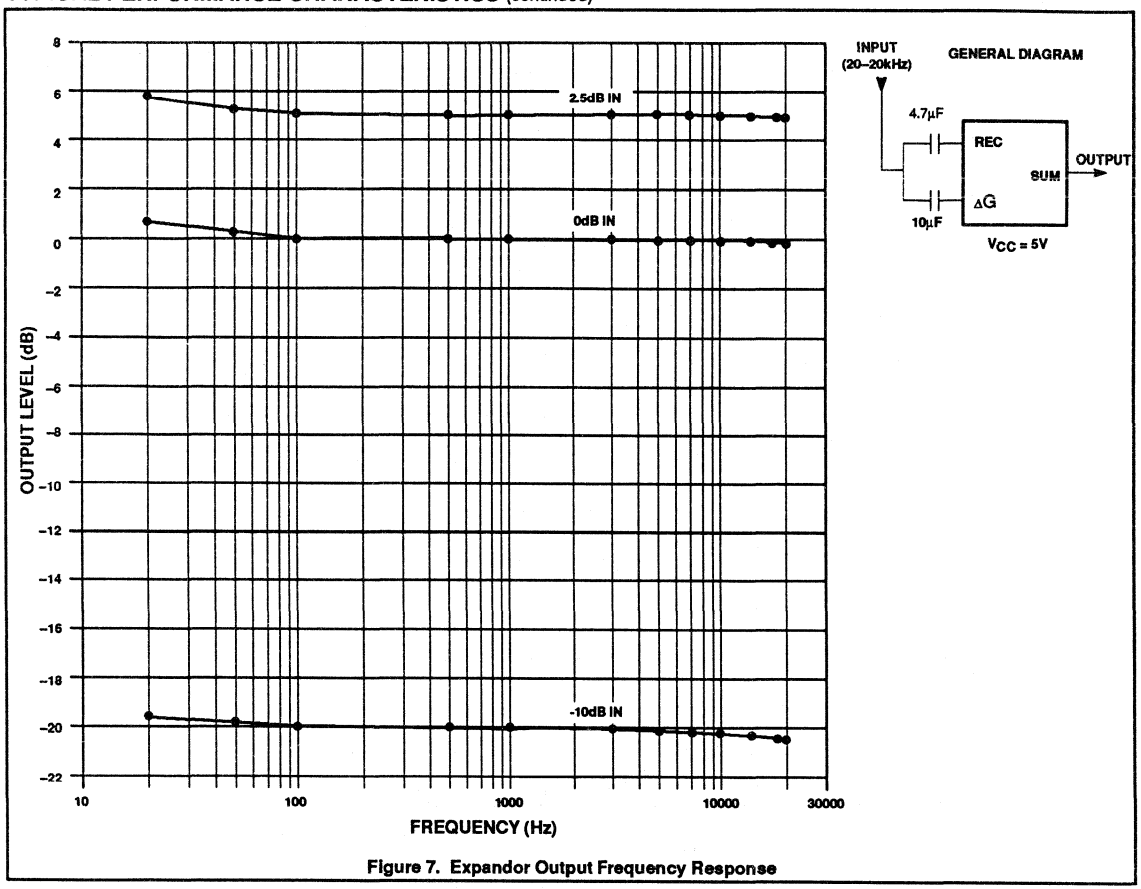


Figure 7. Expandor Output Frequency Response

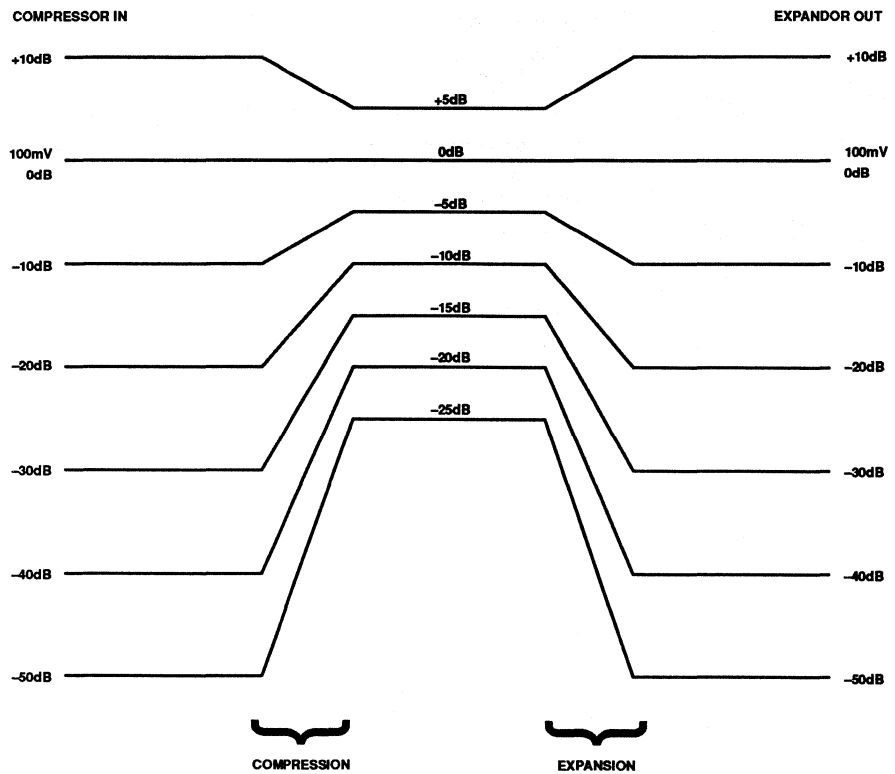


Figure 8. The Companding Function

Low power compandor — NE/SA576

DESCRIPTION

The NE/SA576 is a unity gain level programmable compandor designed for low power applications. The NE576 is internally configured as an expandor and a compressor to minimize external component count.

The NE576 can operate at 1.8V. During normal operations, the NE576 can operate from at least a 2V battery. If the battery voltage drops to 1.8V, this part will still continue to function, however, turning on the part at a V_{CC} of 1.8V requires two external resistors to bring V_{REF} to half V_{CC}. One resistor connects between V_{CC} and V_{REF}; the other connects from V_{REF} to ground. A typical value for these external resistors is approximately 20k. A lower value can be used, but the power consumption will go up.

The NE576 is available in a 14-pin plastic DIP and SO packages.

FEATURES

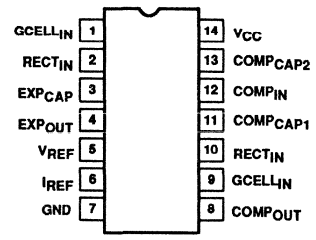
- Operating voltage range: 1.8V to 7V
- Low power consumption (1.4mA @ 3.6V)
- Over 80dB of dynamic range
- Wide input/output swing capability (rail-to-rail)
- Low external component count
- ESD hardened

APPLICATIONS

- Cordless telephone
- Consumer audio
- Wireless microphones
- Modems
- Electric organs
- Hearing aids
- Automatic level control

PIN CONFIGURATION

D and N Packages



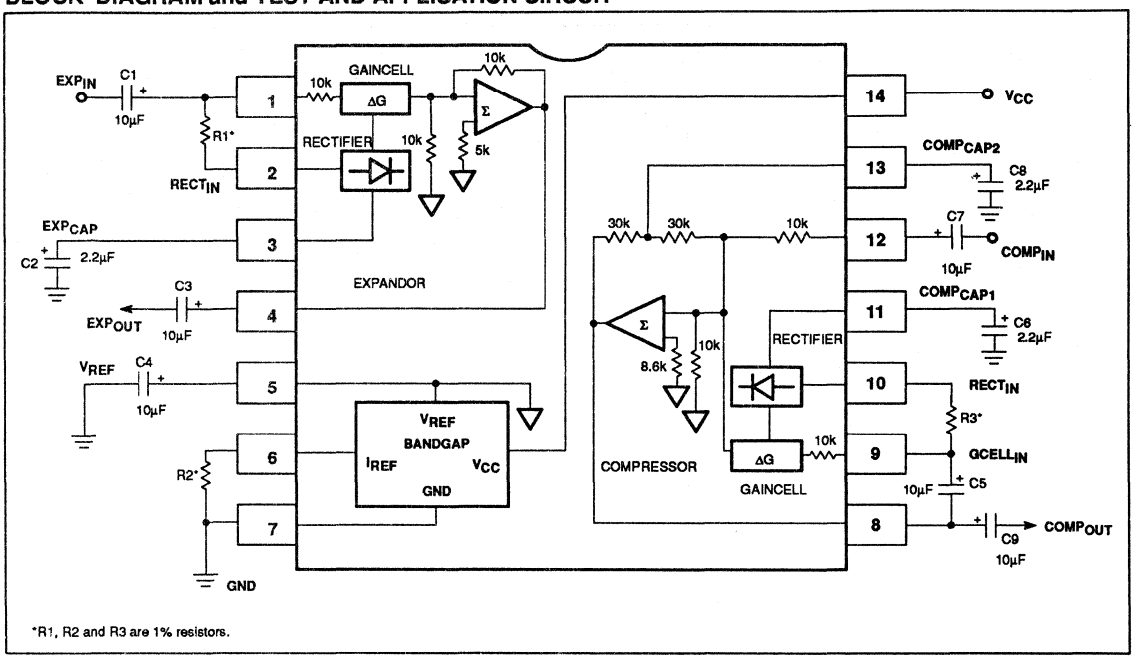
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14-Pin Plastic DIP	0 to +70°C	NE576N	0405B
14-Pin Plastic SO	0 to +70°C	NE576D	0175D
14-Pin Plastic DIP	–40 to +85°C	SA576N	0405B
14-Pin Plastic SO	–40 to +85°C	SA576D	0175D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING		UNITS
		NE576	SA576	
V_{CC}	Supply voltage	8	8	V
T_A	Operating ambient temperature range	0 to +70	–40 to +85	°C
T_{STG}	Storage temperature range	–65 to +150	–65 to +150	°C
θ_{JA}	Thermal impedance DIP SO	90 125	90 125	°C/W °C/W

BLOCK DIAGRAM and TEST AND APPLICATION CIRCUIT



*R1, R2 and R3 are 1% resistors.

ELECTRICAL CHARACTERISTICS

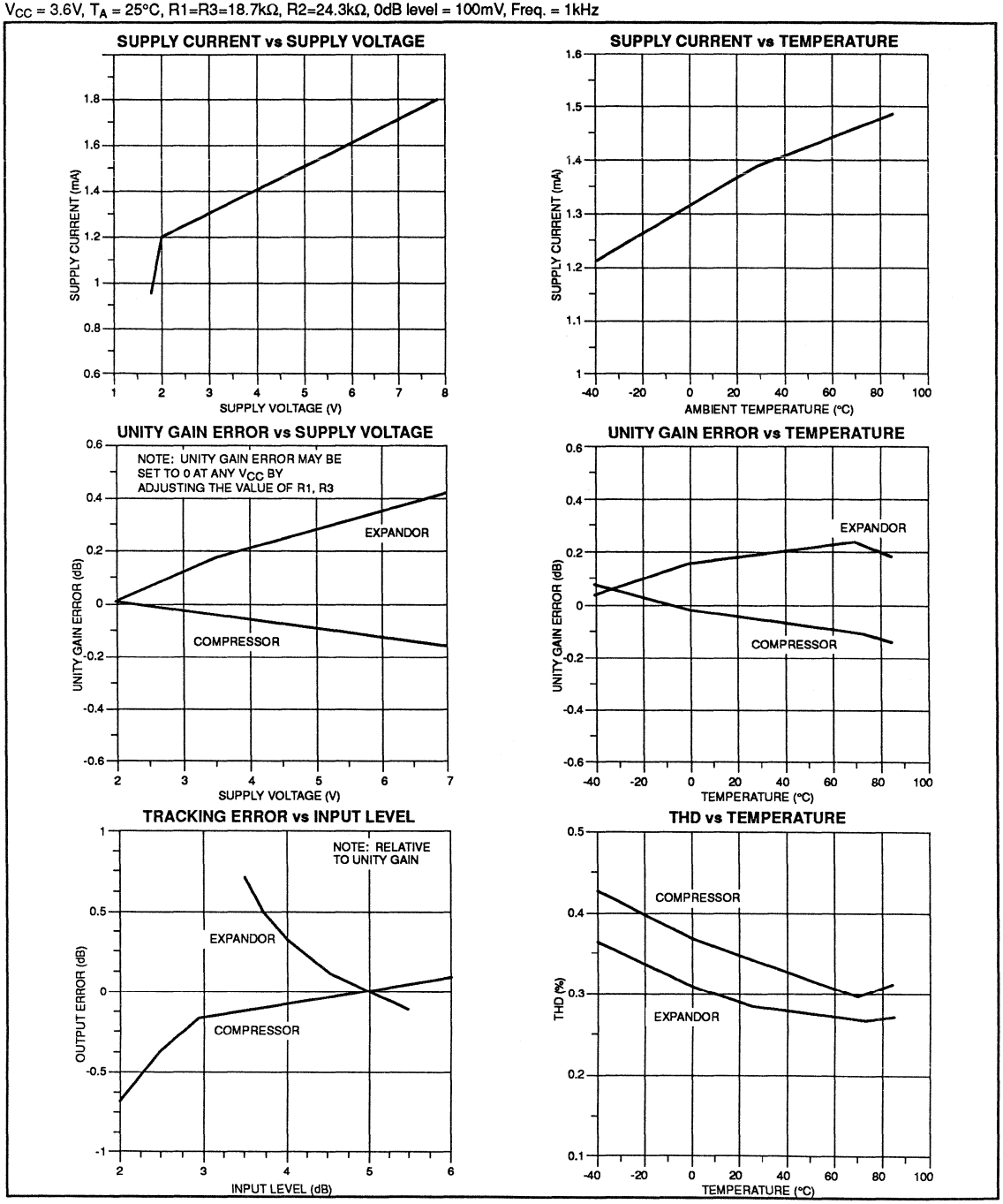
T_A = 25°C, V_{CC} = 3.6VDC, compandor 0dB level = –20dBV = 100mV_{RMS}, output load R_L = 10kΩ, Freq = 1kHz, unless otherwise specified. R1, R2 and R3 are 1% resistors.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS NE/SA576			UNITS
			MIN	TYP	MAX	
V_{CC}	Supply voltage[1]		2	3.6	7	V
I_{CC}	Supply current	No signal R_2 = 100kΩ		1.4	3	mA
V_{REF}	Reference voltage[2]	V_{CC} = 3.6V		1.8		V
R_L	Summing amp output load		10			kΩ
THD	Total harmonic distortion	1kHz, 0dB, BW = 3.5kHz		0.25	1.5	%
E_{NO}	Expandor output noise voltage	BW = 20kHz, R_S = 0Ω		10	30	µV
0dB	Unity gain level	0dB at 1kHz	–1.5	0.18	1.5	dB
V_{OS}	Output voltage offset	No signal	–150	1	150	mV
	Expandor output DC shift	No signal to 0dB	–100	7	100	mV
	Tracking error relative to 0dB output	-20dB expandor	–1.0	0.3	1.0	dB
	Crosstalk, COMP to EXP	1kHz, 0dB, C_{REF} = 10µF		–80		dB
V_O	Output swing low			0.2		V
	Output swing high			V_{CC} – 0.2		V

NOTE:
1. Operation down to V_{CC} = 1.8V is possible, see description on front page of NE576 data sheet.
2. Reference voltage, V_{REF}, is typically at 1/2 V_{CC}.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.6V, T_A = 25°C, R1=R3=18.7kΩ, R2=24.3kΩ, 0dB level = 100mV, Freq. = 1kHz



Unity gain level programmable low power compandor NE/SA577

DESCRIPTION

The NE/SA577 is a unity gain level programmable compandor designed for low power applications. The NE577 is internally configured as an expandor and a compressor to minimize external component count.

The NE577 is available in a 14-pin plastic DIP and SO packages.

FEATURES

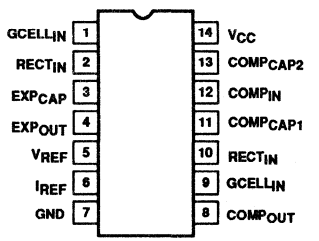
- Operating voltage range: 1.8V to 7V
- Low power consumption (1.4mA @ 3.6V)
- 0dB level programmable ($10mV_{RMS}$ to $1.0V_{RMS}$)
- Over 90dB of dynamic range
- Wide input/output swing capability (rail-to-rail)
- Low external component count
- SA577 meets cellular radio specifications
- ESD hardened

APPLICATIONS

- High performance portable communications
- Cellular radio
- Cordless telephone
- Consumer audio
- Wireless microphones
- Modems
- Electric organs
- Hearing aids
- Automatic level control (ALC)

PIN CONFIGURATION

D and N Packages



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14-Pin Plastic DIP	0 to +70°C	NE577N	0405B
14-Pin Plastic SO	0 to +70°C	NE577D	0175D
14-Pin Plastic DIP	–40 to +85°C	SA577N	0405B
14-Pin Plastic SO	–40 to +85°C	SA577D	0175D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING		UNITS
		NE577	SA577	
V_{CC}	Supply voltage	8	8	V
T_A	Operating ambient temperature range	0 to +70	–40 to +85	°C
T_{STG}	Storage temperature range	–65 to +150	–65 to +150	°C
θ_{JA}	Thermal impedance DIP SO	90 125	90 125	°C/W °C/W

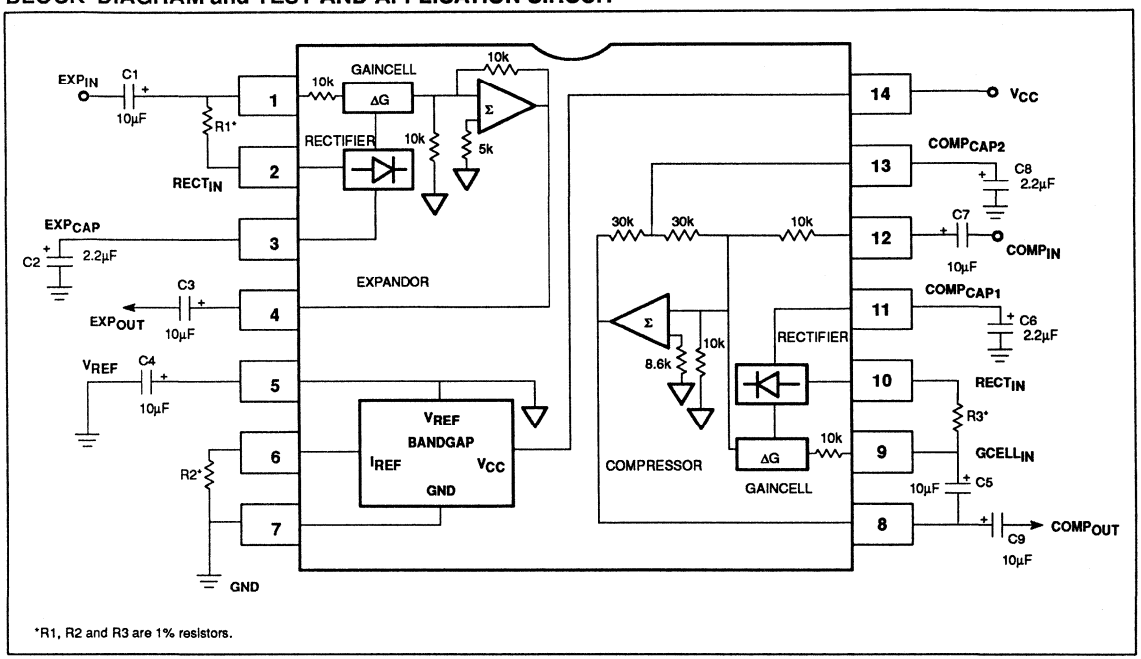
ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 3.6VDC, compandor 0dB level = –20dBV = 100mV_{RMS}, output load R_L = 10kΩ, Freq = 1kHz, unless otherwise specified. R1, R2 and R3 are 1% resistors.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA577			
			MIN	TYP	MAX	
V_{CC}	Supply voltage[1]		2	3.6	7	V
I_{CC}	Supply current	No signal R_2 = 100kΩ		1.4	2	mA
V_{REF}	Reference voltage[2]	V_{CC} = 3.6V	1.7	1.8	1.9	V
R_L	Summing amp output load		10			kΩ
THD	Total harmonic distortion	1kHz, 0dB, BW = 3.5kHz		0.25	1.5	%
E_{NO}	Expandor output noise voltage	BW = 20kHz, R_S = 0Ω		10	25	μV
0dB	Unity gain level	0dB at 1kHz	–1.5	0.18	1.5	dB
	Programmable range[3]	R1 = R3 = 18.7kΩ, R2 = 24.3kΩ		0		dBV
		R1 = R3 = 22.6kΩ, R2 = 100kΩ		–10		dBV
		R1 = R3 = 7.15kΩ, R2 = 100kΩ		–20		dBV
		R1 = R3 = 1.33kΩ, R2 = 200kΩ		–40		dBV
V_{OS}	Output voltage offset	No signal	–150	1	150	mV
	Expandor output DC shift	No signal to 0dB	–100	7	100	mV
	Tracking error relative to 0dB output	-20dB expandor	–1.0	0.3	1.0	dB
	Crosstalk, COMP to EXP	1kHz, 0dB, C_{REF} = 10μF		–80	–65	dB
V_O	Output swing low			0.2		V
	Output swing high			V_{CC} – 0.2		V

NOTE:
1. Operation down to V_{CC} = 1.8V is possible, see application note AN1762.
2. Reference voltage, V_{REF}, is typically at 1/2 V_{CC}.
3. Unity gain level can be adjusted CONTINUOUSLY between –40dBV = 10mV_{RMS} and 0dBV = 1.0V_{RMS}. For details see application note AN1762.

BLOCK DIAGRAM and TEST AND APPLICATION CIRCUIT

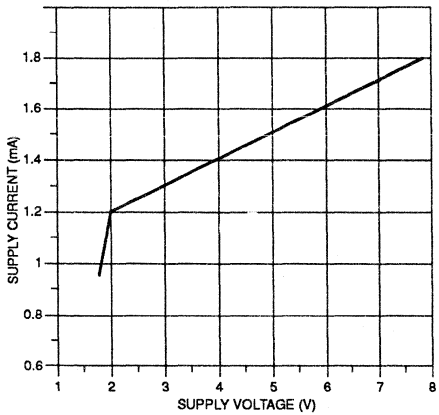


*R1, R2 and R3 are 1% resistors.

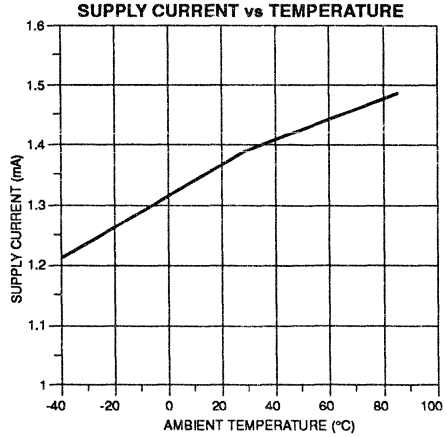
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.6V, T_A = 25°C, R1=R3=18.7kΩ, R2=24.3kΩ, 0dB level = 100mV, Freq. = 1kHz

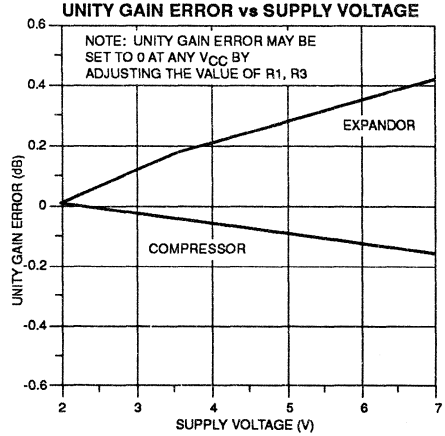
SUPPLY CURRENT vs SUPPLY VOLTAGE



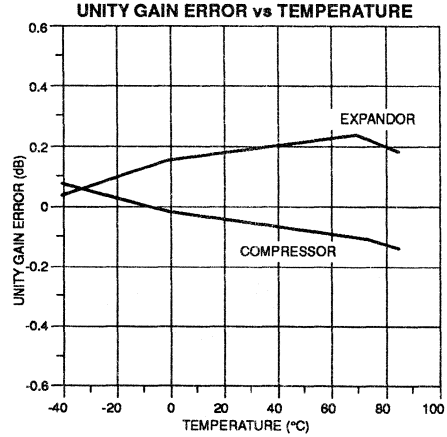
SUPPLY CURRENT vs TEMPERATURE



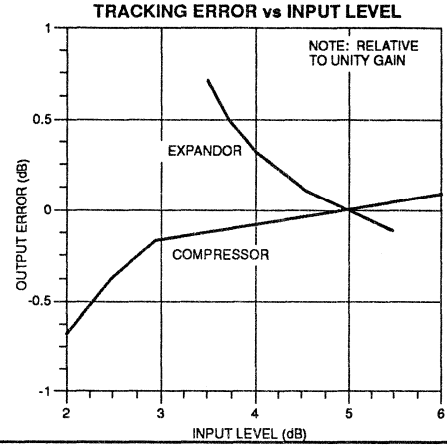
UNITY GAIN ERROR vs SUPPLY VOLTAGE



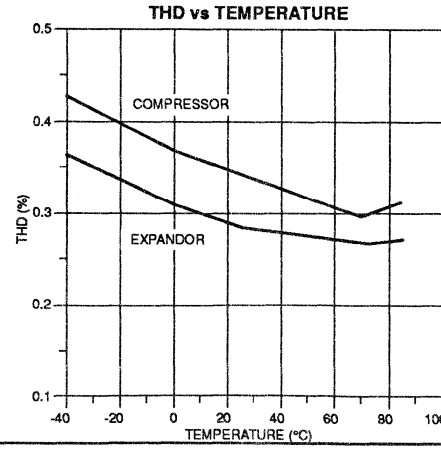
UNITY GAIN ERROR vs TEMPERATURE



TRACKING ERROR vs INPUT LEVEL



THD vs TEMPERATURE



Unity gain level programmable low power compandor — NE/SA578

DESCRIPTION

The NE/SA578 is a unity gain level programmable compandor designed for low power applications. The NE578 is internally configured as an expandor and a compressor to minimize external component count.

The summing amplifiers of the NE578 have 600W drive capability and the inverting input of the compressor amplifier is accessible through Pin 9 for summing multiple external signals. Power Down/Mute function is active low and requires an open collector output logic configuration at Pin 8. If Power Down/Mute is not needed, Pin 8 should be left open. When the part is muted, supply current drops to 170mA at 3.6V. The NE578 is available in a 16-pin plastic DIP and SO packages.

FEATURES

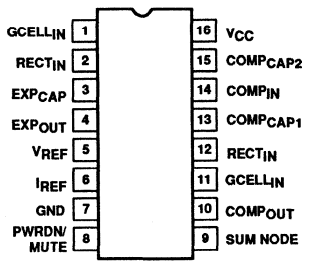
- Operating voltage range: 1.8V to 7V
- Low power consumption (1.4mA @ 3.6V)
- 0dB level programmable ($10mV_{RMS}$ to $1.0V_{RMS}$)
- Over 90dB of dynamic range
- Wide input/output swing capability
- Low external component count
- SA578 meets cellular radio specifications
- ESD hardened
- Power Down mode (I_{CC} = 170µA @ 3.6V)
- Mute function
- Multiple external summing capability
- 600W drive capability

APPLICATIONS

- High performance portable communications
- Cellular radio
- Cordless telephone
- Consumer audio

PIN CONFIGURATION

D and N Packages



- Wireless microphones
- Modems
- Electric organs
- Hearing aids
- Automatic level control (ALC)

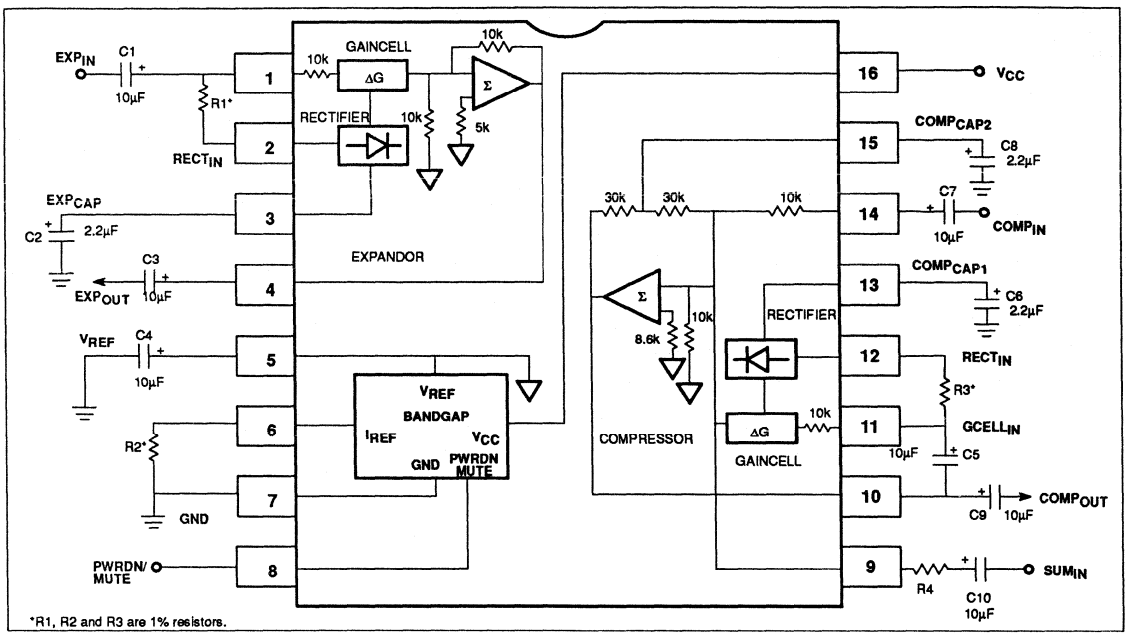
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic DIP	0 to +70°C	NE578N	0406C
16-Pin Plastic SO	0 to +70°C	NE578D	0005D
16-Pin Plastic DIP	–40 to +85°C	SA578N	0406C
16-Pin Plastic SO	–40 to +85°C	SA578D	0005D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING		UNITS
		NE578	SA578	
V_{CC}	Supply voltage	8	8	V
T_A	Operating ambient temperature range	0 to +70	–40 to +85	°C
T_{STG}	Storage temperature range	–65 to +150	–65 to +150	°C
θ_{JA}	Thermal impedance DIP SO	90 125	90 125	°C/W °C/W

BLOCK DIAGRAM and TEST AND APPLICATION CIRCUIT



ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 3.6VDC, compandor 0dB level = –20dBV = 100mV_{RMS}, output load R_L = 10kΩ, Freq = 1kHz, unless otherwise specified. R1, R2 and R3 are 1% resistors.

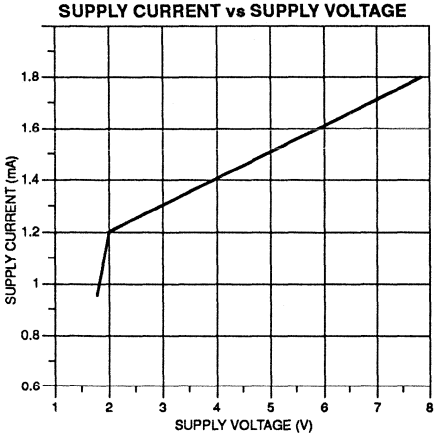
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA578			
			MIN	TYP	MAX	
V_{CC}	Supply voltage[1]		2	3.6	7	V
I_{CC}	Supply current operating power down	No signal, R_2 = 100kΩ		1.4 170	2	mA µA
V_{REF}	Reference voltage[2]	V_{CC} = 3.6V	1.7	1.8	1.9	V
R_L	Summing amp minimum output load			600		Ω
THD	Total harmonic distortion	1kHz, 0dB, BW = 3.5kHz		0.25	1.0	%
E_{NO}	Expandor output noise voltage	BW = 20kHz, R_S = 0Ω		10	20	µV
0dB	Unity gain level	0dB at 1kHz	–1.0	0.18	1.0	dB
	Programmable range[3]	R1 = R3 = 18.7kΩ, R2 = 24.3kΩ		0		dBV
		R1 = R3 = 22.6kΩ, R2 = 100kΩ		–10		dBV
		R1 = R3 = 7.15kΩ, R2 = 100kΩ		–20		dBV
		R1 = R3 = 1.33kΩ, R2 = 200kΩ		–40		dBV
V_{OS}	Output voltage offset	No signal	–150	1	150	mV
	Expandor output DC shift	No signal to 0dB	–100	7	100	mV
	Tracking error relative to 0dB output	-20dB expandor	–1.0	0.3	1.0	dB
	Crosstalk, COMP to EXP	1kHz, 0dB, C_{REF} = 10µF		–80	–65	dB
V_O	Output swing low			0.2		V
	Output swing high			V_{CC} – 0.2		V
	Power Down/Mute low level		0		0.4	V
	Power Down/Mute input current	Pin 8 grounded		–65		µA

NOTE:
1. Operation down to V_{CC} = 1.8V is possible, see application note AN1762.
2. Reference voltage, V_{REF}, is typically at 1/2 V_{CC}.
3. Unity gain level can be adjusted CONTINUOUSLY between –40dBV = 10mV_{RMS} and 0dBV = 1.0V_{RMS}. For details see application note AN1762.

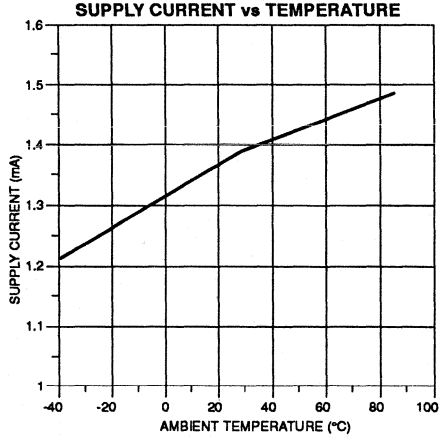
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.6V, T_A = 25°C, R1=R3=18.7kΩ, R2=24.3kΩ, 0dB level = 100mV, Freq. = 1kHz

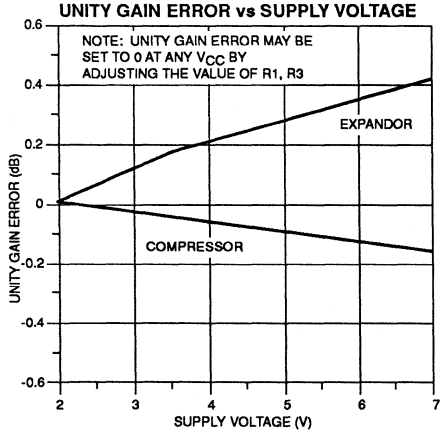
SUPPLY CURRENT vs SUPPLY VOLTAGE



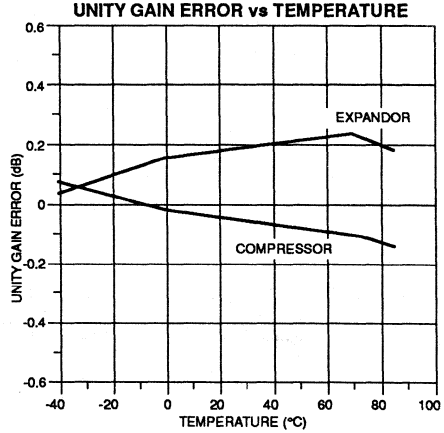
SUPPLY CURRENT vs TEMPERATURE



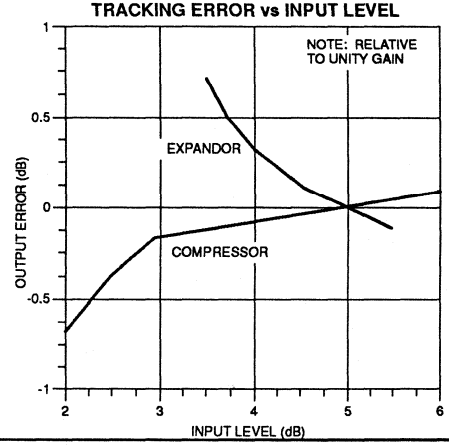
UNITY GAIN ERROR vs SUPPLY VOLTAGE



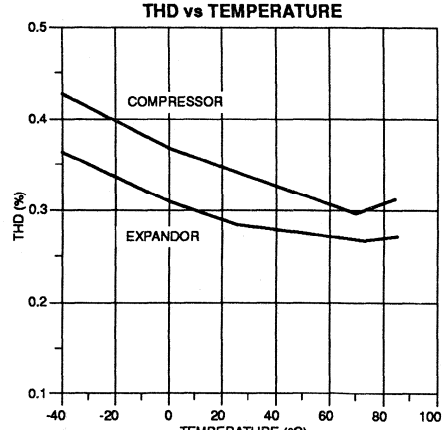
UNITY GAIN ERROR vs TEMPERATURE



TRACKING ERROR vs INPUT LEVEL



THD vs TEMPERATURE



1GHz LNA and mixer — NE/SA600

DESCRIPTION

The NE/SA600 is a combined low noise amplifier (LNA) and mixer designed for high-performance low-power communication systems from 800-1200MHz. The low-noise preamplifier has a 2dB noise figure at 900MHz with 16dB gain and an IM_3 intercept of -10dBm at the input. Input and output impedances are 50Ω and the gain is stabilized by on-chip compensation to vary less than ±0.5dB over the -40 to +85°C temperature range. The wide-dynamic-range mixer has a 14dB noise figure and IM_3 intercept of +6dBm at the input at 900MHz. Mixer input impedance is 50Ω with an open-collector output. The chip incorporates an option so the LNA can be disabled and replaced by a through connection. The amplifier IM_3 intercept increases to +26dBm in this mode; thus, large signals can be handled. The nominal current drawn from a single 5V supply is 13mA and 4.2mA in the LNA thru mode.

FEATURES

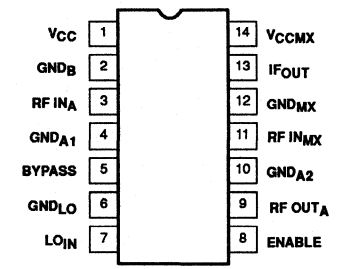
- Low current consumption: 13mA nominal, 4.2mA in the LNA thru mode
- Excellent noise figure: 2dB for the amplifier and 14dB for the mixer at 900MHz
- Excellent gain stability versus temperature
- Switchable overload capability
- Amplifier matched to 50Ω
- Mixer input matched to 50Ω
- Oscillator input matched to 50Ω

APPLICATIONS

- 900MHz front end for GSM/AMPS/TACS/ hand-held units
- RF data links
- UHF frequency conversion
- Portable radio
- Spread spectrum receivers
- 900MHz cordless phones

PIN CONFIGURATION

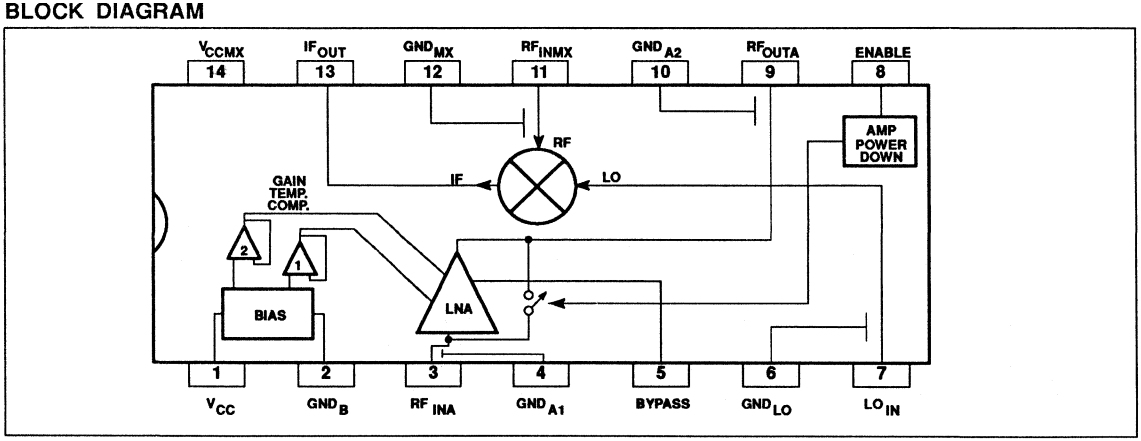
D Package



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14-Pin Plastic SO (Surface-mount)	0 to +70°C	NE600D	0175D
14-Pin Plastic SO (Surface-mount)	-40 to +85°C	SA600D	0175D

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}, V_{CCMX}	Supply voltage[1]	-0.3 to +6.0	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CC}+0.3)	V
ΔV	V_{CC} to V_{CCMX}	-0.3 to +0.3	V
ΔG	Any GND pin to any other GND pin	-0.3 to +0.3	V
P_D	Power dissipation, T_A = 25°C (still air)[2] 14-Pin Plastic SO	980	mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power input/output	+20	dBm
T_{STG}	Storage temperature range	–65 to +150	°C

NOTE:
1. Transients exceeding 9V on V_{CC} pin may damage product.
2. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}:
   14-Pin SO: θ_{JA} = 125°C/W
3. CAUTION: The NE/SA600 is built on a BiCMOS process and is sensitive to electrostatic discharge.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}, V_{CCMX}	Supply voltage	4.5 to 5.5	V
	Operating ambient temperature range		
	NE Grade	0 to +70	°C
T_A	SA Grade	-40 to +85	°C
	Operating junction temperature		
	NE Grade	0 to +90	°C
T_J	SA Grade	-40 to +105	°C

DC ELECTRICAL CHARACTERISTICS[1,2]

V_{CC} = V_{CCMX} = +5V, T_A = 25°C; Test Figure 1, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNITS
			MIN	–3σ	TYP	+3σ	MAX	
I_{CC}	Supply current (Pin 1, 13, 14)	Enable input high	10	11	13.0	15	16	mA
		Enable input low	3.2	3.6	4.2	4.8	5.2	mA
V_T	Enable logic threshold voltage		1.12	1.17	1.27	1.37	1.42	V
V_{IH}	Logic 1 level: LNA gain mode		2.0				V_{CC}	V
V_{IL}	Logic 0 level: LNA thru mode		–0.3				0.8	V
I_{IL}	Enable input current	Enable = 0.4V	-1		0		1	µA
I_{IH}	Enable input current	Enable = 2.4V	-1		0		1	µA
V_{LNA-IN}	LNA input bias voltage	Enable input high			0.78			V
$V_{LNA-OUT}$	LNA output bias voltage	Enable input high			1.27			V
V_{BY}	LNA bypass bias voltage	Enable input high			1.05			V
V_{MX-IN}	Mixer RF input bias voltage				1.43			V
V_{LO-IN}	Mixer LO input bias voltage				3.35			V

NOTE:
1. The ENABLE input must be connected to a valid logic level for proper operation of the NE/SA600.
2. Standard deviations are estimated from design simulations to represent manufacturing variations over the life of the product.

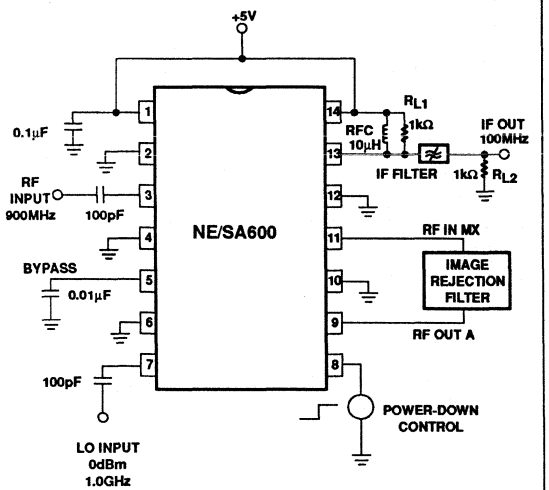
AC ELECTRICAL CHARACTERISTICS[1,2]

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNITS
				–3σ	TYP	+3σ	
LNA (V_{CC} = V_{CCMX} = +5V, T_A = 25°C; Enable = Hi, Test Figure 1, unless otherwise stated.)							
S_{21}	Amplifier gain	900MHz		14.9	16	17.1	dB
S_{21}	Amplifier gain in thru mode	Enable = LO, 900MHz		–9.0	-7.5	–6.0	dB
$\Delta S_{21}/\Delta T$	Gain temperature sensitivity enabled	900MHz			-0.008		dB/°C
$\Delta S_{21}/\Delta T$	Gain temperature sensitivity in thru mode	Enable = LO, 900MHz			-0.014		dB/°C
$\Delta S_{21}/\Delta f$	Gain frequency variation	800MHz - 1.2GHz			-0.014		dB/MHz
S_{12}	Amplifier reverse isolation	900MHz		–47	-42	–37	dB
S_{11}	Amplifier input match[3]	900MHz		–11	-10	–9	dB
S_{22}	Amplifier output match	900MHz		–16.8	-15	–13.2	dB
P_{-1dB}	Amplifier input 1dB gain compression	900MHz		–21.2	-20	–18.8	dBm
IP_3	Amp input 3rd-order intercept	Test Fig. 2, 900MHz		–11.6	-10	–8.6	dBm
	Amp input 3rd-order intercept (thru mode)	Test Fig. 2, 900MHz, Enable = LO			+26		dBm
NF	Amplifier noise figure	900MHz		1.9	2.2	2.5	dB
	Amp noise figure w/shunt 15nH inductor at input	900MHz		1.7	2.0	2.3	dB
t_{ON}	Amplifier turn-on time	Enable Lo → Hi	Coupling = 100pF		30		µs
			Coupling = 0.01µF		3		ms
t_{OFF}	Amplifier turn-off time	Enable Hi → Lo	Coupling = 100pF		10		µs
			Coupling = 0.01µF		1		ms
Mixer (V_{CC} = V_{CCMX} = +5V, T_A = 25°C, Enable = Hi, f_{LO} = 1GHz @ 0dBm, f_{RF} = 900MHz, f_{IF} = 100MHz, Test Fig. 1, unless otherwise stated)							
VG_C	Mixer voltage conversion gain	R_{L1} = R_{L2} = 1kΩ		9.5	10.4	11.3	dB
PG_C	Mixer power conversion gain	R_{L1} = R_{L2} = 1kΩ		–3.05	–2.6	–2.15	dB
S_{11RF}	Mixer input match	900MHz		–23	-20	–17	dB
NF_M	Mixer SSB noise figure	Test Fig. 3, 900MHz, f_{IF} = 80MHz		12.2	14	15.8	dB
P_{-1dB}	Mixer input 1dB gain compression	900MHz		–5.3	-4	–2.7	dBm
IP_{3INT}	Mixer input third order intercept	900MHz		+5	+6	+7	dBm
IP_{2INT}	Mixer input second order intercept	900MHz		+18	+20	+22	dBm
G_{RFM-IF}	Mixer RF feedthrough	900MHz, C_{IF} = 3pF			–7		dB
G_{LO-IF}	Mixer LO feedthrough	900MHz, C_{IF} = 3pF			-10		dB
G_{LO-RFM}	Local oscillator to mixer input feedthrough	900MHz			-33		dB
S_{11LO}	LO input match	900MHz		–24	–20	–16	dB
G_{LO-RF}	Local oscillator to RF input feedthrough	900MHz			-46		dB
$G_{RFO-RFM}$	Filter feedthrough	900MHz			-39		dB
LNA + Mixer (V_{CC}=V_{CCMX}=+5V, T_A=25°C, Enable=Hi, f_{LO}=1GHz @ 0dBm, f_{RF} = 900MHz, f_{IF} = 100MHz, Test Fig. 1, unless otherwise stated)							
PG_C	Overall power conversion gain				13.4		dB
NF	Overall noise figure				3.5		dB
IP_3	Overall input 3rd-order intercept				–13		dBm

NOTE:

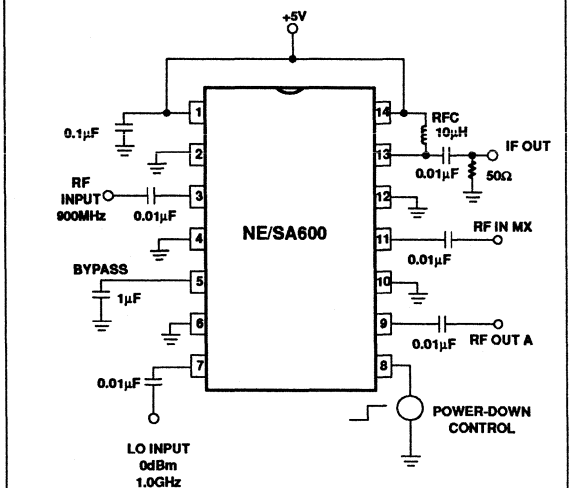
1. All meausrements include the effects of the NE/SA600 Evaluation Board (see Figure) unless otherwise noted. Measurement system impedance is 50Ω.
2. Standard deviations are estimated from design simulations to represent manufacturing variations over the life of the product.
3. With a shunt 15nH inductor at the input of the LNA, the value of S_{11} is typically –15dB.

TYPICAL APPLICATION

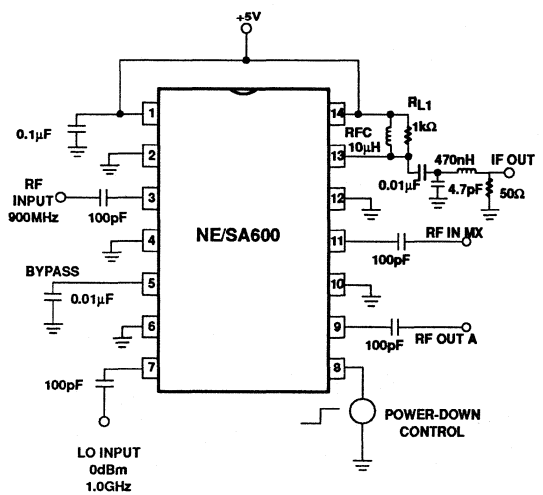


NOTES:
RATIO OF BYPASS TO SIGNAL COUPLING CAPS FOR LNA SHOULD BE 100:1 OR GREATER.
IF FILTER SHOULD BE AC COUPLED.

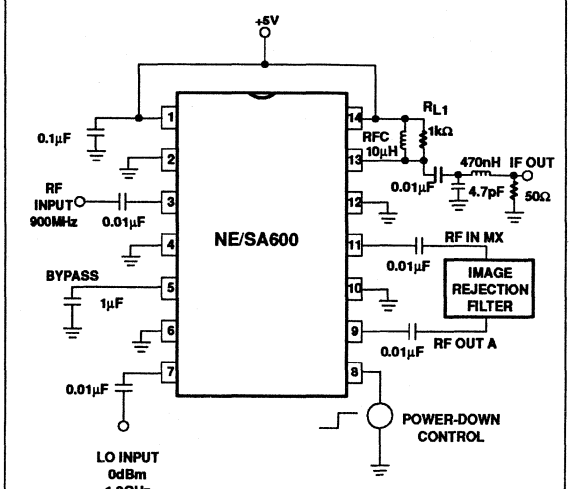
TEST FIGURE 1



TEST FIGURE 2



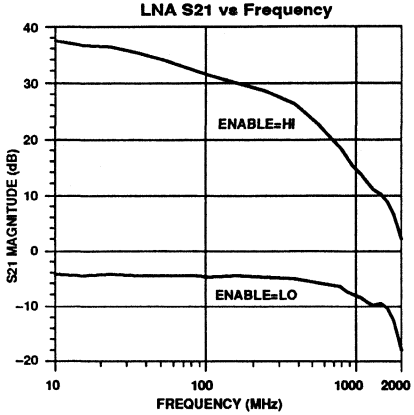
TEST FIGURE 3



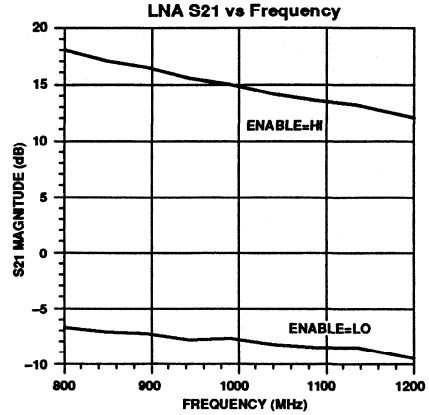
NOTE: All performance curves include the effects of the NE/SA600 evaluation board.

LNA S21 CHARACTERISTICS $4.5V \le V_{CC} = V_{CCMX} \le 5.5V$, Test Figure 1, unless otherwise specified.

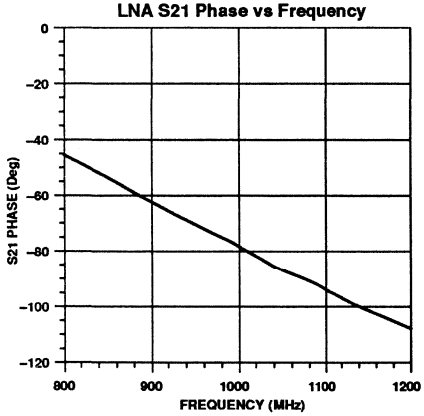
LNA S21 vs Frequency



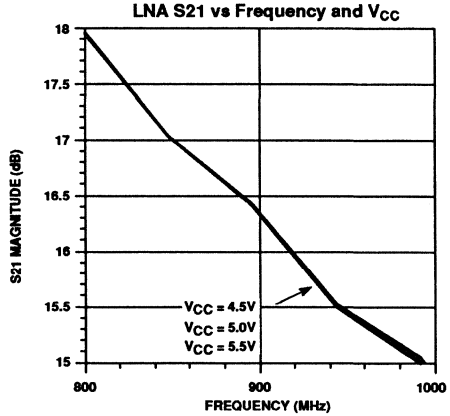
LNA S21 vs Frequency



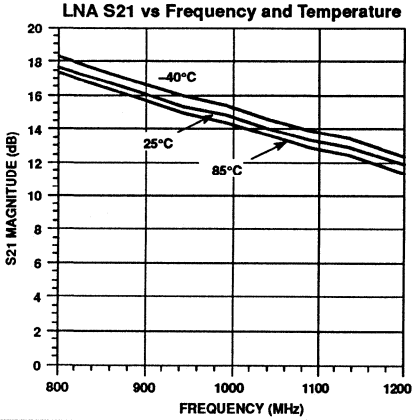
LNA S21 Phase vs Frequency



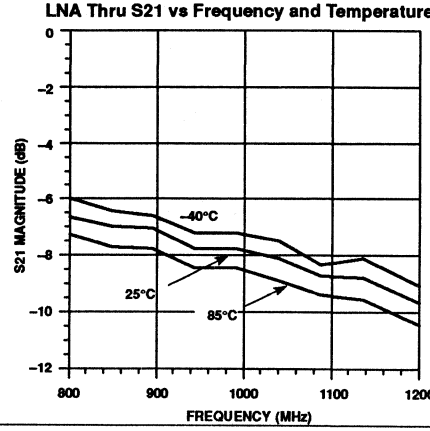
LNA S21 vs Frequency and V_{CC}



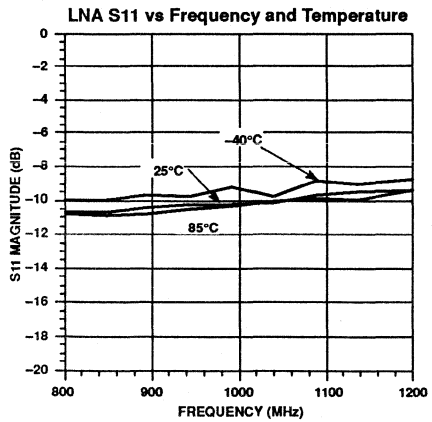
LNA S21 vs Frequency and Temperature

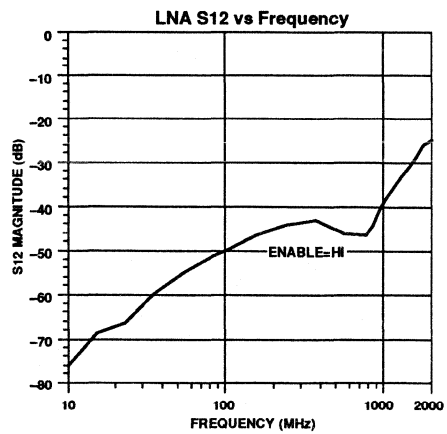


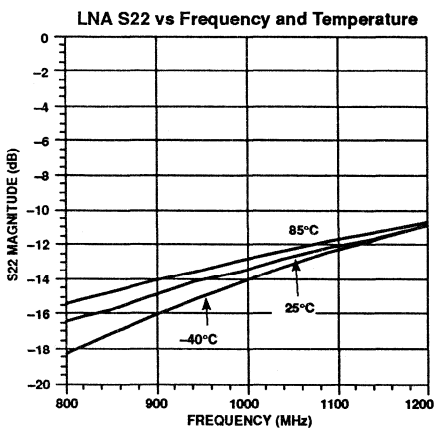
LNA Thru S21 vs Frequency and Temperature



LNA S11/S12/S22 CHARACTERISTICS $4.5V \le V_{CC} = V_{CCMX} \le 5.5V$, Test Figure 1, unless otherwise specified.







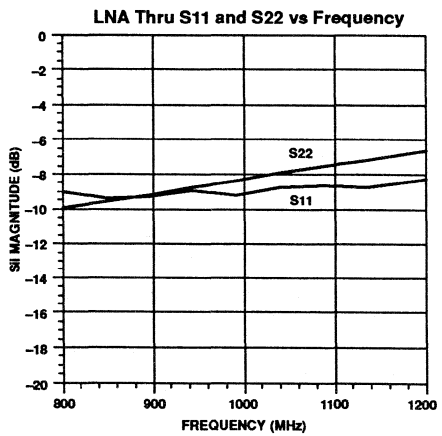
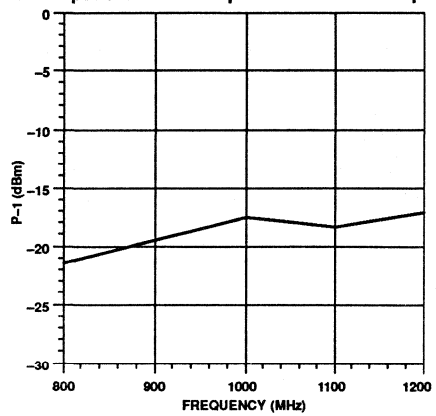


Table 1. S-Parameters

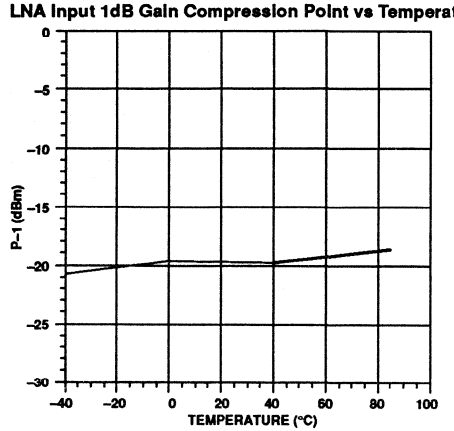
Freq	S11		S12		S21		S22	
MHz	dB	deg.	dB	deg.	dB	deg.	dB	deg.
800	–9.5	–160	–46	8	17.9	125	–18.0	151
900	–9.5	–172	–43	19	16.4	105	–15.8	122
1000	–9.4	–173	–40	17	15.1	88	–14.0	98
1100	–9.1	–200	–37	12	13.8	70	–12.4	77
1200	–8.9	–216	–35	1	12.9	55	–11.1	58

LNA OVERLOAD/NOISE/DISTORTION CHARACTERISTICS $4.5V \leq V_{CC} = V_{CCMX} \leq 5.5V$, Test Fig. 1, unless otherwise specified.

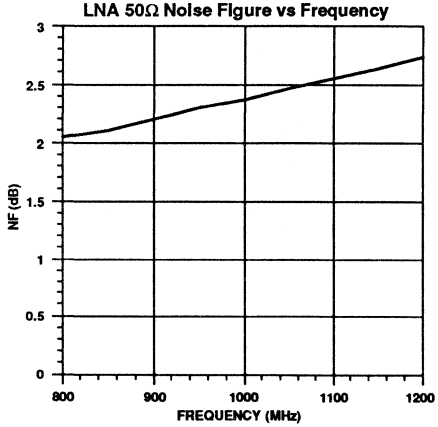
LNA Input 1dB Gain Compression Point vs Frequency



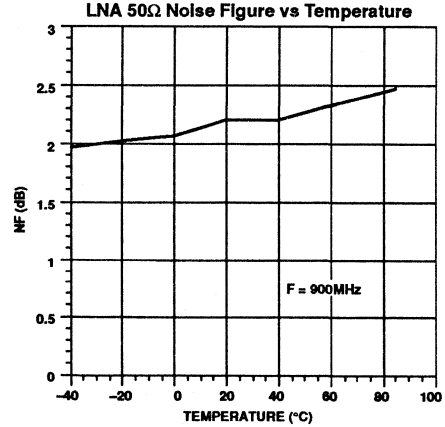
LNA Input 1dB Gain Compression Point vs Temperature



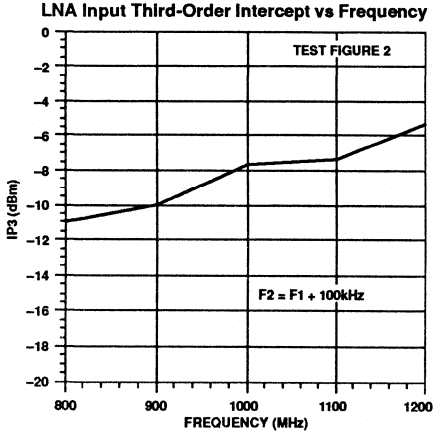
LNA 50Ω Noise Figure vs Frequency



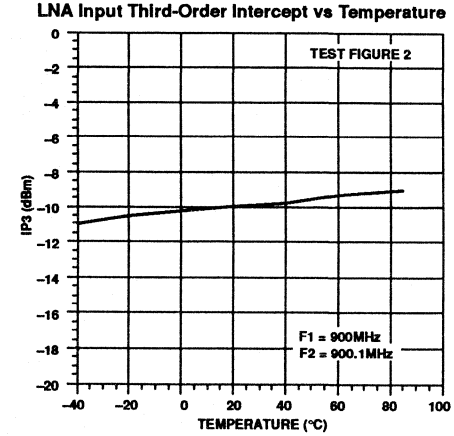
LNA 50Ω Noise Figure vs Temperature



LNA Input Third-Order Intercept vs Frequency

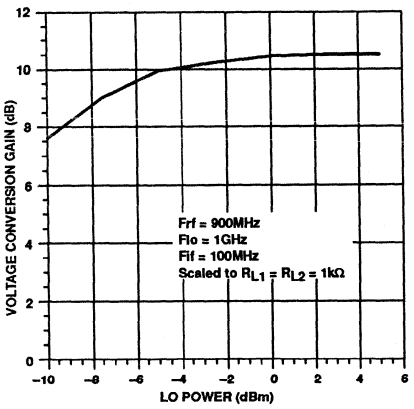


LNA Input Third-Order Intercept vs Temperature

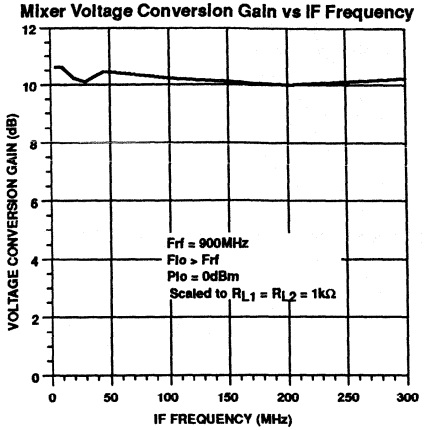


MIXER GAIN/NOISE CHARACTERISTICS $4.5V \le V_{CC} = V_{CCMX} \le 5.5V$, Test Figure 1, unless otherwise specified.

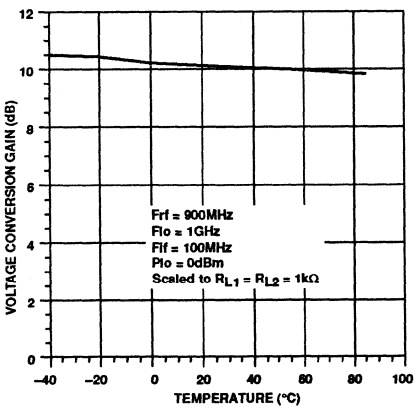
Mixer Voltage Conversion Gain vs LO Power



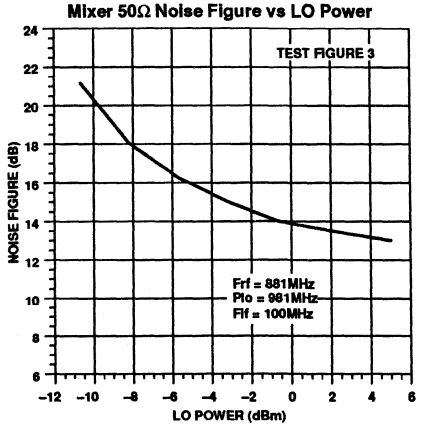
Mixer Voltage Conversion Gain vs IF Frequency



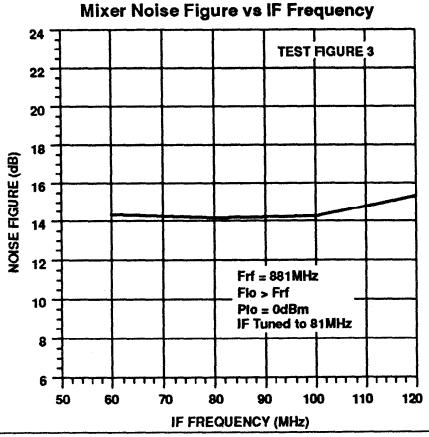
Mixer Voltage Conversion Gain vs Temperature



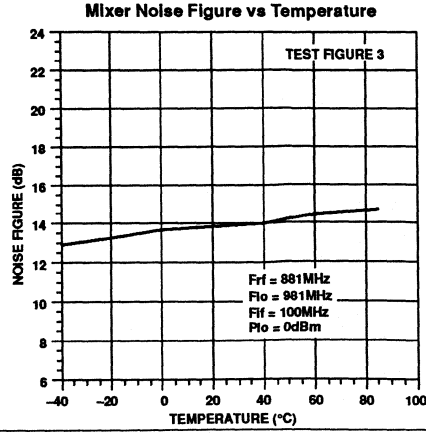
Mixer 50Ω Noise Figure vs LO Power



Mixer Noise Figure vs IF Frequency

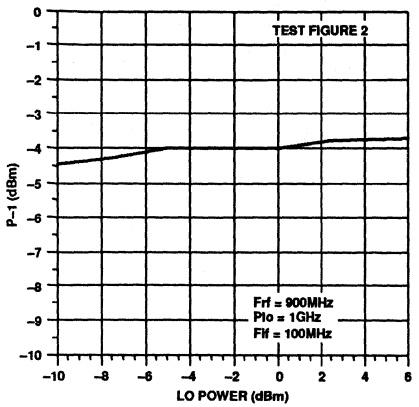


Mixer Noise Figure vs Temperature

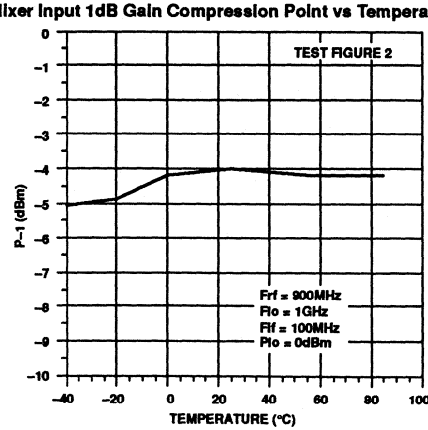


MIXER OVERLOAD/DISTORTION CHARACTERISTICS $4.5 \le V_{CC} = V_{CCMX} \le 5.5V$, Test Fig. 1, unless otherwise specified

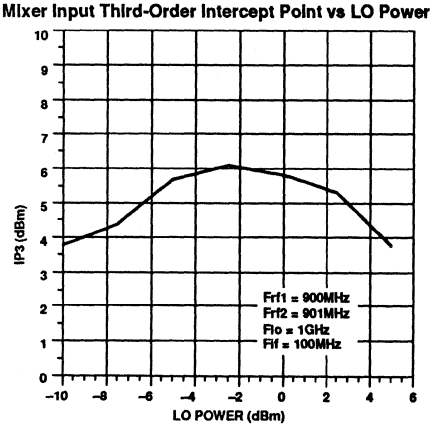
Mixer Input 1dB Gain Compression Point vs LO Power



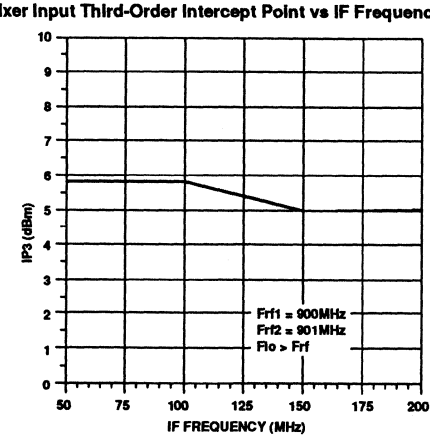
Mixer Input 1dB Gain Compression Point vs Temperature



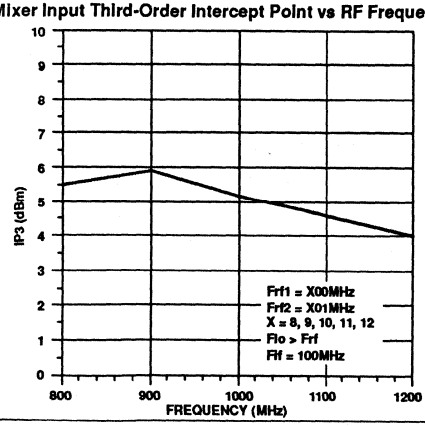
Mixer Input Third-Order Intercept Point vs LO Power



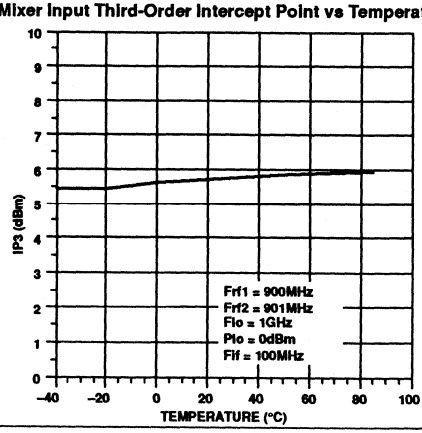
Mixer Input Third-Order Intercept Point vs IF Frequency



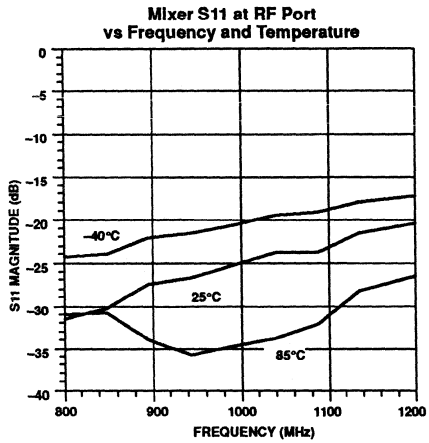
Mixer Input Third-Order Intercept Point vs RF Frequency

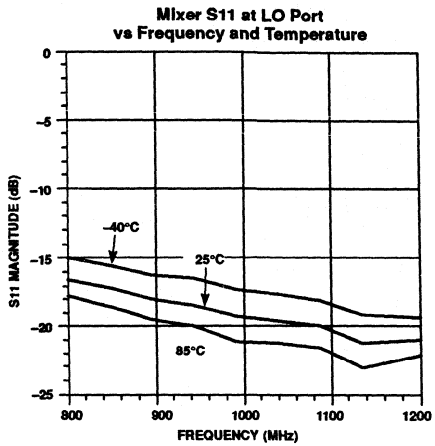


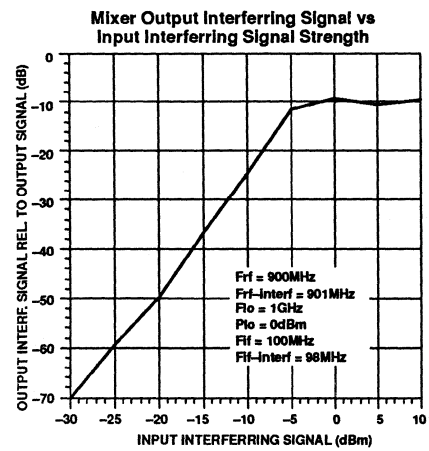
Mixer Input Third-Order Intercept Point vs Temperature

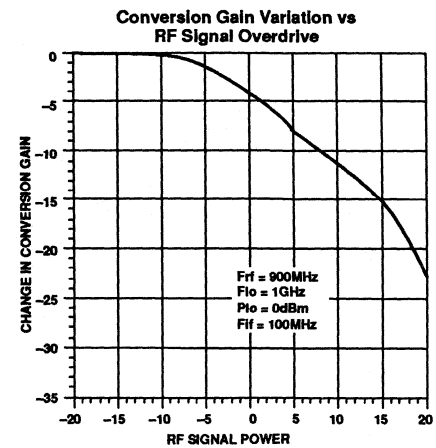


MIXER S11/ISOLATION/INTERFERENCE CHARACTERISTICS $4.5 \le V_{CC} = V_{CCMX} \le 5.5V$, Test Fig. 1, unless otherwise specified

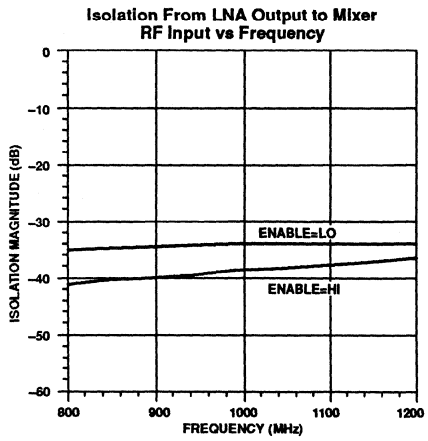


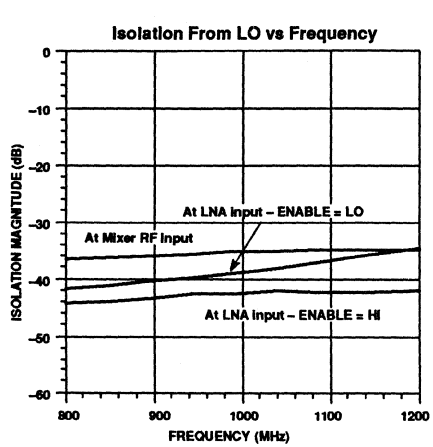






OVERALL PERFORMANCE: ISOLATION CHARACTERISTICS $4.5 \le V_{CC} = V_{CCMX} \le 5.5V$, Test Fig. 1, unless otherwise specified





SPECIFICATIONS

The goal of the Specifications section of the datasheet is to provide information on the NE/SA600 in such a way that the designer can estimate statistical variations, and can reproduce the measurements. To this end the high frequency measurements are specified with a particular PC board layout. Variations in board layout will cause parameter variations (sensitive parameters are discussed in the sections on the LNA and mixer below). For many RF parameters the ±3 sigma limits are specified. Statistically only 0.26% of the units will be outside these limits.

The LNA + mixer conversion gain is measured with an incident 900MHz signal and a 83MHZ SAW filter at the IF output. This measurement along with a gain measurement of the LNA ensure the correct operation of the chip and also allows a calculation of mixer conversion gain.

PIN DESCRIPTIONS AND OPERATIONAL LIMITS

RF_{INA}
Input of LNA, AC coupling required, DC = 0.78V, frequency range from DC to 2GHz, gain at low frequencies is 40dB — so be careful of overload, impedance below 50Ω, shunt 15-18nH inductor helps input match and noise figure.

RF_{OUTA}
Output of LNA, AC coupling required, DC = 1.27V, frequency range from DC to 2GHz, impedance above 50Ω.

BYPASS
Bypass capacitor should be 100 times larger than the largest signal coupling capacitor for the LNA, DC = 1.05V.

RF_{INMX}
Mixer RF port, AC coupling required, DC = 1.43V, frequency range from 100MHz to 2.5GHz, impedance close to 50Ω resistive.

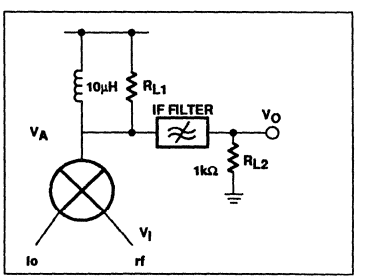
LO_{IN}
Mixer LO port, AC coupling required, DC=3.35V, frequency range from 100MHz to 2.5GHz, impedance close to 50Ω resistive.

IF_{OUT}
Mixer IF port, open-collector output with 1.6mA DC, frequency range DC to 1GHz, impedance approximately 1pF capacitive.

Enable
TTL/CMOS compatible input. Bias current approximately zero.

CONVERSION GAIN DEFINITIONS

Referring to the figure above, we define the ratio of V_A (at the IF frequency) to V_I (at the RF frequency) to be the Available Voltage Conversion Gain, or more simply Voltage Conversion Gain,



$$VG_C = 20\log\left(\frac{V_A}{V_I}\right)$$

where V_A and V_I are expressed in similar voltage units (such as peak-to-peak). The voltage output V_A is decreased by the IF Filter loss (and any other matching required). Typically, VG_C is 10.4dB for the NE/SA600 mixer with the net IF impedance equal to 500Ω.

It is more common to express the conversion gain in terms of power, so we have the Power Conversion Gain,

$$PG_C = 10\log\left(\frac{P_A}{P_I}\right) - 3dB$$

where $P_A = V_A^2 / R_{IF}$ and $P_I = V_I^2 / R_{RF}$. R_{IF} is the net resistance at the IF frequency at the IF port, and R_{RF} is the input impedance at the mixer RF port. With a 500Ω IF impedance and a 50Ω RF input impedance,

the conversion gain works out to –2.6dB typically. The power delivered to the load is down 3dB with respect to the available power because of loss in R_{L1}.

THEORY OF OPERATION

The NE/SA600 is fabricated on the Signetics advanced QUBiC technology that features 1µm channel length MOSFETs and 13GHz FT bipolar transistors.

LNA

The Low Noise Amplifier (LNA) is a two stage design incorporating feedback to stablize the amplifier. An external bypass capacitor of (typically) 0.01µF is used. The inputs and outputs are matched to 50Ω. The amplifier has two gain states: when the ENABLE pin is taken high, the amplifier draws 9mA of current and has 16dB of gain at 900MHz. When the ENABLE pin is low, the amplifier current goes to zero, and the amplifier is replaced by a thru. Typical loss for the thru is 7dB. This dual-gain state approach can be used in bang-bang control systems to achieve a low gain, high overload front-end as well as the more usual high gain, low overload front-end.

The amplifier has gain to frequencies past 2GHz, but a practical upper end is 1.6-1.7GHz. Both the input match and the noise figure (NF) can be improved with a shunt 15-18nH inductor at the input. Typically, the gain increases 0.4dB, the match improves to 13-16dB, and the noise figure drops to 1.95-2dB. Variations of any of the RF parameters with V_{CC} is negliglible, and variation with temperature is minimal.

Mixer

The mixer is a single-balanced topology designed to draw very low current, typically 4mA, and provide a very high input third-order intermodulation intercept point , typically IP3=+6dBm. The RF and LO ports impedances are nearly 50Ω resistive, and the IF output is an open collector. The open-collector output allows direct interfacing with high impedance IF filters, such as surface acoustic wave (SAW) filters without the need for external step-up transformers (which are needed for 50Ω output mixers).

The basic mixer is functional from DC to well over 2.5GHz, but RF and LO return losses degrade below 100MHz. The IF output can be used from DC to 500MHz or more, although typically the intermediate frequency is in the range 45-120MHz in many 900MHz receivers. To achieve the lowest noise, the LO drive level should be increased as high as possible, consistent with power dissipation limitations.

POWER SUPPLY ISSUES

V_{CC} bypassing is important, but not extremely critical because of the internal supply regulation of the NE/SA600. The Pin 1 V_{CC} supplies the LNA and powers overhead circuitry. Typical current draw is 9.8mA while enable is high (1mA powered down). The Pin 14 V_{CCMX} powers the mixer and typically has 3.2mA of current (assuming an inductor biasing the IFout back to V_{CCMX}). Care must be taken to avoid bringing any IC pin above V_{CC} by more than 0.3V, or below any ground by more than 0.3V. For example, this can occur if the enable pin is fed from a microcontroller that is powered up quicker than the NE/SA600. In this condition the internal electrostatic discharge (ESD) protection network may turn-on, possibly causing a part misfunction. Generally this condition is reversible, so long as the source creating the overstress is current limited to less than 100mA. To avoid the problem, make sure both V_{CC} pins are tied together near the IC, and install a 1kΩ resistor in series with the enable pin if it is likely to go above V_{CC}.

BOARD LAYOUT CONSIDERATIONS

The LNA is sensitive to mutual inductance from the input to ground. Therefore long narrow input traces will degrade the input match. Ideally, a top side ground-plane should be employed to maximize LNA gain and minimize stray coupling (such as LO to antenna). To avoid amplifier peaking, the output and input grounds should not be run together. Attach both grounds to a solid ground plane. A solid ground plane beneath the package will maximize gain. Top side to back side ground through holes are highly recommended.

The mixer is relatively insensitive to grounding. Care should be taken to minimize the capacitance on the RF port (Pin 11) for best noise figure. Also, the capacitance on the IFout pin must be kept small to avoid conversion gain rolloff when using high IF frequencies. The purpose of the inductor from IFout to V_{CC} is to set the midpoint of the IF swing to be V_{CC}. Without this inductor the part is sensitive to output overload under low V_{CC} (V_{CC} = 4.5V) and hot temperature conditions. The V_{CCMX} pin must be kept at the same potential as the V_{CC} pin.

APPLICATIONS INFORMATION

The NE/SA600 is a high performance, wide-band, low power, low noise amplifier (LNA) and mixer circuit integrated in a BiCMOS technology. It is ideally suited for RF receiver front-ends for both analog and digital communications systems.

There are several advantages to using the NE/SA600 as a high frequency front-end block instead of a discrete implementation. First is the simplicity of use. The NE/SA600 does not need any external biasing components. Due to the higher level of integration and small footprint (SO14) package it occupies less space on the printed circuit board and reduces the manufacturing cost of the system. Also the higher level of integration improves the reliability of the LNA and mixer over a discrete implementation with several components.

The LNA thru mode in NE/SA600 helps reduce power consumption in applications where the amplifiers can be disabled due to higher received signal strength (RSSI). Other advantages of this feature are described later in this section.

The mixer is an active mixer with excellent conversion gain at low LO input levels, so LO levels as low as -5dBm to -10dBm can be used depending on the applications requirement for mixer gain, mixer noise figure and mixer third order intercept point. This reduces the LO drive requirements from the VCO buffer, thus reducing its current consumption. Also, due to lower LO levels, the shielding requirements can be minimized or eliminated, resulting in substantial cost savings and weight and space reduction.

And last but not least, is the impedance matching at LNA inputs and outputs and mixer RF and LO input ports. Only those who have toiled through discrete transistor implementations for 50Ω input and output impedance matching can truly appreciate the elegance and simplicity of the NE/SA600 input and output impedance matching to 50Ω. Also, the mixer output impedance is high, so matching to a crystal or SAW IF filter becomes extremely easy without the need for additional IF impedance transformers (tapped-C networks with inductors or baluns).

The NE/SA600 applications and demo board features standard low cost 62mil FR-4 board. A top-side ground plane is used and 50Ω coplanar transmission lines are used. LO and RF_{INA} traces are perpendicular. Provisions for the image reject filter between RF_{OUTA} and RF_{INMX} are provided. A simple LC match for 80MHz IF is used so that 50Ω measurements can be made on the demo board.

The NE/SA600 applications evaluation board schematic is shown in Figure 1. The V_{CC} (Pin 1) and V_{CCMX} (Pin 14) are tied together

and the power supply is bypassed with capacitors C5 and C6. These capacitors should be placed as close to the device as practically possible.

C1 is the DC blocking capacitor to the input of the LNA. L1 provides additional input matching to the LNA for an improved return loss (S11). This inductor can be a surface-mount component or can be easily drawn on the printed circuit board (small spiral or serpentine). This additional match improves the gain of the LNA by 0.4dB and lowers the noise figure to 2dB or less. If the typical gain of the LNA of 16dB is acceptable with 2.2dB of noise figure, then L1 can be eliminated. If the LNA input is fed from a duplexer or selectivity filter after the antenna, C1 can also be eliminated since the filter will also provide DC blocking. The LNA bypass capacitor C3 should be at least 100 times C1 or C9 for low frequency stability. Switch S1 toggles the LNA gain/through function. R1 is used only to limit the maximum current into the enable pin and only necessary if enable may power up before the V_{CC}.

C4 is a DC blocking capacitor for the LO input pin and may not be needed in actual applications if the VCO output is isolated and will not upset the internal DC biasing of the mixer. The image reject filter goes between the output of the LNA and the RF input to the mixer. Since the LO input, RF output and mixer input are all 50Ω matched impedances internally, there is no need for any external components. C8 and C9 are DC blocking capacitors to the connectors and will not be needed in an actual application.

R2 and L2 are the load to the mixer output which is typical of the IF crystal or SAW filters. C2 and L3 provide a match from the high impedance mixer output to a 50Ω test set-up (spectrum analyzer, etc.) and C7 is a DC blocking capacitor for the mixer output.

The printed circuit board layout for the schematic of Figure 1 is shown in Figure 3. It is a very simple printed circuit board layout with all the components on a single side. The layout also accomodates a two pole image reject filter between the LNA outupt and mixer input. All the input and output traces to the LNA and mixer should be 50Ω tracks with the exception of mixer output, which can be very narrow due to the higher impedances of the filter.

The NE/SA600 internal supply is very well regulated. This is seen from Figure 4 which shows the I_{CC} vs. V_{CC} for the NE/SA600. Table 1 shows the S11, S21, S22 and S21 for the LNA from 800-1200MHz. Typical measurements at 900MHz for the critical parameters such as gain, noise figure, IP_3, 1dB compression point, etc. as measured on an applications evaluation board are as follows :

LNA gain = 16.5dB
LNA through = –7dB
Mixer gain =–3dB (into a 50Ω load)
LNA noise figure = 2dB
Mixer noise figure = 14dB
LNA IP_3 = –10dBm (in gain mode)
LNA IP_3 = +26dBm (in through mode)
LNA 1dB compression point = –20dBm
Mixer 1dB compression point = –4dBm

The shunt inductor L1 for input match is optional. Figure 5 shows the effect of the inductor value from 8.2nH to 15nH on gain, noise figure and input match.

The total power gain for the LNA and mixer (excluding the image reject filter) in a system where the output of the mixer is loaded with 50Ω is about 14dB. In an actual system the output impedance of the mixer is usually much higher than 50Ω (more like 1kΩ or higher) and so it is more important to consider the voltage gain from the input at the LNA to the mixer output. The voltage gain in this case will be about 29.85V/V. The total noise figure for the LNA and mixer combination is be about 3.27dB. The input third order intercept point for the LNA and mixer is about -11dBm. In the LNA through mode, the intercept point for the combination is higher than +19dBm. This LNA through feature provides an additional boost to the total dynamic range of the system.

The NE/SA600 finds applications in many areas of RF communications. It is an ideal down converter block for high performance, low cost, low power RF communications transceivers. The front-end of a typical AMPS/TACS/NMT/TDMA/CDMA cellular phone is shown in Figure 2. This could also be the front-end of a VHF/UHF handheld transceiver, UHF cordless telephone or a spread spectrum system.

The antenna is connected to the duplexer input. The receiver output of the duplexer is connected to the RF input of the LNA. If the additional improvement in noise figure and gain are not needed to meet the system specifications then L1 and C1 can be eliminated. In TDMA systems, the NE/SA600 can be totally powered down by Q1 and the two resistors. In this mode the current consumption will be zero mA. Care should be taken in the software of the system to insure that the enable pin on NE/SA600 tied to the LNA gain control port is held low while the device is in total power down mode. L2 and C2 can be tuned to the IF frequency and to match to the IF filter impedance.

A complete analysis of the front-end shows that the total voltage gain from the antenna input to the mixer output is about 9.5V/V. This value includes a 3.2dB loss for the duplexer and a 1.8dB loss for the bandpass filter. The noise figure as referred to the antenna is 7dB and the input third order intercept point is about -7.5dBm. In LNA through mode the input third order intercept point increases to about +24dBm.

During normal operation of a handheld RF receiver the received signal strength (RSSI) is nominally greater than -100dBm. The signal only drops below this level due to severe multipath fading, shadow effect or when the receiver is at extreme fringes of cell coverage. The LNA through mode can be used here as a two step gain control such that when RSSI is below a certain threshold level (e.g. -90dBm), the LNA has a -7dB loss and the total current consumption of the NE/SA600 is only 4.3mA. The sensitivity of the system will not suffer because the received RF signal is much higher than the noise floor of the system. When the RSSI falls below a certain threshold (e.g. -95dBm) the LNA is enabled to give the full 16.5dB of gain with 2dB of noise figure. In this mode the current consumption is increased to 13mA. But for hand-held equipment, the average current consumption will be closer to 5-6mA. The other advantage of the LNA through mode besides power savings is the input overload characteristics. Due to the much higher input third order intercept point of the LNA (+26dBm), the receiver is immune to strong adjacent channel interference. Implementing this feature with an FM/IF device such as the NE625/7 with fast RSSI response and a window comparator toggling the LNA mode of NE/SA600, a fast two-step AGC with response time less than 10μs can be achieved. This is a very useful feature to equalize multipath fading effects in a mobile radio system.

In conclusion, the NE/SA600 offers higher level of integration, higher reliability, higher level of performance, ease of use, simpler system design at a cost lower than the discrete multi-transistor implementations. In addition, the NE/SA600 provides unique features to enhance receiver performance which are almost unattainable with discrete implementations.

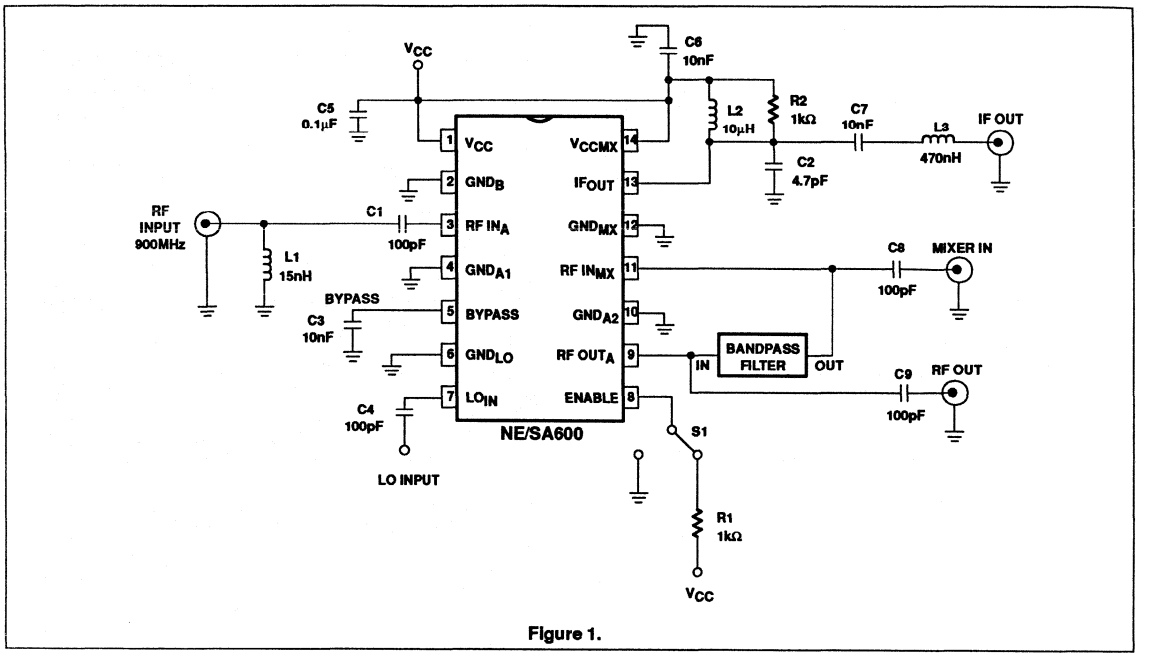


Figure 1.

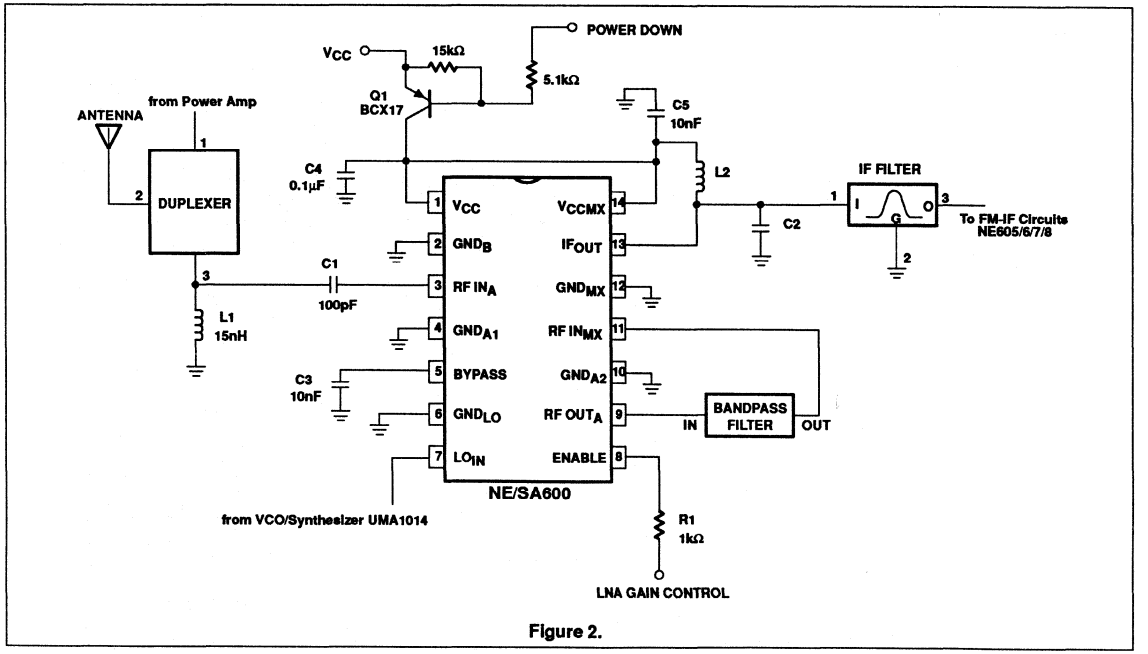


Figure 2.

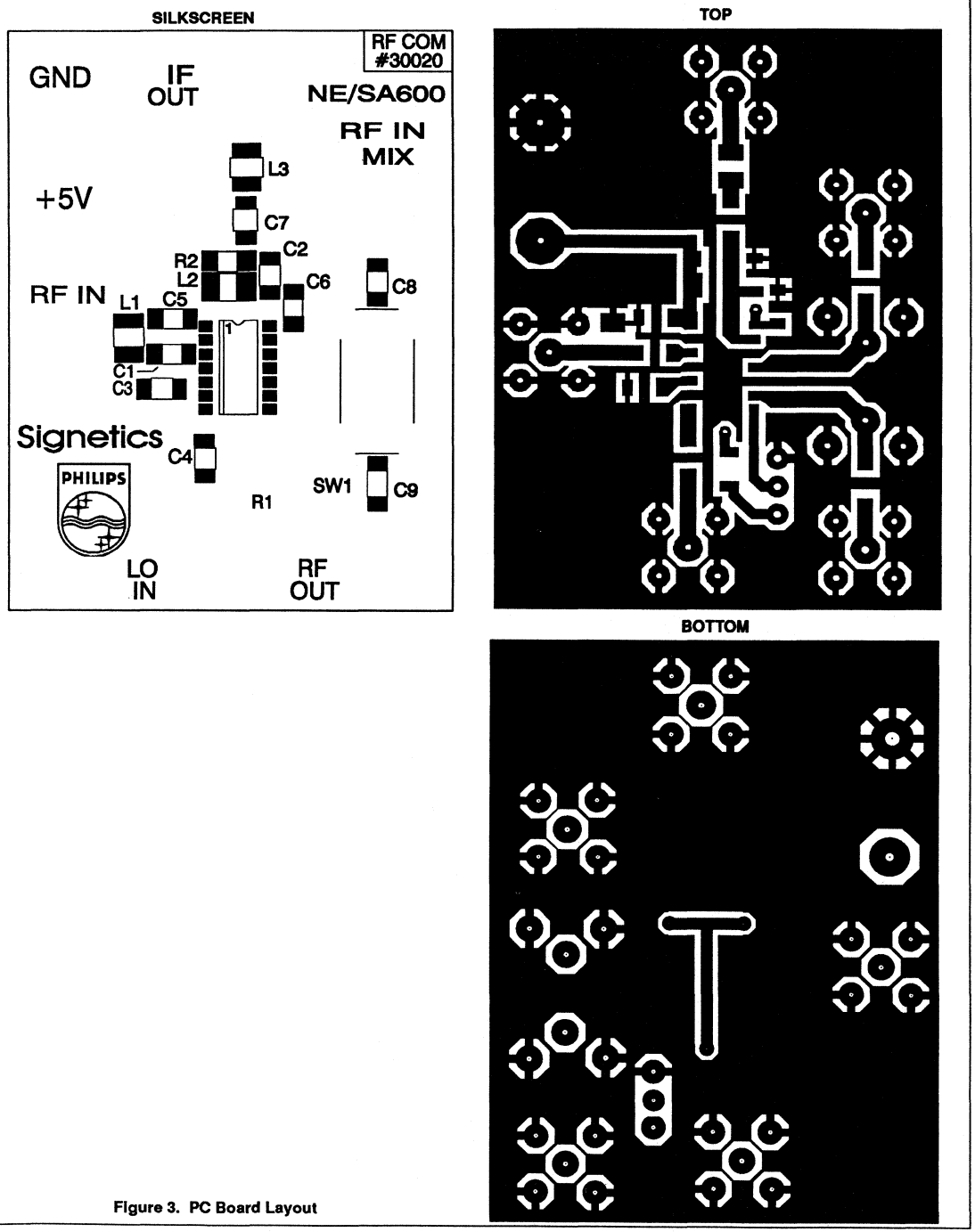
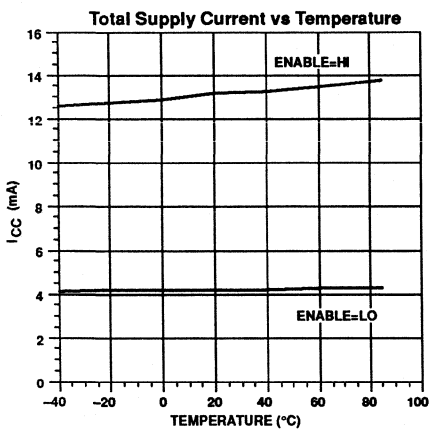


Figure 3. PC Board Layout



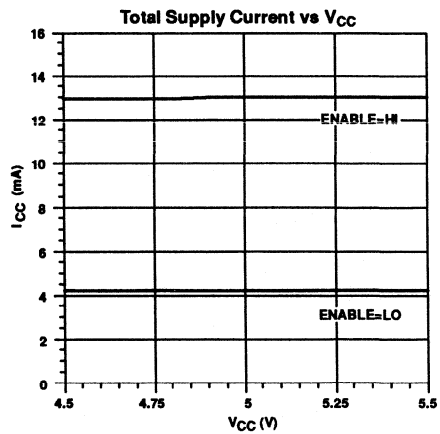
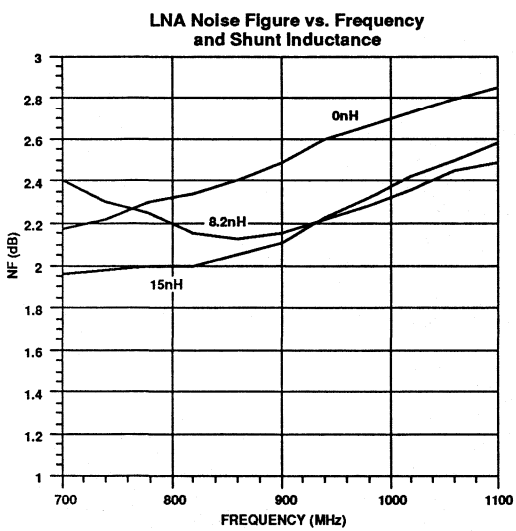


Figure 4.



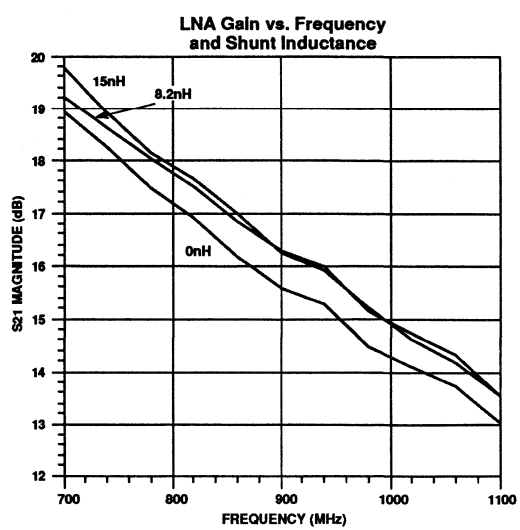


Figure 5.

Document	853–1424
ECN No.	99374
Date of Issue	April 17, 1990
Status	Product Specification
RF Communications	

NE/SA602A

Double-balanced mixer and oscillator

DESCRIPTION

The NE/SA602A is a low-power VHF monolithic double-balanced mixer with input amplifier, on-board oscillator, and voltage regulator. It is intended for high performance, low power communication systems. The guaranteed parameters of the SA602A make this device particularly well suited for cellular radio applications. The mixer is a "Gilbert cell" multiplier configuration which typically provides 18dB of gain at 45MHz. The oscillator will operate to 200MHz. It can be configured as a crystal oscillator, a tuned tank oscillator, or a buffer for an external LO. For higher frequencies the LO input may be externally driven. The noise figure at 45MHz is typically less than 5dB. The gain, intercept performance, low-power and noise characteristics make the NE/SA602A a superior choice for high-performance battery operated equipment. It is available in an 8-lead dual in-line plastic package and an 8-lead SO (surface-mount miniature package).

FEATURES

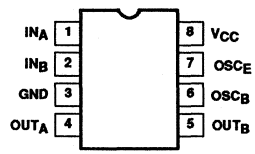
- Low current consumption: 2.4mA typical
- Excellent noise figure: <4.7dB typical at 45MHz
- High operating frequency
- Excellent gain, intercept and sensitivity
- Low external parts count; suitable for crystal/ceramic filters
- SA602A meets cellular radio specifications

APPLICATIONS

- Cellular radio mixer/oscillator
- Portable radio
- VHF transceivers
- RF data links
- HF/VHF frequency conversion
- Instrumentation frequency conversion
- Broadband LANs

PIN CONFIGURATION

F, D and N Packages

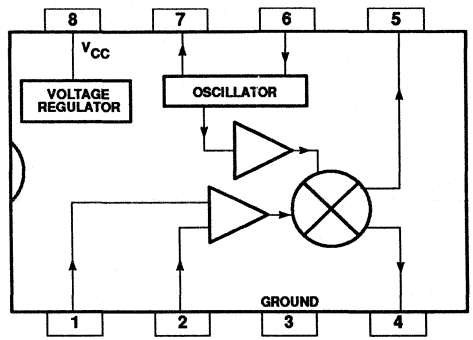


ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	NE602AN
8-Pin Plastic SO (Surface-mount)	0 to +70°C	NE602AD
8-Pin Cerdip	0 to +70°C	NE602AFE
8-Pin Plastic DIP	–40 to +85°C	SA602AN
8-Pin Plastic SO (Surface-mount)	–40 to +85°C	SA602AD
8-Pin Cerdip	–40 to +85°C	SA602AFE

Double–balanced mixer and oscillator NE/SA602A

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Maximum operating voltage	9	V
T_{STG}	Storage temperature range	–65 to +150	°C
T_A	Operating ambient temperature range NE602A	0 to +70	°C
	SA602A	–40 to +85	°C
θ_{JA}	Thermal impedance D package	90	°C/W
	N package	75	°C/W

AC/DC ELECTRICAL CHARACTERISTICS V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS NE/SA602A			UNITS
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		4.5		8.0	V
	DC current drain			2.4	2.8	mA
f_{IN}	Input signal frequency			500		MHz
f_{OSC}	Oscillator frequency			200		MHz
	Noise figure at 45MHz			5.0	5.5	dB
	Third–order intercept point	RF_{IN} = –45dBm: f_1 = 45.0MHz, f_2 = 45.06MHz		–13	–15	dBm
	Conversion gain at 45MHz		14	17		dB
R_{IN}	RF input resistance		1.5			kΩ
C_{IN}	RF input capacitance			3	3.5	pF
	Mixer output resistance	(Pin 4 or 5)		1.5		kΩ

DESCRIPTION OF OPERATION

The NE/SA602A is a Gilbert cell, an oscillator/buffer, and a temperature compensated bias network as shown in the equivalent circuit. The Gilbert cell is a differential amplifier (Pins 1 and 2) which drives a balanced switching cell. The differential input stage provides gain and determines the noise figure and signal handling performance of the system.

The NE/SA602A is designed for optimum low power performance. When used with the SA604 as a 45MHz cellular radio second IF and demodulator, the SA602A is capable of receiving –119dBm signals with a 12dB S/N ratio. Third–order intercept is typically –13dBm (that is approximately +5dBm output intercept because of the RF gain). The system designer must be cognizant of this large signal limitation. When designing LANs or other closed systems where transmission levels are high, and small–signal or signal–to–noise issues are not critical, the input to the NE602A should be appropriately scaled.

Besides excellent low power performance well into VHF, the NE/SA602A is designed to be flexible. The input, RF mixer output and oscillator ports can support a variety of configurations provided the designer understands certain constraints, which will be explained here.

The RF inputs (Pins 1 and 2) are biased internally. They are symmetrical. The equivalent AC input impedance is approximately 1.5k || 3pF through 50MHz. Pins 1 and 2 can be used interchangeably, but they should not be DC biased externally. Figure 3 shows three typical input configurations.

The mixer outputs (Pins 4 and 5) are also internally biased. Each output is connected to the internal positive supply by a 1.5kΩ resistor. This permits direct output termination yet allows for balanced output as well. Figure 4 shows three single ended output configurations and a balanced output.

The oscillator is capable of sustaining oscillation beyond 200MHz in crystal or tuned tank configurations. The upper limit of operation is determined by tank "Q" and required drive levels. The higher the "Q" of the tank or the smaller the required drive, the higher the permissible oscillation frequency. If the required LO is beyond oscillation limits, or the system calls for an external LO, the external signal can be injected at Pin 6 through a DC blocking capacitor. External LO should be at least 200mV_{P-P}.

Figure 5 shows several proven oscillator circuits. Figure 5a is appropriate for cellular radio. As shown, an overtone mode of operation is utilized. Capacitor C3 and inductor L1 suppress oscillation at the crystal fundamental frequency. In the fundamental mode, the suppression network is omitted.

Figure 6 shows a Colpitts varactor tuned tank oscillator suitable for synthesizer–controlled applications. It is important to buffer the output of this circuit to assure that switching spikes from the first counter or prescaler do not end up in the oscillator spectrum. The dual–gate MOSFET provides optimum isolation with low current. The FET offers good isolation, simplicity, and low current, while the bipolar transistors provide the simple solution for non–critical applications. The resistive divider in the emitter–follower circuit should be chosen to provide the minimum input signal which will assure correct system operation.

When operated above 100MHz, the oscillator may not start if the Q of the tank is too low. A 22kΩ resistor from Pin 7 to ground will increase the DC bias current of the oscillator transistor.

This improves the AC operating characteristic of the transistor and should help the oscillator to start. A 22kΩ resistor will not upset the other DC biasing internal to the device, but smaller resistance values should be avoided.

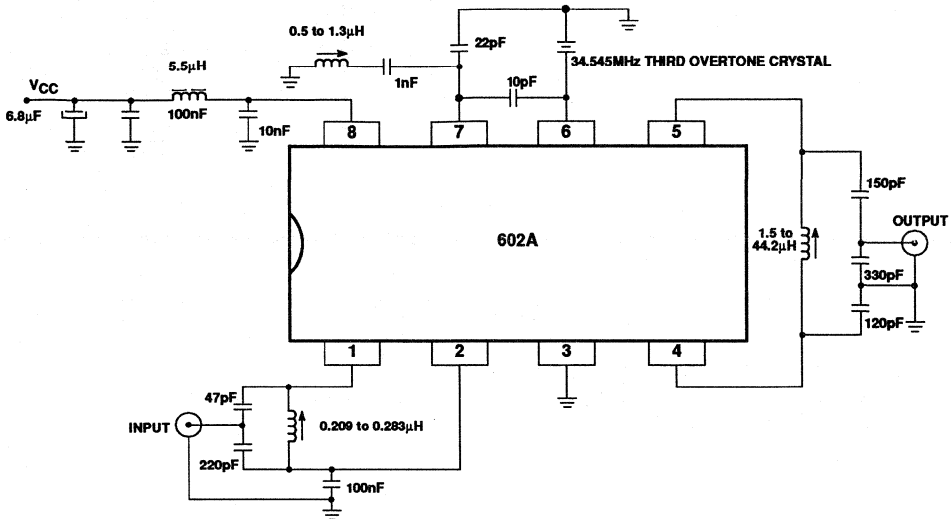


Figure 1. Test Configuration

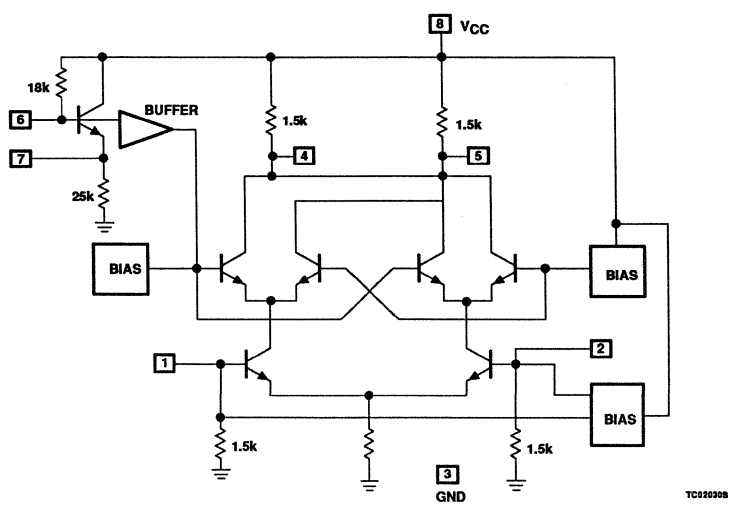
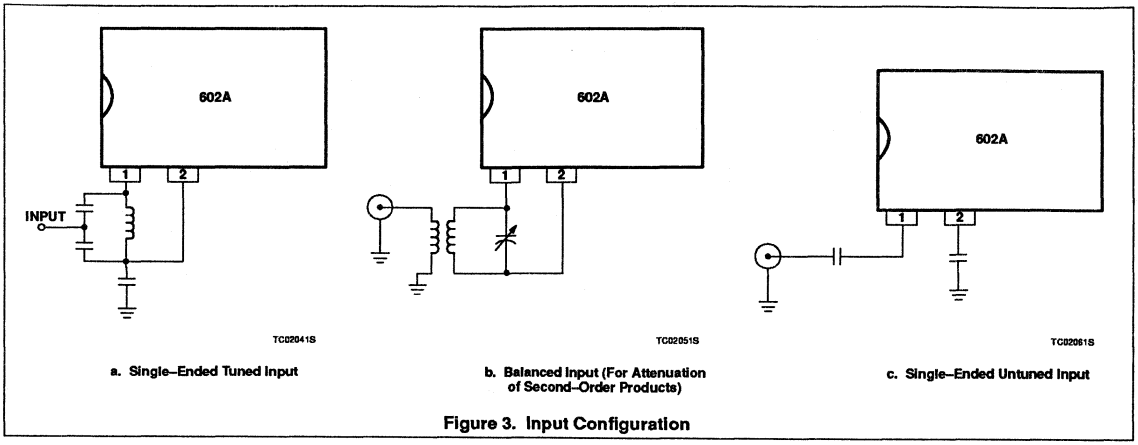


Figure 2. Equivalent Circuit

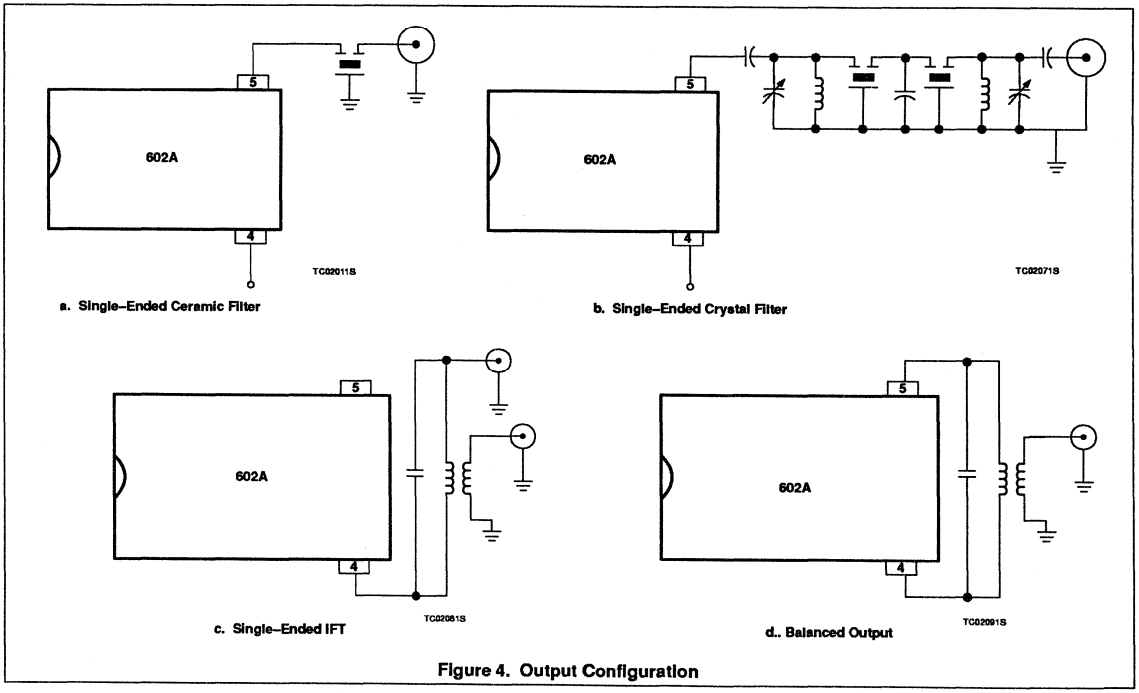


a. Single–Ended Tuned Input

b. Balanced Input (For Attenuation of Second–Order Products)

c. Single–Ended Untuned Input

Figure 3. Input Configuration



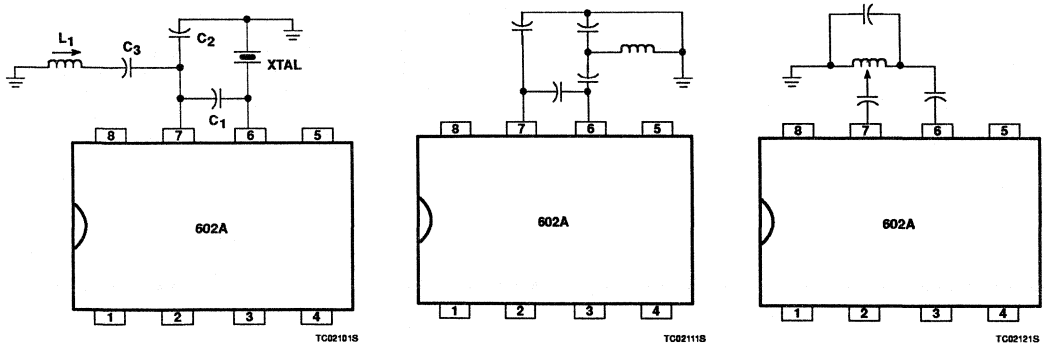
a. Single–Ended Ceramic Filter

b. Single–Ended Crystal Filter

c. Single–Ended IFT

d.. Balanced Output

Figure 4. Output Configuration



a. Colpitts Crystal Oscillator (Overtone Mode)

b. Colpitts L/C Tank Oscillator

c. Hartley L/C Tank Oscillator

Figure 5. Oscillator Circuits

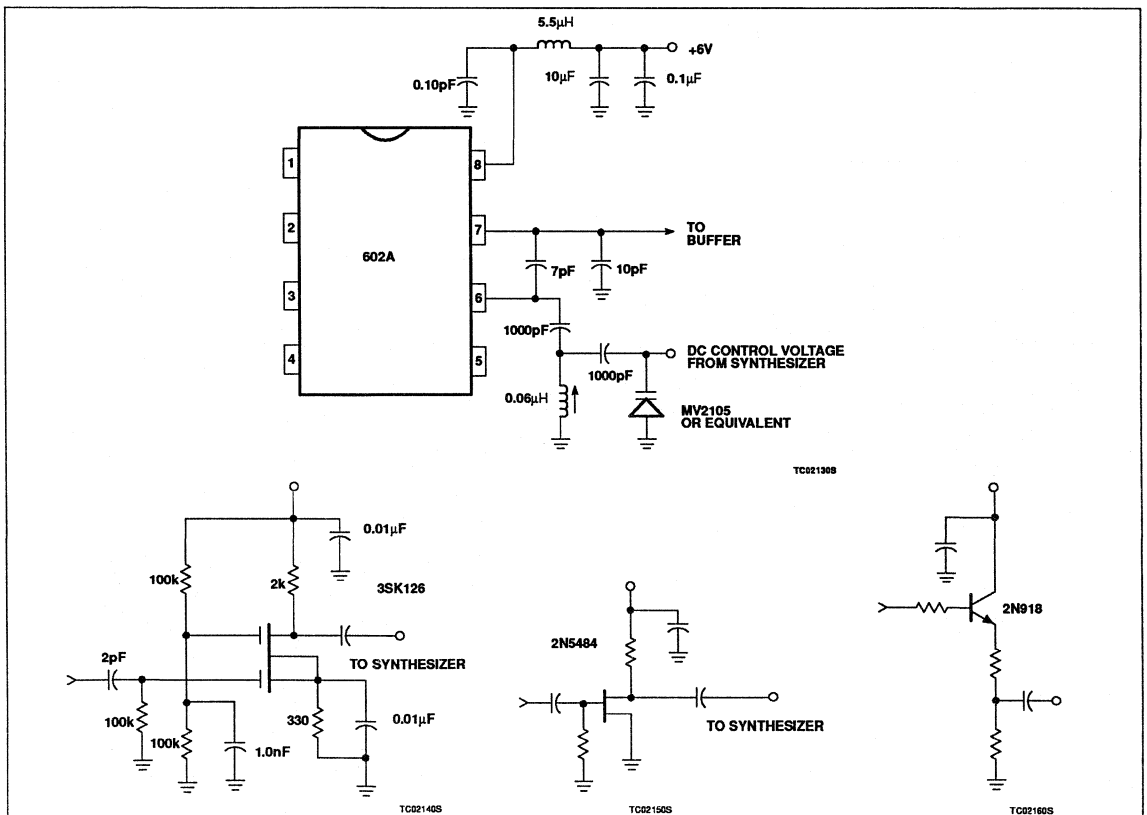


Figure 6. Colpitts Oscillator Suitable for Synthesizer Applications and Typical Buffers

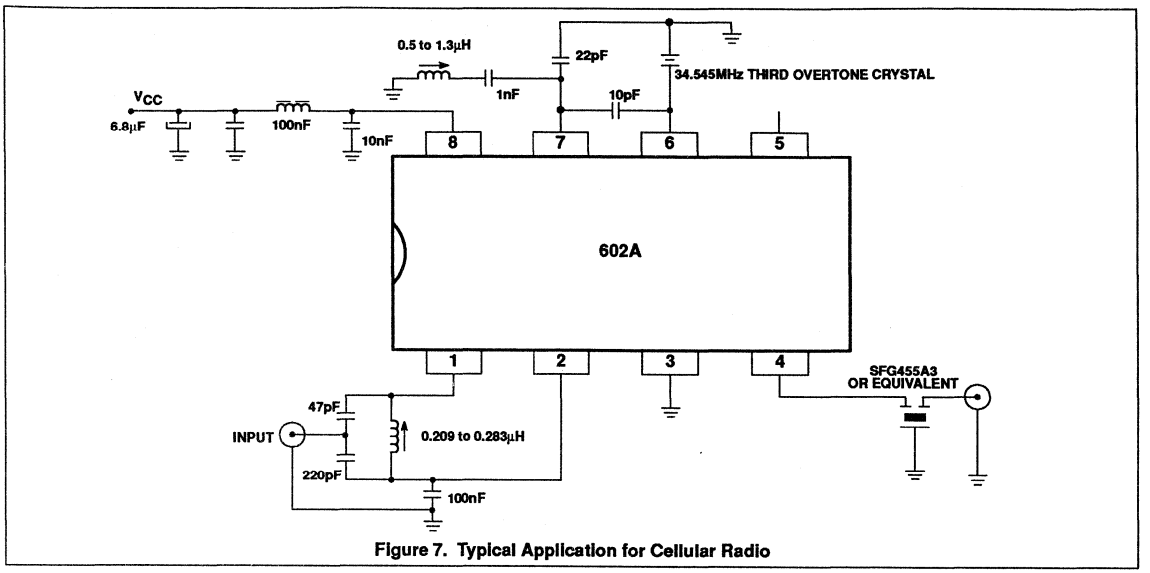


Figure 7. Typical Application for Cellular Radio

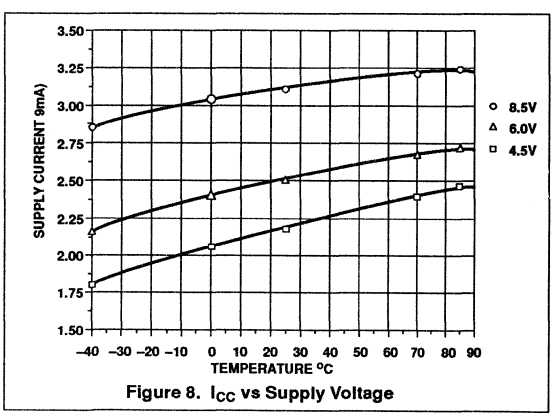


Figure 8. I_{CC} vs Supply Voltage

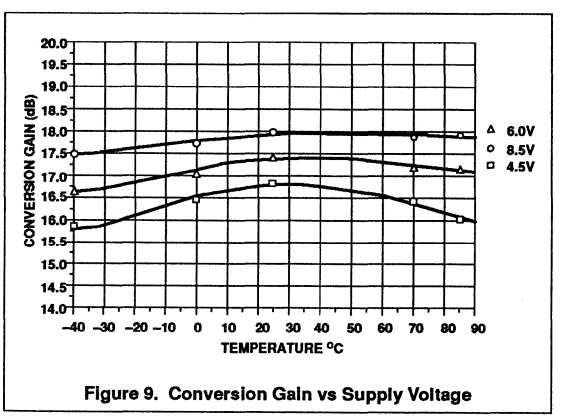


Figure 9. Conversion Gain vs Supply Voltage

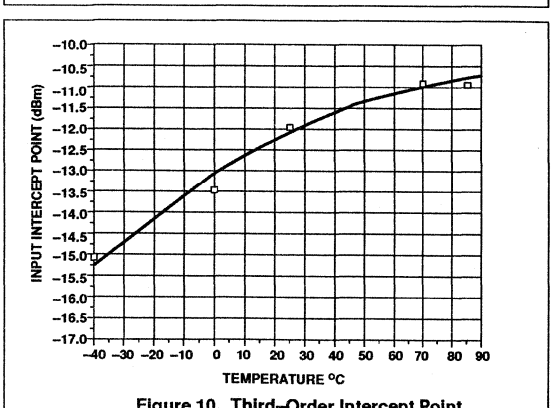


Figure 10. Third–Order Intercept Point

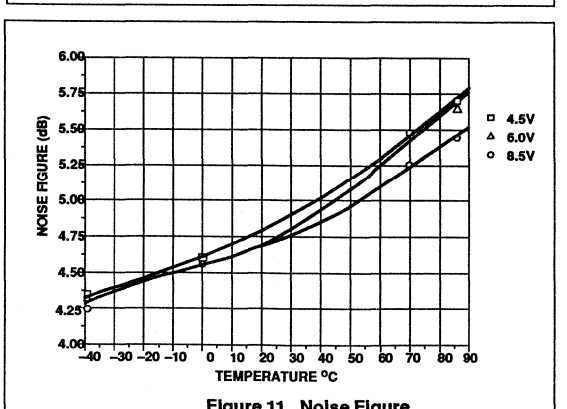


Figure 11. Noise Figure

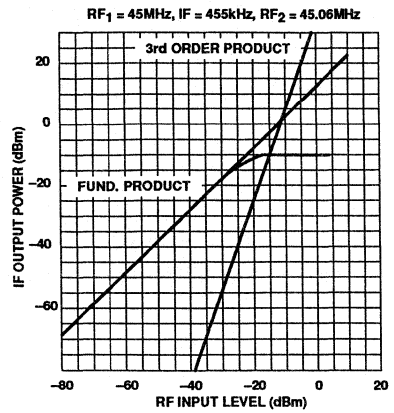


Figure 12. Third–Order Intercept and Compression

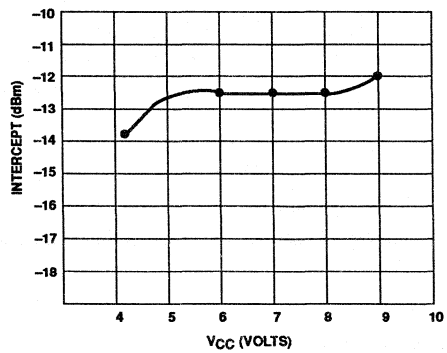


Figure 13. Input Third–Order Intermod Point vs V_{CC}

High performance low power FM IF system — NE/SA604A

DESCRIPTION

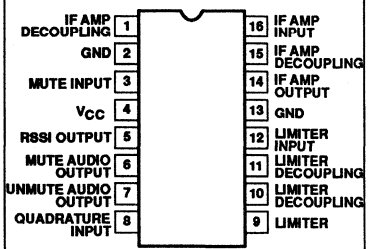
The NE/SA604A is an improved monolithic low-power FM IF system incorporating two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator, and voltage regulator. The NE/SA604A features higher IF bandwidth (25MHz) and temperature compensated RSSI and limiters permitting higher performance application compared with the NE/SA604. The NE/SA604A is available in a 16-lead dual-in-line plastic and 16-lead SO (surface-mounted miniature) package.

APPLICATIONS

- Cellular radio FM IF
- High performance communications receivers
- Intermediate frequency amplification and detection up to 25MHz
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers

PIN CONFIGURATION

D and N Packages



FEATURES

- Low power consumption: 3.3mA typical
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- Two audio outputs - muted and unmuted
- Low external component count; suitable for crystal/ceramic filters
- Excellent sensitivity: 1.5μV across input pins (0.22μV into 50Ω matching network) for 12dB SINAD (Signal to Noise and Distortion ratio) at 455kHz
- SA604A meets cellular radio specifications

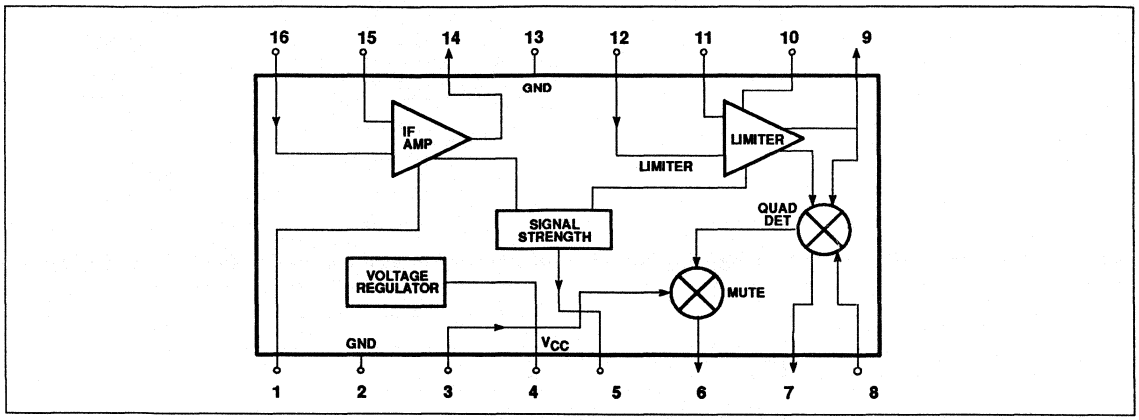
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic DIP	0 to +70°C	NE604AN	0406C
16-Pin Plastic SO (Surface-mount)	0 to +70°C	NE604AD	0005D
16-Pin Plastic DIP	-40 to +85°C	SA604AN	0406C
16-Pin Plastic SO (Surface-mount)	-40 to +85°C	SA604AD	0005D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	9	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range NE604A SA604A	0 to +70 -40 to +85	°C °C
θ_{JA}	Thermal impedance D package N package	90 75	°C/W °C/W

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE604A			SA604A			
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Power supply voltage range		4.5		8.0	4.5		8.0	V
I_{CC}	DC current drain		2.5	3.3	4.0	2.5	3.3	4.0	mA
	Mute switch input threshold (ON) (OFF)		1.7		 1.0	1.7		 1.0	V V

AC ELECTRICAL CHARACTERISTICS

Typical reading at $T_A = 25°C$; $V_{CC} = \pm 6V$, unless otherwise stated. IF frequency = 455kHz; IF level = -47dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

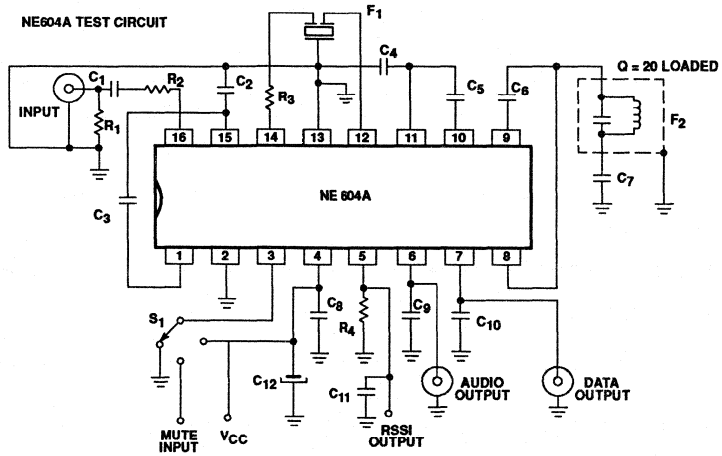
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE604A			SA604A			
			MIN	TYP	MAX	MIN	TYP	MAX	
	Input limiting -3dB	Test at Pin 16		-92			-92		dBm/50Ω
	AM rejection	80% AM 1kHz	30	34		30	34		dB
	Recovered audio level	15nF de-emphasis	110	175	250	80	175	260	mV_{RMS}
	Recovered audio level	150pF de-emphasis		530			530		mV_{RMS}
THD	Total harmonic distortion		-35	-42		-34	-42		dB
S/N	Signal-to-noise ratio	No modulation for noise		73			73		dB
	RSSI output[1]	RF level = -118dBm	0	160	550	0	160	650	mV
		RF level = -68dBm	2.0	2.65	3.0	1.9	2.65	3.1	V
		RF level = -18dBm	4.1	4.85	5.5	4.0	4.85	5.6	V
	RSSI range	R_4 = 100k (Pin 5)		90			90		dB
	RSSI accuracy	R_4 = 100k (Pin 5)		±1.5			±1.5		dB
	IF input impedance		1.4	1.6		1.4	1.6		kΩ
	IF output impedance		0.85	1.0		0.85	1.0		kΩ
	Limiter input impedance		1.4	1.6		1.4	1.6		kΩ
	Unmuted audio output resistance			58			58		kΩ
	Muted audio output resistance			58			58		kΩ

NOTE:

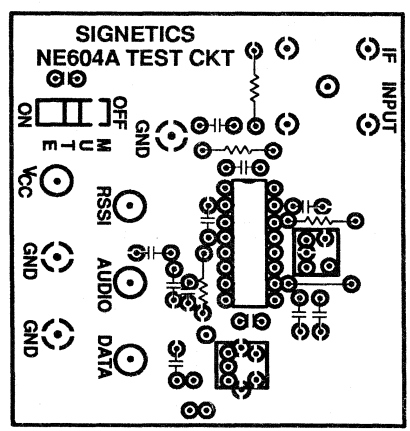
1. NE604 data sheets refer to power at 50Ω input termination; about 21dB less power actually enters the internal 1.5k input.

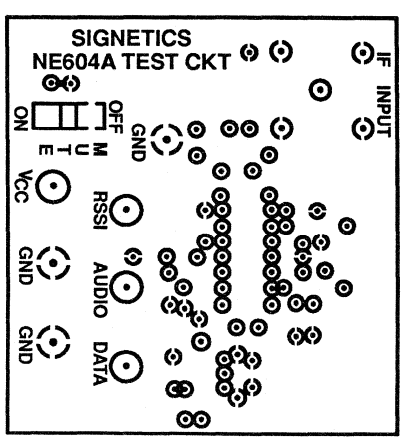
NE604 (50)	NE604A (1.5k)/NE605 (1.5k
-97dBm	-118dBm
-47dBm	-68dBm
+3dBm	-18dBm

The NE605 and NE604A are both derived from the same basic die. The NE605 performance plots are directly applicable to the NE604A.



C1	100nF + 80 – 20% 63V K10000–25V Ceramic
C2	100nF +10% 50V
C3	100nF ±10% 50V
C4	100nF +10% 50V
C5	100nF ±10% 50V
C6	10pF ±2% 100V NPO Ceramic
C7	100nF ±10% 50V
C8	100nF ±10% 50V
C9	15nF ±10% 50V
C10	150pF ±2% 100V N1500 Ceramic
C11	1nF ±10% 100V K2000-Y5P Ceramic
C12	6.8µF ±20% 25V Tantalum
F1	455kHz Ceramic Filter Murata SFG455A3
F2	455kHz (Ce = 180pF) TOKO RMC 2A6597H
R1	51Ω ±1% 1/4W Metal Film
R2	1500Ω ±1% 1/4W Metal Film
R3	1500Ω ±5% 1/8W Carbon Composition
R4	100kΩ ±1% 1/4W Metal Film





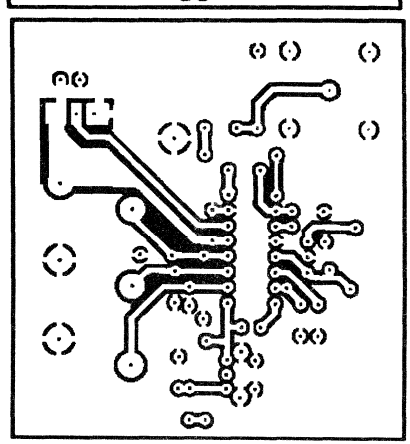


Figure 1. NE/SA604A Test Circuit

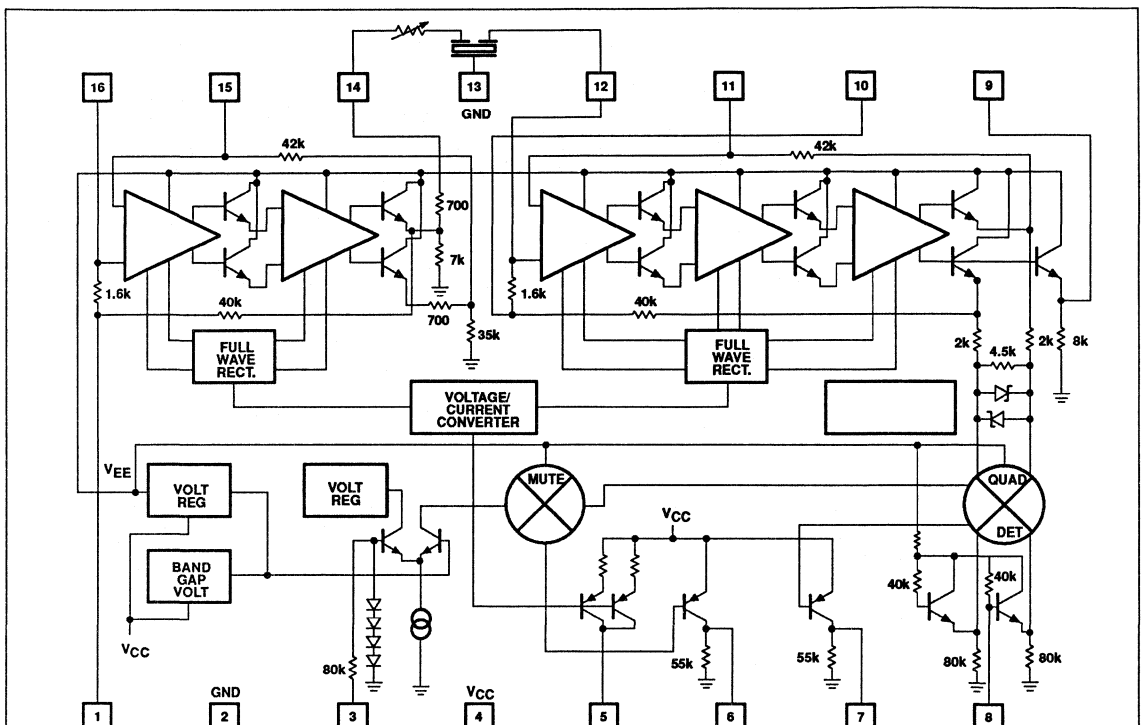


Figure 2. Equivalent Circuit

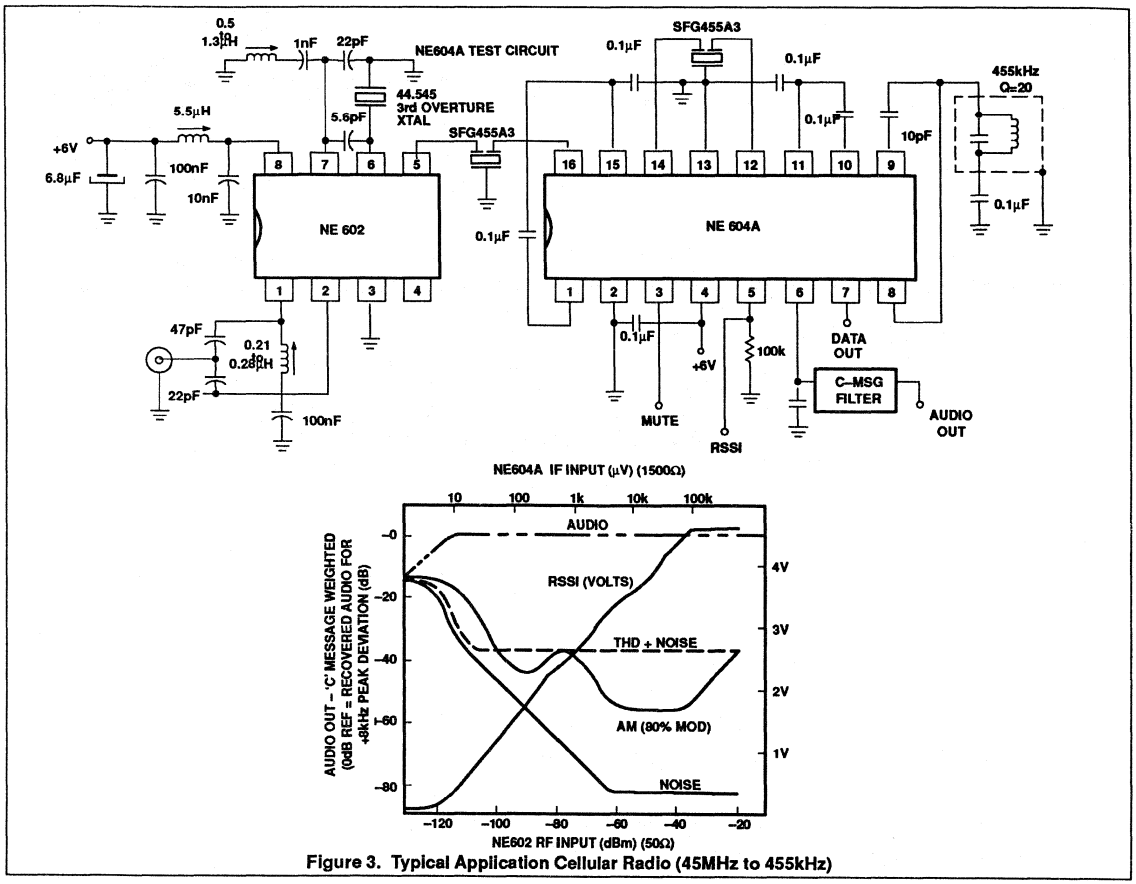


Figure 3. Typical Application Cellular Radio (45MHz to 455kHz)

CIRCUIT DESCRIPTION

The NE/SA604A is a very high gain, high frequency device. Correct operation is not possible if good RF layout and gain stage practices are not used. The NE/SA604A cannot be evaluated independent of circuit, components, and board layout. A physical layout which correlates to the electrical limits is shown in Figure 1. This configuration can be used as the basis for production layout.

The NE/SA604A is an IF signal processing system suitable for IF frequencies as high as 21.4MHz. The device consists of two limiting amplifiers, quadrature detector, direct audio output, muted audio output, and signal strength indicator (with output characteristic). The sub-systems are shown in Figure 2. A typical application with 45MHz input and 455kHz IF is shown in Figure 3.

IF Amplifiers

The IF amplifier section consists of two log-limiting stages. The first consists of two differential amplifiers with 39dB of gain and a small signal bandwidth of 41MHz (when driven from a 50Ω source). The output of the first limiter is a low impedance emitter follower with 1kΩ of equivalent series resistance. The second limiting stage consists of three differential amplifiers with a gain of 62dB and a small signal AC bandwidth of 28MHz. The outputs of the final differential stage are buffered to the internal quadrature detector. One of the outputs is available at Pin 9 to drive an external quadrature capacitor and L/C quadrature tank.

Both of the limiting amplifier stages are DC biased using feedback. The buffered output of the final differential amplifier is fed back to the input through 42kΩ resistors. As shown in Figure 2, the input impedance is established for each stage by tapping one of the feedback resistors 1.6kΩ from the input. This requires one additional decoupling capacitor from the tap point to ground.

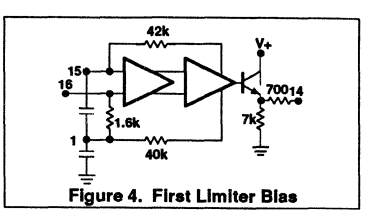


Figure 4. First Limiter Bias

Because of the very high gain, bandwidth and input impedance of the limiters, there is a very real potential for instability at IF frequencies above 455kHz. The basic phenomenon is shown in Figure 6. Distributed feedback (capacitance, inductance and radiated fields)

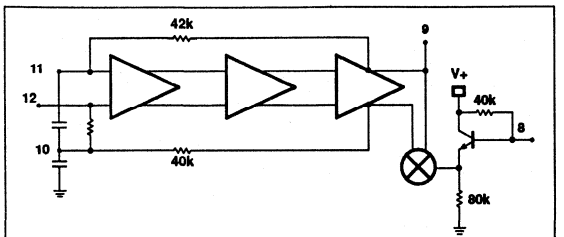


Figure 5. Second Limiter and Quadrature Detector

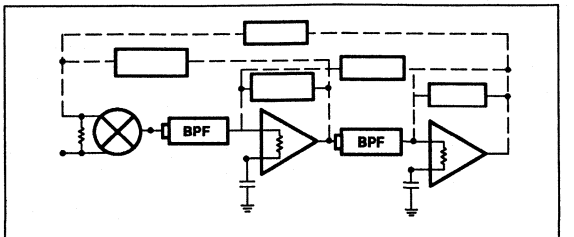
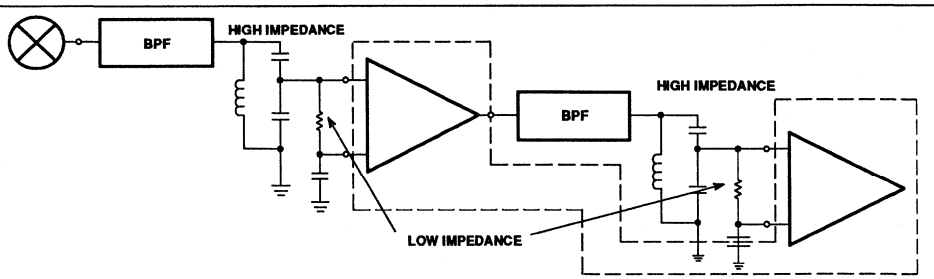
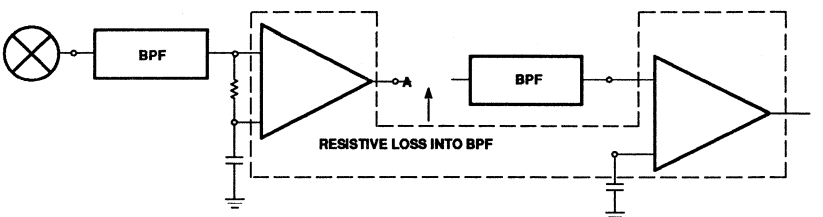


Figure 6. Feedback Paths



7a. Terminating High Impedance Filters with Transformation to Low Impedance



7b. Low Impedance Termination and Gain Reduction

Figure 7. Practical Termination

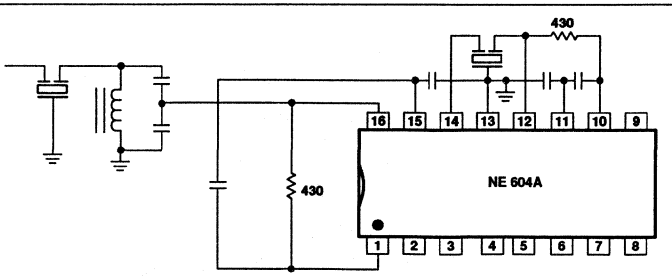


Figure 8. Crystal Input Filter with Ceramic Interstage Filter

forms a divider from the output of the limiters back to the inputs (including RF input). If this feedback divider does not cause attenuation greater than the gain of the forward path, then oscillation or low level regeneration is likely. If regeneration occurs, two symptoms may be present: (1)The RSSI output will be high with no signal input (should nominally be 250mV or lower), and (2) the demodulated output will demonstrate a threshold. Above a certain input level, the limited signal will begin to dominate the regeneration, and the demodulator will begin to operate in a "normal" manner.

There are three primary ways to deal with regeneration: (1) Minimize the feedback by gain stage isolation, (2) lower the stage input impedances, thus increasing the feedback attenuation factor, and (3) reduce the gain. Gain reduction can effectively be accomplished by adding attenuation between stages. This can also lower the input impedance if well planned. Examples of impedance/gain adjustment are shown in

Figure 7. Reduced gain will result in reduced limiting sensitivity.

A feature of the NE604A IF amplifiers, which is not specified, is low phase shift. The NE604A is fabricated with a 10GHz process with very small collector capacitance. It is advantageous in some applications that the phase shift changes only a few degrees over a wide range of signal input amplitudes.

Stability Considerations

The high gain and bandwidth of the NE604A in combination with its very low currents permit circuit implementation with superior performance. However, stability must be maintained and, to do that, every possible feedback mechanism must be addressed. These mechanisms are: 1) Supply lines and ground, 2) stray layout inductances and capacitances, 3) radiated fields, and 4) phase shift. As the system IF increases, so must the attention to fields and strays. However, ground and supply loops cannot be overlooked, especially at lower frequencies. Even at 455kHz, using the test layout in Figure 1, instability will occur if the supply line is not decoupled with two high quality RF capacitors, a 0.1μF monolithic right at the V_{CC} pin, and a 6.8μF tantalum on the supply line. An electrolytic is not an adequate substitute. At 10.7MHz, a 1μF tantalum has proven acceptable with this layout. Every layout must be evaluated on its own merit, but don't underestimate the importance of good supply bypass.

At 455kHz, if the layout of Figure 1 or one substantially similar is used, it is possible to directly connect ceramic filters to the input and between limiter stages with no special consideration. At frequencies above 2MHz, some input impedance reduction is usually necessary. Figure 7 demonstrates a practical means.

As illustrated in Figure 8, 430Ω external resistors are applied in parallel to the internal 1.6kΩ load resistors, thus presenting approximately 330Ω to the filters. The input filter is a crystal type for narrowband selectivity. The filter is terminated with a tank which transforms to 330Ω. The interstage filter is a ceramic type which doesn't contribute to system selectivity, but does suppress wideband noise and stray signal pickup. In wideband 10.7MHz IFs the input filter can also be ceramic, directly connected to Pin 16.

In some products it may be impractical to utilize shielding, but this mechanism may be appropriate to 10.7MHz and 21.4MHz IF. One of the benefits of low current is lower radiated field strength, but lower does not mean non-existent. A spectrum analyzer with an active probe will clearly show IF energy with the probe held in the proximity of the second limiter output or quadrature coil. No specific recommendations are provided, but mechanical shielding should be considered if layout, bypass, and input impedance reduction do not solve a stubborn instability.

The final stability consideration is phase shift. The phase shift of the limiters is very low, but there is phase shift contribution from the quadrature tank and the filters. Most filters demonstrate a large phase shift across their passband (especially at the edges). If the quadrature detector is tuned to the edge of the filter passband, the combined filter and quadrature phase shift can aggravate stability. This is not usually a problem, but should be kept in mind.

Quadrature Detector

Figure 5 shows an equivalent circuit of the NE604A quadrature detector. It is a multiplier cell similar to a mixer stage. Instead of mixing two different frequencies, it mixes two signals of common frequency but different phase. Internal to the device, a constant amplitude (limited) signal is differentially applied to the lower port of the multiplier. The same signal is applied single-ended to an external capacitor at Pin 9. There is a 90° phase shift across the plates of this capacitor, with the phase shifted signal applied to the upper port of the multiplier at Pin 8. A quadrature tank (parallel L/C network) permits frequency selective phase shifting at the IF frequency. This quadrature tank must be returned to ground through a DC blocking capacitor.

The loaded Q of the quadrature tank impacts three fundamental aspects of the detector: Distortion, maximum modulated peak deviation, and audio output amplitude. Typical quadrature curves are illustrated in Figure 10. The phase angle translates to a shift in the multiplier output voltage.

Thus a small deviation gives a large output with a high Q tank. However, as the deviation from resonance increases, the non-linearity of the curve increases (distortion), and, with too much deviation, the signal will be outside the quadrature region (limiting the peak deviation which can be demodulated). If the same peak deviation is applied to a lower Q tank, the deviation will remain in a region of the curve which is more linear (less distortion), but creates a smaller phase angle (smaller output amplitude). Thus the Q of the quadrature tank must be tailored to the design. Basic equations and an example for determining Q are shown below. This explanation includes first-order effects only.

Frequency Discriminator Design Equations for NE604A

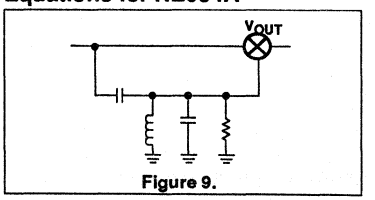


Figure 9.

$$V_O = \frac{C_S}{C_P + C_S} \bullet \frac{1}{1 + \frac{\omega_1}{Q_1 S} + \left(\frac{\omega_1}{S}\right)^2} \bullet V_{IN} \quad (1a)$$

$$\text{where } \omega_1 = \frac{1}{\sqrt{L(C_P + C_S)}} \quad (1b)$$

$$Q_1 = R\,(C_P + C_S)\,\omega_1 \quad (1c)$$

From the above equation, the phase shift between nodes 1 and 2, or the phase across C_S will be:

$$\phi = \angle V_O - \angle V_{IN} = t_g^{-1}\left[\frac{\frac{\omega_1}{Q_1\omega}}{1 - \left(\frac{\omega_1}{\omega}\right)^2}\right] \quad (2)$$

Figure 10 is the plot of ϕ vs. $\left(\frac{\omega}{\omega_1}\right)$

It is notable that at $\omega = \omega_1$, the phase shift is $\frac{\pi}{2}$ and the response is close to a straight line with a slope of $\frac{\Delta\phi}{\Delta\omega} = \frac{2Q_1}{\omega_1}$

The signal V_O would have a phase shift of $\left[\frac{\pi}{2} - \frac{2Q_1}{\omega_1}\,\omega\right]$ with respect to the V_{IN}.

$$\text{If } V_{IN} = A \sin \omega t \Rightarrow V_O = A \sin\left[\omega t + \frac{\pi}{2} - \frac{2Q_1}{\omega_1}\,\omega\right] \quad (3)$$

Multiplying the two signals in the mixer, and low pass filtering yields:

$$V_{IN} \bullet V_O = A^2 \sin \omega t \sin\left[\omega t + \frac{\pi}{2} - \frac{2Q_1}{\omega_1}\,\omega\right] \quad (4)$$

after low pass filtering

$$\Rightarrow V_{OUT} = \frac{1}{2} A^2 \cos\left[\frac{\pi}{2} - \frac{2Q_1}{\omega_1}\,\omega\right] \quad (5)$$

$$= \frac{1}{2} A^2 \sin\left(\frac{2Q_1}{\omega_1}\right)\omega$$

$$V_{OUT} \propto 2Q_1 \frac{\omega_1}{\omega} = \left[2Q_1 \left(\frac{\omega_1 + \Delta\omega}{\omega_1} \right) \right] \quad (6)$$

For $\frac{2Q_1\omega}{\omega_1} << \frac{\pi}{2}$

Which is discriminated FM output. (Note that $\Delta\omega$ is the deviation frequency from the carrier ω_1.

Ref. Krauss, Raab, Bastian; Solid State Radio Eng.; Wiley, 1980, p. 311. Example: At 455kHz IF, with ±5kHz FM deviation. The maximum normalized frequency will be

$$\frac{455 \pm 5kHz}{455} = 1.010 \text{ or } 0.990$$

Go to the f vs. normalized frequency curves (Figure 10) and draw a vertical straight line at $\frac{\omega}{\omega_1} = 1.01$.

The curves with Q = 100, Q = 40 are not linear, but Q = 20 and less shows better linearity for this application. Too small Q decreases the amplitude of the discriminated FM signal. (Eq. 6) $\Rightarrow$ Choose a Q = 20

The internal R of the 604A is 40k. From Eq. 1c, and then 1b, it results that

$C_P + C_S = 174pF$ and $L = 0.7mH$.

A more exact analysis including the source resistance of the previous stage shows that there is a series and a parallel resonance in the phase detector tank. To make the parallel and series resonances close, and to get maximum attenuation of higher harmonics at 455kHz IF, we have found that a $C_S = 10pF$ and $C_P = 164pF$ (commercial values of 150pF or 180pF may be practical), will give the best results. A variable inductor which can be adjusted around 0.7mH should be chosen and optimized for minimum distortion. (For 10.7MHz, a value of $C_S = 1pF$ is recommended.)

Audio Outputs

Two audio outputs are provided. Both are PNP current-to-voltage converters with 55kΩ nominal internal loads. The unmuted output is always active to permit the use of signaling tones in systems such as cellular radio. The other output can be muted with 70dB typical attenuation. The two outputs have an internal 180° phase difference.

The nominal frequency response of the audio outputs is 300kHz. this response can be increased with the addition of external resistors from the output pins to ground in parallel with the internal 55k resistors, thus lowering the output time constant. Singe the output structure is a current-to-voltage converter (current is driven into the resistance, creating a voltage drop), adding external parallel resistance also has the effect of lowering the output audio amplitude and DC level.

This technique of audio bandwidth expansion can be effective in many applications such as SCA receivers and data transceivers.

Because the two outputs have a 180° phase relationship, FSK demodulation can be accomplished by applying the two output differentially across the inputs of an op amp or comparator. Once the threshold of the reference frequency (or "no-signal" condition) has been established, the two outputs will shift in opposite directions (higher or lower output voltage) as the input frequency shifts. The output of the comparator will be logic output. The choice of op amp or comparator will depend on the data rate. With high IF frequency (10MHz and above), and wide IF bandwidth (L/C filters) data rates in excess of 4Mbaud are possible.

RSSI

The "received signal strength indicator", or RSSI, of the NE604A demonstrates monotonic logarithmic output over a range of 90dB. The signal strength output is derived from the summed stage currents in the limiting amplifiers. It is essentially independent of the IF frequency. Thus, unfiltered signals at the limiter inputs, spurious products, or regenerated signals will manifest themselves as RSSI outputs. An RSSI output of greater than 250mV with no signal (or a very small signal) applied, is an indication of possible regeneration or oscillation.

In order to achieve optimum RSSI linearity, there must be a 12dB insertion loss between the first and second limiting amplifiers. With a typical 455kHz ceramic filter, there is a nominal 4dB insertion loss in the filter. An additional 6dB is lost in the interface between the filter and the input of the second limiter. A small amount of additional loss must be introduced with a typical ceramic filter. In the test circuit used for cellular radio applications (Figure 3) the optimum linearity was achieved with a 5.1kΩ resistor from the output of the first limiter (Pin 14) to the input of the interstage filter. With this resistor from Pin 14 to the filter, sensitivity of 0.25μV for 12dB SINAD was achieved. With the 3.6kΩ resistor, sensitivity was optimized at 0.22μV for 12dB SINAD with minor change in the RSSI linearity.

Any application which requires optimized RSSI linearity, such as spectrum analyzers, cellular radio, and certain types of telemetry, will require careful attention to limiter interstage component selection. This will be especially true with high IF frequencies which require insertion loss or impedance reduction for stability.

At low frequencies the RSSI makes an excellent logarithmic AC voltmeter.

For data applications the RSSI is effective as an amplitude shift keyed (ASK) data slicer. If a comparator is applied to the RSSI and the threshold set slightly above the no signal level, when an in-band signal is received the comparator will be sliced. Unlike FSK demodulation, the maximum data rate is somewhat limited. An internal capacitor limits the RSSI frequency response to about 100kHz. At high data rates the rise and fall times will not be symmetrical.

The RSSI output is a current-to-voltage converter similar to the audio outputs. However, an external resistor is required. With a 91kΩ resistor, the output characteristic is 0.5V for a 10dB change in the input amplitude.

Additional Circuitry

Internal to the NE604A are voltage and current regulators which have been temperature compensated to maintain the performance of the device over a wide temperature range. These regulators are not accessible to the user.

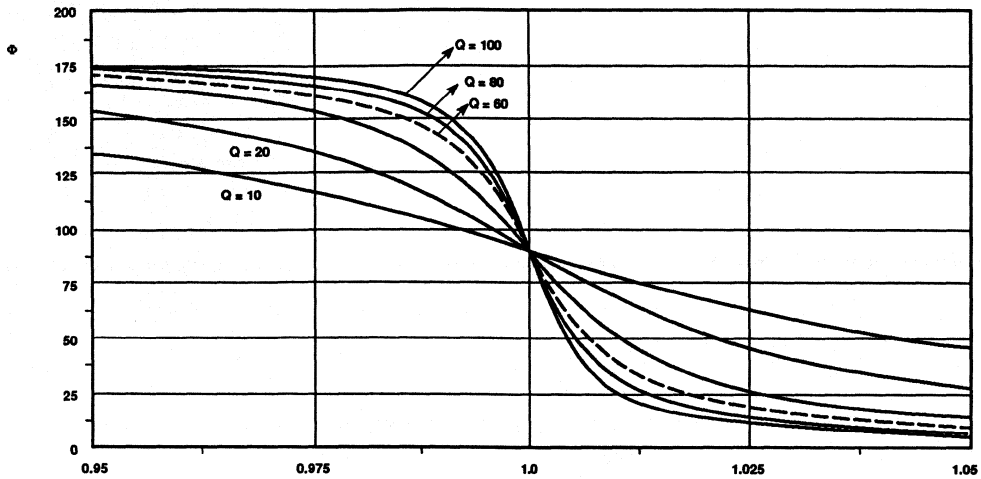


Figure 10. Phase vs Normalized IF Frequency $\frac{\omega}{\omega_1} = 1 + \frac{\Delta\omega}{\omega_1}$

High performance low power mixer FM IF system — NE/SA605

DESCRIPTION

The NE/SA605 is a high performance monolithic low-power FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator (RSSI), and voltage regulator. The NE/SA605 combines the functions of Signetics' NE602 and NE604A, but features a higher mixer input intercept point, higher IF bandwidth (25MHz) and temperature compensated RSSI and limiters permitting higher performance application. The NE/SA605 is available in 20-lead dual-in-line plastic, 20-lead SOL (surface-mounted miniature package) and 20-lead SSOP (shrink small outline package).

The NE/SA605 and NE/SA615 are functionally the same device types. The difference between the two devices lies in the guaranteed specifications. The NE/SA615 has a higher I_{CC}, lower input third order intercept point, lower conversion mixer gain, lower limiter gain, lower AM rejection, lower SINAD, higher THD, and higher RSSI error than the NE/SA605. Both the NE/SA605 and NE/SA615 devices will meet the EIA specifications for AMPS and TACS cellular radio applications.

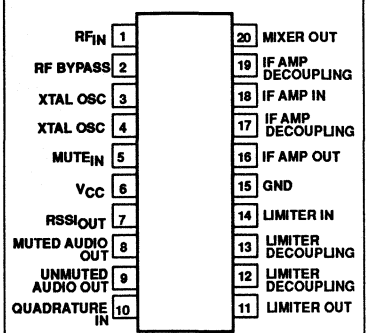
For additional technical information please refer to application notes AN1994, 1995 and 1996, which include example application diagrams, a complete overview of the product, and artwork for reference.

FEATURES

- Low power consumption: 5.7mA typical at 6V
- Mixer input to >500MHz
- Mixer conversion power gain of 13dB at 45MHz
- Mixer noise figure of 4.6dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator to 1GHz local oscillator can be injected)
- 102dB of IF Amp/Limiter gain
- 25MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- Two audio outputs - muted and unmuted
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.22μV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone with RF at 45MHz and IF at 455kHz
- SA605 meets cellular radio specifications
- ESD hardened

PIN CONFIGURATION

N, D and DK Packages



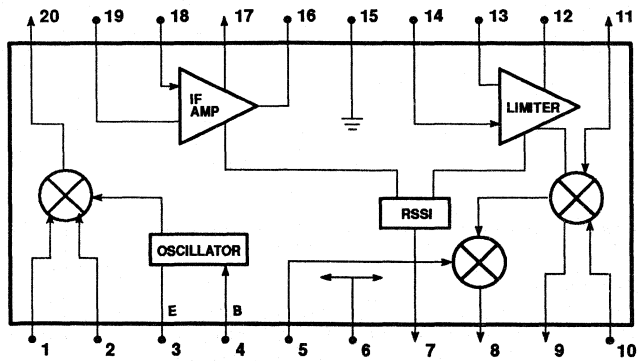
APPLICATIONS

- Cellular radio FM IF
- High performance communications receivers
- Single conversion VHF/UHF receivers
- SCA receivers
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Wideband low current amplification

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic DIP	0 to +70°C	NE605N	0408B
20-Pin Plastic DIP	–40 to +85°C	SA605N	0408B
20-Pin Plastic SOL	0 to +70°C	NE605D	0172D
20-Pin Plastic SOL	–40 to +85°C	SA605D	0172D
20-Pin Plastic SSOP	0 to +70°C	NE605DK	1563
20-Pin Plastic SSOP	–40 to +85°C	SA605DK	1563

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		RATING	UNITS
V_{CC}	Single supply voltage		9	V
T_{STG}	Storage temperature range		-65 to +150	°C
T_A	Operating ambient temperature range NE605		0 to +70	°C
		SA605	-40 to +85	°C
θ_{JA}	Thermal impedance	D package N package SSOP package	90 75 117	°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE605			SA605			
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Power supply voltage range		4.5		8.0	4.5		8.0	V
I_{CC}	DC current drain		5.1	5.7	6.5	4.55	5.7	6.55	mA
	Mute switch input threshold (ON)		1.7			1.7			V
	(OFF)				1.0			1.0	V

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +6V, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step-up; IF frequency = 455kHz; R17 = 5.1k; RF level = -45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE605			SA605			
			MIN	TYP	MAX	MIN	TYP	MAX	
Mixer/Osc section (ext LO = 300mV)									
f_{IN}	Input signal frequency			500			500		MHz
f_{OSC}	Crystal oscillator frequency			150			150		MHz
	Noise figure at 45MHz			5.0			5.0		dB
	Third-order input intercept point	f1 = 45.0; f2 = 45.06MHz		-10			-10		dBm
	Conversion power gain	Matched 14.5dBV step-up	10.5	13	14.5	10	13	15	dB
		50Ω source		-1.7			-1.7		dB
	RF input resistance	Single-ended input	3.5	4.7		3.0	4.7		kΩ
	RF input capacitance			3.5	4.0		3.5	4.0	pF
	Mixer output resistance	(Pin 20)	1.3	1.5		1.25	1.5		kΩ
IF section									
	IF amp gain	50Ω source		39.7			39.7		dB
	Limiter gain	50Ω source		62.5			62.5		dB
	Input limiting -3dB, R_{17} = 5.1k	Test at Pin 18		-113			-113		dBm
	AM rejection	80% AM 1kHz	30	34	42	29	34	43	dB
	Audio level, R_{10} = 100k	15nF de-emphasis	110	150	250	80	150	260	mV_{RMS}
	Unmuted audio level, R_{11} = 100k	150pF de-emphasis		480			480		mV
	SINAD sensitivity	RF level -118dB		16			16		dB
THD	Total harmonic distortion		-35	-42		-34	-42		dB
S/N	Signal-to-noise ratio	No modulation for noise		73			73		dB
	IF RSSI output, R_9 = 100kΩ[1]	IF level = -118dBm	0	160	550	0	160	650	mV
		IF level = -68dBm	2.0	2.5	3.0	1.9	2.5	3.1	V
		IF level = -18dBm	4.1	4.8	5.5	4.0	4.8	5.6	V
	RSSI range	R_9 = 100kΩ Pin 16		90			90		dB
	RSSI accuracy	R_9 = 100kΩ Pin 16		±1.5			±1.5		dB
	IF input impedance		1.40	1.6		1.40	1.6		kΩ
	IF output impedance		0.85	1.0		0.85	1.0		kΩ
	Limiter input impedance		1.40	1.6		1.40	1.6		kΩ
	Unmuted audio output resistance			58			58		kΩ
	Muted audio output resistance			58			58		kΩ
RF/IF section (Int LO)									
	Unmuted audio level	4.5V = V_{CC}, RF level = -27dBm		450			450		mV_{RMS}
	System RSSI output	4.5V = V_{CC}, RF level = -27dBm		4.3			4.3		V

NOTE:

1. The generator source impedance is 50Ω, but the NE/SA605 input impedance at Pin 18 is 1500Ω. As a result, IF level refers to the actual signal that enters the NE/SA605 input (Pin 8) which is about 21dB less than the "available power" at the generator.

CIRCUIT DESCRIPTION

The NE/SA605 is an IF signal processing system suitable for second IF or single conversion systems with input frequency as high as 1GHz. The bandwidth of the IF amplifier is about 40MHz, with 39.7dB(v) of gain from a 50Ω source. The bandwidth of the limiter is about 28MHz with about 62.5dB(v) of gain from a 50Ω source. However, the gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 5dB, conversion gain of 13dB, and input third-order intercept of -10dBm. The oscillator will operate in excess of 1GHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

The output of the mixer is internally loaded with a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor can be added between the first IF output (Pin 16) and the interstage network.

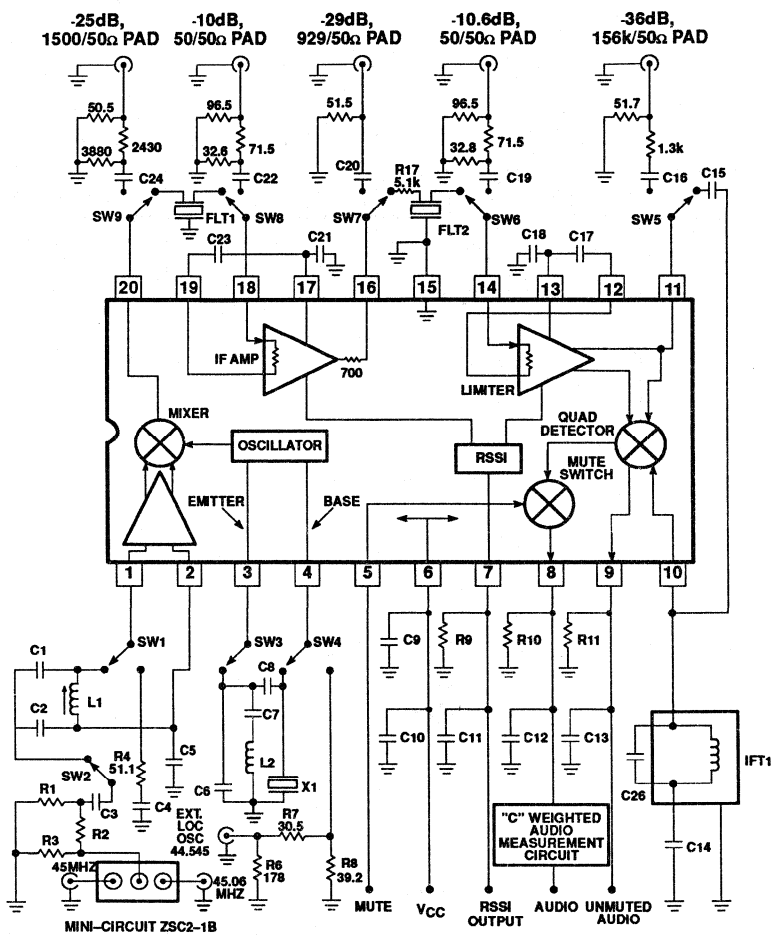
The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

Overall, the IF section has a gain of 90dB. For operation at intermediate frequencies greater than 455kHz, special care must be given to layout, termination, and interstage loss to avoid instability.

The demodulated output of the quadrature detector is available at two pins, one continuous and one with a mute switch. Signal attenuation with the mute activated is greater than 60dB. The mute input is very high impedance and is compatible with CMOS or TTL levels.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone.

NOTE: $dB(v) = 20\log V_{OUT}/V_{IN}$

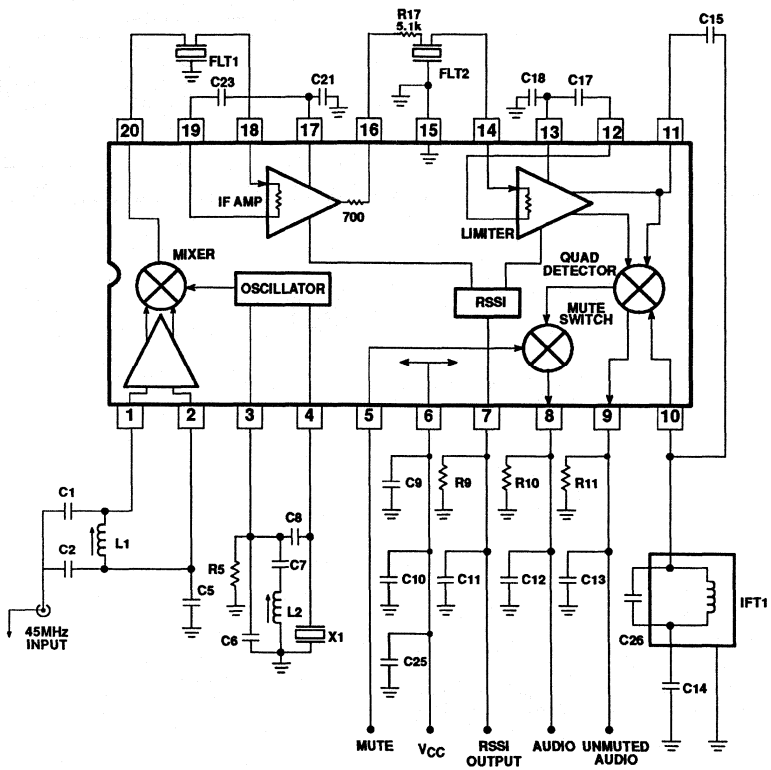


Automatic Test Circuit Component List

C1	47pF NPO Ceramic	C21	100nF ±10% Monolithic Ceramic
C2	180pF NPO Ceramic	C23	100nF ±10% Monolithic Ceramic
C5	100nF ±10% Monolithic Ceramic	C25	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic	C26	390pF ±10% Monolithic Ceramic
C7	1nF Ceramic	Flt 1	Ceramic Filter Murata SFG455A3 or equiv
C8	10.0pF NPO Ceramic	Flt 2	Ceramic Filter Murata SFG455A3 or equiv
C9	100nF ±10% Monolithic Ceramic	IFT 1	455kHz 270μH TOKO #303LN-1129
C10	6.8μF Tantalum (minimum) *	L1	300nH TOKO #5CB-1055Z
C11	100nF ±10% Monolithic Ceramic	L2	0.8μH TOKO 292CNS–T1038Z
C12	15nF ±10% Ceramic	X1	44.545MHz Crystal ICM4712701
C13	150pF ±2% N1500 Ceramic	R9	100k ±1% 1/4W Metal Film
C14	100nF ±10% Monolithic Ceramic	R17	5.1k ±5% 1/4W Carbon Composition
C15	10pF NPO Ceramic	R10	100k ±1% 1/4W Metal Film (optional)
C17	100nF ±10% Monolithic Ceramic	R11	100k ±1% 1/4W Metal Film (optional)
C18	100nF ±10% Monolithic Ceramic		

* NOTE: This value can be reduced when a battery is the power source.

Figure 1. NE/SA605 45MHz Test Circuit (Relays as shown)



Application Component List

C1	47pF NPO Ceramic
C2	180pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	6.8μF Tantalum (minimum)
C11	100nF ±10% Monolithic Ceramic
C12	15nF ±10% Ceramic
C13	150pF ±2% N1500 Ceramic
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
C26	390pF ±10% Monolithic Ceramic
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	455kHz 270μH TOKO #303LN-1129
L1	300nH TOKO #5CB-1055Z
L2	0.8μH TOKO 292CNS–T1038Z
X1	44.545MHz Crystal ICM4712701
R9	100k ±1% 1/4W Metal Film
R17	5.1k ±5% 1/4W Carbon Composition
R10	100k ±1% 1/4W Metal Film (optional)
R11	100k ±1% 1/4W Metal Film (optional)

* NOTE: This value can be reduced when a battery is the power source.

Figure 2. NE/SA605 45MHz Application Circuit

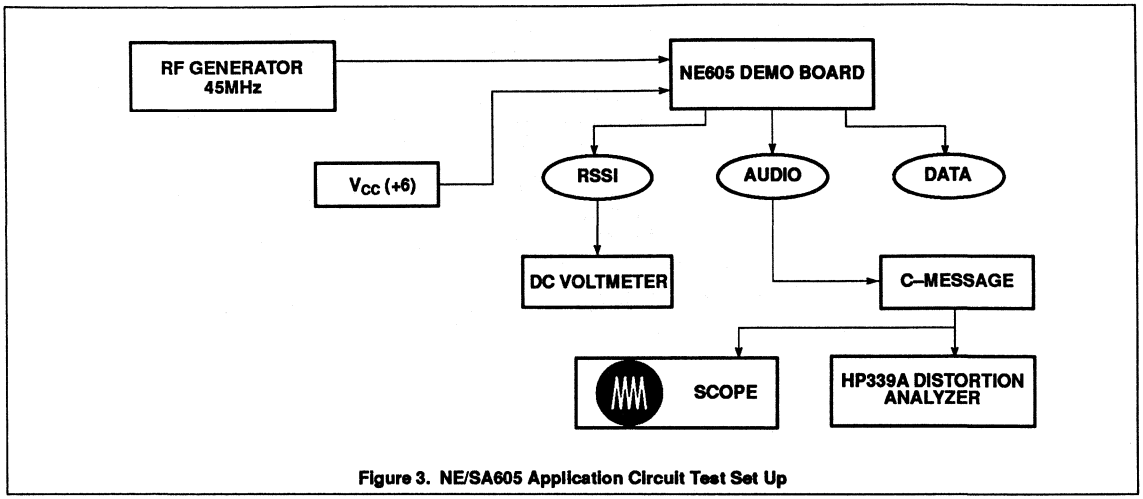


Figure 3. NE/SA605 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message filter has a peak gain of 100 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.22μV or -120dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 250mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10-15μF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1μF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2-3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 22kΩ, but should not be below 10kΩ.

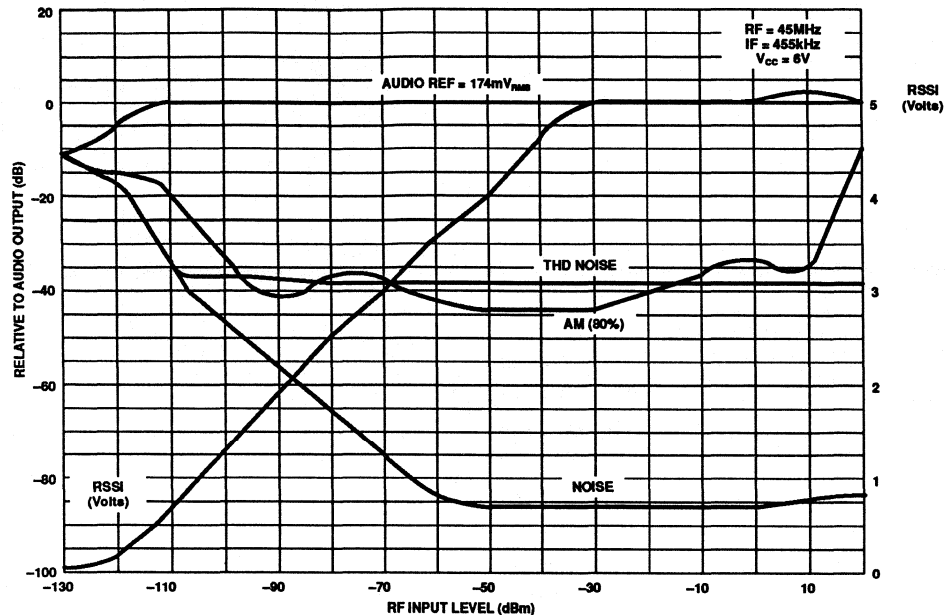


Figure 4. NE605 Application Board at 25°C

Low-voltage high performance mixer FM IF system — NE/SA606

DESCRIPTION

The NE/SA606 is a low-voltage high performance monolithic FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), voltage regulator and audio and RSSI op amps. The NE/SA606 is available in 20-lead dual-in-line plastic, 20-lead SOL (surface-mounted small outline large package) and 20-lead SSOP (shrink small outline package).

The NE606 was designed for portable communication applications and will function down to 2.7V. The RF section is similar to the famous NE605. The audio and RSSI outputs have amplifiers with access to the feedback path. This enables the designer to level adjust the outputs or add filtering.

FEATURES

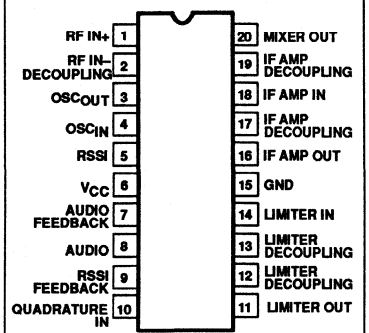
- Low power consumption: 3.5mA typical at 3V
- Mixer input to >150MHz
- Mixer conversion power gain of 17dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator or external oscillator can be used at higher frequencies)
- 102dB of IF Amp/Limiter gain
- 2MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a 90dB dynamic range
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.31μV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone with RF at 45MHz and IF at 455kHz
- SA606 meets cellular radio specifications
- Audio output internal op amp
- RSSI output internal op amp
- Internal op amps with rail-to-rail outputs
- ESD protection: Human Body Model 2kV
  Robot Model 200V

APPLICATIONS

- Portable cellular radio FM IF
- Cordless phones
- Wireless systems
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Portable high performance communication receiver
- Single conversion VHF receivers

PIN CONFIGURATION

D, DK and N Packages



ORDERING INFORMATION

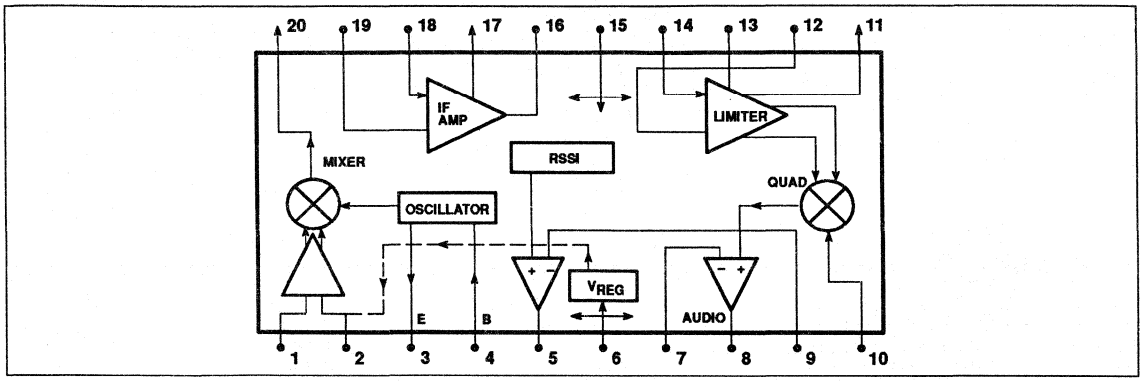
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic DIP	0 to +70°C	NE606N	0408B
20-Pin Plastic SOL (Surface-mount)	0 to +70°C	NE606D	0172D
20-Pin Plastic SSOP (Surface-mount)	0 to +70°C	NE606DK	1563
20-Pin Plastic DIP	-40 to +85°C	SA606N	0408B
20-Pin Plastic SOL (Surface-mount)	-40 to +85°C	SA606D	0172D
20-Pin Plastic SSOP (Surface-mount)	-40 to +85°C	SA606DK	1563

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		RATING	UNITS
V_{CC}	Single supply voltage		7	V
T_{STG}	Storage temperature range		–65 to +150	°C
T_A	Operating ambient temperature range	NE606	0 to +70	°C
		SA606	–40 to +85	°C
θ_{JA}	Thermal impedance	D package DK package N package	90 117 75	°C/W

Low-voltage high performance mixer FM IF system | NE/SA606

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS NE/SA606			UNITS
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		2.7		7.0	V
I_{CC}	DC current drain			3.5	4.2	mA

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +3V, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step-up; IF frequency = 455kHz; R17 = 2.4kΩ and R18 = 3.3kΩ; RF level = –45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with de-emphasis filter and C-message weighted filter. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS NE/SA606			UNITS
			MIN	TYP	MAX	
Mixer/Osc section (ext LO = 220mV$_{RMS}$)						
f_{IN}	Input signal frequency			150		MHz
f_{OSC}	Crystal oscillator frequency			150		MHz
	Noise figure at 45MHz			6.2		dB
	Third–order input intercept point (50Ω source)	f1 = 45.0; f2 = 45.06MHz Input RF level = –52dBm		–9		dBm
	Conversion power gain	Matched 14.5dBV step–up	13.5	17	19.5	dB
		50Ω source		+2.5		dB
	RF input resistance	Single–ended input		8		kΩ
	RF input capacitance			3.0	4.0	pF
	Mixer output resistance	(Pin 20)	1.25	1.5		kΩ
IF section						
	IF amp gain	50Ω source		44		dB
	Limiter gain	50Ω source		58		dB
	Input limiting –3dB, R_{17a} = 2.4k, R_{17b} = 3.3k	Test at Pin 18		–109		dBm
	AM rejection	80% AM 1kHz		45		dB
	Audio level	Gain of two (2kΩ AC load)	70	120	160	mV
	SINAD sensitivity	IF level –110dBm		17		dB

AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE606			
			MIN	TYP	MAX	
THD	Total harmonic distortion		–35	–50		dB
S/N	Signal–to–noise ratio	No modulation for noise		62		dB
	IF RSSI output, R_9 = 2kΩ[1]	IF level = –118dBm		0.3	.80	V
		IF level = –68dBm	.70	1.1	1.80	V
		IF level = –23dBm	1.20	1.8	2.50	V
	RSSI range			90		dB
	RSSI accuracy			±1.5		dB
	IF input impedance	Pin 18	1.3	1.5		kΩ
	IF output impedance	Pin 16		0.3		kΩ
	Limiter input impedance	Pin 14	1.3	1.5		kΩ
	Limiter output impedance	Pin 11		0.3		kΩ
	Limiter output voltage	Pin 11		130		mV_{RMS}
RF/IF section (Int LO)						
	Audio level	3V = V_{CC}, RF level = –27dBm		120		mV_{RMS}
	System RSSI output	3V = V_{CC}, RF level = –27dBm		2.2		V
	System SINAD sensitivity	RF level = –117dBm		12		dB

NOTE:
1. The generator source impedance is 50Ω, but the NE/SA606 input impedance at Pin 18 is 1500Ω. As a result, IF level refers to the actual signal that enters the NE/SA606 input (Pin 18) which is about 21dB less than the "available power" at the generator.

CIRCUIT DESCRIPTION

The NE/SA606 is an IF signal processing system suitable for second IF systems with input frequency as high as 150MHz. The bandwidth of the IF amplifier and limiter is at least 2MHz with 90dB of gain. The gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 6.2dB, conversion gain of 17dB, and input third-order intercept of –9dBm. The oscillator will operate in excess of 200MHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

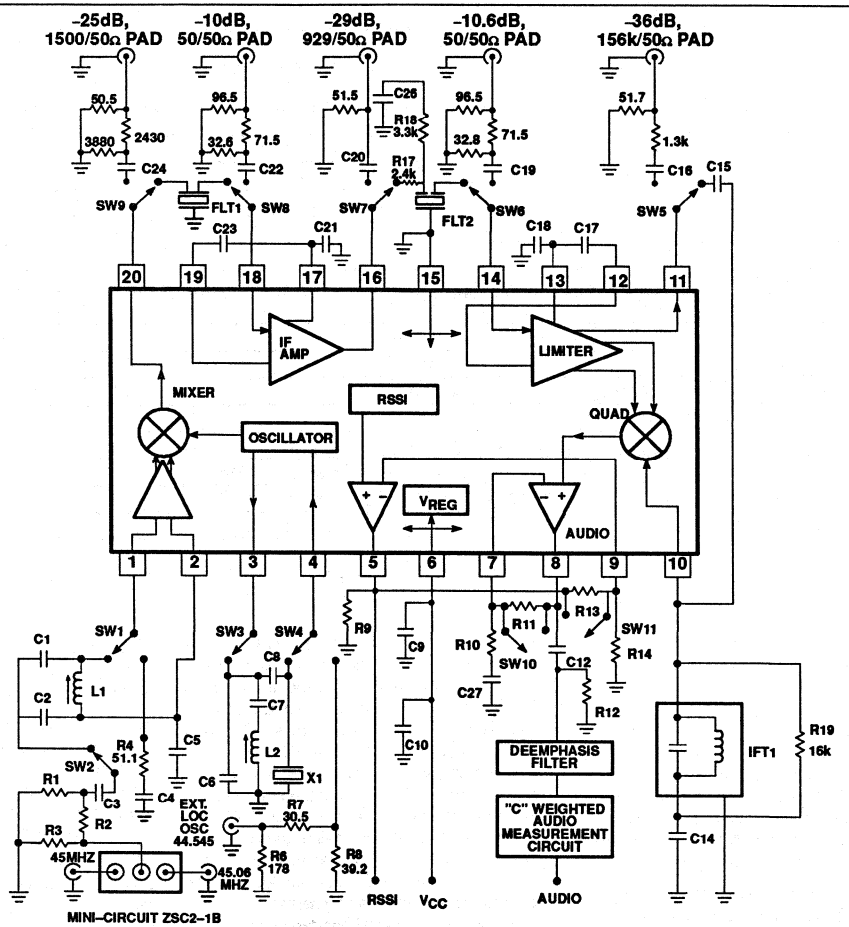
The output impedance of the mixer is a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. The IF amplifier has 43dB of gain and 5.5MHz bandwidth. The IF limiter has 60dB of gain and 4.5MHz bandwidth. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor or an L pad for simultaneous loss and impedance matching can be added between the first IF output (Pin 16) and the interstage network. The overall gain will then be 90dB with 2MHz bandwidth.

The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

The demodulated output of the quadrature drives an internal op amp. This op amp can be configured as a unity gain buffer, or for simultaneous gain, filtering, and 2nd-order temperature compensation if needed. It can drive an AC load as low as 5kΩ with a rail-to-rail output.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone. This signal drives an internal op amp. The op amp is capable of rail-to-rail output. It can be used for gain, filtering, or 2nd-order temperature compensation of the RSSI, if needed.

NOTE: $dB(v) = 20\log V_{OUT}/V_{IN}$

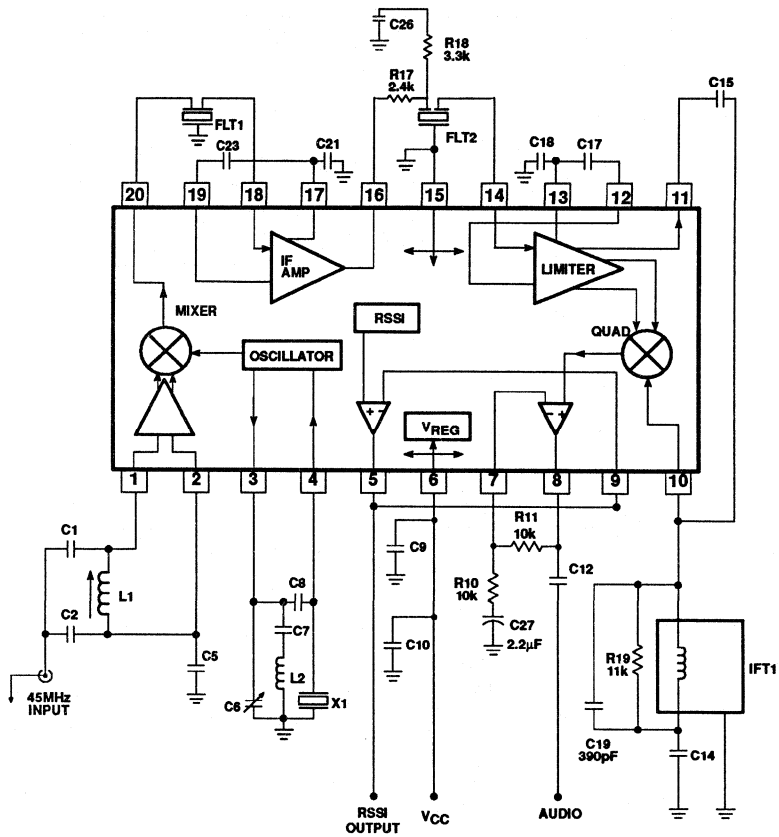


Automatic Test Circuit Component List

C1	100pF NPO Ceramic	C27	2.2µF ±10% Monolithic Ceramic
C2	390pF NPO Ceramic	Flt 1	Ceramic Filter Murata SFG455A3 or equiv
C5	100nF ±10% Monolithic Ceramic	Flt 2	Ceramic Filter Murata SFG455A3 or equiv
C6	22pF NPO Ceramic	IFT 1	455kHz (Ce = 180pF) Toko RMC–2A6597H
C7	1nF Ceramic	L1	147–160nH Coilcraft UNI–10/142–04J08S
C8	10.0pF NPO Ceramic	L2	0.8µH nominal Toko 292CNS–T1038Z
C9	100nF ±10% Monolithic Ceramic		
C10	10µF Tantalum (minimum) *	X1	44.545MHz Crystal ICM4712701
C12	2.2µF	R9	2kΩ ±1% 1/4W Metal Film
C14	100nF ±10% Monolithic Ceramic	R10	10kΩ ±1%
C15	10pF NPO Ceramic	R11	10kΩ ±1%
C17	100nF ±10% Monolithic Ceramic	R12	2kΩ ±1%
C18	100nF ±10% Monolithic Ceramic	R13	20kΩ ±1%
C21	100nF ±10% Monolithic Ceramic	R14	10kΩ ±1%
C23	100nF ±10% Monolithic Ceramic	R17	2.4kΩ ±5% 1/4W Carbon Composition
C25	100nF ±10% Monolithic Ceramic	R18	3.3kΩ
C26	100nF ±10% Monolithic Ceramic	R19	16kΩ

*NOTE: This value can be reduced when a battery is the power source.

Figure 1. NE/SA606 45MHz Test Circuit (Relays as shown)



NE606D/DK Demo Board
Application Component List

C1	51pF NPO Ceramic
C2	220pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	5-30pF trim cap
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	10µF Tantalum (minimum) *
C12	2.2µF ±10% Tantalum
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C19	390pF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C26	100nF ±10% Monolithic Ceramic
C27	2.2µF Tantalum
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	330µH TOKO 303LN-1130
L1	.33µH TOKO SCB-1320Z
L2	1.2µH
X1	44.545MHz Crystal ICM4712701
R5	Not Used in Application Board (see Note 8, pg 8)
R10	8.2k ±5% 1/4W Carbon Composition
R11	10k ±5% 1/4W Carbon Composition
R17	2.4k ±5% 1/4W Carbon Composition
R18	3.3k ±5% 1/4W Carbon Composition
R19	11k ±5% 1/4W Carbon Composition

* NOTE: This value can be reduced when a battery is the power source.

Figure 2. NE/SA606 45MHz Application Circuit

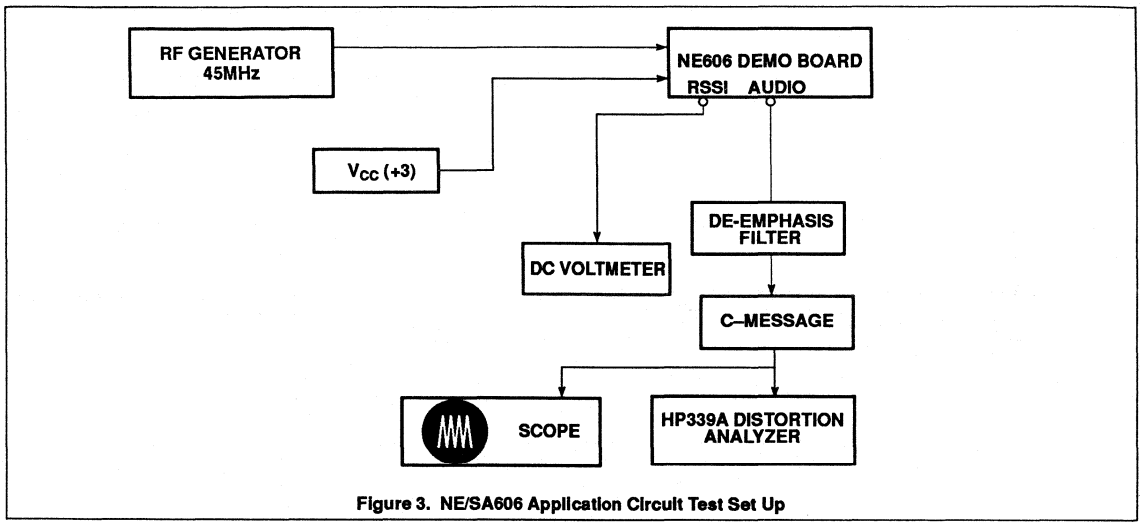


Figure 3. NE/SA606 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message and de-emphasis filter combination has a peak gain of 10 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer. The de-emphasis filter has a fixed -6dB/Octave slope between 300Hz and 3kHz.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.35μV or –116dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 500mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10-15μF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1μF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2-3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 10kΩ.

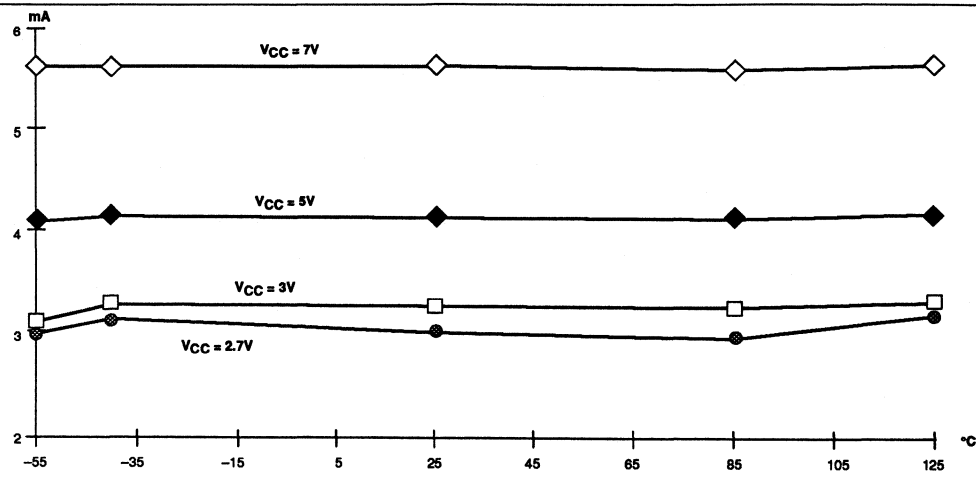


Figure 4. I_{CC} vs Temperature

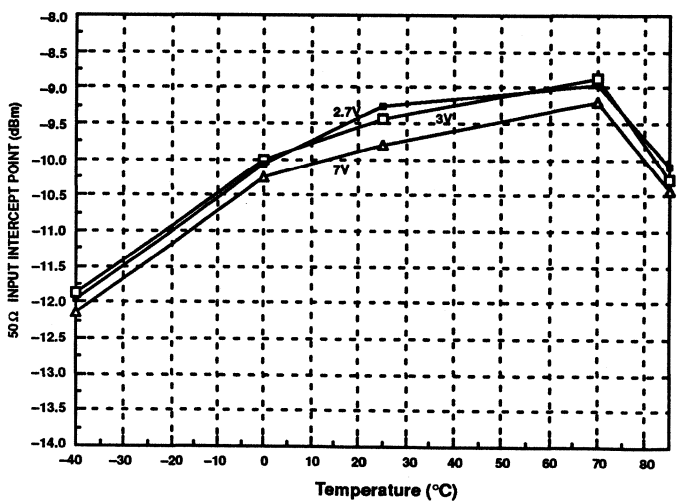


Figure 5. Third Order Intercept Point vs Supply Voltage

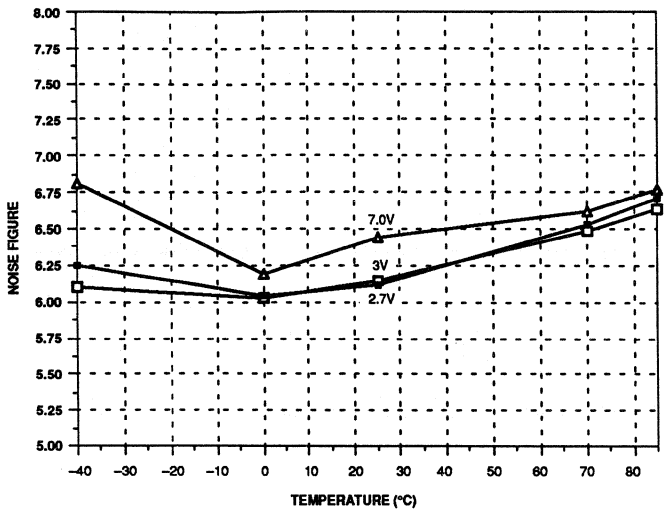


Figure 6. Mixer Noise Figure vs Supply Voltage

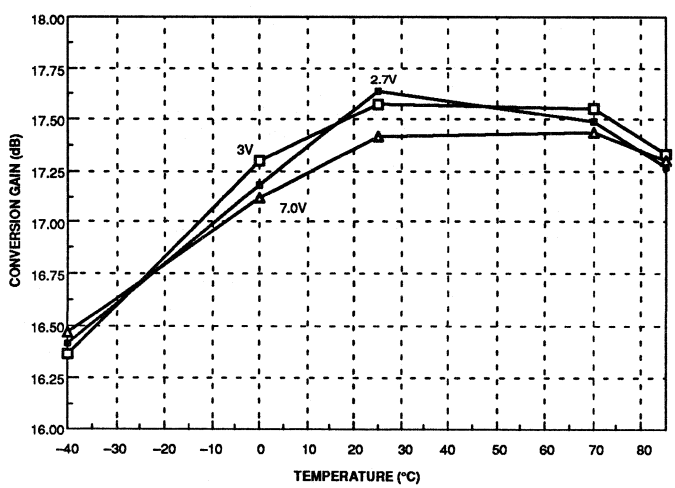
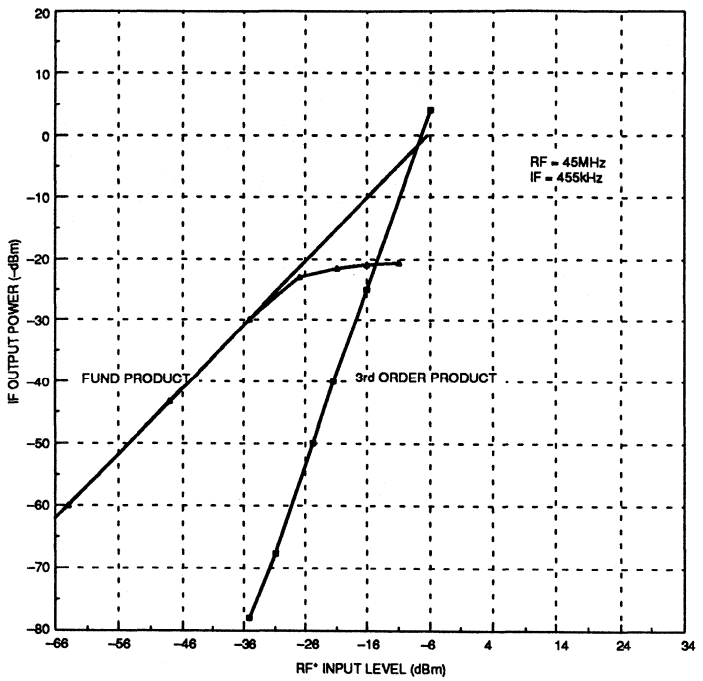


Figure 7. Conversion Gain vs Supply Voltage



*50Ω INPUT

Figure 8. Mixer Third Order Intercept and Compression

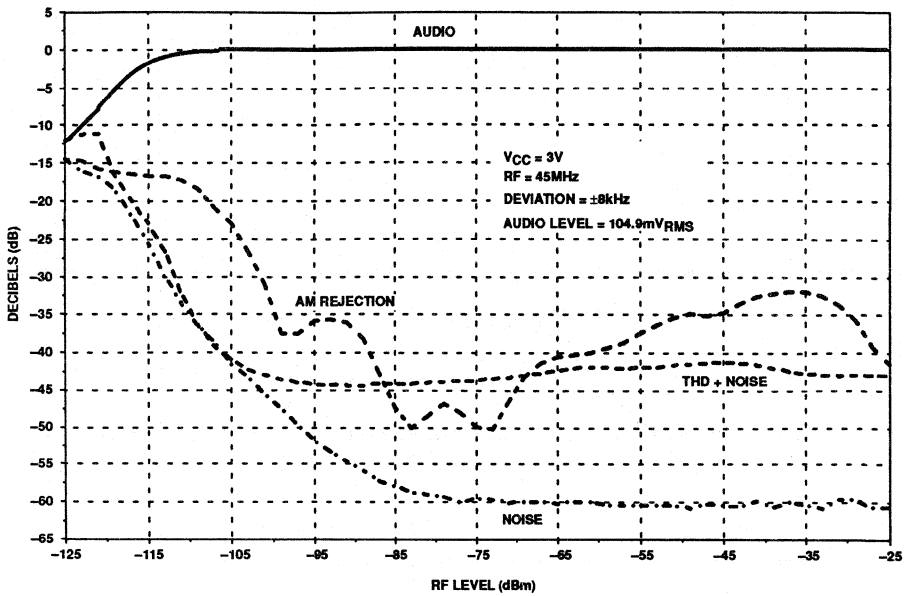


Figure 9. Sensitivity vs RF Level (–40°C)

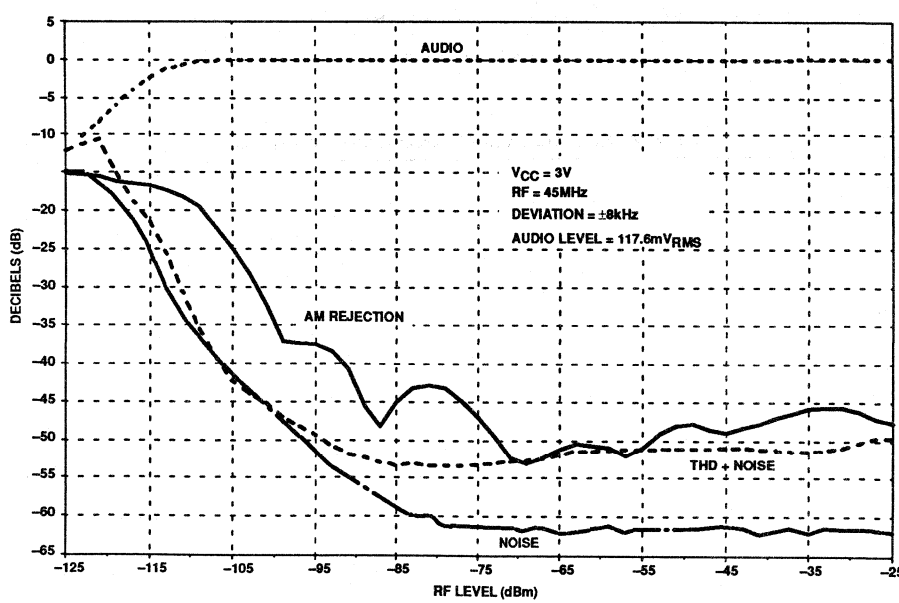


Figure 10. Sensitivity vs RF Level (+25°C)

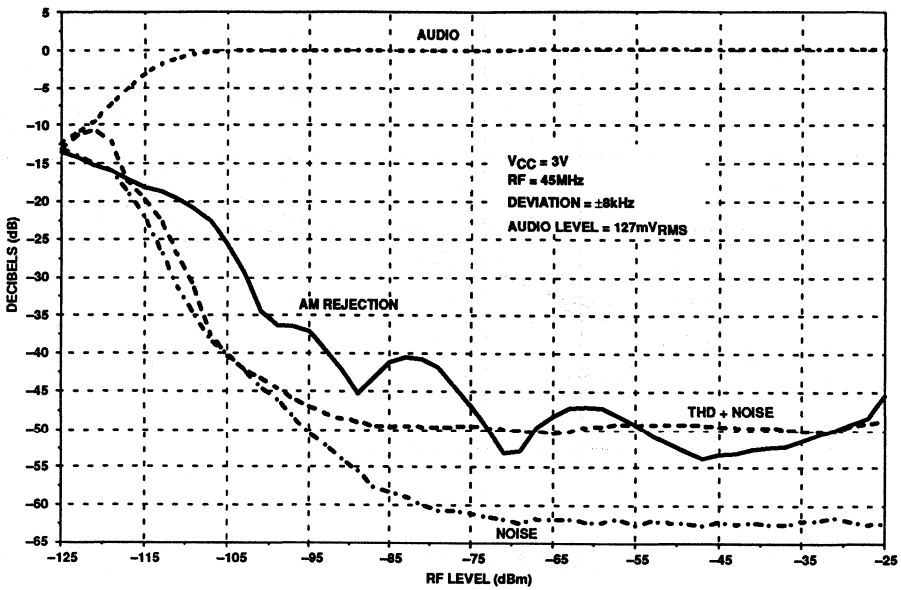


Figure 11. Sensitivity vs RF Level (Temperature 85°C)

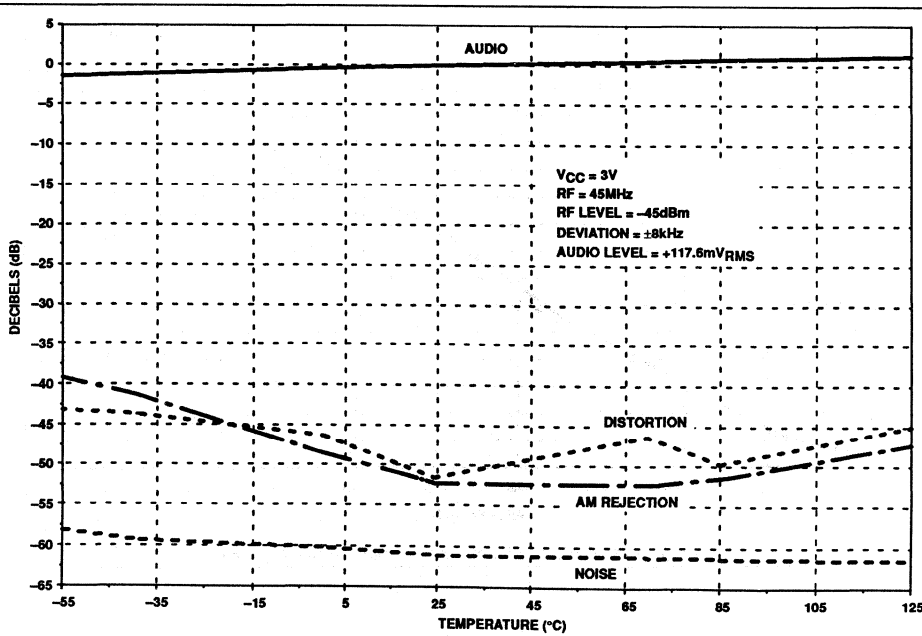


Figure 12. Relative Audio Level, Distortion, AM Rejection and Noise vs Temperature

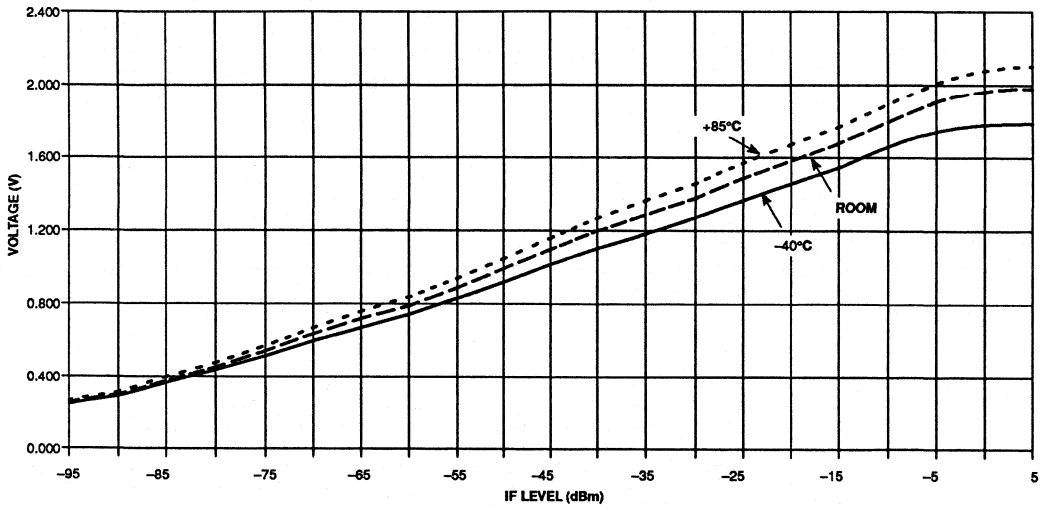


Figure 13. RSSI (455kHz IF @ 3V)

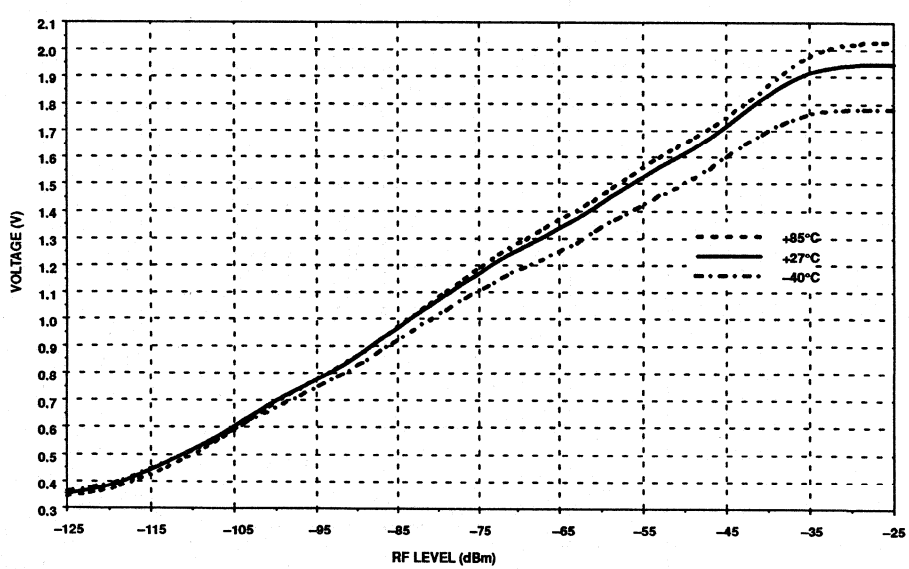


Figure 14. RSSI vs RF Level and Temperature - V_{CC} = 3V

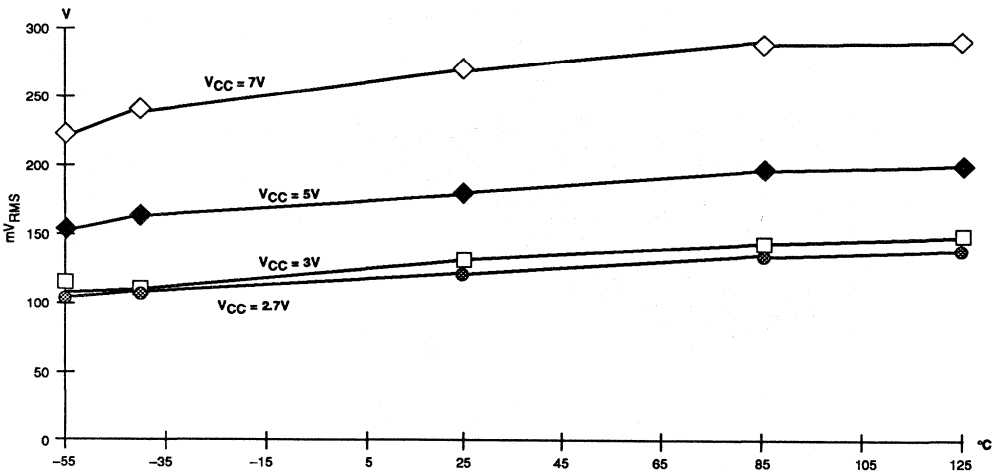
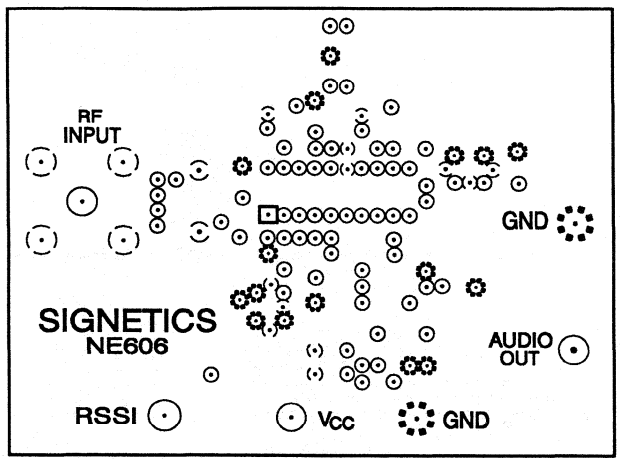


Figure 15. Audio Output vs Temperature



*Applies to Stand-Alone data sheets only.

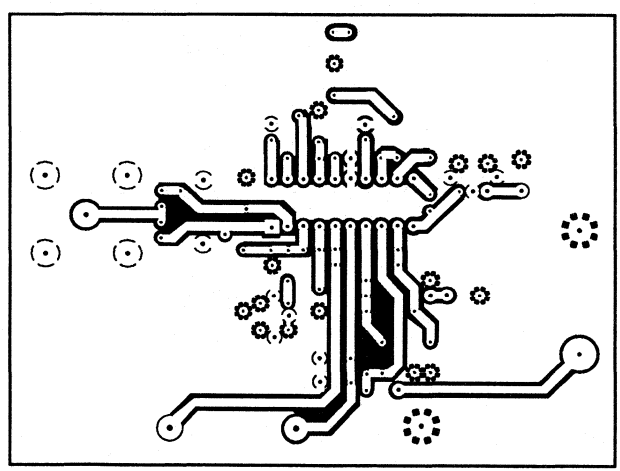
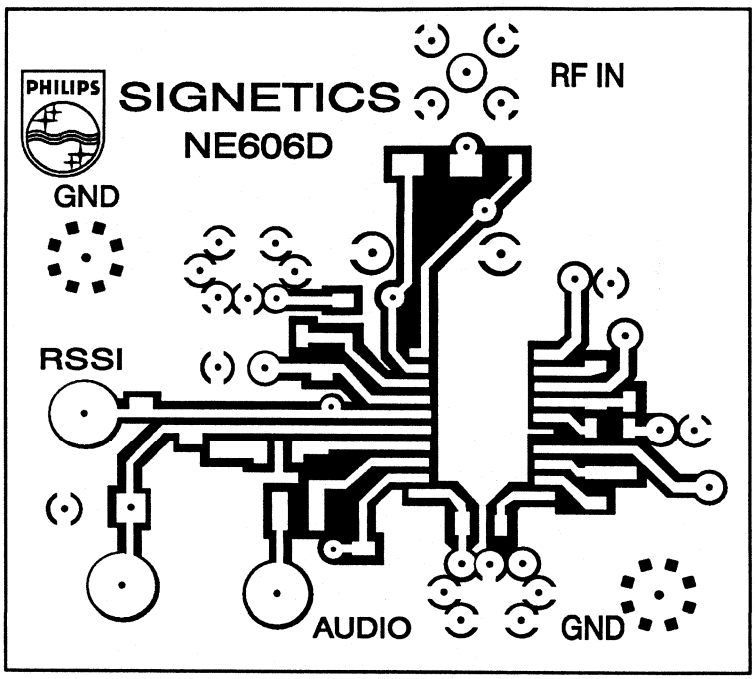


Figure 16. NE/SA606N DIP Product Board Layout (Actual Size* — For Reference Use Only)



*Applies to Stand-Alone data sheets only.

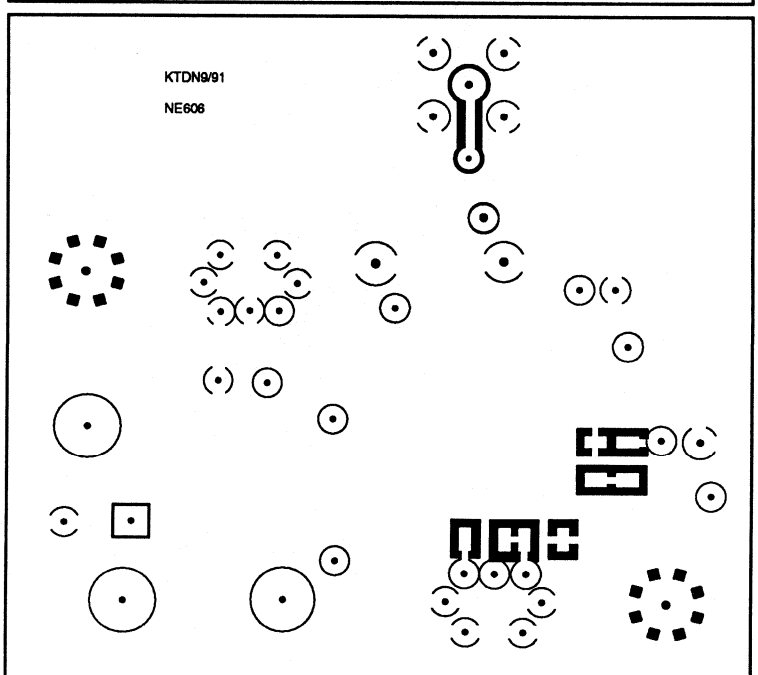
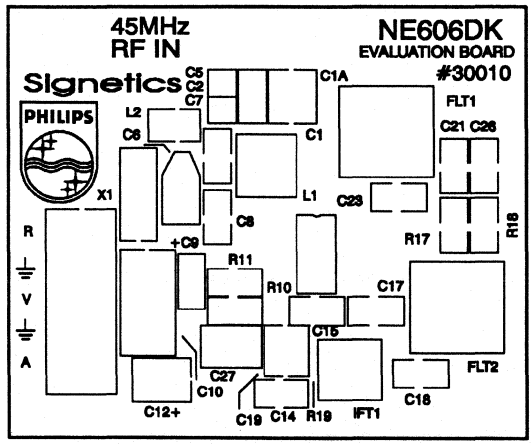
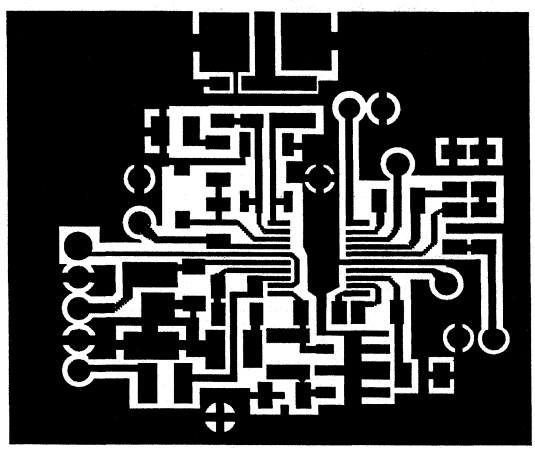


Figure 17. NE/SA606D SOL Product Board Layout (2X Actual Size* — For Reference Use Only)

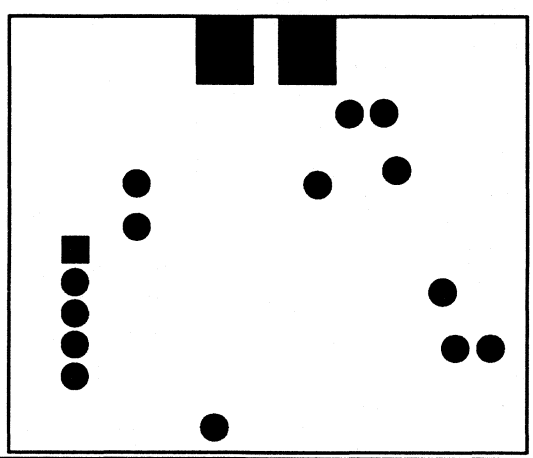
606 Silk Screen



606 TOP



606 BOTTOM



NOTE;
All views are TOP VIEW and not actual size. For reference only.

Double-balanced mixer and oscillator — NE/SA612A

DESCRIPTION

The NE/SA612A is a low-power VHF monolithic double-balanced mixer with on-board oscillator and voltage regulator. It is intended for low cost, low power communication systems with signal frequencies to 500MHz and local oscillator frequencies as high as 200MHz. The mixer is a "Gilbert cell" multiplier configuration which provides gain of 14dB or more at 45MHz.

The oscillator can be configured for a crystal, a tuned tank operation, or as a buffer for an external L.O. Noise figure at 45MHz is typically below 6dB and makes the device well suited for high performance cordless phone/cellular radio. The low power consumption makes the NE/SA612A excellent for battery operated equipment. Networking and other communications products can benefit from very low radiated energy levels within systems. The NE/SA612A is available in an 8-lead dual in-line plastic package and an 8-lead SO (surface mounted miniature package).

FEATURES

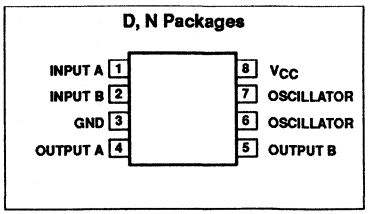
- Low current consumption
- Low cost
- Operation to 500MHz
- Low radiated energy
- Low external parts count; suitable for crystal/ceramic filter
- Excellent sensitivity, gain, and noise figure

APPLICATIONS

- Cordless telephone
- Portable radio
- VHF transceivers
- RF data links
- Sonabuoys
- Communications receivers
- Broadband LANs
- HF and VHF frequency conversion
- Cellular radio mixer/oscillator

PIN CONFIGURATION

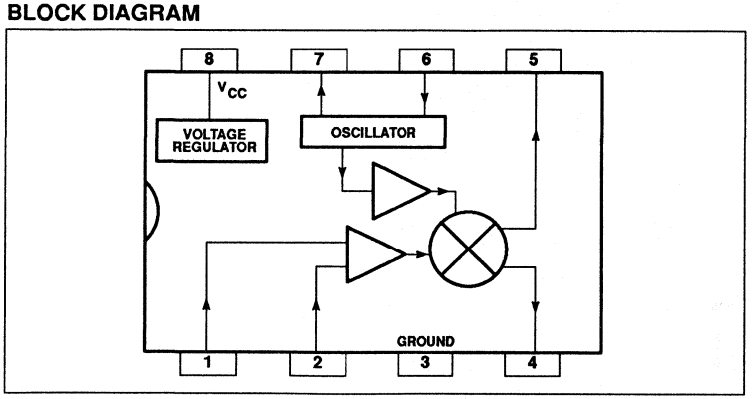
D, N Packages



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	NE612AN
8-Pin Plastic SO (Surface-Mount)	0 to +70°C	NE612AD
8-Pin Plastic DIP	-40 to +85°C	SA612AN
8-Pin Plastic SO (Surface-Mount)	-40 to +85°C	SA612AD

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Maximum operating voltage	9	V
T_{STG}	Storage temperature	-65 to +150	°C
T_A	Operating ambient temperature range NE SA	 0 to +70 -40 to +85	°C

AC/DC ELECTRICAL CHARACTERISTICS

T_A=25°C, V_{CC} = 6V, Figure 1

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Power supply voltage range		4.5		8.0	V
	DC current drain			2.4	3.0	mA
f_{IN}	Input signal frequency			500		MHz
f_{OSC}	Oscillator frequency			200		MHz
	Noise figured at 45MHz			5.0		dB
	Third-order intercept point at 45MHz	RF_{IN}=-45dBm		-13		dBm
	Conversion gain at 45MHz		14	17		dB
R_{IN}	RF input resistance		1.5			kΩ
C_{IN}	RF input capacitance			3		pF
	Mixer output resistance	(Pin 4 or 5)		1.5		kΩ

DESCRIPTION OF OPERATION

The NE/SA612A is a Gilbert cell, an oscillator/buffer, and a temperature compensated bias network as shown in the equivalent circuit. The Gilbert cell is a differential amplifier (Pins 1 and 2) which drives a balanced switching cell. The differential input stage provides gain and determines the noise figure and signal handling performance of the system.

The NE/SA612A is designed for optimum low power performance. When used with the NE614A as a 45MHz cordless phone/cellular radio 2nd IF and demodulator, the NE/SA612A is capable of receiving -119dBm signals with a 12dB S/N ratio. Third-order intercept is typically -15dBm (that's approximately +5dBm output intercept because of the RF gain). The system designer must be cognizant of this large signal limitation. When designing LANs or other closed systems where transmission levels are high, and small-signal or signal-to-noise issues not critical, the input to the NE/SA612A should be appropriately scaled.

TEST CONFIGURATION

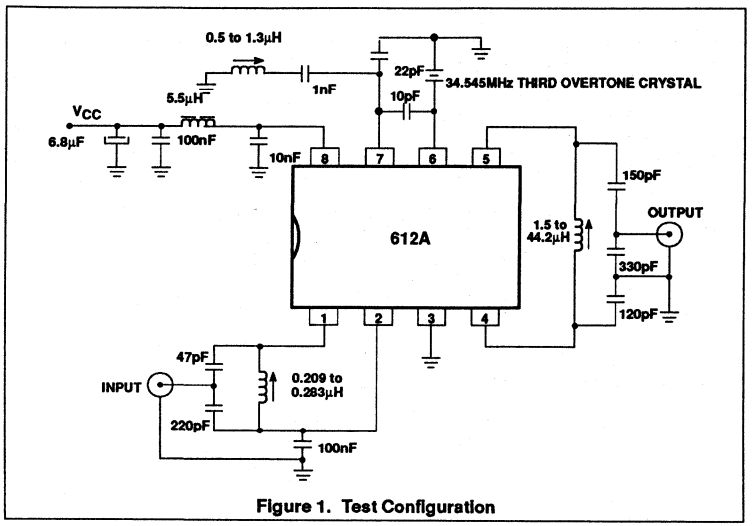


Figure 1. Test Configuration

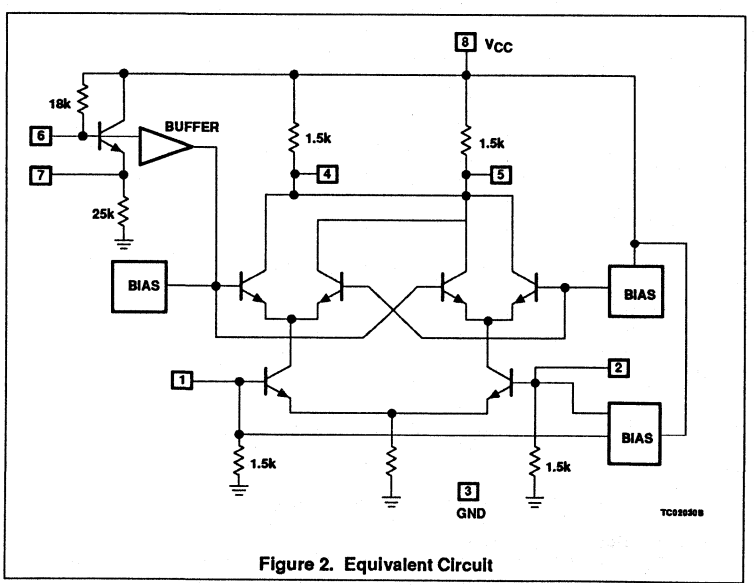


Figure 2. Equivalent Circuit

Besides excellent low power performance well into VHF, the NE/SA612A is designed to be flexible. The input, output, and oscillator ports can support a variety of configurations provided the designer understands certain constraints, which will be explained here.

The RF inputs (Pins 1 and 2) are biased internally. They are symmetrical. The equivalent AC input impedance is approximately 1.5k || 3pF through 50MHz. Pins 1 and 2 can be used interchangeably, but they should not be DC biased externally. Figure 3 shows three typical input configurations.

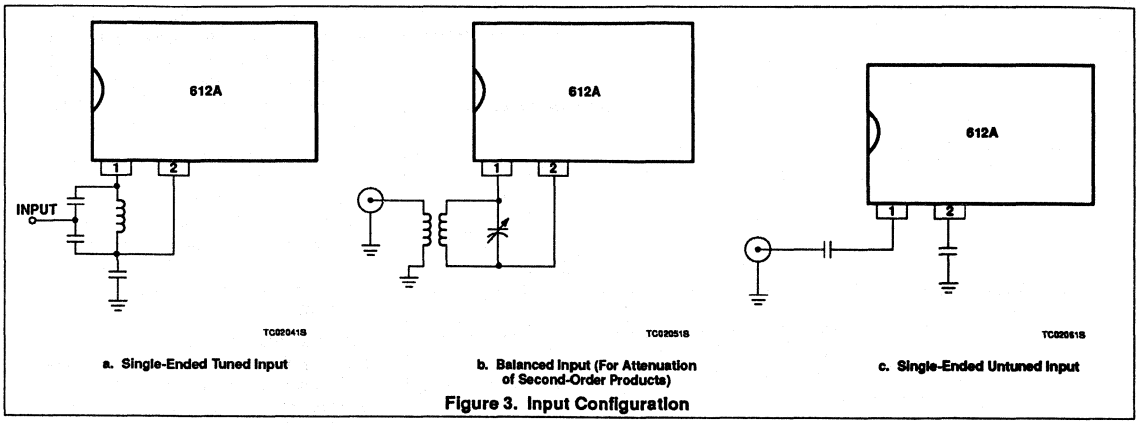
The mixer outputs (Pins 4 and 5) are also internally biased. Each output is connected to the internal positive supply by a 1.5kΩ resistor. This permits direct output termination yet allows for balanced output as well. Figure 4 shows three single-ended output configurations and a balanced output.

The oscillator is capable of sustaining oscillation beyond 200MHz in crystal or tuned tank configurations. The upper limit of operation is determined by tank "Q" and required drive levels. The higher the Q of the tank or the smaller the required drive, the higher the

permissible oscillation frequency. If the required L.O. is beyond oscillation limits, or the system calls for an external L.O., the external signal can be injected at Pin 6 through a DC blocking capacitor. External L.O. should be 200mV$_{P-P}$ minimum to 300mV$_{P-P}$ maximum.

Figure 5 shows several proven oscillator circuits. Figure 5a is appropriate for cordless phones/cellular radio. In this circuit a third overtone parallel-mode crystal with approximately 5pF load capacitance should be specified. Capacitor C3 and inductor L1 act as a fundamental trap. In fundamental mode oscillation the trap is omitted.

Figure 6 shows a Colpitts varacter tuned tank oscillator suitable for synthesizer-controlled applications. It is important to buffer the output of this circuit to assure that switching spikes from the first counter or prescaler do not end up in the oscillator spectrum. The dual-gate MOSFET provides optimum isolation with low current. The FET offers good isolation, simplicity, and low current, while the bipolar circuits provide the simple solution for non-critical applications. The resistive divider in the emitter-follower circuit should be chosen to provide the minimum input signal which will assume correct system operation.

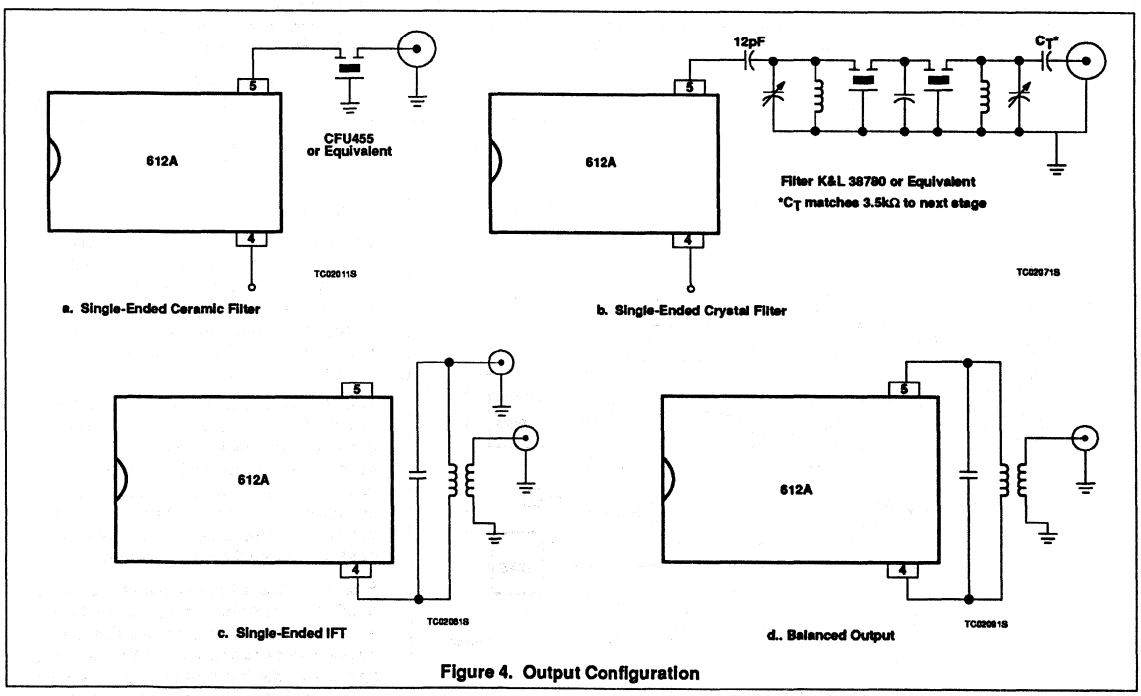


a. Single-Ended Tuned Input

b. Balanced Input (For Attenuation of Second-Order Products)

c. Single-Ended Untuned Input

Figure 3. Input Configuration



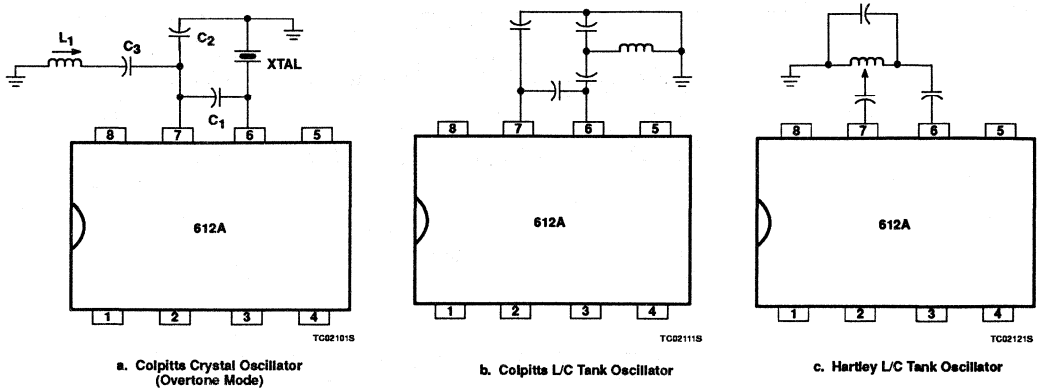
a. Single-Ended Ceramic Filter

b. Single-Ended Crystal Filter

c. Single-Ended IFT

d.. Balanced Output

Figure 4. Output Configuration



a. Colpitts Crystal Oscillator (Overtone Mode)

b. Colpitts L/C Tank Oscillator

c. Hartley L/C Tank Oscillator

Figure 5. Oscillator Circuits

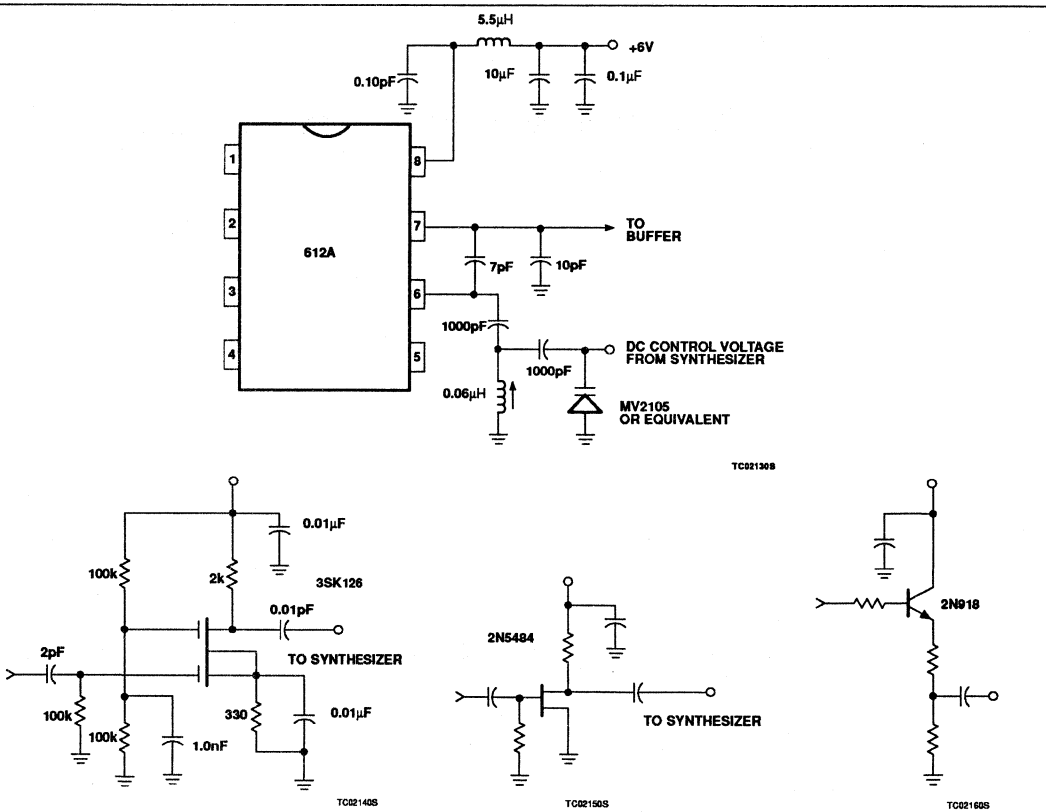


Figure 6. Colpitts Oscillator Suitable for Synthesizer Applications and Typical Buffers

TEST CONFIGURATION

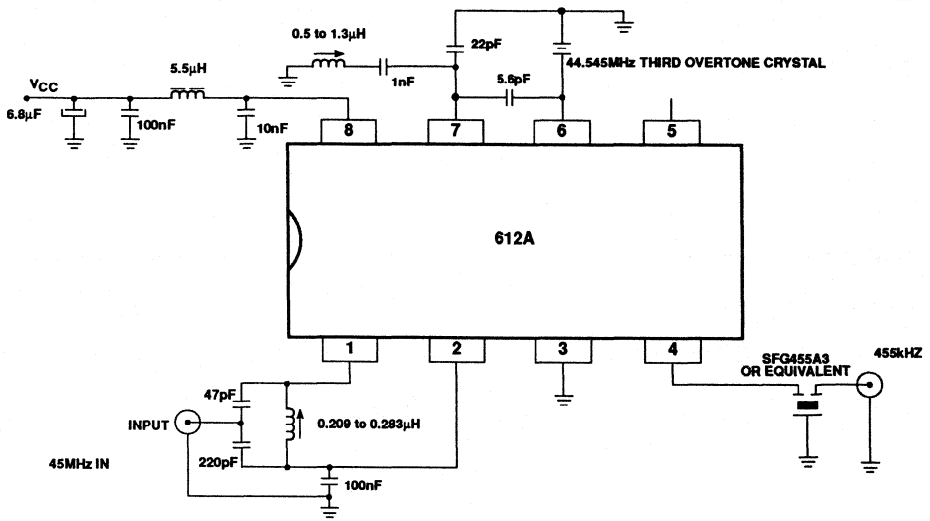


Figure 7. Typical Application for Cordless/Cellular Radio

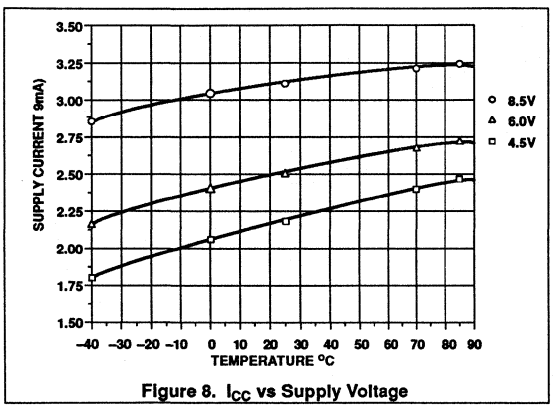


Figure 8. I_{CC} vs Supply Voltage

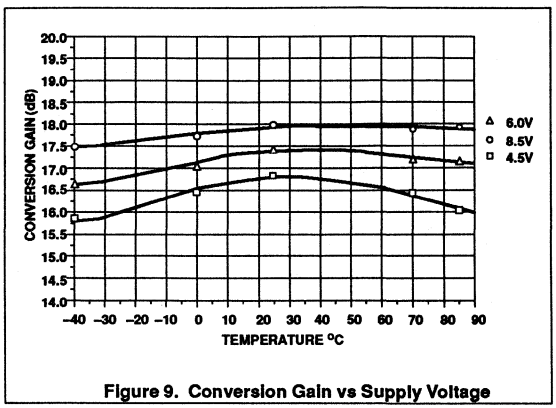


Figure 9. Conversion Gain vs Supply Voltage

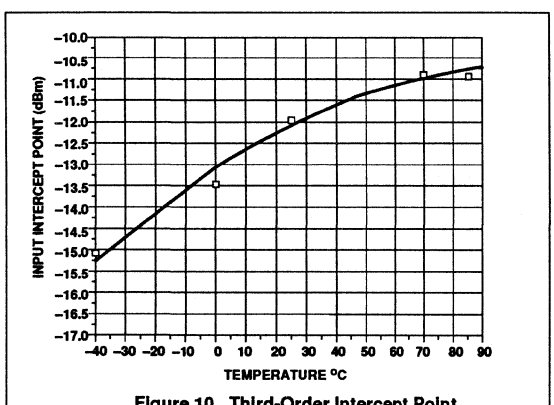


Figure 10. Third-Order Intercept Point

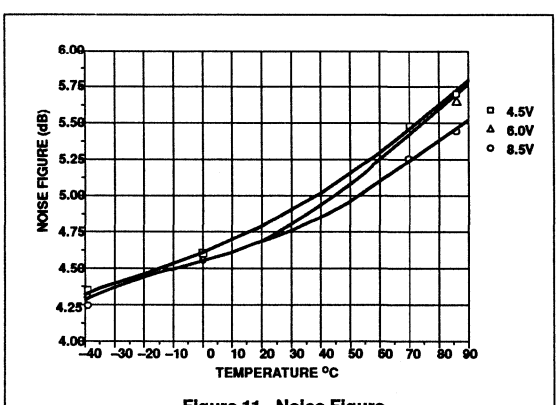


Figure 11. Noise Figure

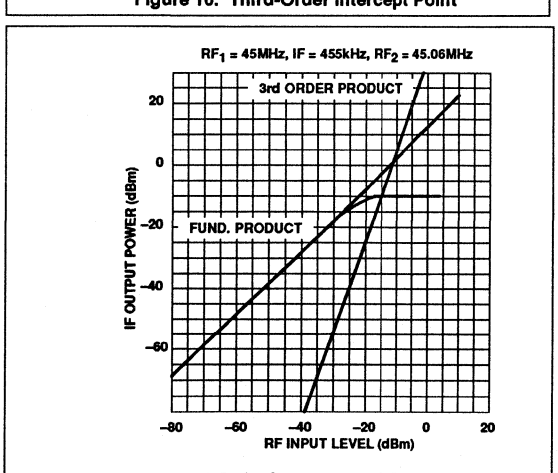


Figure 12. Third-Order Intercept and Compression

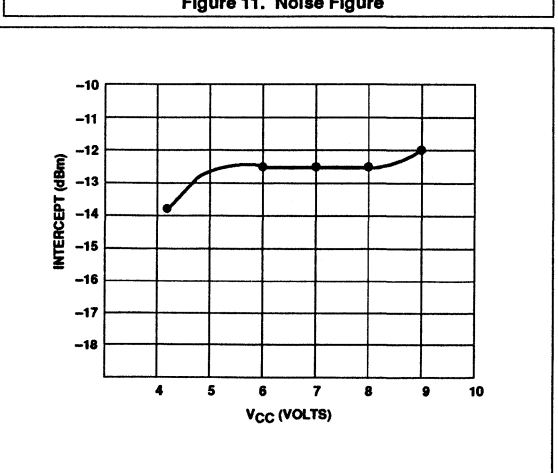


Figure 13. Input Third-Order Intermod Point vs V_{CC}

Low power FM IF system — NE/SA614A

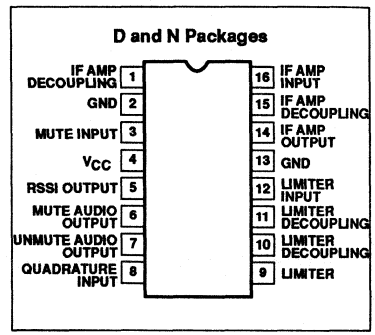
DESCRIPTION

The NE/SA614A is an improved monolithic low-power FM IF system incorporating two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator, and voltage regulator. The NE/SA614A features higher IF bandwidth (25MHz) and temperature compensated RSSI and limiters permitting higher performance application compared with the NE/SA604. The NE/SA614A is available in a 16-lead dual-in-line plastic and 16-lead SO (surface-mounted miniature) package.

FEATURES

- Low power consumption: 3.3mA typical
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- Two audio outputs - muted and unmuted
- Low external component count; suitable for crystal/ceramic filters
- Excellent sensitivity: 1.5μV across input pins (0.22μV into 50Ω matching network) for 12dB SINAD (Signal to Noise and Distortion ratio) at 455kHz
- SA614A meets cellular radio specifications

PIN CONFIGURATION



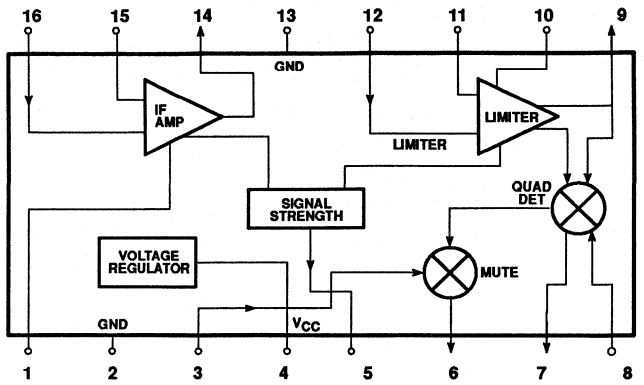
APPLICATIONS

- Cellular radio FM IF
- High performance communications receivers
- Intermediate frequency amplification and detection up to 25MHz
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic DIP	0 to +70°C	NE614AN	0406C
16-Pin Plastic SO (Surface-mount)	0 to +70°C	NE614AD	0005D
16-Pin Plastic DIP	-40 to +85°C	SA614AN	0406C
16-Pin Plastic SO (Surface-mount)	-40 to +85°C	SA614AD	0005D

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	9	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range NE614A SA614A	0 to +70 -40 to +85	°C °C
θ_{JA}	Thermal impedance D package N package	90 75	°C/W °C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE614A			SA614A			
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Power supply voltage range		4.5		8.0	4.5		8.0	V
I_{CC}	DC current drain		2.5	3.3	4.0	2.5	3.3	4.0	mA
	Mute switch input threshold (ON) (OFF)		1.7		 1.0	1.7		 1.0	V V

AC ELECTRICAL CHARACTERISTICS

Typical reading at T_A = 25°C; V_{CC} = ±6V, unless otherwise stated. IF frequency = 455kHz; IF level = -47dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

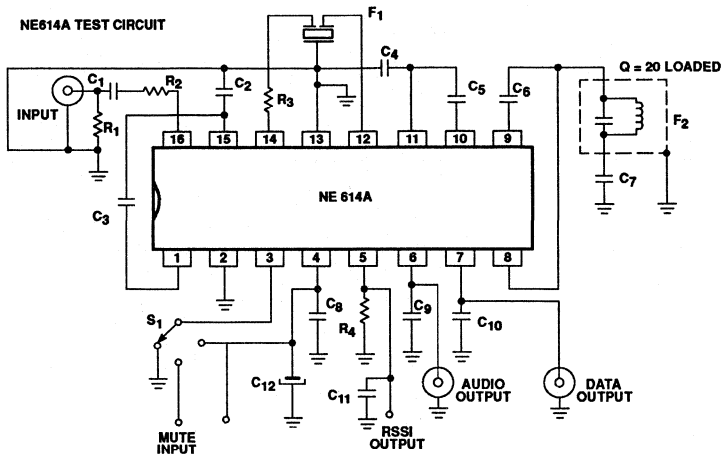
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA614A			
			MIN	TYP	MAX	
	Input limiting -3dB	Test at Pin 16		-92		dBm/50Ω
	AM rejection	80% AM 1kHz	25	33		dB
	Recovered audio level	15nF de-emphasis	60	175	260	mV_{RMS}
	Recovered audio level	150pF de-emphasis		530		mV_{RMS}
THD	Total harmonic distortion		-30	-42		dB
S/N	Signal-to-noise ratio	No modulation for noise		68		dB
	RSSI output[1]	RF level = -118dBm	0	160	800	mV
		RF level = -68dBm	1.7	2.50	3.3	V
		RF level = -18dBm	3.6	4.80	5.8	V
	RSSI range	R_4 = 100k (Pin 5)		80		dB
	RSSI accuracy	R_4 = 100k (Pin 5)		±2.0		dB
	IF input impedance		1.4	1.6		kΩ
	IF output impedance		0.85	1.0		kΩ
	Limiter input impedance		1.4	1.6		kΩ
	Unmuted audio output resistance			58		kΩ
	Muted audio output resistance			58		kΩ

NOTE:

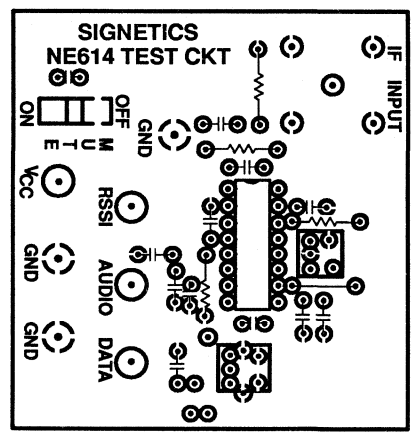
1. NE614A data sheets refer to power at 50Ω input termination; about 21dB less power actually enters the internal 1.5k input.

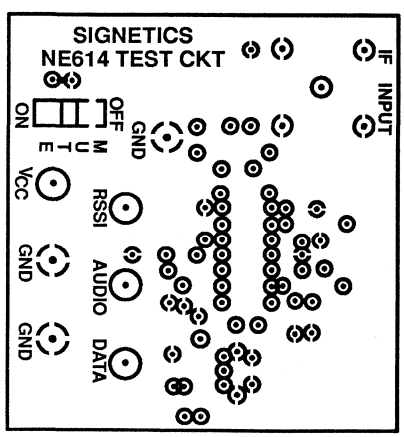
NE614A (50)	NE614A (1.5k)/NE615 (1.5k
-97dBm	-118dBm
-47dBm	-68dBm
+3dBm	-18dBm

The NE615 and NE614A are both derived from the same basic die. The NE615 performance plots are directly applicable to the NE614A.



C1	100nF + 80 – 20% 63V K10000–25V Ceramic
C2	100nF +10% 50V
C3	100nF ±10% 50V
C4	100nF +10% 50V
C5	100nF ±10% 50V
C6	10pF ±2% 100V NPO Ceramic
C7	100nF ±10% 50V
C8	100nF ±10% 50V
C9	15nF ±10% 50V
C10	150pF ±2% 100V N1500 Ceramic
C11	1nF ±10% 100V K2000-Y5P Ceramic
C12	6.8µF ±20% 25V Tantalum
F1	455kHz Ceramic Filter Murata SFG455A3
F2	455kHz (Ce = 180pF) TOKO RMC 2A6597H
R1	51Ω ±1% 1/4W Metal Film
R2	1500Ω ±1% 1/4W Metal Film
R3	1500Ω ±5% 1/8W Carbon Composition
R4	100kΩ ±1% 1/4W Metal Film





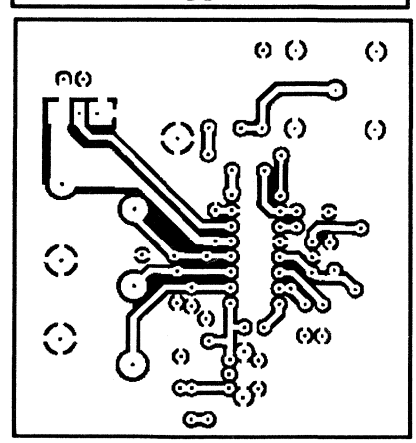


Figure 1. NE/SA614A Test Circuit

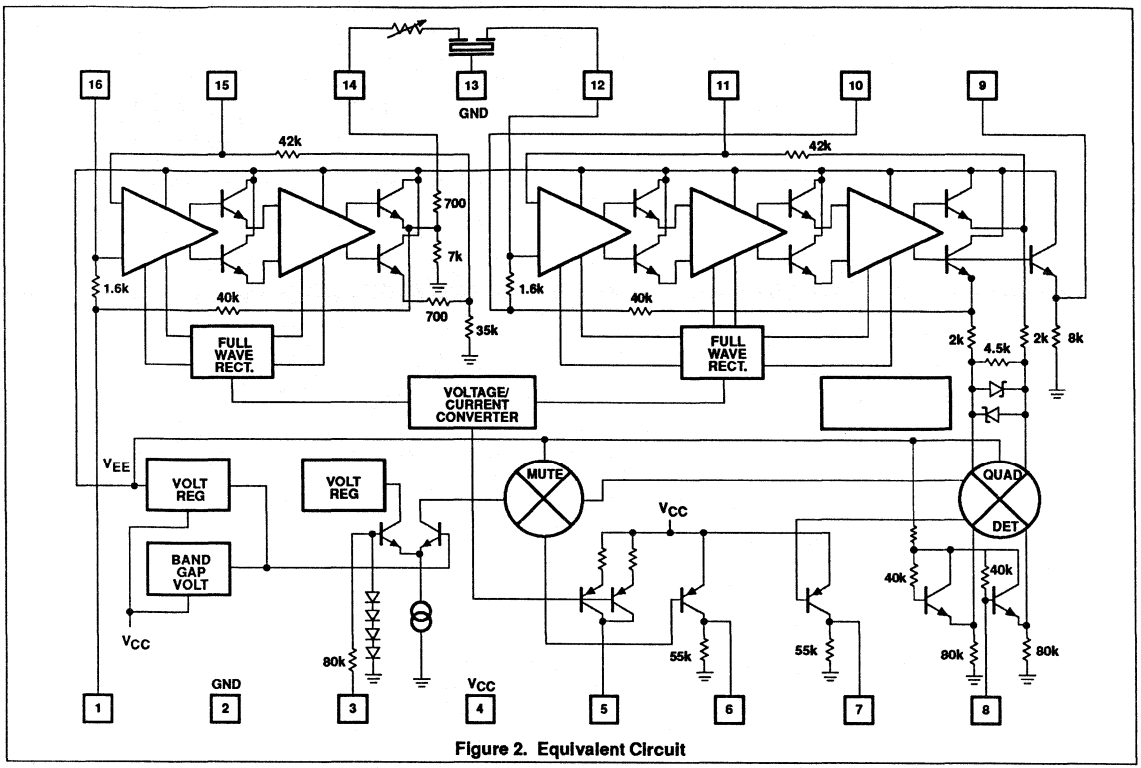


Figure 2. Equivalent Circuit

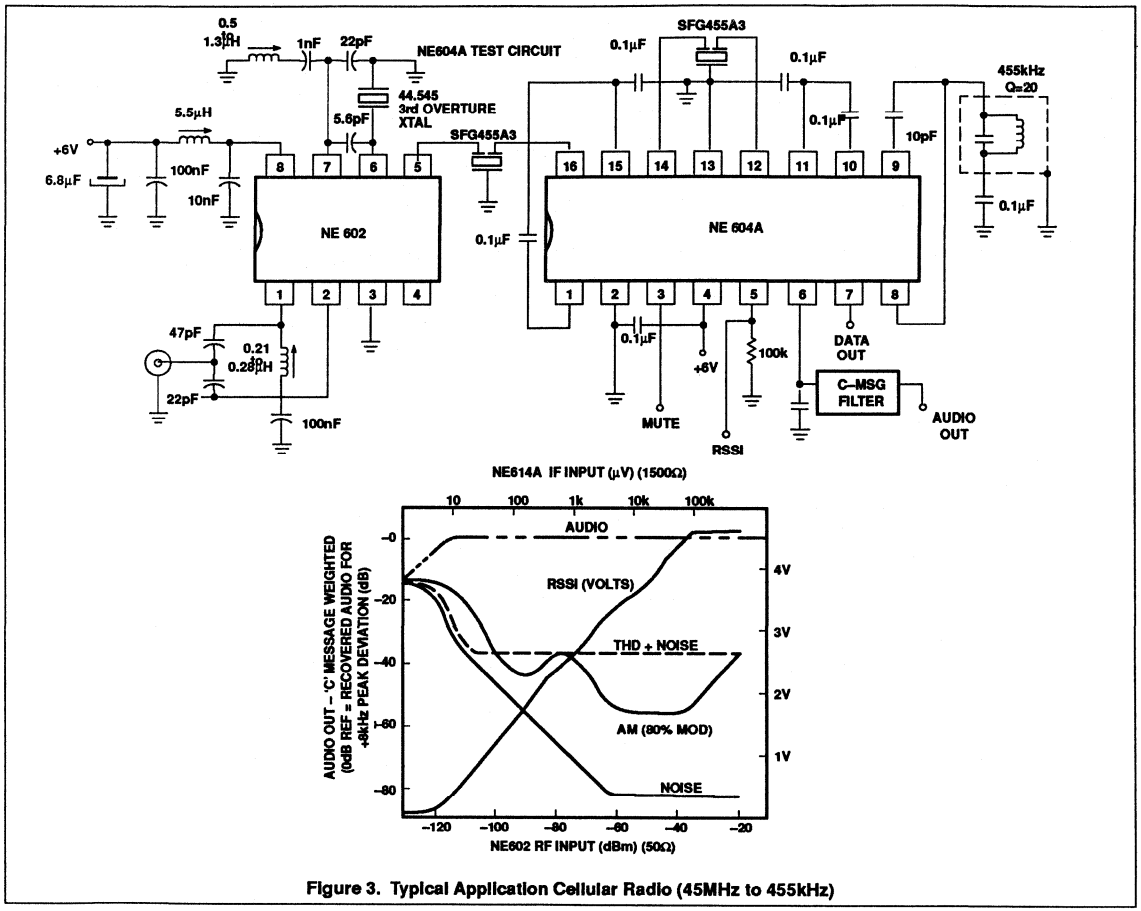


Figure 3. Typical Application Cellular Radio (45MHz to 455kHz)

CIRCUIT DESCRIPTION

The NE/SA614A is a very high gain, high frequency device. Correct operation is not possible if good RF layout and gain stage practices are not used. The NE/SA614A cannot be evaluated independent of circuit, components, and board layout. A physical layout which correlates to the electrical limits is shown in Figure 1. This configuration can be used as the basis for production layout.

The NE/SA614A is an IF signal processing system suitable for IF frequencies as high as 21.4MHz. The device consists of two limiting amplifiers, quadrature detector, direct audio output, muted audio output, and signal strength indicator (with log output characteristic). The sub-systems are shown in Figure 2. A typical application with 45MHz input and 455kHz IF is shown in Figure 3.

IF Amplifiers

The IF amplifier section consists of two log-limiting stages. The first consists of two differential amplifiers with 39dB of gain and a small signal bandwidth of 41MHz (when driven from a 50Ω source). The output of the first limiter is a low impedance emitter follower with 1kΩ of equivalent series resistance. The second limiting stage consists of three differential amplifiers with a gain of 62dB and a small signal AC bandwidth of 28MHz. The outputs of the final differential stage are buffered to the internal quadrature detector. One of the outputs is available at Pin 9 to drive an external quadrature capacitor and L/C quadrature tank.

Both of the limiting amplifier stages are DC biased using feedback. The buffered output of the final differential amplifier is fed back to the input through 42kΩ resistors. As shown in Figure 2, the input impedance is established for each stage by tapping one of the feedback resistors 1.6kΩ from the input. This requires one additional decoupling capacitor from the tap point to ground.

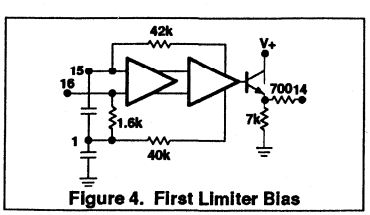


Figure 4. First Limiter Bias

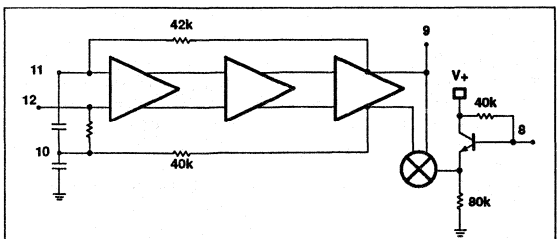


Figure 5. Second Limiter and Quadrature Detector

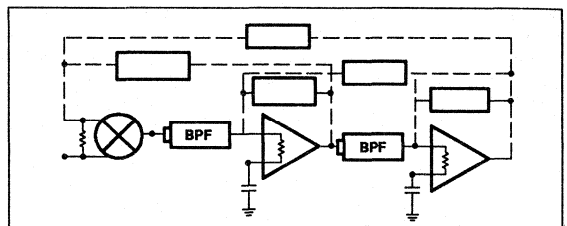
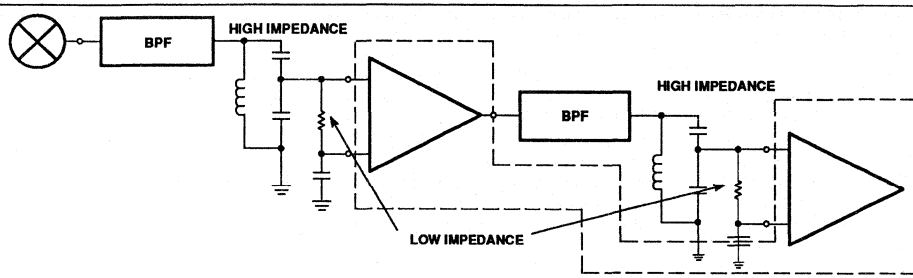
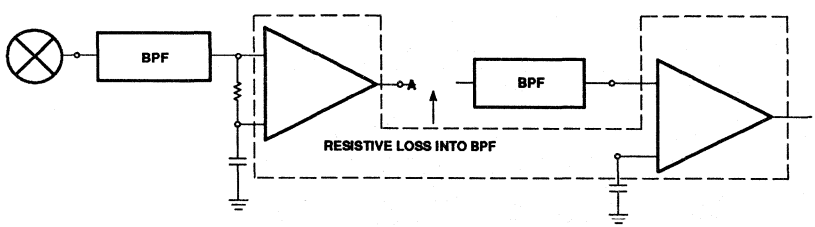


Figure 6. Feedback Paths



7a. Terminating High Impedance Filters with Transformation to Low Impedance



7b. Low Impedance Termination and Gain Reduction

Figure 7. Practical Termination

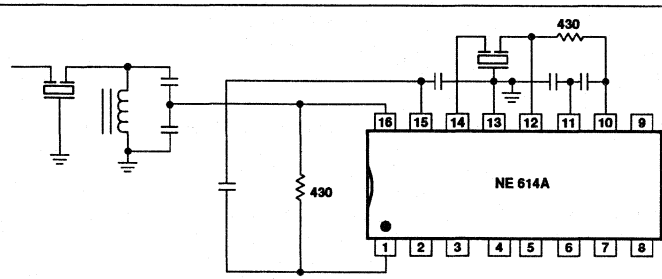


Figure 8. Crystal Input Filter with Ceramic Interstage Filter

Because of the very high gain, bandwidth and input impedance of the limiters, there is a very real potential for instability at IF frequencies above 455kHz. The basic phenomenon is shown in Figure 6. Distributed feedback (capacitance, inductance and radiated fields) forms a divider from the output of the limiters back to the inputs (including RF input). If this feedback divider does not cause attenuation greater than the gain of the forward path, then oscillation or low level regeneration is likely. If regeneration occurs, two symptoms may be present: (1)The RSSI output will be high with no signal input (should nominally be 250mV or lower), and (2) the demodulated output will demonstrate a threshold. Above a certain input level, the limited signal will begin to dominate the regeneration, and the demodulator will begin to operate in a "normal" manner.

There are three primary ways to deal with regeneration: (1) Minimize the feedback by gain stage isolation, (2) lower the stage input impedances, thus increasing the feedback attenuation factor, and (3) reduce the gain.

Gain reduction can effectively be accomplished by adding attenuation between stages. This can also lower the input impedance if well planned. Examples of impedance/gain adjustment are shown in Figure 7. Reduced gain will result in reduced limiting sensitivity.

A feature of the NE614A IF amplifiers, which is not specified, is low phase shift. The NE614A is fabricated with a 10GHz process with very small collector capacitance. It is advantageous in some applications that the phase shift changes only a few degrees over a wide range of signal input amplitudes.

Stability Considerations

The high gain and bandwidth of the NE614A in combination with its very low currents permit circuit implementation with superior performance. However, stability must be maintained and, to do that, every possible feedback mechanism must be addressed. These mechanisms are: 1) Supply lines and ground, 2) stray layout inductances and capacitances, 3) radiated fields, and 4) phase shift. As the system IF increases, so must the attention to fields and strays. However, ground and supply loops cannot be overlooked, especially at lower frequencies. Even at 455kHz, using the test layout in Figure 1, instability will occur if the supply line is not decoupled with two high quality RF capacitors, a 0.1μF monolithic right at the V_{CC} pin, and a 6.8μF tantalum on the supply line. An electrolytic is not an adequate substitute. At 10.7MHz, a 1μF tantalum has proven acceptable with this layout. Every layout must be evaluated on its own merit, but don't underestimate the importance of good supply bypass.

At 455kHz, if the layout of Figure 1 or one substantially similar is used, it is possible to directly connect ceramic filters to the input and between limiter stages with no special consideration. At frequencies above 2MHz, some input impedance reduction is usually necessary. Figure 7 demonstrates a practical means.

As illustrated in Figure 8, 430Ω external resistors are applied in parallel to the internal 1.6kΩ load resistors, thus presenting approximately 330Ω to the filters. The input filter is a crystal type for narrowband selectivity. The filter is terminated with a tank which transforms to 330Ω. The interstage filter is a ceramic type which doesn't contribute to system selectivity, but does suppress wideband noise and stray signal pickup. In wideband 10.7MHz IFs the input filter can also be ceramic, directly connected to Pin 16.

In some products it may be impractical to utilize shielding, but this mechanism may be appropriate to 10.7MHz and 21.4MHz IF. One of the benefits of low current is lower radiated field strength, but lower does not mean non-existent. A spectrum analyzer with an active probe will clearly show IF energy with the probe held in the proximity of the second limiter output or quadrature coil. No specific recommendations are provided, but mechanical shielding should be considered if layout, bypass, and input impedance reduction do not solve a stubborn instability.

The final stability consideration is phase shift. The phase shift of the limiters is very low, but there is phase shift contribution from the quadrature tank and the filters. Most filters demonstrate a large phase shift across their passband (especially at the edges). If the quadrature detector is tuned to the edge of the filter passband, the combined filter and quadrature phase shift can aggravate stability. This is not usually a problem, but should be kept in mind.

Quadrature Detector

Figure 5 shows an equivalent circuit of the NE614A quadrature detector. It is a multiplier cell similar to a mixer stage. Instead of mixing two different frequencies, it mixes two signals of common frequency but different phase. Internal to the device, a constant amplitude (limited) signal is differentially applied to the lower port of the multiplier. The same signal is applied single-ended to an external capacitor at Pin 9. There is a 90° phase shift across the plates of this capacitor, with the phase shifted signal applied to the upper port of the multiplier at Pin 8. A quadrature tank (parallel L/C network) permits frequency selective phase shifting at the IF frequency. This quadrature tank must be returned to ground through a DC blocking capacitor.

The loaded Q of the quadrature tank impacts three fundamental aspects of the detector: Distortion, maximum modulated peak deviation, and audio output amplitude. Typical quadrature curves are illustrated in Figure 10. The phase angle translates to a shift in the multiplier output voltage.

Thus a small deviation gives a large output with a high Q tank. However, as the deviation from resonance increases, the non-linearity of the curve increases (distortion), and, with too much deviation, the signal will be outside the quadrature region (limiting the peak deviation which can be demodulated). If the same peak deviation is applied to a lower Q tank, the deviation will remain in a region of the curve which is more linear (less distortion), but creates a smaller phase angle (smaller output amplitude). Thus the Q of the quadrature tank must be tailored to the design. Basic equations and an example for determining Q are shown below. This explanation includes first-order effects only.

Frequency Discriminator Design Equations for NE614A

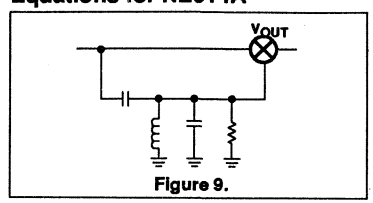


Figure 9.

$$V_O = \frac{C_S}{C_P + C_S} \bullet \frac{1}{1 + \frac{\omega_1}{Q_1 S} + \left(\frac{\omega_1}{S}\right)^2} \bullet V_{IN} \quad (1a)$$

$$\text{where } \omega_1 = \frac{1}{\sqrt{L(C_P + C_S)}} \quad (1b)$$

$$Q_1 = R\,(C_P + C_S)\,\omega_1 \quad (1c)$$

From the above equation, the phase shift between nodes 1 and 2, or the phase across C_S will be:

$$\phi = \angle V_O - \angle V_{IN} = t_g^{-1}\left[\frac{\frac{\omega_1}{Q_1\omega}}{1 - \left(\frac{\omega_1}{\omega}\right)^2}\right] \quad (2)$$

Figure 10 is the plot of ϕ vs. $\left(\frac{\omega}{\omega_1}\right)$

It is notable that at $\omega = \omega_1$, the phase shift is $\frac{\pi}{2}$ and the response is close to a straight line with a slope of $\frac{\Delta\phi}{\Delta\omega} = \frac{2Q_1}{\omega_1}$

The signal V_O would have a phase shift of $\left[\frac{\pi}{2} - \frac{2Q_1}{\omega_1}\,\omega\right]$ with respect to the V_{IN}.

$$\text{If } V_{IN} = A \sin \omega t \Rightarrow V_O = A \quad (3)$$

$$\sin\left[\omega t + \frac{\pi}{2} - \frac{2Q_1}{\omega_1}\,\omega\right]$$

Multiplying the two signals in the mixer, and low pass filtering yields:

$$V_{IN} \bullet V_O = A^2 \sin \omega t \quad (4)$$

$$\sin\left[\omega t + \frac{\pi}{2} - \frac{2Q_1}{\omega_1}\,\omega\right]$$

after low pass filtering

$$\Rightarrow V_{OUT} = \frac{1}{2} A^2 \, Cos\left[\frac{\pi}{2} - \frac{2Q_1}{\omega_1}\omega\right] \quad (5)$$

$$= \frac{1}{2} A^2 \, Sin\left(\frac{2Q_1}{\omega_1}\right)\omega$$

$$V_{OUT} \propto 2Q_1 \frac{\omega_1}{\omega} = \left[2Q_1\left(\frac{\omega_1 + \Delta\omega}{\omega_1}\right)\right] \quad (6)$$

$$\text{For } \frac{2Q_1\omega}{\omega_1} << \frac{\pi}{2}$$

Which is discriminated FM output. (Note that $\Delta\omega$ is the deviation frequency from the carrier ω_1.

Ref. Krauss, Raab, Bastian; Solid State Radio Eng.; Wiley, 1980, p. 311. Example: At 455kHz IF, with ±5kHz FM deviation. The maximum normalized frequency will be

$$\frac{455 \pm 5kHz}{455} = 1.010 \text{ or } 0.990$$

Go to the f vs. normalized frequency curves (Figure 10) and draw a vertical straight line at $\frac{\omega}{\omega_1} = 1.01$.

The curves with Q = 100, Q = 40 are not linear, but Q = 20 and less shows better linearity for this application. Too small Q decreases the amplitude of the discriminated FM signal. (Eq. 6) ⇒ Choose a Q = 20

The internal R of the 614A is 40k. From Eq. 1c, and then 1b, it results that

$C_P + C_S = 174pF$ and $L = 0.7mH$.

A more exact analysis including the source resistance of the previous stage shows that there is a series and a parallel resonance in the phase detector tank. To make the parallel and series resonances close, and to get maximum attenuation of higher harmonics at 455kHz IF, we have found that a C_S = 10pF and C_P = 164pF (commercial values of 150pF or 180pF may be practical), will give the best results. A variable inductor which can be adjusted around 0.7mH should be chosen and optimized for minimum distortion. (For 10.7MHz, a value of C_S = 1pF is recommended.)

Audio Outputs

Two audio outputs are provided. Both are PNP current-to-voltage converters with 55kΩ nominal internal loads. The unmuted output is always active to permit the use of signaling tones in systems such as cellular radio. The other output can be muted with 70dB typical attenuation. The two outputs have an internal 180° phase difference.

The nominal frequency response of the audio outputs is 300kHz. this response can be increased with the addition of external resistors from the output pins to ground in parallel with the internal 55k resistors, thus lowering the output time constant. Singe the output structure is a current-to-voltage converter (current is driven into the resistance, creating a voltage drop), adding external parallel resistance also has the effect of lowering the output audio amplitude and DC level.

This technique of audio bandwidth expansion can be effective in many applications such as SCA receivers and data transceivers.

Because the two outputs have a 180° phase relationship, FSK demodulation can be accomplished by applying the two output differentially across the inputs of an op amp or comparator. Once the threshold of the reference frequency (or "no-signal" condition) has been established, the two outputs will shift in opposite directions (higher or lower output voltage) as the input frequency shifts. The output of the comparator will be logic output. The choice of op amp or comparator will depend on the data rate. With high IF frequency (10MHz and above), and wide IF bandwidth (L/C filters) data rates in excess of 4Mbaud are possible.

RSSI

The "received signal strength indicator", or RSSI, of the NE614A demonstrates monotonic logarithmic output over a range of 90dB. The signal strength output is derived from the summed stage currents in the limiting amplifiers. It is essentially independent of the IF frequency. Thus, unfiltered signals at the limiter inputs, spurious products, or regenerated signals will manifest themselves as RSSI outputs. An RSSI output of greater than 250mV with no signal (or a very small signal) applied, is an indication of possible regeneration or oscillation.

In order to achieve optimum RSSI linearity, there must be a 12dB insertion loss between the first and second limiting amplifiers. With a typical 455kHz ceramic filter, there is a nominal 4dB insertion loss in the filter. An additional 6dB is lost in the interface between the filter and the input of the second limiter. A small amount of additional loss must be introduced with a typical ceramic filter. In the test circuit used for cellular radio applications (Figure 3) the optimum linearity was achieved with a 5.1kΩ resistor from the output of the first limiter (Pin 14) to the input of the interstage filter. With this resistor from Pin 14 to the filter, sensitivity of 0.25μV for 12dB SINAD was achieved. With the 3.6kΩ resistor, sensitivity was optimized at 0.22μV for 12dB SINAD with minor change in the RSSI linearity.

Any application which requires optimized RSSI linearity, such as spectrum analyzers, cellular radio, and certain types of telemetry, will require careful attention to limiter interstage component selection. This will be especially true with high IF frequencies which require insertion loss or impedance reduction for stability.

At low frequencies the RSSI makes an excellent logarithmic AC voltmeter.

For data applications the RSSI is effective as an amplitude shift keyed (ASK) data slicer. If a comparator is applied to the RSSI and the threshold set slightly above the no signal level, when an in-band signal is received the comparator will be sliced. Unlike FSK demodulation, the maximum data rate is somewhat limited. An internal capacitor limits the RSSI frequency response to about 100kHz. At high data rates the rise and fall times will not be symmetrical.

The RSSI output is a current-to-voltage converter similar to the audio outputs. However, an external resistor is required. With a 91kΩ resistor, the output characteristic is 0.5V for a 10dB change in the input amplitude.

Additional Circuitry

Internal to the NE614A are voltage and current regulators which have been temperature compensated to maintain the performance of the device over a wide temperature range. These regulators are not accessible to the user.

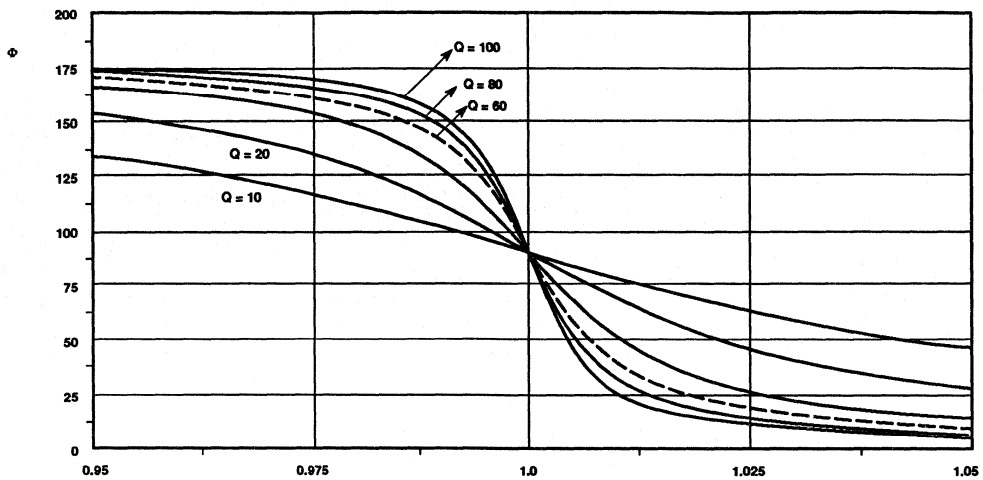


Figure 10. Phase vs Normalized IF Frequency $\frac{\omega}{\omega_I} = 1 + \frac{\Delta\omega}{\omega_I}$

High performance low power mixer FM IF system — NE/SA615

DESCRIPTION

The NE/SA615 is a high performance monolithic low-power FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator (RSSI), and voltage regulator. The NE/SA615 combines the functions of Signetics' NE602 and NE604A, but features a higher mixer input intercept point, higher IF bandwidth (25MHz) and temperature compensated RSSI and limiters permitting higher performance application. The NE/SA615 is available in 20-lead dual-in-line plastic, 20-lead SOL (surface-mounted miniature package) and 20-lead SSOP (shrink small outline package).

The NE/SA605 and NE/SA615 are functionally the same device types. The difference between the two devices lies in the guaranteed specifications. The NE/SA615 has a higher I_{CC}, lower input third order intercept point, lower conversion mixer gain, lower limiter gain, lower AM rejection, lower SINAD, higher THD, and higher RSSI error than the NE/SA615. Both the NE/SA605 and NE/SA615 devices will meet the EIA specifications for AMPS and TACS cellular radio applications.

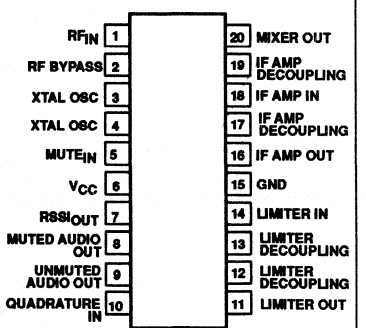
For additional technical information please refer to application notes AN1994, 1995 and 1996, which include example application diagrams, a complete overview of the product, and artwork for reference.

FEATURES

- Low power consumption: 5.7mA typical at 6V
- Mixer input to >500MHz
- Mixer conversion power gain of 13dB at 45MHz
- Mixer noise figure of 4.6dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator to 1GHz local oscillator can be injected)
- 102dB of IF Amp/Limiter gain
- 25MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- Two audio outputs – muted and unmuted
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.22μV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone with RF at 45MHz and IF at 455kHz
- SA615 meets cellular radio specifications
- ESD hardened

PIN CONFIGURATION

N, D and DK Packages



NOTE:
See back page for package dimensions

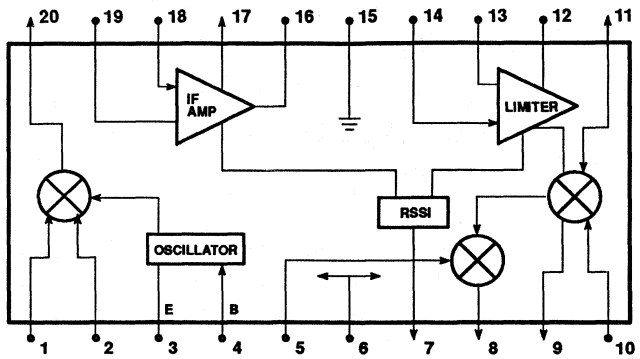
APPLICATIONS

- Cellular radio FM IF
- High performance communications receivers
- Single conversion VHF/UHF receivers
- SCA receivers
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Wideband low current amplification

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic DIP	0 to +70°C	NE615N	0408B
20-Pin Plastic DIP	–40 to +85°C	SA615N	0408B
20-Pin Plastic SOL	0 to +70°C	NE615D	0175D
20-Pin Plastic SOL	–40 to +85°C	SA615D	0175D
20-Pin Plastic SSOP	0 to +70°C	NE615DK	1563
20-Pin Plastic SSOP	–40 to +85°C	SA615DK	1563

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		RATING	UNITS
V_{CC}	Single supply voltage		9	V
T_{STG}	Storage temperature range		–65 to +150	°C
T_A	Operating ambient temperature range	NE615	0 to +70	°C
		SA615	–40 to +85	°C
θ_{JA}	Thermal impedance	D package N package SSOP package	90 75 117	°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS			UNITS
				NE/SA615			
				MIN	TYP	MAX	
V_{CC}	Power supply voltage range			4.5		8.0	V
I_{CC}	DC current drain				5.7	7.4	mA
	Mute switch input threshold	(ON)		1.7			V
		(OFF)				1.0	V

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +6V, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step–up; IF frequency = 455kHz; R17 = 5.1k; RF level = –45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA615			
			MIN	TYP	MAX	
Mixer/Osc section (ext LO = 300mV)						
f_{IN}	Input signal frequency			500		MHz
f_{OSC}	Crystal oscillator frequency			150		MHz
	Noise figure at 45MHz			5.0		dB
	Third-order input intercept point	f1 = 45.00; f2 = 45.06MHz		-12		dBm
	Conversion power gain	Matched 14.5dBV step-up	8.0	13		dB
		50Ω source		-1.7		dB
	RF input resistance	Single-ended input	3.0	4.7		kΩ
	RF input capacitance			3.5	4.0	pF
	Mixer output resistance	(Pin 20)	1.25	1.50		kΩ
IF section						
	IF amp gain	50Ω source		39.7		dB
	Limiter gain	50Ω source		62.5		dB
	Input limiting -3dB, R_{17} = 5.1k	Test at Pin 18		-109		dBm
	AM rejection	80% AM 1kHz	25	33	43	dB
	Audio level, R_{10} = 100k	15nF de-emphasis	60	150	260	mV_{RMS}
	Unmuted audio level, R_{11} = 100k	150pF de-emphasis		530		mV
	SINAD sensitivity	RF level -118dB		12		dB
THD	Total harmonic distortion		-30	-42		dB
S/N	Signal-to-noise ratio	No modulation for noise		68		dB
	IF RSSI output, R_9 = 100kΩ[1]	IF level = -118dBm	0	160	800	mV
		IF level = -68dBm	1.7	2.5	3.3	V
		IF level = -18dBm	3.6	4.8	5.8	V
	RSSI range	R_9 = 100kΩ Pin 16		80		dB
	RSSI accuracy	R_9 = 100kΩ Pin 16		±2		dB
	IF input impedance		1.40	1.6		kΩ
	IF output impedance		0.85	1.0		kΩ
	Limiter intput impedance		1.40	1.6		kΩ
	Unmuted audio output resistance			58		kΩ
	Muted audio output resistance			58		kΩ
RF/IF section (Int LO)						
	Unmuted audio level	4.5V = V_{CC}, RF level = -27dBm		450		mV_{RMS}
	System RSSI output	4.5V = V_{CC}, RF level = -27dBm		4.3		V

NOTE:
1. The generator source impedance is 50Ω, but the NE/SA605 input impedance at Pin 18 is 1500Ω. As a result, IF level refers to the actual signal that enters the NE/SA605 input (Pin 8) which is about 21dB less than the "available power" at the generator.

CIRCUIT DESCRIPTION

The NE/SA615 is an IF signal processing system suitable for second IF or single conversion systems with input frequency as high as 1GHz. The bandwidth of the IF amplifier is about 40MHz, with 39.7dB(v) of gain from a 50Ω source. The bandwidth of the limiter is about 28MHz with about 62.5dB(v) of gain from a 50Ω source. However, the gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 5dB, conversion gain of 13dB, and input third-order intercept of –10dBm. The oscillator will operate in excess of 1GHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to

100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

The output of the mixer is internally loaded with a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor can be added between the first IF output (Pin 16) and the interstage network.

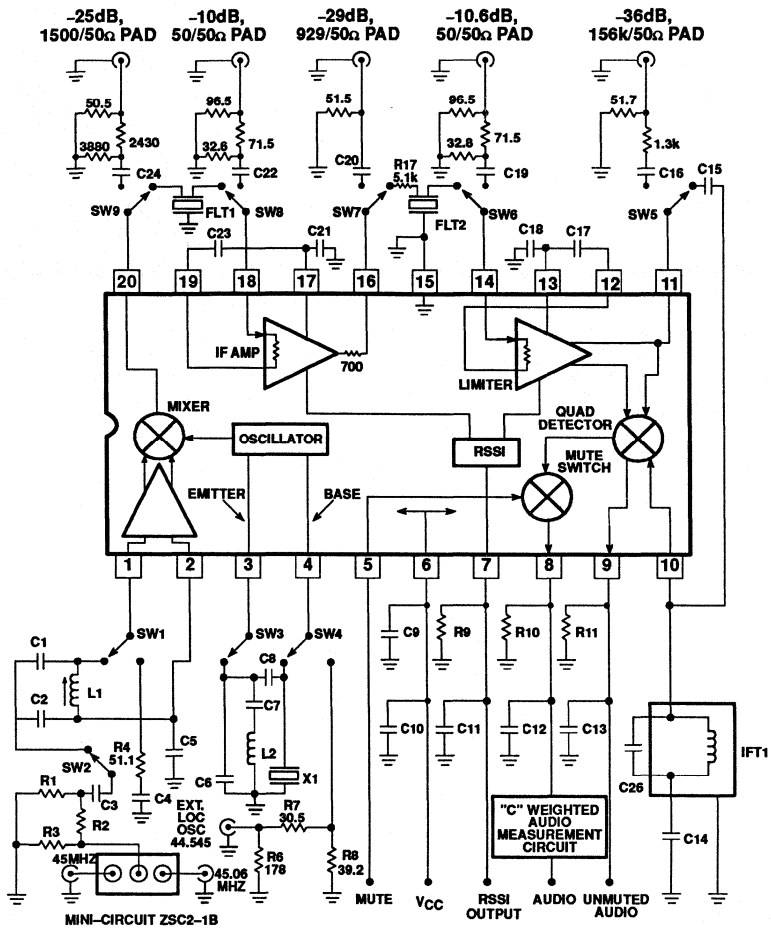
The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

Overall, the IF section has a gain of 90dB. For operation at intermediate frequencies greater than 455kHz, special care must be given to layout, termination, and interstage loss to avoid instability.

The demodulated output of the quadrature detector is available at two pins, one continuous and one with a mute switch. Signal attenuation with the mute activated is greater than 60dB. The mute input is very high impedance and is compatible with CMOS or TTL levels.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone.

NOTE: $dB(v) = 20\log V_{OUT}/V_{IN}$

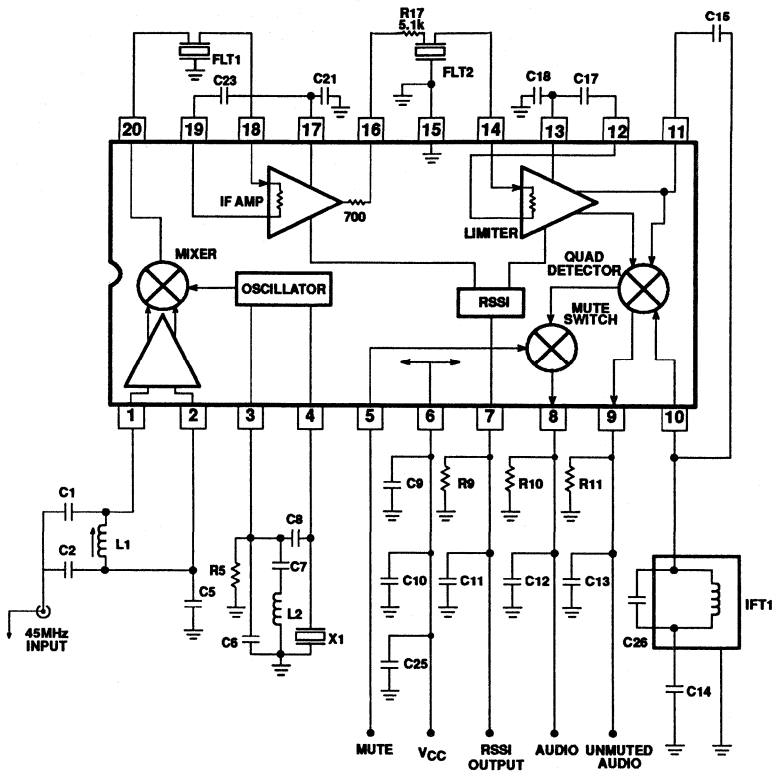


Automatic Test Circuit Component List

C1	47pF NPO Ceramic
C2	180pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	6.8μF Tantalum (minimum) *
C11	100nF ±10% Monolithic Ceramic
C12	15nF ±10% Ceramic
C13	150pF ±2% N1500 Ceramic
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
C26	390pF ±10% Monolithic Ceramic
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	455kHz 270μH TOKO #303LN-1129
L1	300nH TOKO #5CB-1055Z
L2	0.8μH TOKO 292CNS-T1038Z
X1	44.545MHz Crystal ICM4712701
R9	100k ±1% 1/4W Metal Film
R17	5.1k ±5% 1/4W Carbon Composition
R10	100k ±1% 1/4W Metal Film (optional)
R11	100k ±1% 1/4W Metal Film (optional)

*NOTE: This value can be reduced when a battery is the power source.

Figure 1. NE/SA615 45MHz Test Circuit (Relays as shown)



NE/SA615N
Application Component List

C1	47pF NPO Ceramic
C2	180pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	6.8µF Tantalum (minimum) *
C11	100nF ±10% Monolithic Ceramic
C12	15nF ±10% Ceramic
C13	150pF ±2% N1500 Ceramic
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
C26	390pF ±10% Monolithic Ceramic
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	455kHz 270µH TOKO #303LN-1129
L1	300nH TOKO #5CB-1055Z
L2	0.8µH TOKO 292CNS–T1038Z
X1	44.545MHz Crystal ICM4712701
R9	100k ±1% 1/4W Metal Film
R17	5.1k ±5% 1/4W Carbon Composition
R10	100k ±1% 1/4W Metal Film (optional)
R11	100k ±1% 1/4W Metal Film (optional)

*NOTE: This value can be reduced when a battery is the power source.

Figure 2. NE/SA615 45MHz Application Circuit

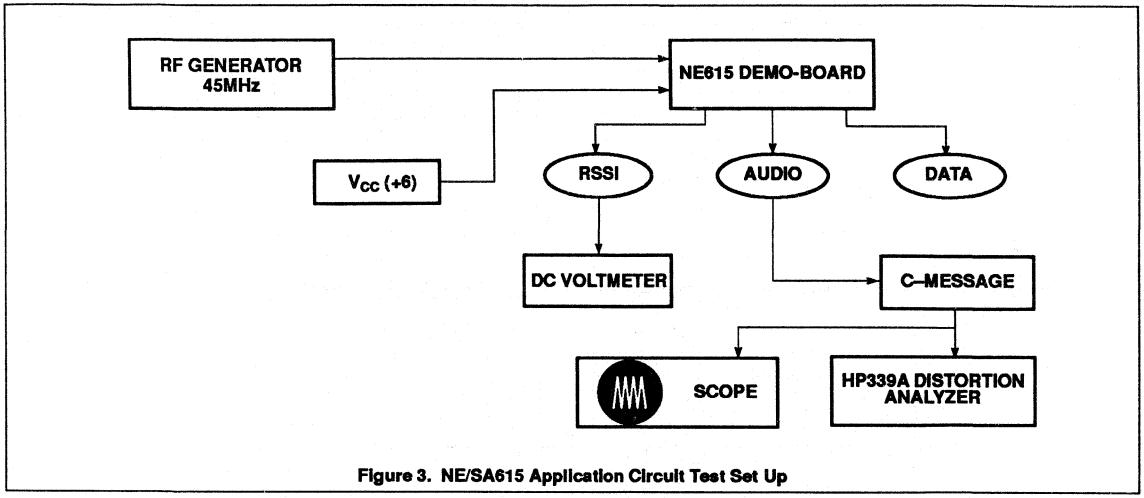


Figure 3. NE/SA615 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message filter has a peak gain of 100 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.22μV or –120dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 250mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10–15μF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1μF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2–3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 22kΩ, but should not be below 10kΩ.

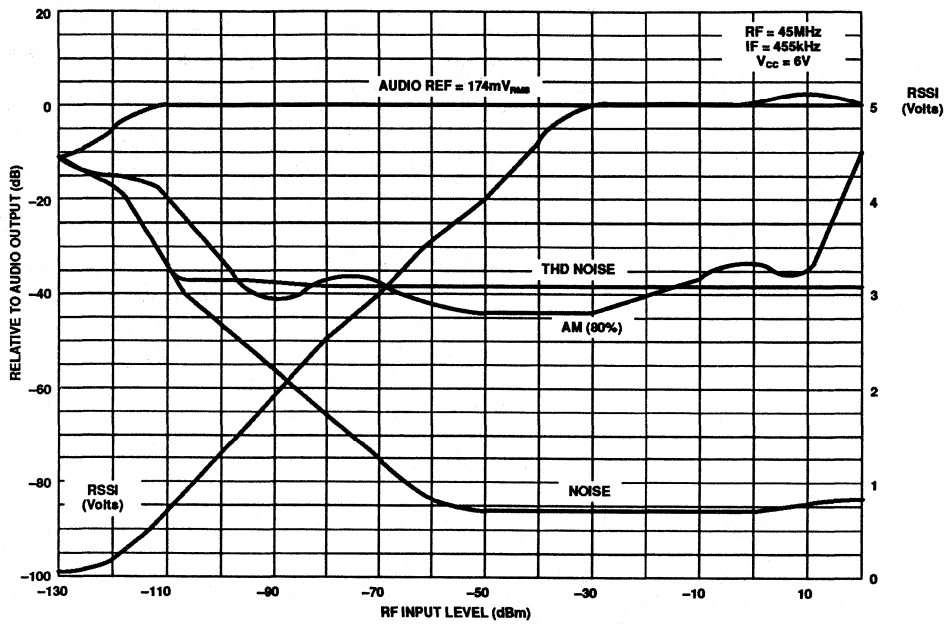


Figure 4. NE615 Application Board at 25°C

Low-voltage high performance mixer FM IF system — NE/SA616

DESCRIPTION

The NE/SA616 is a low-voltage high performance monolithic FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), voltage regulator and audio and RSSI op amps. The NE/SA616 is available in 20-lead dual-in-line plastic, 20-lead SOL (surface-mounted small outline large package) and 20-lead SSOP (shrink small outline package).

The NE616 was designed for portable communication applications and will function down to 2.7V. The RF section is similar to the famous NE615. The audio and RSSI outputs have amplifiers with access to the feedback path. This enables the designer to adjust the output levels or add filtering.

FEATURES

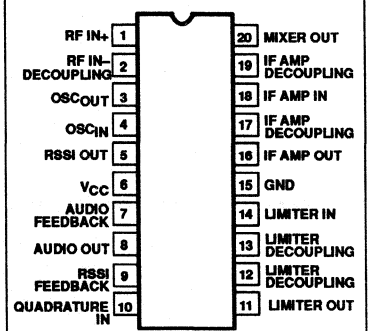
- Low power consumption: 3.5mA typical at 3V
- Mixer input to >150MHz
- Mixer conversion power gain of 17dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator or external oscillator can be used at higher frequencies)
- 102dB of IF Amp/Limiter gain
- 2MHz IF amp/limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a 80dB dynamic range
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.31μV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone with RF at 45MHz and IF at 455kHz
- SA616 meets cellular radio specifications
- Audio output internal op amp
- RSSI output internal op amp
- Internal op amps with rail-to-rail outputs
- ESD protection: Human Body Model 2kV
  Robot Model 200V

APPLICATIONS

- Portable cellular radio FM IF
- Cordless phones
- Wireless systems
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Portable high performance communication receiver
- Single conversion VHF receivers

PIN CONFIGURATION

D, DK and N Packages



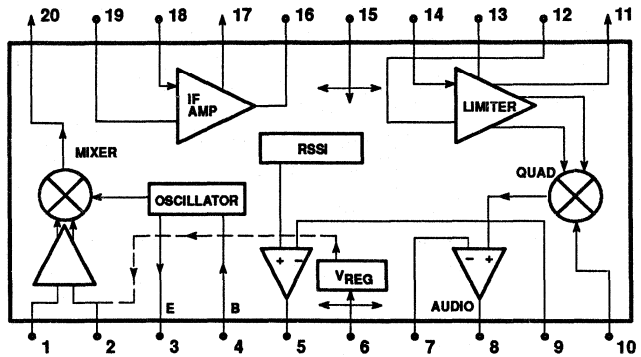
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic DIP	0 to +70°C	NE616N	0408B
20-Pin Plastic SOL (Surface-mount)	0 to +70°C	NE616D	0172D
20-Pin Plastic SSOP (Surface-mount)	0 to +70°C	NE616DK	1563
20-Pin Plastic DIP	-40 to +85°C	SA616N	0408B
20-Pin Plastic SOL (Surface-mount)	-40 to +85°C	SA616D	0172D
20-Pin Plastic SSOP (Surface-mount)	-40 to +85°C	SA616DK	1563

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		RATING	UNITS
V_{CC}	Single supply voltage		7	V
T_{STG}	Storage temperature range		–65 to +150	°C
T_A	Operating ambient temperature range	NE616	0 to +70	°C
		SA616	–40 to +85	°C
θ_{JA}	Thermal impedance	D package	90	°C/W
		DK package	117	
		N package	75	

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA616			
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		2.7		7.0	V
I_{CC}	DC current drain			3.5	5.0	mA

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +3V, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step-up; IF frequency = 455kHz; R17 = 2.4kΩ and R18 = 3.3kΩ; RF level = –45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with de-emphasis filter and C-message weighted filter. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA616			
			MIN	TYP	MAX	
Mixer/Osc section (ext LO = 220mV$_{RMS}$)						
f_{IN}	Input signal frequency			150		MHz
f_{OSC}	Crystal oscillator frequency			150		MHz
	Noise figure at 45MHz			6.8		dB
	Third–order input intercept point (50Ω source)	f1 = 45.0; f2 = 45.06MHz Input RF level = –52dBm		–9		dBm
	Conversion power gain	Matched 14.5dBV step–up	11	17		dB
		50Ω source		+2.5		dB
	RF input resistance	Single–ended input		8		kΩ
	RF input capacitance			3.0	4.0	pF
	Mixer output resistance	(Pin 20)	1.25	1.5		kΩ
IF section						
	IF amp gain	50Ω source		44		dB
	Limiter gain	50Ω source		58		dB

AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE616			
			MIN	TYP	MAX	
	Input limiting –3dB, R_{17a} = 2.4k, R_{17b} = 3.3k	Test at Pin 18		–105		dBm
	AM rejection	80% AM 1kHz		40		dB
	Audio level	Gain of two (2kΩ AC load)	60	120		mV
	SINAD sensitivity	IF level –110dBm		17		dB
THD	Total harmonic distortion		–30	–45		dB
S/N	Signal–to–noise ratio	No modulation for noise		62		dB
	IF RSSI output, R_9 = 2kΩ[1]	IF level = –118dBm		0.3	.80	V
		IF level = –68dBm	.70	1.1	2	V
		IF level = –23dBm	1.0	1.8	2.50	V
	RSSI range			80		dB
	RSSI accuracy			±2		dB
	IF input impedance	Pin 18	1.3	1.5		kΩ
	IF output impedance	Pin 16		0.3		kΩ
	Limiter input impedance	Pin 14	1.3	1.5		kΩ
	Limiter output impedance	Pin 11		0.3		kΩ
	Limiter output voltage	Pin 11		130		mV_{RMS}
RF/IF section (int LO)						
	Audio level	3V = V_{CC}, RF level = –27dBm		120		mV_{RMS}
	System RSSI output	3V = V_{CC}, RF level = –27dBm		2.2		V
	System SINAD sensitivity	RF level = –117dBm		12		dB

NOTE:
1. The generator source impedance is 50Ω, but the NE/SA616 input impedance at Pin 18 is 1500Ω. As a result, IF level refers to the actual signal that enters the NE/SA616 input (Pin 18) which is about 21dB less than the "available power" at the generator.

CIRCUIT DESCRIPTION

The NE/SA616 is an IF signal processing system suitable for second IF systems with input frequency as high as 150MHz. The bandwidth of the IF amplifier and limiter is at least 2MHz with 90dB of gain. The gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 6.2dB, conversion gain of 17dB, and input third-order intercept of –9dBm. The oscillator will operate in excess of 200MHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

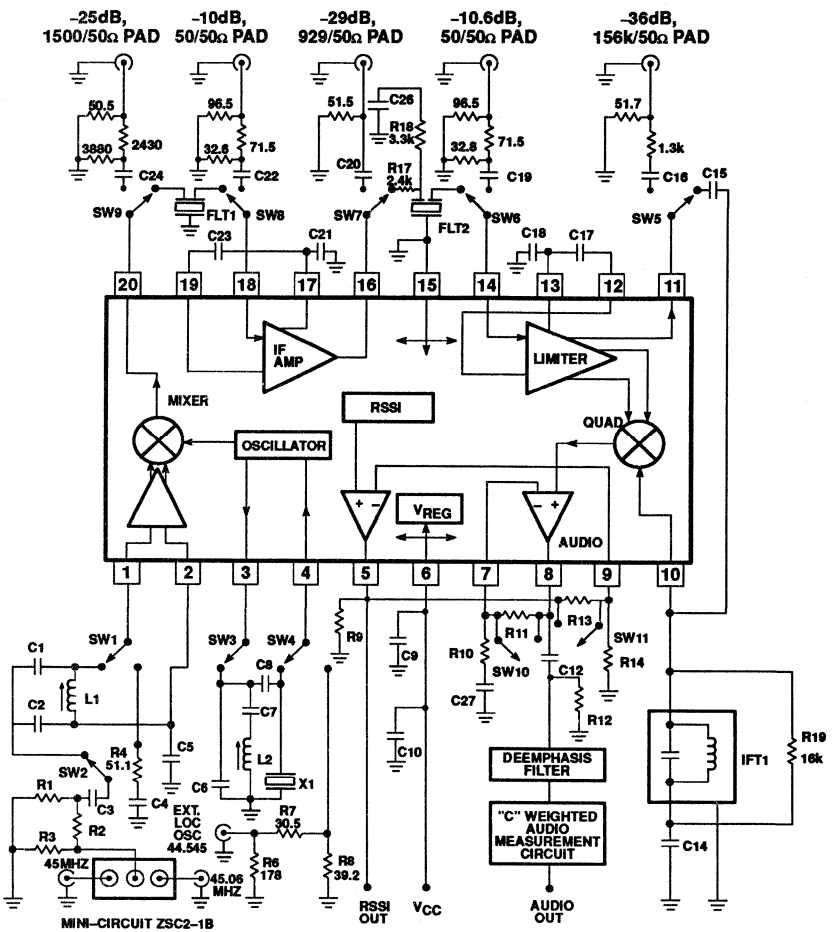
The output impedance of the mixer is a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. The IF amplifier has 43dB of gain and 5.5MHz bandwidth. The IF limiter has 60dB of gain and 4.5MHz bandwidth. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor or an L pad for simultaneous loss and impedance matching can be added between the first IF output (Pin 16) and the interstage network. The overall gain will then be 90dB with 2MHz bandwidth.

The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

The demodulated output of the quadrature drives an internal op amp. This op amp can be configured as a unity gain buffer, or for simultaneous gain, filtering, and 2nd-order temperature compensation if needed. It can drive an AC load as low as 5kΩ with a rail-to-rail output.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone. This signal drives an internal op amp. The op amp is capable of rail-to-rail output. It can be used for gain, filtering, or 2nd-order temperature compensation of the RSSI, if needed.

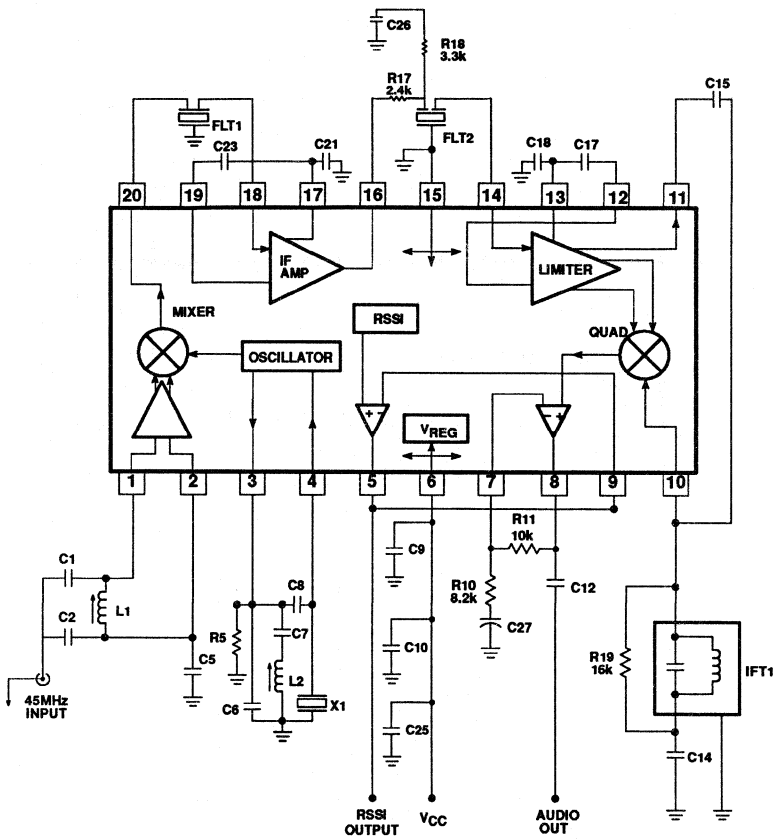
NOTE: $dB(v) = 20\log V_{OUT}/V_{IN}$



Automatic Test Circuit Component List

C1	100pF NPO Ceramic	C27	100nF ±10% Monolithic Ceramic
C2	390pF NPO Ceramic	Flt 1	Ceramic Filter Murata SFG455A3 or equiv
C5	100nF ±10% Monolithic Ceramic	Flt 2	Ceramic Filter Murata SFG455A3 or equiv
C6	22pF NPO Ceramic	IFT 1	455kHz (Ce = 180pF) Toko RMC–2A6597H
C7	1nF Ceramic	L1	147–160nH Coilcraft UNI–10/142–04J08S
C8	10.0pF NPO Ceramic	L2	0.8μH nominal
C9	100nF ±10% Monolithic Ceramic		Toko 292CNS–T1038Z
C10	15μF Tantalum (minimum)	X1	44.545MHz Crystal ICM4712701
C12	2.2μF	R9	2kΩ ±1% 1/4W Metal Film
C14	100nF ±10% Monolithic Ceramic	R10	8.2kΩ ±1%
C15	10pF NPO Ceramic	R11	10kΩ ±1%
C17	100nF ±10% Monolithic Ceramic	R12	2kΩ ±1%
C18	100nF ±10% Monolithic Ceramic	R13	20kΩ ±1%
C21	100nF ±10% Monolithic Ceramic	R14	10kΩ ±1%
C23	100nF ±10% Monolithic Ceramic	R17	2.4kΩ ±5% 1/4W Carbon Composition
C25	100nF ±10% Monolithic Ceramic	R18	3.3kΩ
C26	100nF ±10% Monolithic Ceramic	R19	16kΩ

Figure 1. NE/SA616 45MHz Test Circuit (Relays as shown)

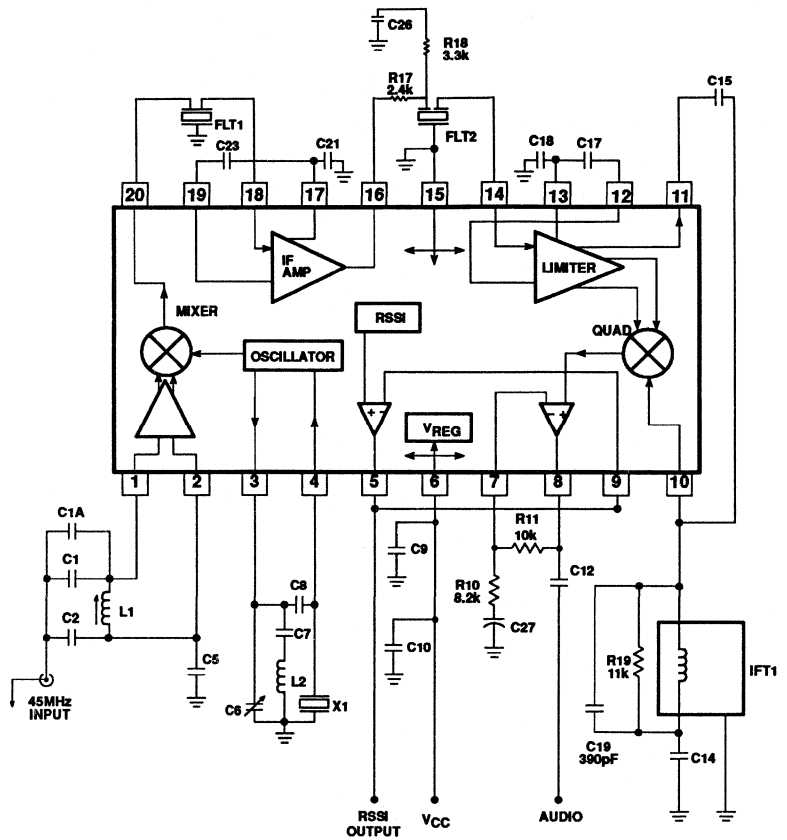


NE616D/DK Demo Board
Application Component List

C1	100pF NPO Ceramic
C2	390pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	10μF Tantalum (minimum) *
C12	2.2μF ±10% Ceramic
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
C26	100nF ±10% Monolithic Ceramic
C27	2.2μF Tantalum or Electrolytic
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	455kHz (Ce = 180pF) Toko RMC–2A6597H
L1	147–160nH Coilcraft UNI–10/142–04J08S
L2	0.8μH nominal Toko 292CNS–T1038Z
X1	44.545MHz Crystal ICM4712701
R5	Not Used in Application Board (see Note 8, pg 8)
R10	8.2k ±5% 1/4W Carbon Composition
R11	10k ±5% 1/4W Carbon Composition
R17	2.4k ±5% 1/4W Carbon Composition
R18	3.3k ±5% 1/4W Carbon Composition
R19	16k ±5% 1/4W Carbon Composition

*NOTE: This value can be reduced when a battery is the power source.

Figure 2. NE/SA616 45MHz Application Circuit



NE616DK Demoboard
Application Component List

C1A	18pF NPO Ceramic
C1	33pF NPO Ceramic
C2	220pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	30pF trim cap
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	15µF Tantalum (minimum)
C12	2.2µF ±10% Tantalum
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C19	390pF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C26	100nF ±10% Monolithic Ceramic
C27	2.2µF Tantalum
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	330µH TOKO 303LN-1130
L1	.33µH TOKO SCB-1320Z
L2	1.2µH
X1	44.545MHz Crystal ICM4712701
R5	Not Used in Application Board (see Note 8, pg 8)
R10	8.2k ±5% 1/4W Carbon Composition
R11	10k ±5% 1/4W Carbon Composition
R17	2.4k ±5% 1/4W Carbon Composition
R18	3.3k ±5% 1/4W Carbon Composition
R19	11k ±5% 1/4W Carbon Composition

Figure 3. NE/SA616 45MHz Application Circuit

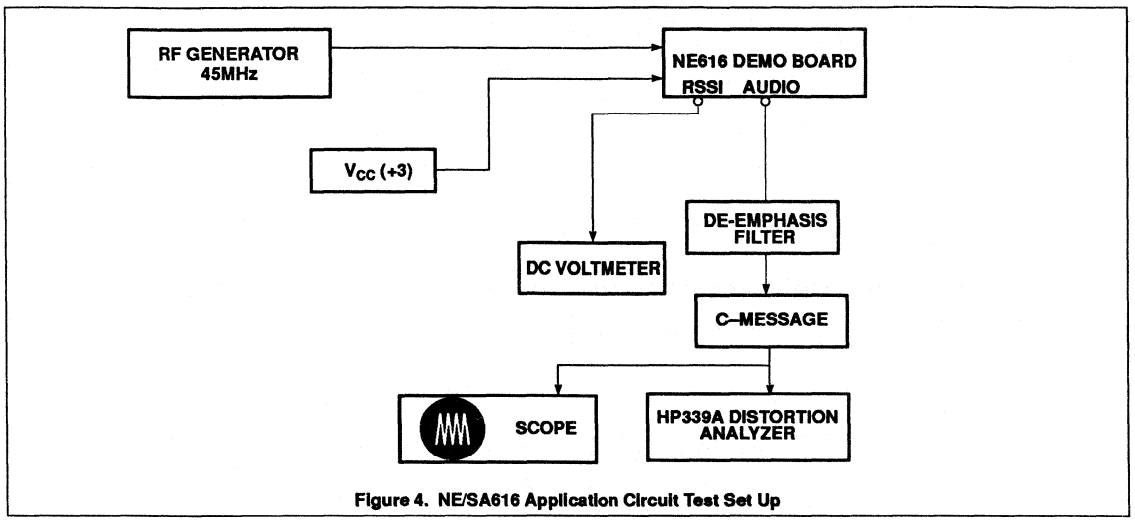


Figure 4. NE/SA616 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message and de-emphasis filter combination has a peak gain of 10 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer. The de-emphasis filter has a fixed -6dB/Octave slope between 300Hz and 3kHz.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.35μV or –116dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 500mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10-15μF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1μF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2-3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 22kΩ, but should not be below 10kΩ.

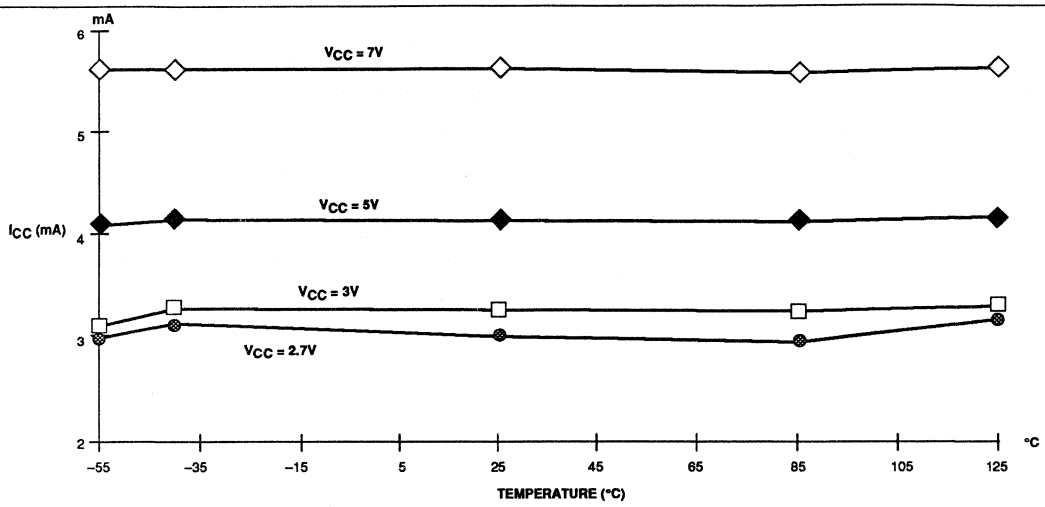


Figure 5. I_{CC} vs Temperature

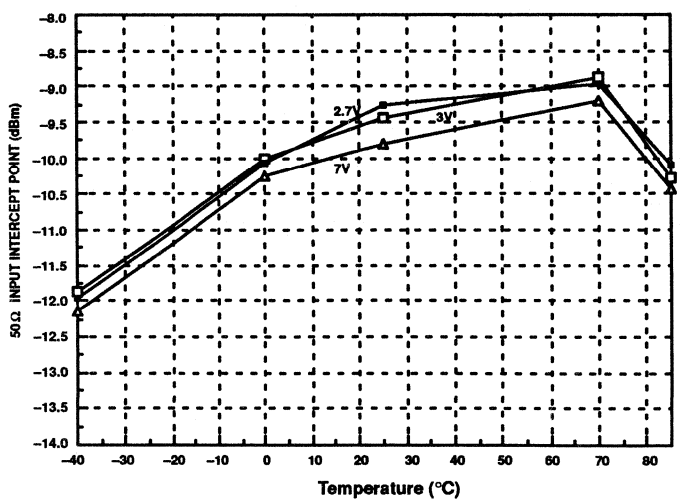


Figure 6. Third Order Intercept Point vs Supply Voltage

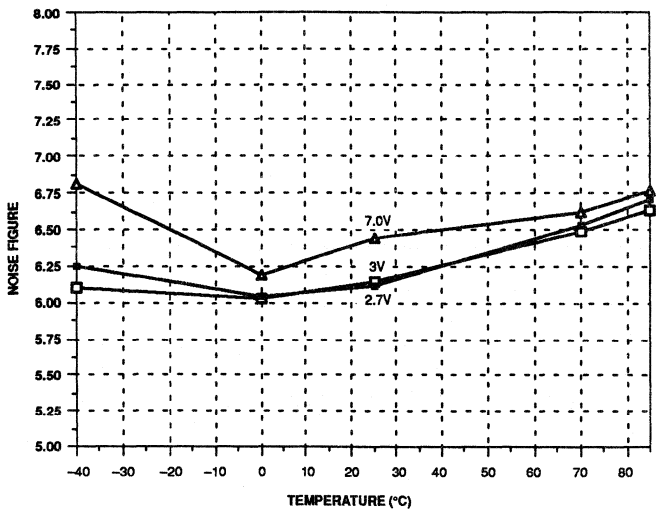


Figure 7. Mixer Noise Figure vs Supply Voltage

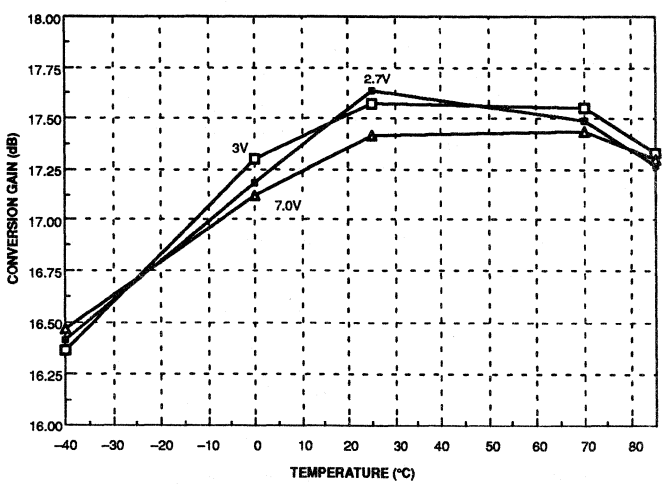


Figure 8. Conversion Gain vs Supply Voltage

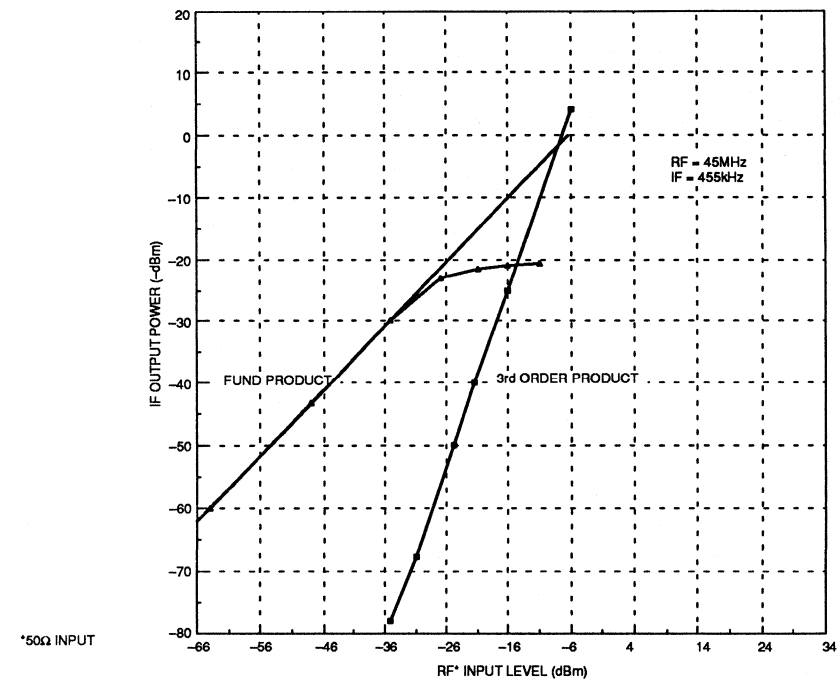


Figure 9. Mixer Third Order Intercept and Compression

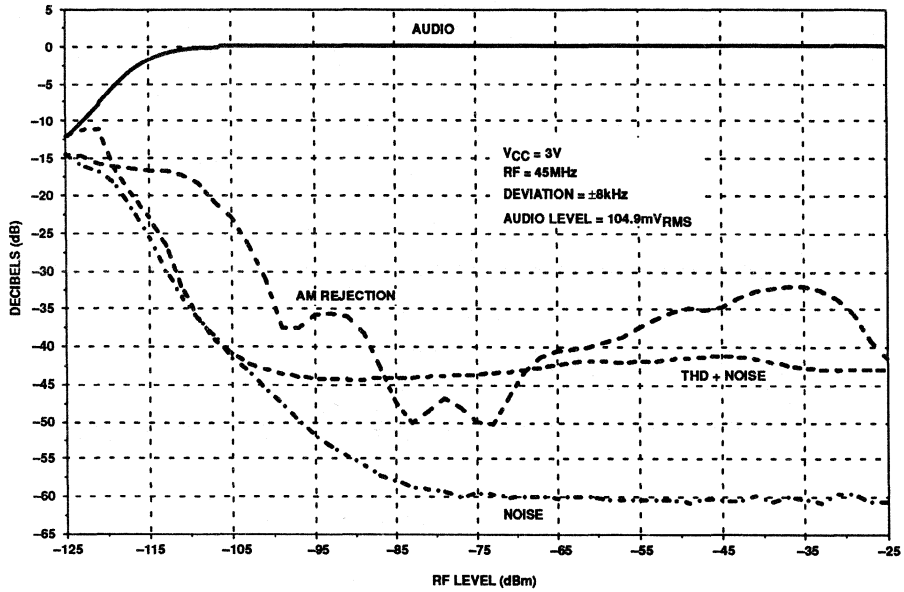


Figure 10. Sensitivity vs RF Level (–40°C)

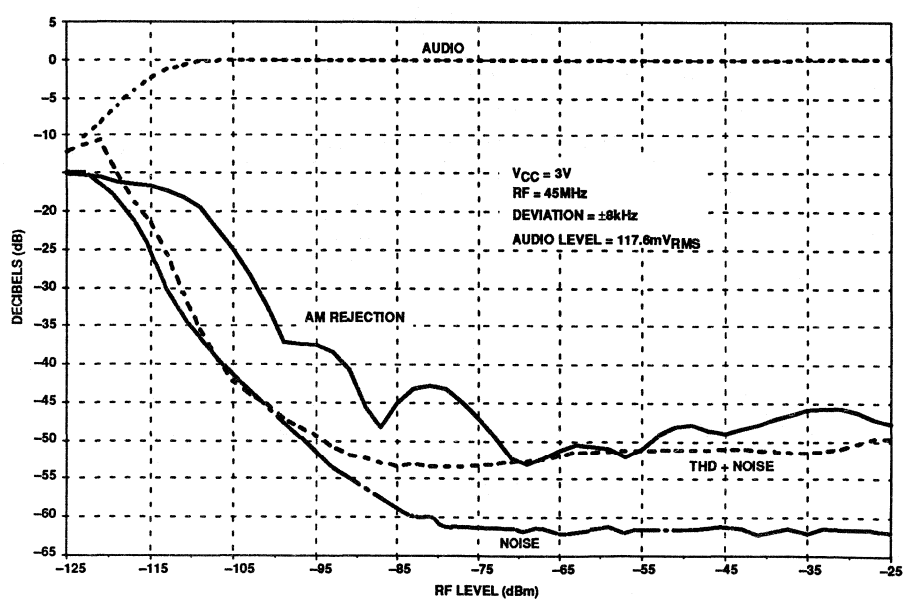


Figure 11. Sensitivity vs RF Level (+25°C)

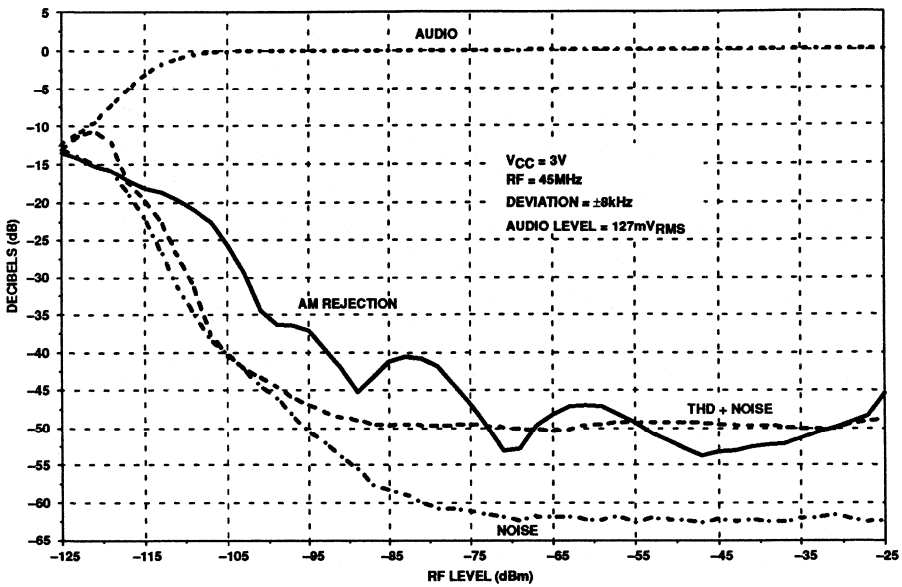


Figure 12. Sensitivity vs RF Level (Temperature 85°C)

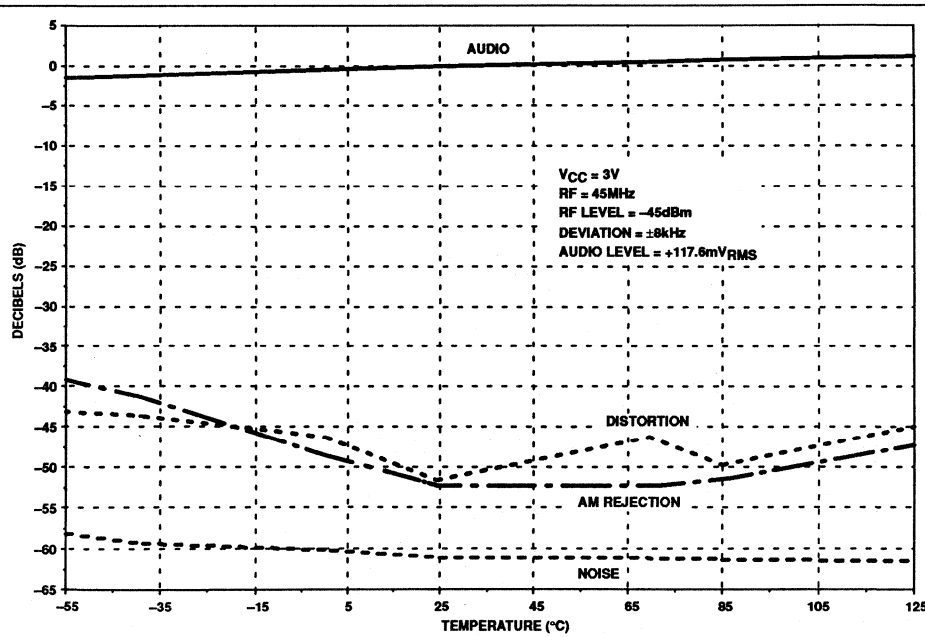


Figure 13. Relative Audio Level, Distortion, AM Rejection and Noise vs Temperature

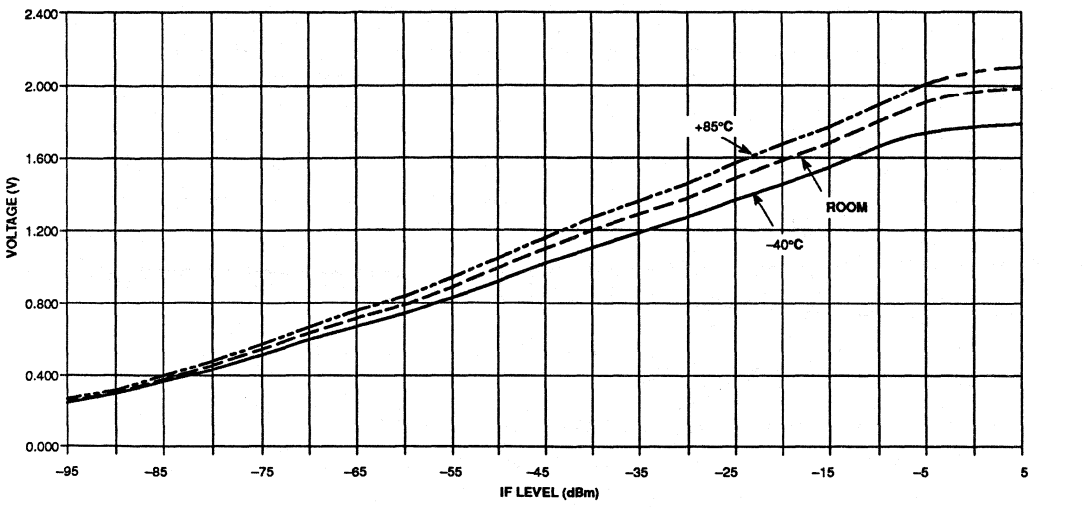


Figure 14. RSSI (455kHz IF @ 3V)

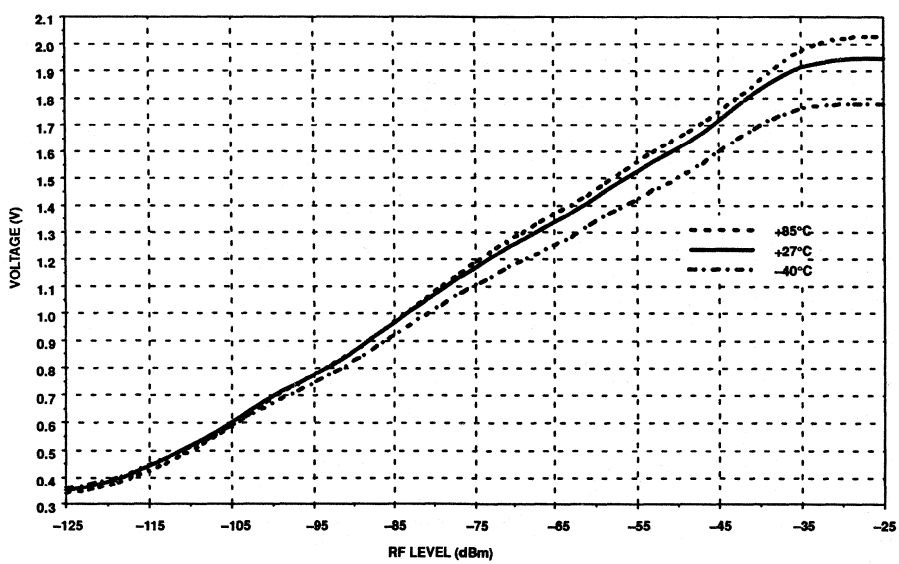


Figure 15. RSSI vs RF Level and Temperature - V_{CC} = 3V

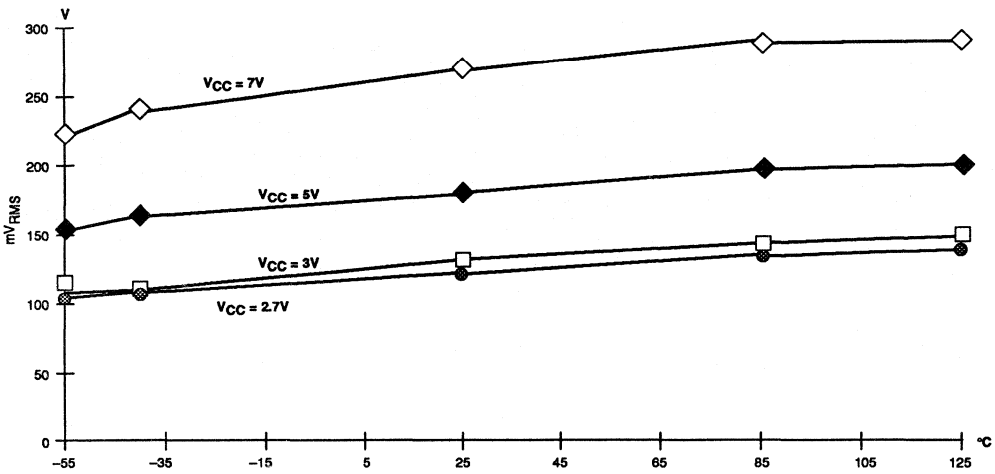
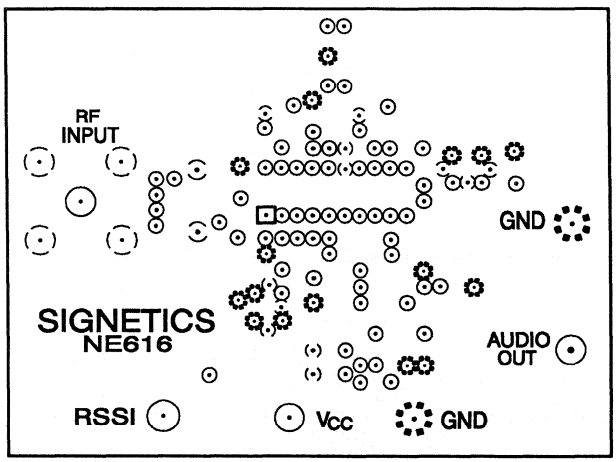


Figure 16. Audio Output vs Temperature



*Applies to Stand-Alone data sheets only.

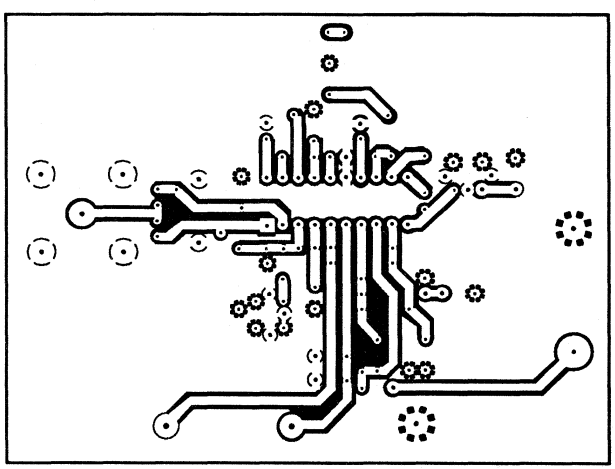
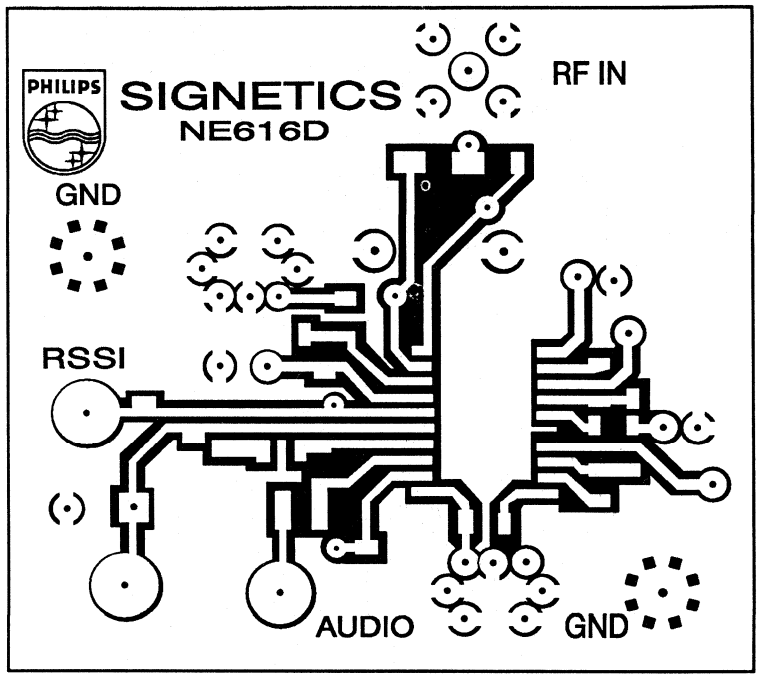


Figure 17. NE/SA616N DIP Product Board Layout (Actual Size* — For Reference Use Only)



*Applies to Stand-Alone data sheets only.

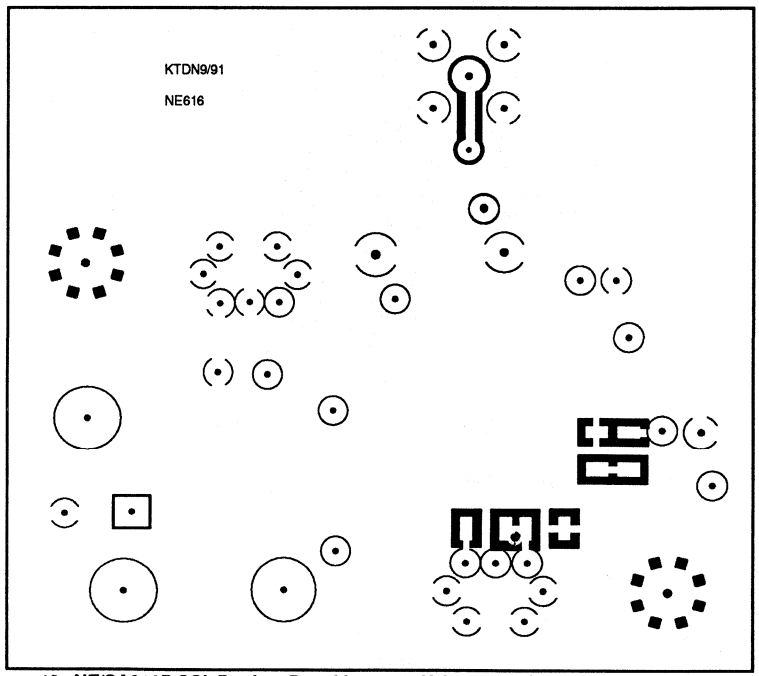
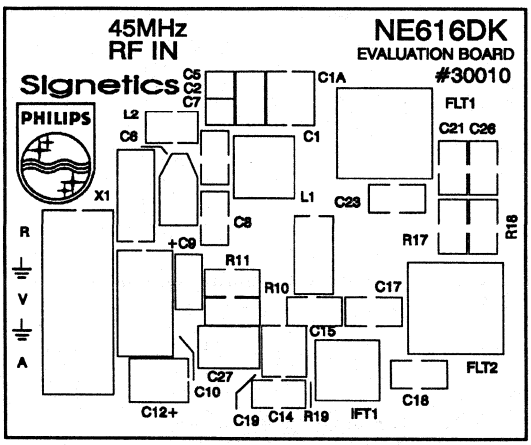
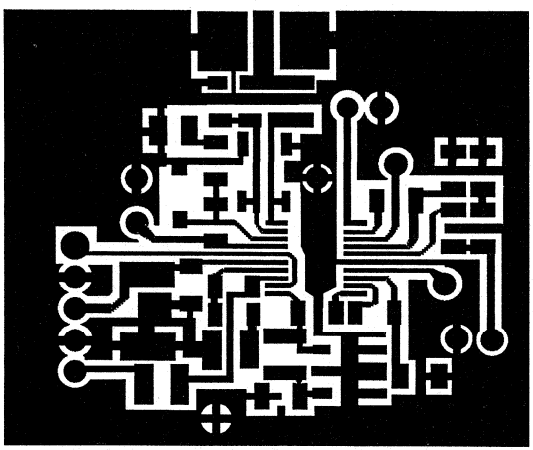


Figure 18. NE/SA616D SOL Product Board Layout (2X Actual Size* — For Reference Use Only)

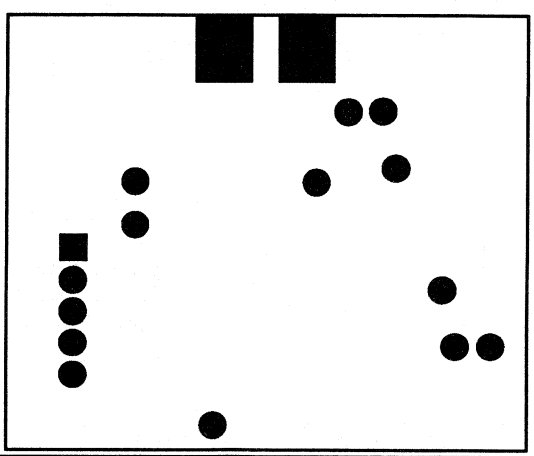
616 Silk Screen



616 TOP



616 BOTTOM



NOTE;
All views are TOP VIEW and not actual size. For reference only.

RF gain stage, VCO and mixer — 1GHz | NE/SA620

DESCRIPTION

The NE/SA620 is a combined RF amplifier, VCO and mixer designed for high-performance low-power communication systems from 800-1200MHz. The low-noise preamplifier has a 1.6dB noise figure at 900MHz with 11dB gain and an IM_3 intercept of -6dBm at the input. Input and output impedances are 50Ω and the gain is stabilized by on-chip compensation to vary less than ±0.2dB over -40 to +85°C temperature range. The wide-dynamic-range mixer has an 8dB noise figure and IM_3 intercept of +0dBm at the input at 900MHz. The mixer has an open-collector output. The chip incorporates a thru-mode option so the RF amplifier can be disabled and replaced by a through connection. The nominal current drawn from a single 3V supply is 9mA and 6.5mA in the thru-mode.

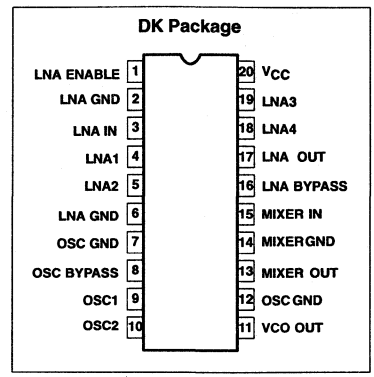
FEATURES

- Low current consumption: 9mA nominal, 6.5mA with thru-mode activated
- Outstanding noise figure: 1.6dB for the amplifier and 8dB for the mixer at 900MHz
- Excellent gain stability versus temperature and supply voltage
- Switchable overload capability
- Amplifier matched to 50Ω
- Internal VCO automatic leveling loop
- Monotonic VCO frequency vs control voltage
- Buffered VCO output

APPLICATIONS

- 900MHz front end
- RF data links
- UHF frequency conversion
- Portable radio
- Spread spectrum receivers
- 900MHz cordless phones

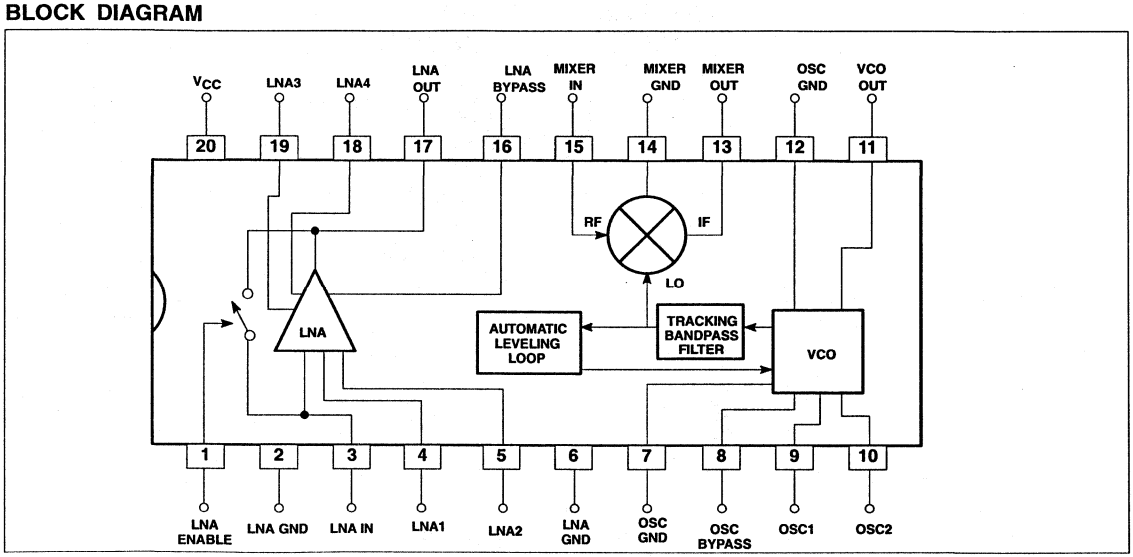
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic SSOP (Surface-mount)	0 to +70°C	NE620DK
20-Pin Plastic SSOP (Surface-mount)	-40 to +85°C	SA620DK

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage[1]	-0.3 to +6	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CC} + 0.3)	V
P_D	Power dissipation, T_A = 25°C (still air)[2] 20-Pin Plastic SSOP	980	mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power input/output	+20	dBm
T_{STG}	Storage temperature range	–65 to +150	°C

NOTE:
1. Transients exceeding 8V on V_{CC} pin may damage product.
2. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}:
   20-Pin SSOP: θ_{JA} = 110°C/W

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	2.7 to 5.5	V
	Operating ambient temperature range		
	NE Grade	0 to +70	°C
T_A	SA Grade	-40 to +85	°C
	Operating junction temperature		
	NE Grade	0 to +90	°C
T_J	SA Grade	-40 to +105	°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
I_{CC}	Supply current	Enable input high		9		mA
		Enable input low		6.5		mA
V_T	Enable logic threshold voltage[1]		1.12	1.27	1.42	V
V_{IH}	Logic 1 level	RF amp on	2.0		V_{CC}	V
V_{IL}	Logic 0 level	RF amp off	–0.3		0.8	V
I_{IL}	Enable input current	Enable = 0.4V	-1	0	1	µA
I_{IH}	Enable input current	Enable = 2.4V	-1	0	1	µA
V_{LNA-IN}	LNA input bias voltage	Enable = 2.4V		0.78		V
$V_{LNA-OUT}$	LNA output bias voltage	Enable = 2.4V		1.7		V
V_{BY}	LNA bypass bias voltage	Enable = 2.4V		1.7		V
V_{MX-IN}	Mixer RF input bias voltage			0.94		V

NOTE:
1. The ENABLE input must be connected to a valid logic level for proper operation of the NE/SA620.

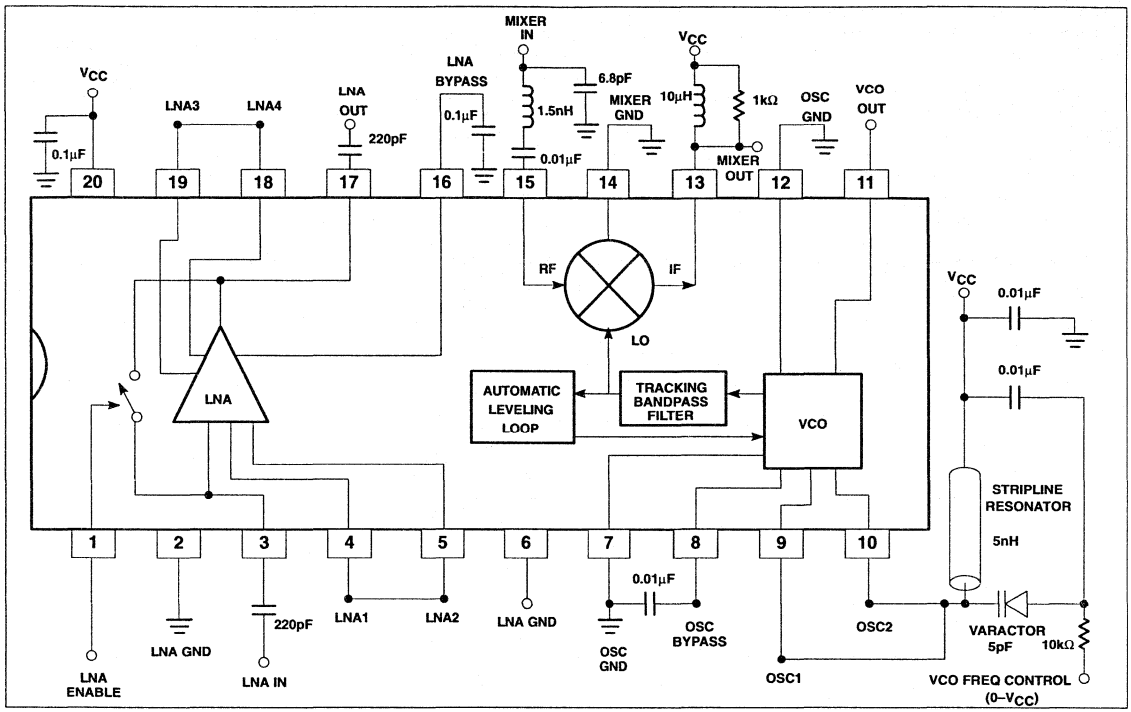
AC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; Enable = +3V; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
S_{21}	Amplifier gain	900MHz		11		dB
S_{21}	Amplifier gain in power-down mode	Enable = 0.4V, 900MHz		–9		dB
$\Delta S_{21}/\Delta T$	Gain temperature sensitivity in pwr-dwn mode	900MHz		–0.014		dB/°C
$\Delta S_{21}/\Delta T$	Gain temperature sensitivity enabled	900MHz		0.003		dB/°C
$\Delta S_{21}/\Delta f$	Gain frequency variation	800MHz - 1.2GHz		0.01		dB/MHz
S_{12}	Amplifier reverse isolation	900MHz		–20		dB
S_{11}	Amplifier input match	900MHz		-10		dB
S_{22}	Amplifier output match	900MHz		-12		dB
P_{-1dB}	Amplifier input 1dB gain compression	900MHz		-16		dBm
IM_{3INT}	Amplifier input third order intercept	900MHz		-5		dBm
NF	Amplifier noise figure	900MHz		1.6		dB
t_{ON}	Amplifier turn-on time (Enable Lo → Hi)	LNA coupling = 220pF LNA bypass = 0.1µF		7		µs
t_{OFF}	Amplifier turn-off time (Enable Hi → Lo)	LNA coupling = 220pF LNA bypass = 0.1µF		0.5		µs
VG_C	Mixer voltage conversion gain: $R_P = R_L$ = 1kΩ, P_{LO} = 2dBm	f_S = 0.9GHz, f_{LO} = 1.0GHz, f_{IF} = 100MHz		+16		dB
PG_C	Mixer power conversion gain: $R_P = R_L$ = 1kΩ, P_{LO} = 2dBm	f_S = 0.9GHz, f_{LO} = 1.0GHz, f_{IF} = 100MHz		+3		dB
S_{11M}	Mixer input match[1]	900MHz		-10		dB
NF_M	Mixer SSB noise figure	900MHz		8		dB
P_{-1dB}	Mixer input 1dB gain compression	900MHz		-6		dBm
IP_{3INT}	Mixer input third order intercept	900MHz		0		dBm
IP_{2INT}	Mixer input second order intercept	900MHz		+20		dBm
G_{RFM-IF}	Mixer RF feedthrough	900MHz		–3		dB
G_{LO-IF}	LO feedthrough to IF	900MHz		–8		dBm
G_{LO-RFM}	LO to mixer input feedthrough	900MHz		–30		dBm
G_{LO-RF}	LO to RF input feedthrough	900MHz		–40		dBm
P_{VCO}	VCO buffer out	900MHz		–16		dBm
	VCO frequency range		500		1500	MHz

NOTE:
1. Additional L/C elements are needed to achieve –10dB return loss at the RF input.

TYPICAL APPLICATION



CIRCUIT TECHNOLOGY

LNA

Impedance Match: Both input and output ports are pre-matched to 50Ω at 900MHz.

However, user can fine tune the center frequency, if necessary, by inserting an inductor or capacitor between Pins 4 and 5 for input match adjustment; or between Pins 18 and 19 for output match adjustment.

Noise Match: Advanced QUBiC process technology and extensive circuit optimizations yield an unprecedented 1.6dB NF at 900MHz from silicon IC, while maintaining good impedance match at both input and output.

Thru-Mode: A series switch can be activated to feed RF signals from LNA input to output directly. As a result, the power handling is much improved and current consumption is reduced by 2.5mA as well.

Programmable Current: The LNA has a default bias current of 3mA. However, it can be increased by connecting a low impedance resistor ($\Delta I = \frac{1200}{R} mA$, if $V_{CC} = 3V$) between LNA OUT and LNA ENABLE to maintain full LNA power-down capability in Thru-Mode; or between LNA OUT and V_{CC} for board layout convenience. Additionally there is a third method to increase the bias current by connecting a resistor between the V_{CC} and LNA BYPASS $\Delta I = \frac{R}{8000} mA$ if V_{CC} = 5V). This method is preferred over the first two approaches for higher gain and output power, but is applicable only when higher supply voltage (V_{CC} > 4V) is available. It also retains the full LNA power-down capability in thru-mode. In any event, it is recommended not to increase the LNA current by more than 3mA. On the other hand, the LNA current also can be reduced by connecting a high impedance resistor between LNA BYPASS and ground ($\Delta I = \frac{108000}{R} mA$, if $V_{CC} = 3V$).

Temperature Compensation: The LNA has built-in temperature compensation scheme to reduce the gain drift to 0.003dB/°C from –40°C to +85°C.

Supply Voltage Compensation: Unique circuitry provides gain stabilization over wide supply voltage range. Generally speaking, the gain changes no more than 0.25dB when V_{CC} increases from 3V to 5V.

Mixer

Input Match: The mixer is configured for maximum gain and best noise figure. But the user needs to supply L/C elements to achieve those performances. However, if high third-order input intercept point is required, then the user can insert a 27Ω series resistance to attain good impedance match and 6dB higher intercept point simultaneously, although the conversion gain and noise figure will be degraded by approximately 6dB.

Tracking Bandpass Filter: At the LO input port of the mixer there is a tracking bandpass filter to track the VCO center frequency, and adjusts the bandpass filter accordingly. The result is the elimination of low frequency noise injecting into the mixer LO port for improved mixer performance.

VCO

Resonator Sensor: OSC1 at Pin 9 is an independent sensing terminal. It should be connected to the point where main resonator

resides using separate trace from Pin 10. By doing so, all parasitic elements between main resonator and NE620 Pin 10 are suppressed to minimum effect.

Automatic Leveling Loop: On-chip detector and loop amplifier are provided to regulate the VCO amplitude regardless of the Q-factor (>10) that comes with the resonator and varactor diode, thus achieving constant mixer conversion gain over varieties of resonator and varactor combinations.

Buffered VCO Output: The VCO signal is buffered and delivered to the output via Pin 11 to drive the external prescaler directly. The drive capability can be doubled by connecting a 470Ω resistor between Pin 11 and ground.

External LO Drive: If the user has a high quality source available, and wishes to use it to drive the mixer, then OSC BYPASS at Pin 8 can be connected to ground to disable the on-chip VCO.

Next, the resonator and varactor diode should be replaced by a high impedance choke between Pin 10 and V_{CC}. The internal tracking bandpass filter will be deactivated automatically under this condition. The external LO drive signal can then be AC-coupled to OSC2 at Pin 10.

High performance low power FM IF system with high-speed RSSI

NE/SA624

DESCRIPTION

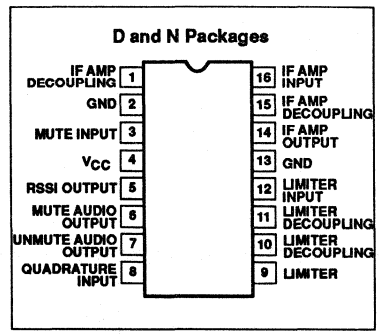
The NE/SA624 is pin-to-pin compatible with the NE/SA604A, but has faster RSSI rise and fall time. The NE/SA624 is an improved monolithic low-power FM IF system incorporating two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator, and voltage regulator. The NE/SA624 features higher IF bandwidth (25MHz) and temperature compensated RSSI and limiters permitting higher performance application compared with the NE/SA604. The NE/SA624 is available in a 16-lead dual-in-line plastic and 16-lead SO (surface-mounted miniature) package.

APPLICATIONS

- Digital cellular base station
- Cellular radio FM IF
- High performance communications receivers
- Intermediate frequency amplification and detection up to 25MHz
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers

PIN CONFIGURATION

D and N Packages



FEATURES

- Low power consumption: 3.4mA typical
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- Fast RSSI rise and fall time
- Two audio outputs - muted and unmuted
- Low external component count; suitable for crystal/ceramic filters
- Excellent sensitivity: 1.5μV across input pins (0.22μV into 50Ω matching network) for 12dB SINAD (Signal to Noise and Distortion ratio) at 455kHz
- SA624 meets cellular radio specifications

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic DIP	0 to +70°C	NE624N	0406C
16-Pin Plastic SO (Surface-mount)	0 to +70°C	NE624D	0005D
16-Pin Plastic DIP	-40 to +85°C	SA624N	0406C
16-Pin Plastic SO (Surface-mount)	-40 to +85°C	SA624D	0005D

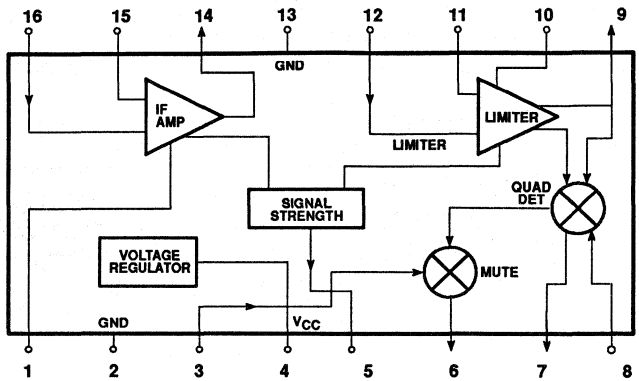
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	9	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range NE624 SA624	0 to +70 -40 to +85	°C °C
θ_{JA}	Thermal impedance D package N package	90 75	°C/W °C/W

High performance low power FM IF system with high-speed RSSI

NE/SA624

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE624			SA624			
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Power supply voltage range		4.5		8.0	4.5		8.0	V
I_{CC}	DC current drain		2.5	3.4	4.2	2.5	3.4	4.2	mA
	Mute switch input threshold (ON) (OFF)		1.7		 1.0	1.7		 1.0	V V

AC ELECTRICAL CHARACTERISTICS

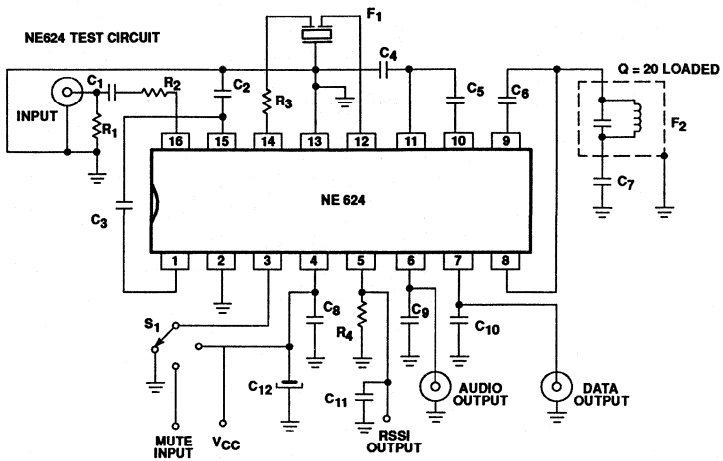
Typical reading at $T_A = 25°C$; $V_{CC} = \pm 6V$, unless otherwise stated. IF frequency = 455kHz; IF level = -47dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE624			SA624			
			MIN	TYP	MAX	MIN	TYP	MAX	
	Input limiting -3dB	Test at Pin 16		-92			-92		dBm/50Ω
	AM rejection	80% AM 1kHz	30	34		30	34		dB
	Recovered audio level	15nF de-emphasis	110	175	250	80	175	260	mV_{RMS}
	Recovered audio level	150pF de-emphasis		530			530		mV_{RMS}
THD	Total harmonic distortion		-35	-42		-34	-42		dB
S/N	Signal-to-noise ratio	No modulation for noise		73			73		dB
	RSSI output[1]	RF level = -118dBm	0	160	550	0	160	650	mV
		RF level = -68dBm	2.0	2.65	3.0	1.9	2.65	3.1	V
		RF level = -18dBm	4.1	4.85	5.5	4.0	4.85	5.6	V
	RSSI output rise time (10kHz pulse, no IF filter)	IF freq. = 455kHz							
		IF level = -44dBm		1.1			1.1		µs
		IF level = -16dBm		1.2			1.2		µs
		IF freq. = 10.7MHz							
		IF level = -44dBm		1.2			1.2		µs
		IF level = -16dBm		1.1			1.1		µs
	RSSI output fall time (10kHz pulse, no IF filter)	IF freq. = 455kHz							
		IF level = -44dBm		1.3			1.3		µs
		IF level = -16dBm		4.7			4.7		µs
		IF freq. = 10.7MHz							
		IF level = -44dBm		1.6			1.6		µs
		IF level = -16dBm		4.2			4.2		µs
	RSSI range	R_4 = 100k (Pin 5)		90			90		dB
	RSSI accuracy	R_4 = 100k (Pin 5)		±1.5			±1.5		dB
	IF input impedance		1.4	1.6		1.4	1.6		kΩ
	IF output impedance		0.85	1.0		0.85	1.0		kΩ
	Limiter input impedance		1.4	1.6		1.4	1.6		kΩ
	Limiter output impedance			300			300		Ω
	Limiter output level no load			280			280		mV_{RMS}
	Unmuted audio output resistance			58			58		kΩ
	Muted audio output resistance			58			58		kΩ

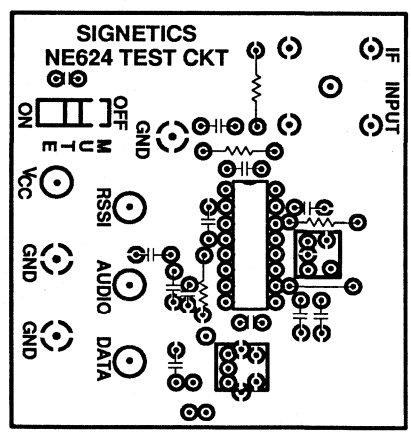
NOTE:

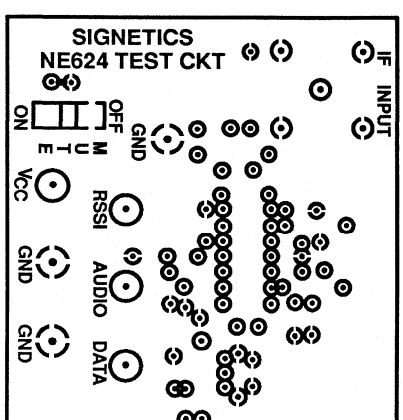
1. NE604 data sheets refer to power at 50Ω input termination; about 21dB less power actually enters the internal 1.5k input.

NE604 (50)	NE624 (1.5k)/NE605 (1.5k)
-97dBm	-118dBm
-47dBm	-68dBm
+3dBm	-18dBm



C1	100nF + 80 – 20% 63V K10000-25V Ceramic
C2	100nF +10% 50V
C3	100nF ±10% 50V
C4	100nF +10% 50V
C5	100nF ±10% 50V
C6	10pF ±2% 100V NPO Ceramic
C7	100nF ±10% 50V
C8	100nF ±10% 50V
C9	15nF ±10% 50V
C10	150pF ±2% 100V N1500 Ceramic
C11	1nF ±10% 100V K2000-Y5P Ceramic
C12	6.8µF ±20% 25V Tantalum
F1	455kHz Ceramic Filter Murata SFG455A3
F2	455kHz (Ce = 180pF) TOKO RMC 2A6597H
R1	51Ω ±1% 1/4W Metal Film
R2	1500Ω ±1% 1/4W Metal Film
R3	1500Ω ±5% 1/8W Carbon Composition
R4	100kΩ ±1% 1/4W Metal Film





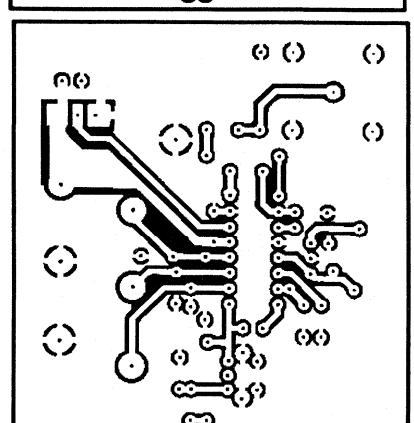


Figure 1. NE/SA624 Test Circuit

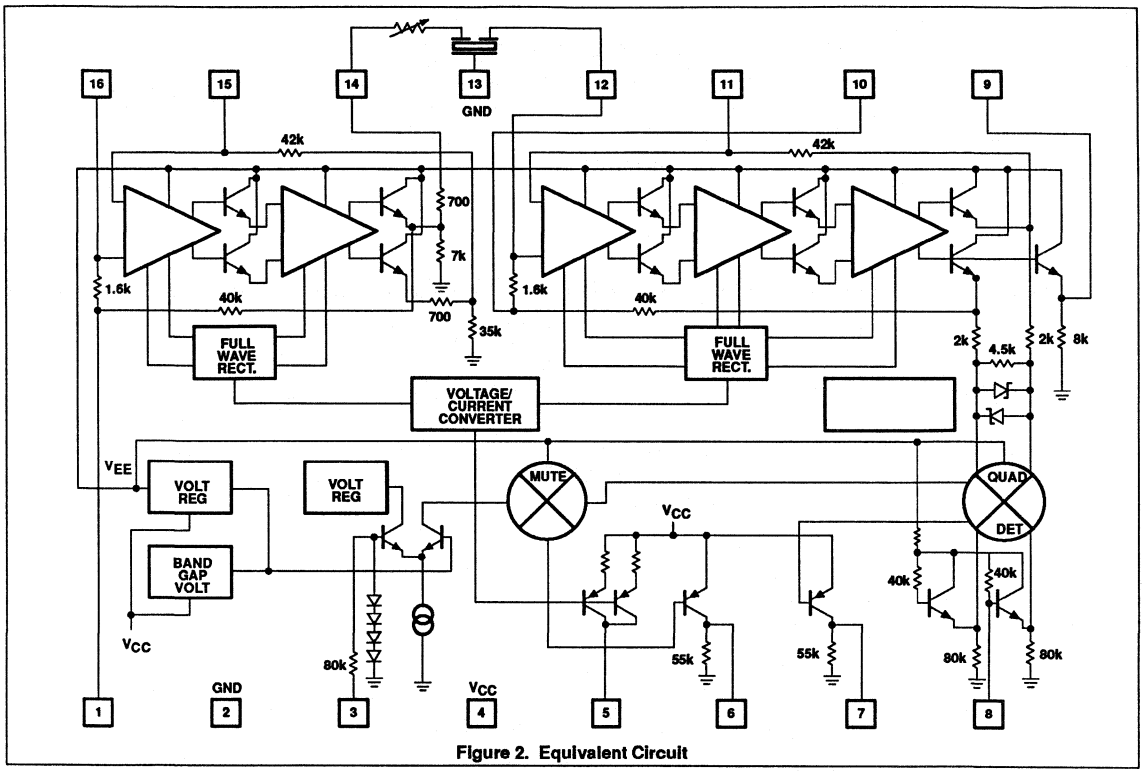


Figure 2. Equivalent Circuit

High performance low power FM IF system with high-speed RSSI

NE/SA624

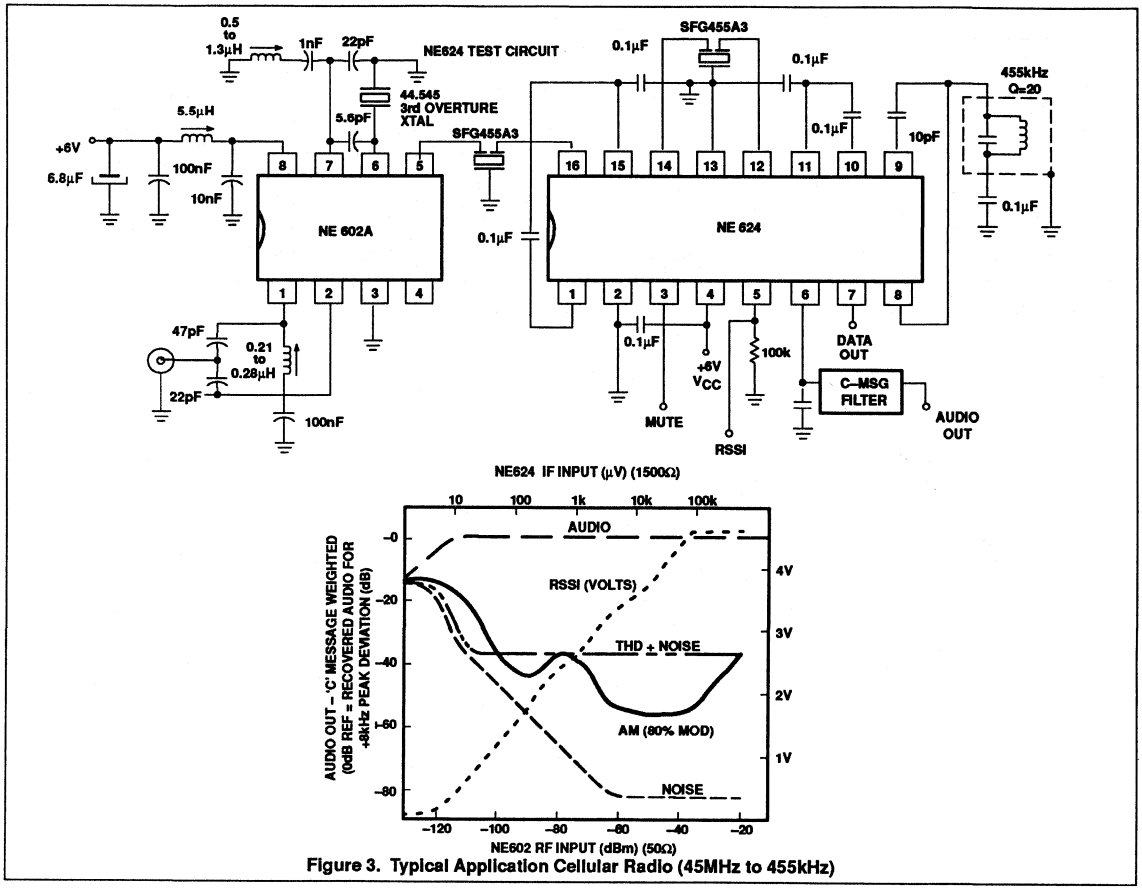


Figure 3. Typical Application Cellular Radio (45MHz to 455kHz)

CIRCUIT DESCRIPTION

The NE/SA624 is a very high gain, high frequency device. Correct operation is not possible if good RF layout and gain stage practices are not used. The NE/SA624 cannot be evaluated independent of circuit, components, and board layout. A physical layout which correlates to the electrical limits is shown in Figure 1. This configuration can be used as the basis for production layout.

The NE/SA624 is an IF signal processing system suitable for IF frequencies as high as 21.4MHz. The device consists of two limiting amplifiers, quadrature detector, direct audio output, muted audio output, and signal strength indicator (with output characteristic). The sub-systems are shown in Figure 2. A typical application with 45MHz input and 455kHz IF is shown in Figure 3.

IF Amplifiers

The IF amplifier section consists of two log-limiting stages. The first consists of two differential amplifiers with 39dB of gain and a small signal bandwidth of 41MHz (when driven from a 50Ω source). The output of the first limiter is a low impedance emitter follower with 1kΩ of equivalent series resistance. The second limiting stage consists of three differential amplifiers with a gain of 62dB and a small signal AC bandwidth of 28MHz. The outputs of the final differential stage are buffered to the internal quadrature detector. One of the outputs is available at Pin 9 to drive an external quadrature capacitor and L/C quadrature tank.

Both of the limiting amplifier stages are DC biased using feedback. The buffered output of the final differential amplifier is fed back to the input through 42kΩ resistors. As shown in Figure 2, the input impedance is established for each stage by tapping one of the feedback resistors 1.6kΩ from the input. This requires one additional decoupling capacitor from the tap point to ground.

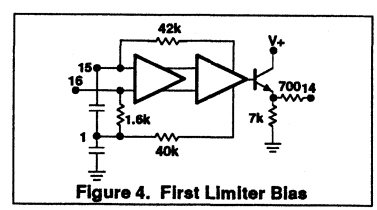


Figure 4. First Limiter Bias

Because of the very high gain, bandwidth and input impedance of the limiters, there is a very real potential for instability at IF frequencies above 455kHz. The basic phenomenon is shown in Figure 6. Distributed feedback (capacitance, inductance and radiated fields)

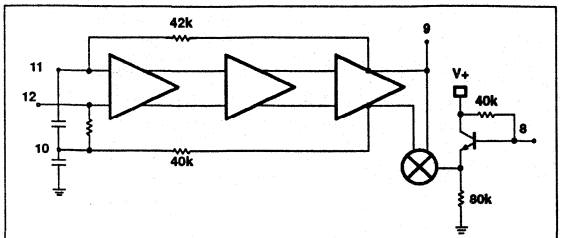


Figure 5. Second Limiter and Quadrature Detector

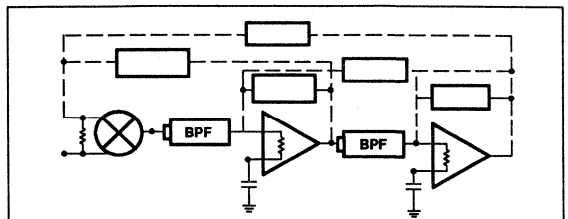
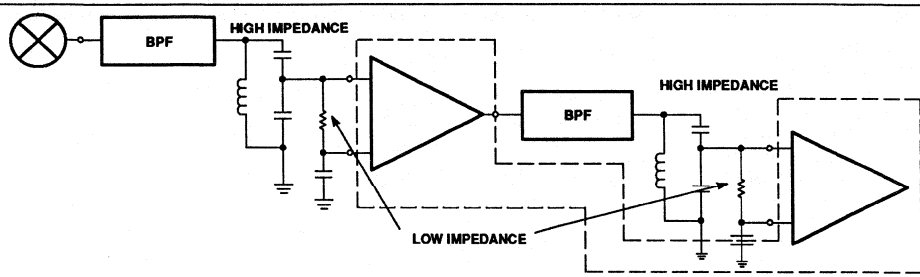
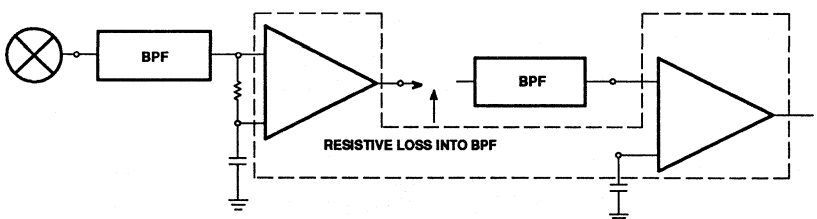


Figure 6. Feedback Paths



a. Terminating High Impedance Filters with Transformation to Low Impedance



b. Low Impedance Termination and Gain Reduction

Figure 7. Practical Termination

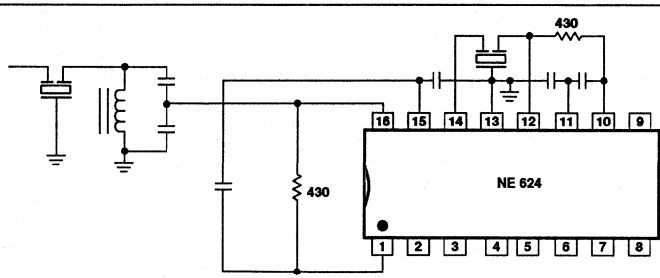


Figure 8. Crystal Input Filter with Ceramic Interstage Filter

forms a divider from the output of the limiters back to the inputs (including RF input). If this feedback divider does not cause attenuation greater than the gain of the forward path, then oscillation or low level regeneration is likely. If regeneration occurs, two symptoms may be present: (1)The RSSI output will be high with no signal input (should nominally be 250mV or lower), and (2) the demodulated output will demonstrate a threshold. Above a certain input level, the limited signal will begin to dominate the regeneration, and the demodulator will begin to operate in a "normal" manner.

There are three primary ways to deal with regeneration: (1) Minimize the feedback by gain stage isolation, (2) lower the stage input impedances, thus increasing the feedback attenuation factor, and (3) reduce the gain. Gain reduction can effectively be accomplished by adding attenuation between stages. This can also lower the input impedance if well planned. Examples of impedance/gain adjustment are shown in

Figure 7. Reduced gain will result in reduced limiting sensitivity.

A feature of the NE624 IF amplifiers, which is not specified, is low phase shift. The NE624 is fabricated with a 10GHz process with very small collector capacitance. It is advantageous in some applications that the phase shift changes only a few degrees over a wide range of signal input amplitudes. Additional information will be provided in the upcoming product specification (this is a preliminary specification) when characterization is complete.

Stability Considerations

The high gain and bandwidth of the NE624 in combination with its very low currents permit circuit implementation with superior performance. However, stability must be maintained and, to do that, every possible feedback mechanism must be addressed. These mechanisms are: 1) Supply lines and ground, 2) stray layout inductances and capacitances, 3) radiated fields, and 4) phase shift. As the system IF increases, so must the attention to fields and strays. However, ground and supply loops cannot be overlooked, especially at lower frequencies. Even at 455kHz, using the test layout in Figure 1, instability will occur if the supply line is not decoupled with two high quality RF capacitors, a 0.1μF monolithic right at the V_{CC} pin, and a 6.8μF tantalum on the supply line. An electrolytic is not an adequate substitute. At 10.7MHz, a 1μF tantalum has proven acceptable with this layout. Every layout must be evaluated on its own merit, but don't underestimate the importance of good supply bypass.

At 455kHz, if the layout of Figure 1 or one substantially similar is used, it is possible to directly connect ceramic filters to the input and between limiter stages with no special consideration. At frequencies above 2MHz, some input impedance reduction is usually necessary. Figure 7 demonstrates a practical means.

As illustrated in Figure 8, 430Ω external resistors are applied in parallel to the internal 1.6kΩ load resistors, thus presenting approximately 330Ω to the filters. The input filter is a crystal type for narrowband selectivity. The filter is terminated with a tank which transforms to 330Ω. The interstage filter is a ceramic type which doesn't contribute to system selectivity, but does suppress wideband noise and stray signal pickup. In wideband 10.7MHz IFs the input filter can also be ceramic, directly connected to Pin 16.

In some products it may be impractical to utilize shielding, but this mechanism may be appropriate to 10.7MHz and 21.4MHz IF. One of the benefits of low current is lower radiated field strength, but lower does not mean non-existent. A spectrum analyzer with an active probe will clearly show IF energy with the probe held in the proximity of the second limiter output or quadrature coil. No specific recommendations are provided, but mechanical shielding should be considered if layout, bypass, and input impedance reduction do not solve a stubborn instability.

The final stability consideration is phase shift. The phase shift of the limiters is very low, but there is phase shift contribution from the quadrature tank and the filters. Most filters demonstrate a large phase shift across their passband (especially at the edges). If the quadrature detector is tuned to the edge of the filter passband, the combined filter and quadrature phase shift can aggravate stability. This is not usually a problem, but should be kept in mind.

Quadrature Detector

Figure 5 shows an equivalent circuit of the NE624 quadrature detector. It is a multiplier cell similar to a mixer stage. Instead of mixing two different frequencies, it mixes two signals of common frequency but different phase. Internal to the device, a constant amplitude (limited) signal is differentially applied to the lower port of the multiplier. The same signal is applied single-ended to an external capacitor at Pin 9. There is a 90° phase shift across the plates of this capacitor, with the phase shifted signal applied to the upper port of the multiplier at Pin 8. A quadrature tank (parallel L/C network) permits frequency selective phase shifting at the IF frequency. This quadrature tank must be returned to ground through a DC blocking capacitor.

The loaded Q of the quadrature tank impacts three fundamental aspects of the detector: Distortion, maximum modulated peak deviation, and audio output amplitude. Typical quadrature curves are illustrated in Figure 10. The phase angle translates to a shift in the multiplier output voltage.

Thus a small deviation gives a large output with a high Q tank. However, as the deviation from resonance increases, the non-linearity of the curve increases (distortion), and, with too much deviation, the signal will be outside the quadrature region (limiting the peak deviation which can be demodulated). If the same peak deviation is applied to a lower Q tank, the deviation will remain in a region of the curve which is more linear (less distortion), but creates a smaller phase angle (smaller output amplitude). Thus the Q of the quadrature tank must be tailored to the design. Basic equations and an example for determining Q are shown below. This explanation includes first-order effects only.

Frequency Discriminator Design Equations for NE624

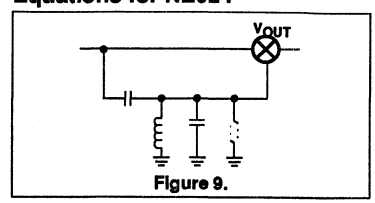


Figure 9.

$$V_O = \frac{C_S}{C_P + C_S} \bullet \frac{1}{1 + \frac{\omega_1}{Q_1 S} + \left(\frac{\omega_1}{S}\right)^2} \bullet V_{IN} \quad (1a)$$

$$\text{where } \omega_1 = \frac{1}{\sqrt{L(C_P + C_S)}} \quad (1b)$$

$$Q_1 = R\,(C_P + C_S)\,\omega_1 \quad (1c)$$

From the above equation, the phase shift between nodes 1 and 2, or the phase across C_S will be:

$$\phi = \angle V_O - \angle V_{IN} = t_g^{-1}\left[\frac{\frac{\omega_1}{Q_1 \omega}}{1 - \left(\frac{\omega_1}{\omega}\right)^2}\right] \quad (2)$$

Figure 10 is the plot of ϕ vs. $\left(\frac{\omega}{\omega_1}\right)$

It is notable that at $\omega = \omega_1$, the phase shift is $\frac{\pi}{2}$ and the response is close to a straight line with a slope of $\frac{\Delta\phi}{\Delta\omega} = \frac{2Q_1}{\omega_1}$

The signal V_O would have a phase shift of $\left[\frac{\pi}{2} - \frac{2Q_1}{\omega_1}\,\omega\right]$ with respect to the V_{IN}.

$$\text{If } V_{IN} = A \sin \omega t \Rightarrow V_O = A \quad (3)$$

$$\sin\left[\omega t + \frac{\pi}{2} - \frac{2Q_1}{\omega_1}\,\omega\right]$$

Multiplying the two signals in the mixer, and low pass filtering yields:

$$V_{IN} \bullet V_O = A^2 \sin \omega t \quad (4)$$

$$\sin\left[\omega t + \frac{\pi}{2} - \frac{2Q_1}{\omega_1}\,\omega\right]$$

after low pass filtering

$$\Rightarrow V_{OUT} = \frac{1}{2} A^2 \cos\left[\frac{\pi}{2} - \frac{2Q_1}{\omega_1}\,\omega\right] \quad (5)$$

$$= \frac{1}{2} A^2 \sin\left(\frac{2Q_1}{\omega_1}\right)\omega$$

$$V_{OUT} \propto 2Q_1 \frac{\omega_1}{\omega} = \left[2Q_1\left(\frac{\omega_1 + \Delta\omega}{\omega_1}\right)\right] \quad (6)$$

For $\frac{2Q_1\omega}{\omega_1} << \frac{\pi}{2}$

Which is discriminated FM output. (Note that $\Delta\omega$ is the deviation frequency from the carrier ω_1.

Ref. Krauss, Raab, Bastian; Solid State Radio Eng.; Wiley, 1980, p. 311. Example: At 455kHz IF, with ±5kHz FM deviation. The maximum normalized frequency will be

$$\frac{455 \pm 5kHz}{455} = 1.010 \text{ or } 0.990$$

Go to the f vs. normalized frequency curves (Figure 10) and draw a vertical straight line at $\frac{\omega}{\omega_1} = 1.01$.

The curves with Q = 100, Q = 40 are not linear, but Q = 20 and less shows better linearity for this application. Too small Q decreases the amplitude of the discriminated FM signal. (Eq. 6) ⇒ Choose a Q = 20

The internal R of the 624 is 40k. From Eq. 1c, and then 1b, it results that

$C_P + C_S = 174pF$ and $L = 0.7mH$.

A more exact analysis including the source resistance of the previous stage shows that there is a series and a parallel resonance in the phase detector tank. To make the parallel and series resonances close, and to get maximum attenuation of higher harmonics at 455kHz IF, we have found that a $C_S = 10pF$ and $C_P = 164pF$ (commercial values of 150pF or 180pF may be practical), will give the best results. A variable inductor which can be adjusted around 0.7mH should be chosen and optimized for minimum distortion. (For 10.7MHz, a value of $C_S = 1pF$ is recommended.)

Audio Outputs

Two audio outputs are provided. Both are PNP current-to-voltage converters with 55kΩ nominal internal loads. The unmuted output is always active to permit the use of signaling tones in systems such as cellular radio. The other output can be muted with 70dB typical attenuation. The two outputs have an internal 180° phase difference.

The nominal frequency response of the audio outputs is 300kHz. this response can be increased with the addition of external resistors from the output pins to ground in parallel with the internal 55k resistors, thus lowering the output time constant. Singe the output structure is a current-to-voltage converter (current is driven into the resistance, creating a voltage drop), adding external parallel resistance also has the effect of lowering the output audio amplitude and DC level.

This technique of audio bandwidth expansion can be effective in many applications such as SCA receivers and data transceivers.

Because the two outputs have a 180° phase relationship, FSK demodulation can be accomplished by applying the two output differentially across the inputs of an op amp or comparator. Once the threshold of the reference frequency (or "no-signal" condition) has been established, the two outputs will shift in opposite directions (higher or lower output voltage) as the input frequency shifts. The output of the comparator will be logic output. The choice of op amp or comparator will depend on the data rate. With high IF frequency (10MHz and above), and wide IF bandwidth (L/C filters) data rates in excess of 4Mbaud are possible.

RSSI

The "received signal strength indicator", or RSSI, of the NE624 demonstrates monotonic logarithmic output over a range of 90dB. The signal strength output is derived from the summed stage currents in the limiting amplifiers. It is essentially independent of the IF frequency. Thus, unfiltered signals at the limiter inputs, spurious products, or regenerated signals will manifest themselves as RSSI outputs. An RSSI output of greater than 250mV with no signal (or a very small signal) applied, is an indication of possible regeneration or oscillation.

In order to achieve optimum RSSI linearity, there must be a 12dB insertion loss between the first and second limiting amplifiers. With a typical 455kHz ceramic filter, there is a nominal 4dB insertion loss in the filter. An additional 6dB is lost in the interface between the filter and the input of the second limiter. A small amount of additional loss must be introduced with a typical ceramic filter. In the test circuit used for cellular radio applications (Figure 3) the optimum linearity was achieved with a 5.1kΩ resistor from the output of the first limiter (Pin 14) to the input of the interstage filter. With this resistor from Pin 14 to the filter, sensitivity of 0.25μV for 12dB SINAD was achieved. With the 3.6kΩ resistor, sensitivity was optimized at 0.22μV for 12dB SINAD with minor change in the RSSI linearity.

Any application which requires optimized RSSI linearity, such as spectrum analyzers, cellular radio, and certain types of telemetry, will require careful attention to limiter interstage component selection. This will be especially true with high IF frequencies which require insertion loss or impedance reduction for stability.

At low frequencies the RSSI makes an excellent logarithmic AC voltmeter.

For data applications the RSSI is effective as an amplitude shift keyed (ASK) data slicer. If a comparator is applied to the RSSI and the threshold set slightly above the no signal level, when an in-band signal is received the comparator will be sliced. Unlike FSK demodulation, the maximum data rate is somewhat limited. An internal capacitor limits the RSSI frequency response to about 100kHz. At high data rates the rise and fall times will not be symmetrical.

The RSSI output is a current-to-voltage converter similar to the audio outputs. However, an external resistor is required. With a 91kΩ resistor, the output characteristic is 0.5V for a 10dB change in the input amplitude.

Additional Circuitry

Internal to the NE624 are voltage and current regulators which have been temperature compensated to maintain the performance of the device over a wide temperature range. These regulators are not accessible to the user.

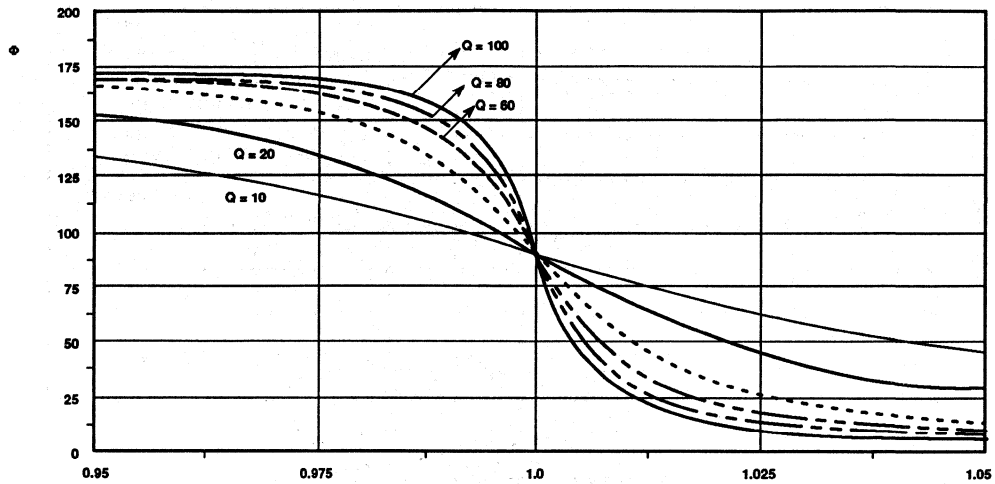


Figure 10. Phase vs Normalized IF Frequency $\frac{\omega}{\omega_1} = 1 + \frac{\Delta\omega}{\omega_1}$

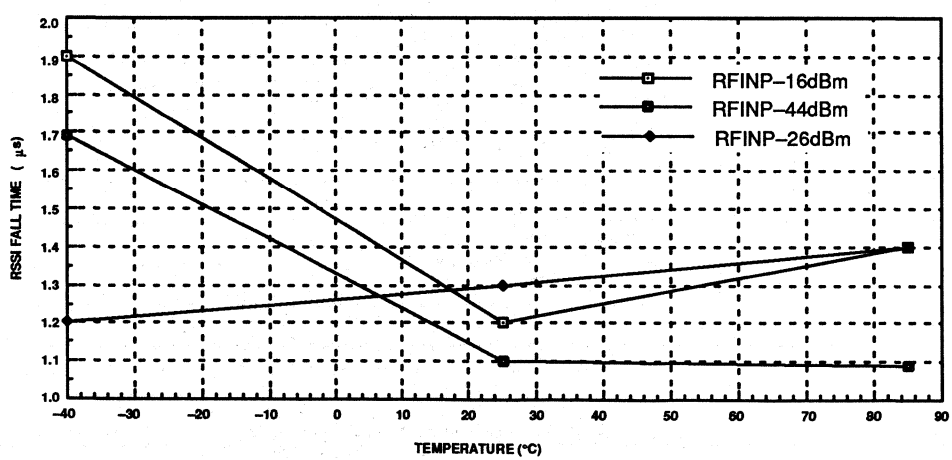


Figure 11. NE/SA624 Rise Time 455kHz IF Frequency

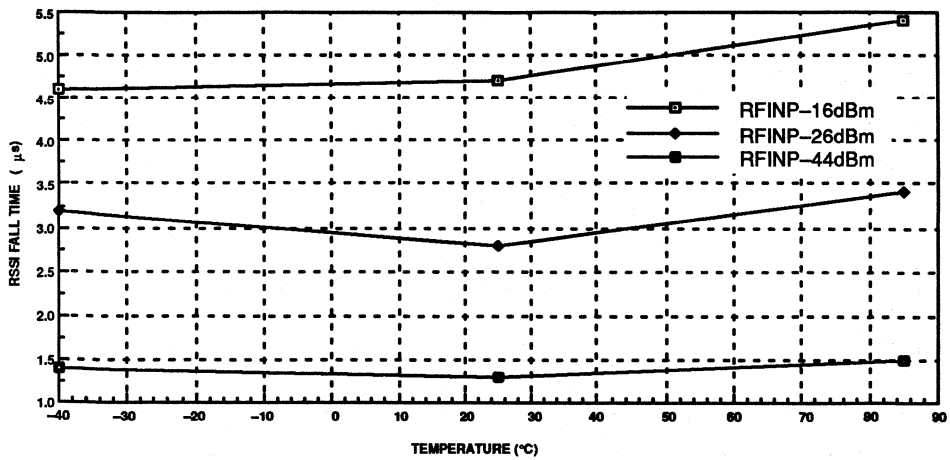


Figure 12. NE/SA624 Fall Time 455kHz IF Frequency

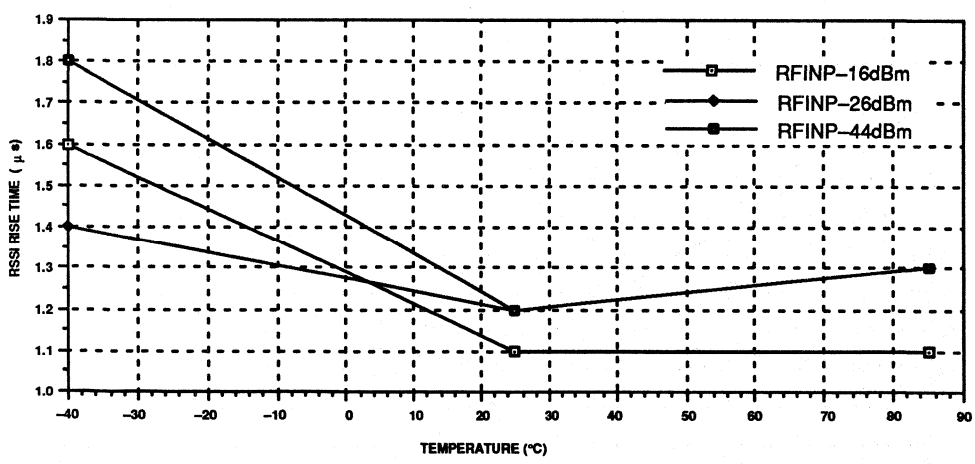


Figure 13. NE/SA624 Rise Time 10.7MHz IF Frequency

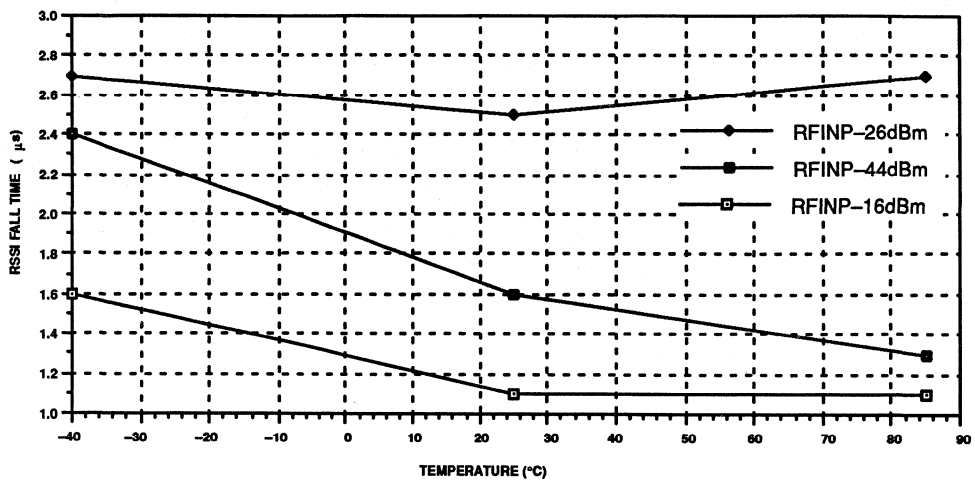


Figure 14. NE/SA624 Fall Time 10.7MHz IF Frequency

High performance low power mixer FM IF system with high-speed RSSI

NE/SA625

DESCRIPTION

The NE/SA625 is pin-to-pin compatible with the NE/SA605, but has faster RSSI rise and fall times. The NE/SA625 is a high performance monolithic low-power FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator (RSSI) with fast rise and fall time, and voltage regulator. The NE/SA625 combines the functions of Signetics' NE602A and NE624. The NE/SA625 is available in 20-lead dual-in-line plastic and 20-lead SOL (surface-mounted miniature package) and 20-lead SSOP (shrink small outline package).

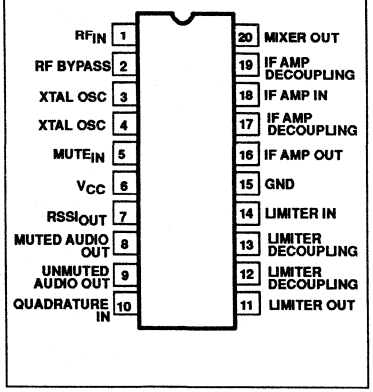
For additional technical information please refer to application notes AN1994, 1995 and 1996, which include example application diagrams, a complete overview of the product and artwork for reference.

FEATURES

- Fast RSSI rise and fall times
- Low power consumption: 5.8mA typical at 6V
- Mixer input to >500MHz
- Mixer conversion power gain of 13dB at 45MHz
- Mixer noise figure of 4.6dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator to 1GHz local oscillator can be injected)
- 102dB of IF Amp/Limiter gain
- 25MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- Two audio outputs - muted and unmuted
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.22μV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone with RF at 45MHz and IF at 455kHz
- SA625 meets cellular radio specifications
- ESD hardened

PIN CONFIGURATION

D, DK and N Packages



APPLICATIONS

- Digital cellular base stations
- High performance communications receivers
- Single conversion VHF/UHF receivers
- SCA receivers
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Wideband low current amplification
- Digital cordless telephones

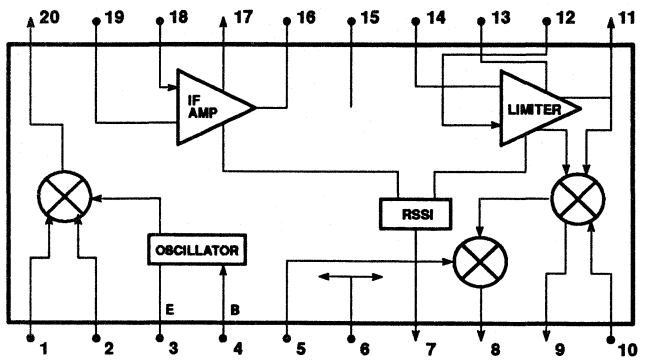
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic DIP	0 to +70°C	NE625N	0408B
20-Pin Plastic SOL (Surface-mount)	0 to +70°C	NE625D	0172D
20-Pin Plastic SSOP (Surface-mount)	0 to +70°C	NE625DK	1563
20-Pin Plastic DIP	-40 to +85°C	SA625N	0408B
20-Pin Plastic SOL (Surface-mount)	-40 to +85°C	SA625D	0172D
20-Pin Plastic SSOP (Surface-mount)	-40 to +85°C	SA625DK	1563

High performance low power mixer FM IF system with high-speed RSSI

NE/SA625

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		RATING	UNITS
V_{CC}	Single supply voltage		9	V
T_{STG}	Storage temperature range		-65 to +150	°C
T_A	Operating ambient temperature range NE625		0 to +70	°C
		SA625	-40 to +85	°C
θ_{JA}	Thermal impedance	D package	90	°C/W
		N package	75	°C/W
		DK package	117	°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE625			SA625			
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Power supply voltage range		4.5		8.0	4.5		8.0	V
I_{CC}	DC current drain		5.1	5.8	6.7	4.55	5.8	6.75	mA
	Mute switch input threshold (ON)		1.7			1.7			V
	(OFF)				1.0			1.0	V

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +6V, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step-up; IF frequency = 455kHz; R17 = 5.1k; RF level = -45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characteristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE625			SA625			
			MIN	TYP	MAX	MIN	TYP	MAX	
Mixer/Osc section (ext LO = 300mV)									
f_{IN}	Input signal frequency			500			500		MHz
f_{OSC}	Crystal oscillator frequency			150			150		MHz
	Noise figure at 45MHz			5.0			5.0		dB
	Third-order input intercept point	f1 = 45.0; f2 = 45.06MHz		-10			-10		dBm
	Conversion power gain	Matched 14.5dBV step-up	10.5	13	14.5	10	13	15	dB
		50Ω source		-1.7			-1.7		dB
	RF input resistance	Single-ended input	3.5	4.7		3.0	4.7		kΩ
	RF input capacitance			3.5	4.0		3.5	4.0	pF
	Mixer output resistance	(Pin 20)	1.3	1.5		1.25	1.5		kΩ
IF section									
	IF amp gain	50Ω source		39.7			39.7		dB
	Limiter gain	50Ω source		62.5			62.5		dB
	Input limiting -3dB, R_{17} = 5.1k	Test at Pin 18		-113			-113		dBm
	AM rejection	80% AM 1kHz	30	34	42	29	34	43	dB
	Audio level, R_{10} = 100k	15nF de-emphasis	110	150	250	80	150	260	mV_{RMS}
	Unmuted audio level, R_{11} = 100k	150pF de-emphasis		480			480		mV
	SINAD sensitivity	RF level -118dB		16			16		dB
THD	Total harmonic distortion		-35	-42		-34	-42		dB
S/N	Signal-to-noise ratio	No modulation for noise		73			73		dB
	IF RSSI output, R_9 = 100kΩ[1]	IF level = -118dBm	0	160	550	0	160	650	mV
		IF level = -68dBm	2.0	2.5	3.0	1.9	2.5	3.1	V
		IF level = -18dBm	4.1	4.8	5.5	4.0	4.8	5.6	V
	IF RSSI output rise time (10kHz pulse, no 455kHz filter) (no RSSI bypass capacitor)	IF frequency = 455kHz							
		RF level = -56dBm		1.2			1.2		µs
		RF level = -28dBm		1.2			1.2		µs
		IF frequency = 10.7MHz							
		RF level = -56dBm		1.2			1.2		µs
		RF level = -28dBm		1.1			1.1		µs
	IF RSSI output fall time (10kHz pulse, no 455kHz filter) (no RSSI bypass capacitor)	IF frequency = 455kHz							
		RF level = -56dBm		2.1			2.1		µs
		RF level = -28dBm		7.6			7.6		µs
		IF frequency = 10.7MHz							
		RF level = -56dBm		2.0			2.0		µs
		RF level = -28dBm		7.3			7.3		µs
	RSSI range	R_9 = 100kΩ Pin 16		90			90		dB
	RSSI accuracy	R_9 = 100kΩ Pin 16		±1.5			±1.5		dB
	IF input impedance		1.40	1.6		1.40	1.6		kΩ
	IF output impedance		0.85	1.0		0.85	1.0		kΩ
	Limiter intput impedance		1.40	1.6		1.40	1.6		kΩ
	Limiter output impedance			300			300		Ω
	Limiter output level with no load			280			280		mV_{RMS}

AC ELECTRICAL CHARACTERISTICS(Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE625			SA625			
			MIN	TYP	MAX	MIN	TYP	MAX	
IF section (continued)									
	Unmuted audio output resistance			58			58		kΩ
	Muted audio output resistance			58			58		kΩ
RF/IF section (Int LO)									
	Unmuted audio level	4.5V = V_{CC}, RF level = -27dBm		450			450		mV_{RMS}
	System RSSI output	4.5V = V_{CC}, RF level = -27dBm		4.3			4.3		V

NOTE:
1. The generator source impedance is 50Ω, but the NE/SA625 input impedance at Pin 18 is 1500Ω. As a result, IF level refers to the actual signal that enters the NE/SA625 input (Pin 8) which is about 21dB less than the "available power" at the generator.

CIRCUIT DESCRIPTION

The NE/SA625 is an IF signal processing system suitable for second IF or single conversion systems with input frequency as high as 1GHz. The bandwidth of the IF amplifier is about 40MHz, with 39.7dB(v) of gain from a 50Ω source. The bandwidth of the limiter is about 28MHz with about 62.5dB(v) of gain from a 50Ω source. However, the gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 5dB, conversion gain of 13dB, and input third-order intercept of -10dBm. The oscillator will operate in excess of 1GHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

The output of the mixer is internally loaded with a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor can be added between the first IF output (Pin 16) and the interstage network.

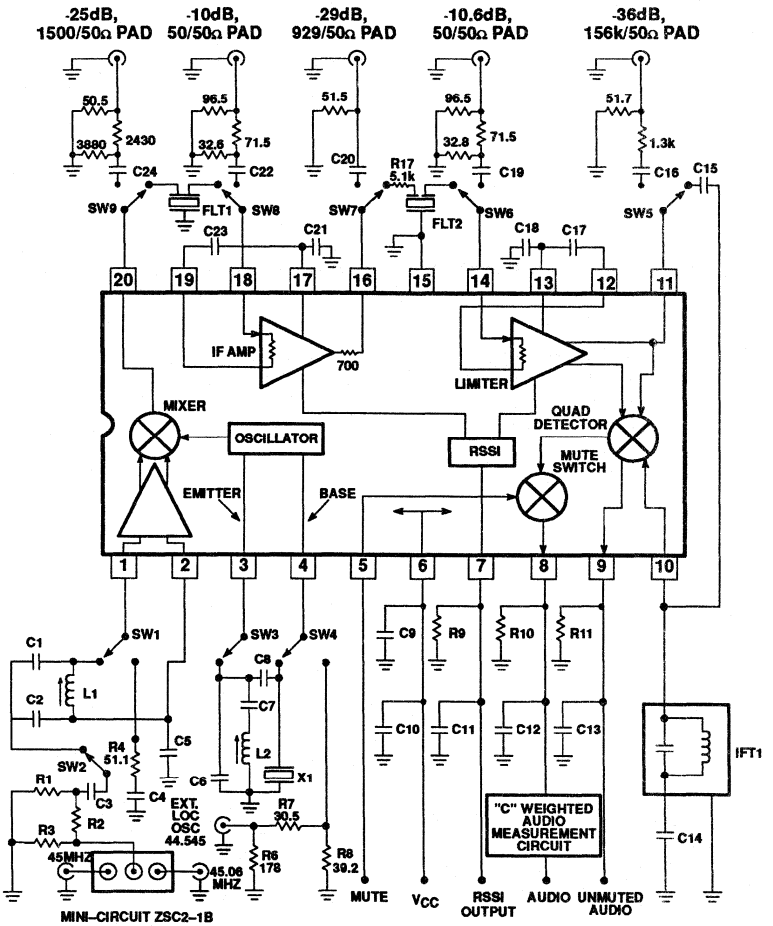
The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

Overall, the IF section has a gain of 90dB. For operation at intermediate frequencies greater than 455kHz, special care must be given to layout, termination, and interstage loss to avoid instability.

The demodulated output of the quadrature detector is available at two pins, one continuous and one with a mute switch. Signal attenuation with the mute activated is greater than 60dB. The mute input is very high impedance and is compatible with CMOS or TTL levels.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone.

NOTE: $dB(v) = 20\log V_{OUT}/V_{IN}$



Automatic Test Circuit Component List

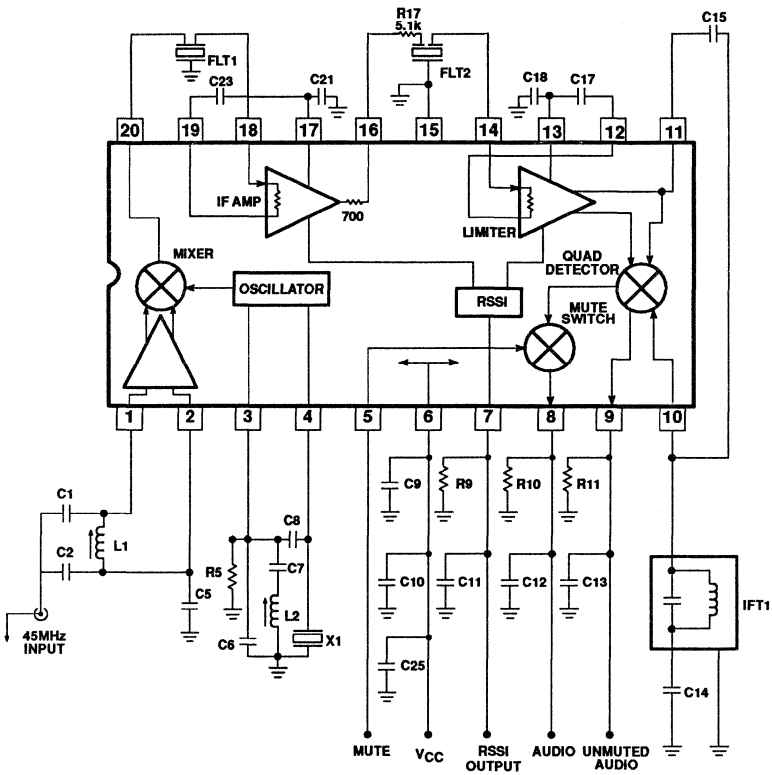
C1	100pF NPO Ceramic
C2	390pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	6.8μF Tantalum (minimum) *
C11	100nF ±10% Monolithic Ceramic
C12	15nF ±10% Ceramic
C13	150pF ±2% N1500 Ceramic
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	455kHz (Ce = 180pF) Toko RMC-2A6597H
L1	147-160nH Coilcraft UNI-10/142-04J08S
L2	0.8μH nominal Toko 292CNS-T1038Z
X1	44.545MHz Crystal ICM4712701
R9	100k ±1% 1/4W Metal Film
R17	5.1k ±5% 1/4W Carbon Composition
R10	100k ±1% 1/4W Metal Film (optional)
R11	100k ±1% 1/4W Metal Film (optional)

*NOTE: This value can be reduced when a battery is the power source.

Figure 1. NE/SA625 45MHz Test Circuit (Relays as shown)

High performance low power mixer FM IF system with high-speed RSSI

NE/SA625



Application Component List

C1	100pF NPO Ceramic
C2	390pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	6.8μF Tantalum (minimum) *
C11	100nF ±10% Monolithic Ceramic
C12	15nF ±10% Ceramic
C13	150pF ±2% N1500 Ceramic
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	455kHz (Ce = 180pF) Toko RMC–2A6597H
L1	147–160nH Coilcraft UNI–10/142–04J08S
L2	0.8μH nominal Toko 292CNS–T1038Z
X1	44.545MHz Crystal ICM4712701
R9	100k ±1% 1/4W Metal Film
R17	5.1k ±5% 1/4W Carbon Composition
R5	Not Used in Application Board (see Note 8)
R10	100k ±1% 1/4W Metal Film (optional)
R11	100k ±1% 1/4W Metal Film (optional)

*NOTE: This value can be reduced when a battery is the power source.

Figure 2. NE/SA625 45MHz Application Circuit

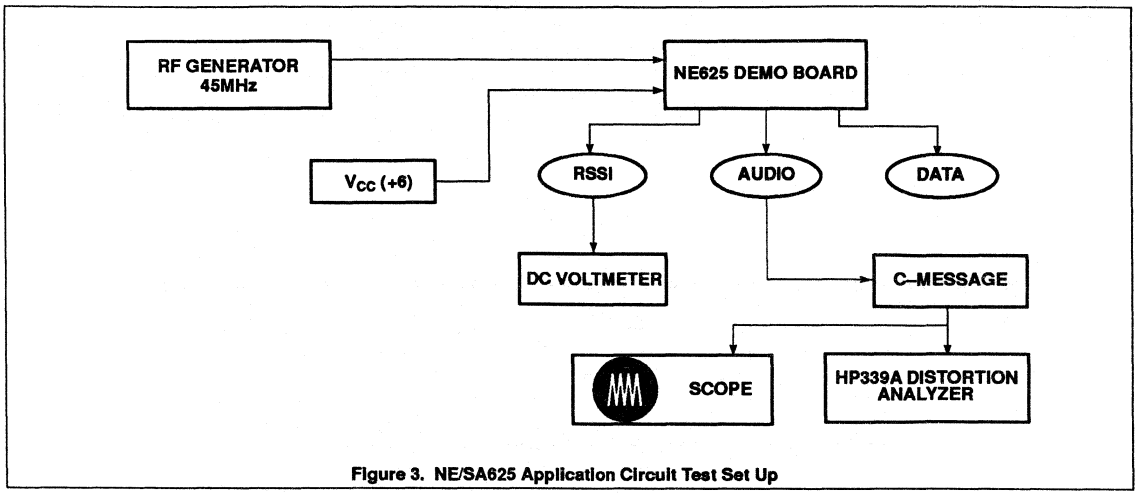


Figure 3. NE/SA625 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message filter has a peak gain of 100 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.22μV or -120dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 250mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10-15μF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1μF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2-3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 22kΩ, but should not be below 10kΩ.

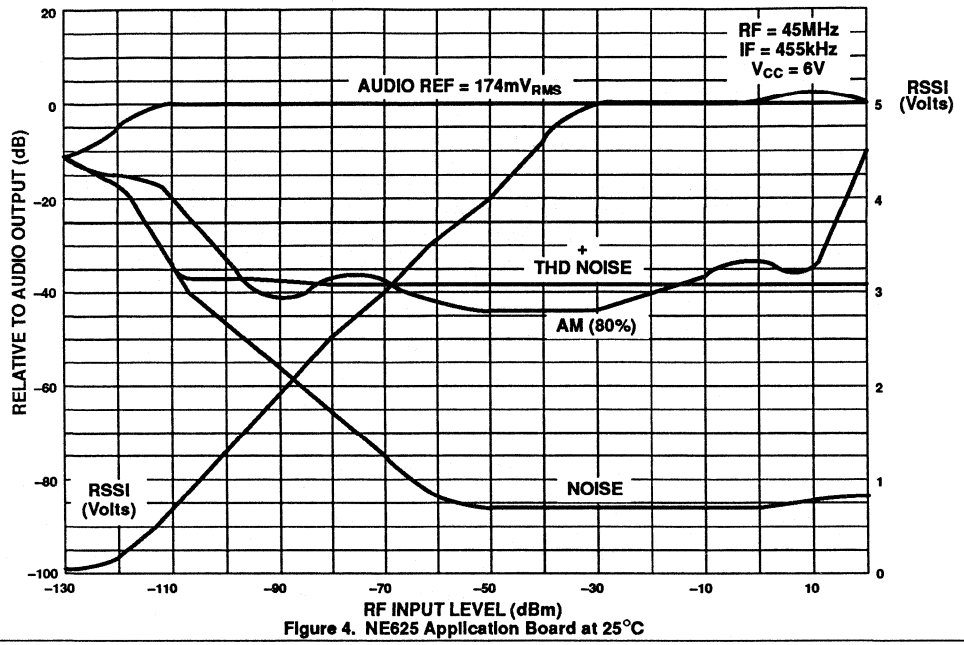


Figure 4. NE625 Application Board at 25°C

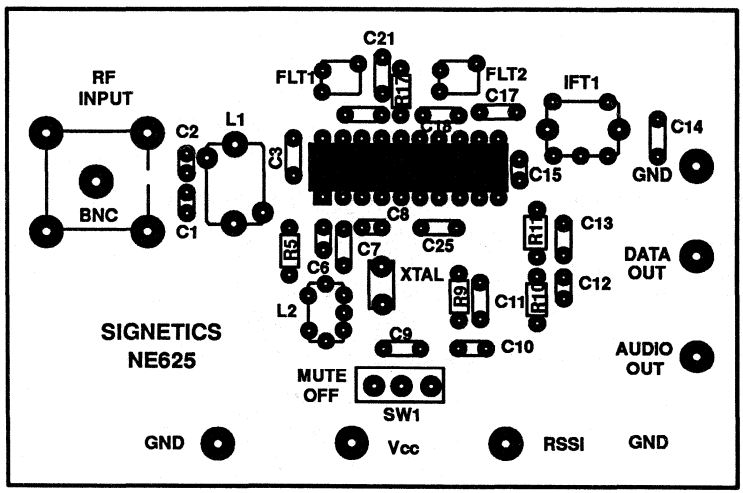
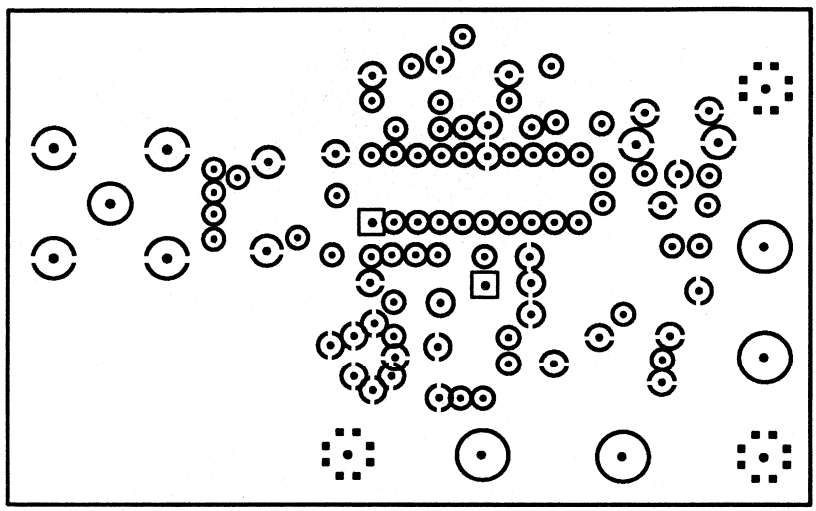
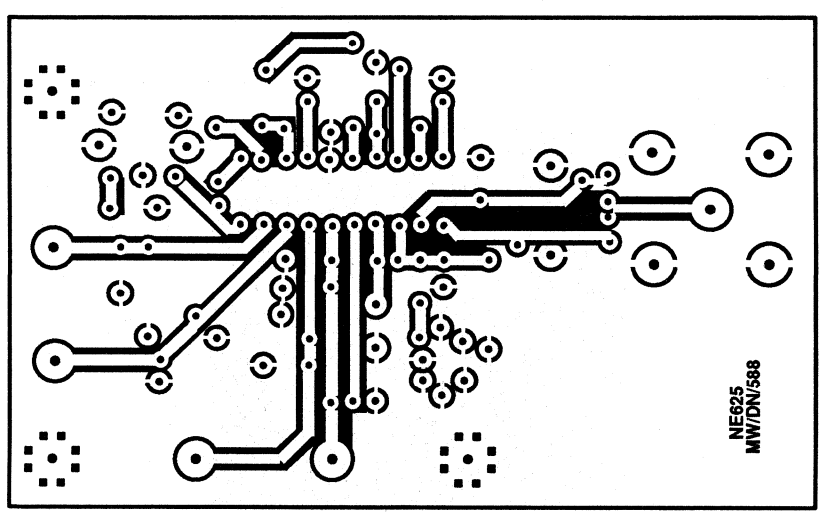


Figure 5. Component Placement for NE625 Application Circuit



TOP VIEW



BOTTOM VIEW

Figure 6. Layout for NE/SA625 Application Board

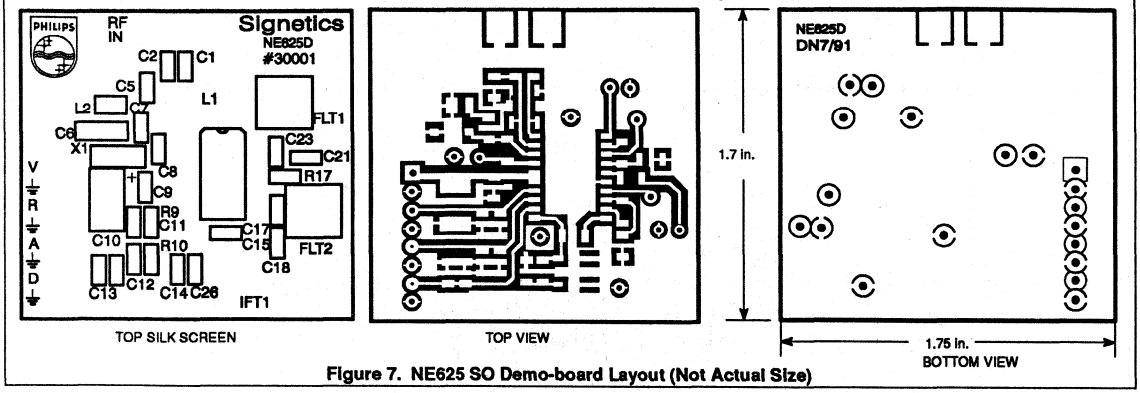


Figure 7. NE625 SO Demo-board Layout (Not Actual Size)

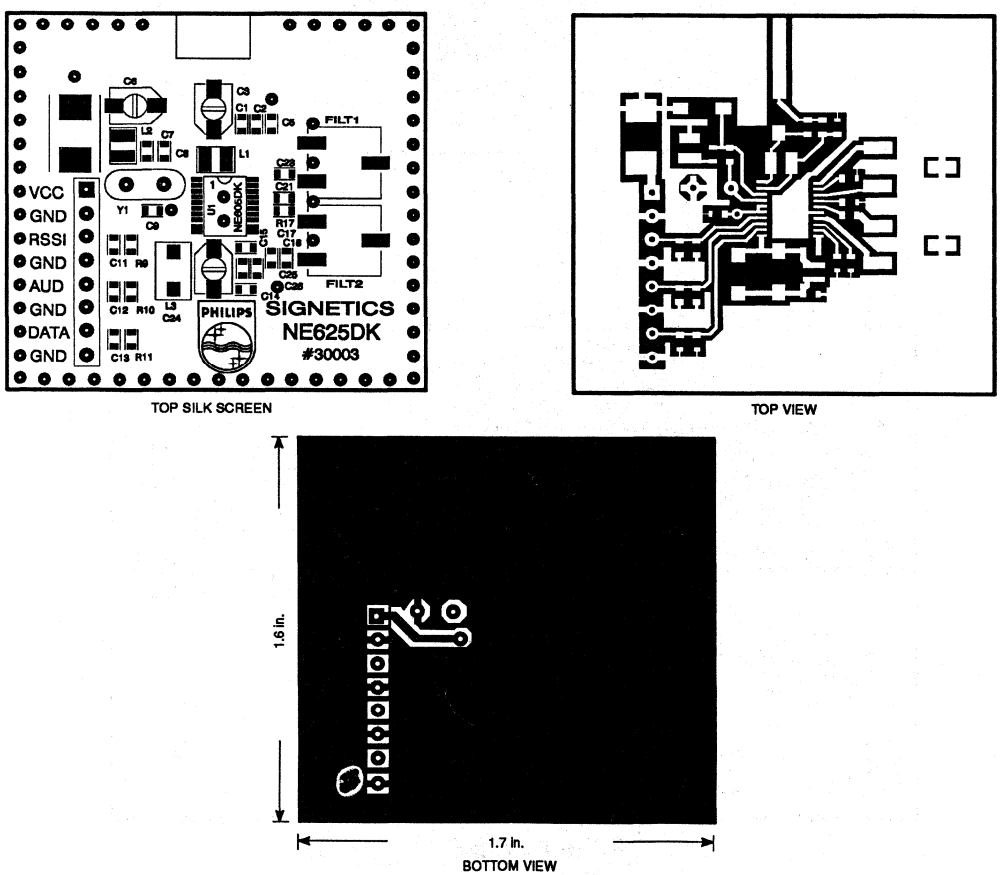


Figure 8. NE625 SSOP Demo-board Layout (Not Actual Size)

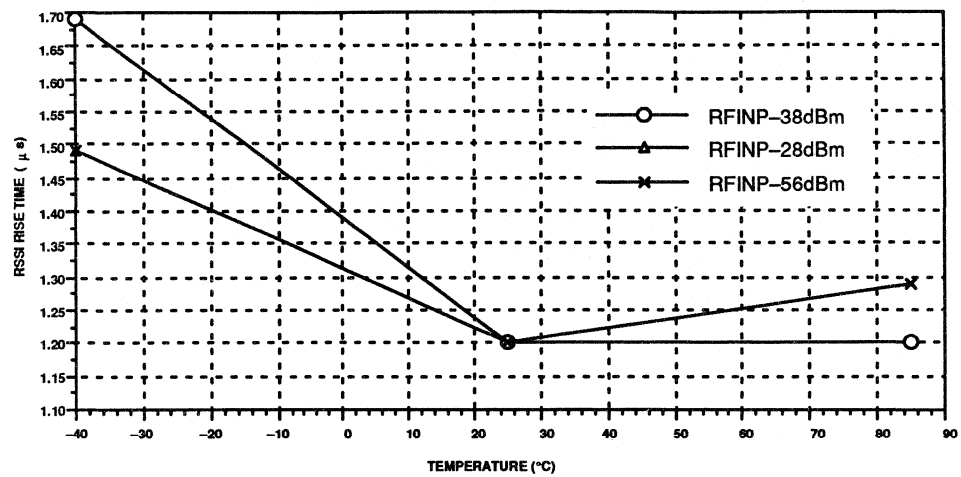


Figure 9. NE/SA625 Rise Time 455kHz IF Frequency

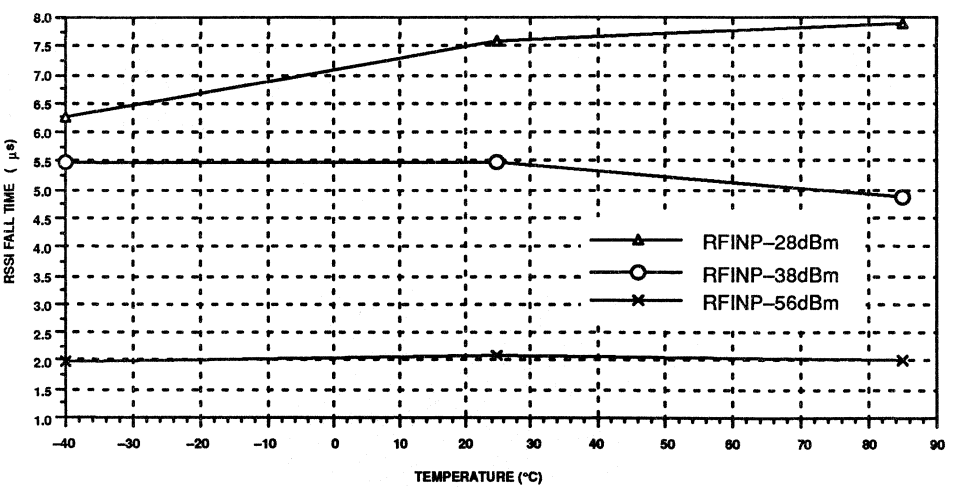


Figure 10. NE/SA625 Fall Time 455kHz IF Frequency

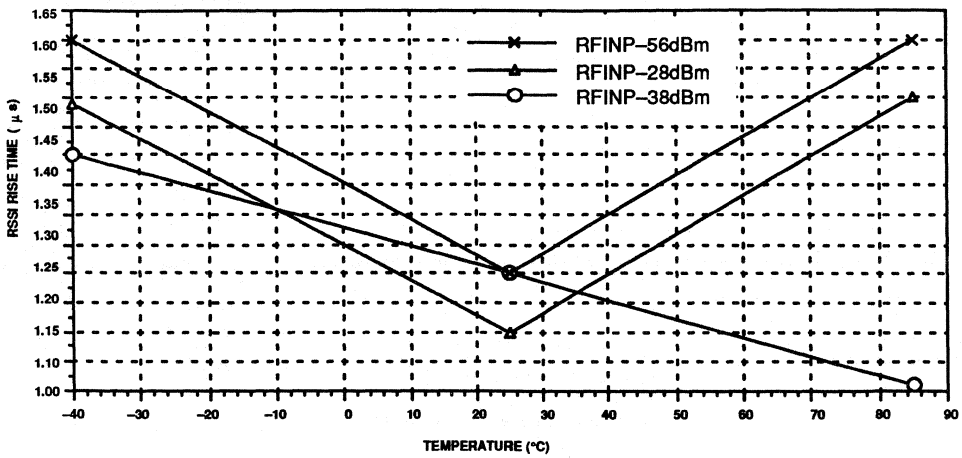


Figure 11. NE/SA625 Rise Time 10.7MHz IF Frequency

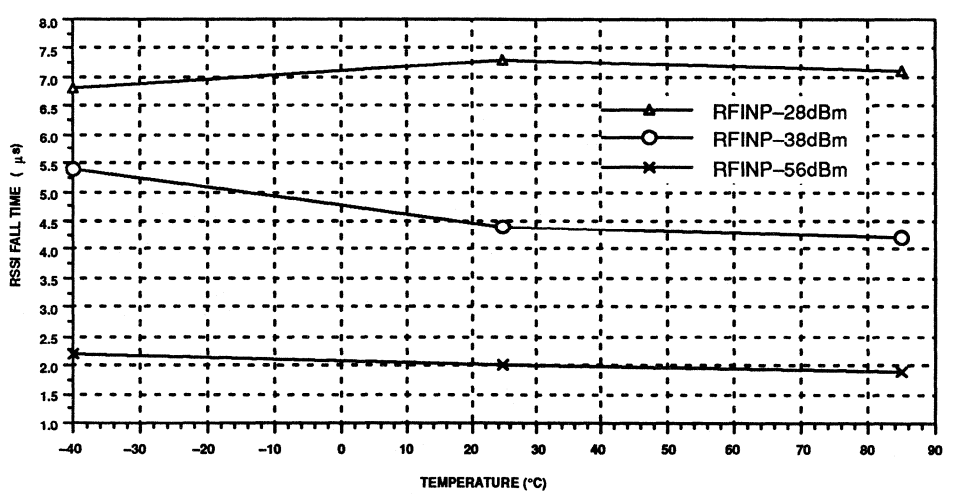


Figure 12. NE/SA625 Fall Time 10.7MHz IF Frequency

High performance low power mixer FM IF system with high-speed RSSI

NE/SA627

DESCRIPTION

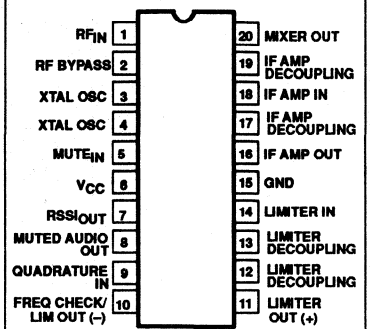
The NE/SA627 has faster RSSI rise and fall times. The NE/SA627 is a high performance monolithic low-power FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator (RSSI) with fast rise and fall time, voltage regulator and frequency check/limiter out (–). The NE/SA627 also has an extra limiter output. This signal is buffered from the output of the limiter and provides a negative (–) limiter output. This can be used to provide a frequency check function. The NE/SA627 is available in 20-lead dual-in-line plastic and 20-lead SOL (surface-mounted miniature package) and 20-lead SSOP (shrink small outline package).

FEATURES

- Fast RSSI rise and fall times
- Low power consumption: 5.8mA typical at 6V
- Mixer input to >500MHz
- Mixer conversion power gain of 13dB at 45MHz
- Mixer noise figure of 4.6dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator to 1GHz local oscillator can be injected)
- 102dB of IF Amp/Limiter gain
- 25MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- Audio output - mutable
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.22μV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone, 8kHz deviation with RF at 45MHz and IF at 455kHz
- SA627 meets cellular radio specifications
- ESD hardened

PIN CONFIGURATION

D, DK and N Packages



APPLICATIONS

- Digital cellular base stations
- High performance communications receivers
- Single conversion VHF/UHF receivers
- SCA receivers
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Wideband low current amplification
- Digital cordless telephones

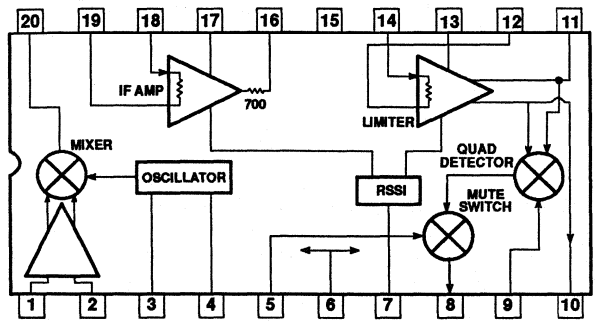
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic DIP	0 to +70°C	NE627N	0408B
20-Pin Plastic SOL (Surface-mount)	0 to +70°C	NE627D	0172D
20-Pin Plastic SSOP (Surface-mount)	0 to +70°C	NE627DK	1563
20-Pin Plastic DIP	-40 to +85°C	SA627N	0408B
20-Pin Plastic SOL (Surface-mount)	-40 to +85°C	SA627D	0172D
20-Pin Plastic SSOP (Surface-mount)	-40 to +85°C	SA627DK	1563

High performance low power mixer FM IF system with high-speed RSSI

NE/SA627

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		RATING	UNITS
V_{CC}	Single supply voltage		9	V
T_{STG}	Storage temperature range		-65 to +150	°C
T_A	Operating ambient temperature range	NE627	0 to +70	°C
		SA627	-40 to +85	°C
θ_{JA}	Thermal impedance	D package	90	°C/W
		N package	75	°C/W
		DK package	117	°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE627			SA627			
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Power supply voltage range		4.5		8.0	4.5		8.0	V
I_{CC}	DC current drain		5.1	5.8	6.7	4.55	5.8	6.75	mA
	Mute switch input threshold (ON)		1.7			1.7			V
	(OFF)				1.0			1.0	V

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +6V, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step-up; IF frequency = 455kHz; R17 = 5.1k; RF level = -45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE627			SA627			
			MIN	TYP	MAX	MIN	TYP	MAX	
Mixer/Osc section (ext LO = 300mV)									
f_{IN}	Input signal frequency			500			500		MHz
f_{OSC}	Crystal oscillator frequency			150			150		MHz
	Noise figure at 45MHz			5.0			5.0		dB
	Third-order input intercept point	f1 = 45.0; f2 = 45.06MHz		-10			-10		dBm
	Conversion power gain	Matched 14.5dBV step-up	10.5	13	14.5	10	13	15	dB
		50Ω source		-1.7			-1.7		dB
	RF input resistance	Single-ended input	3.5	4.7		3.0	4.7		kΩ
	RF input capacitance			3.5	4.0		3.5	4.0	pF
	Mixer output resistance	(Pin 20)	1.3	1.5		1.25	1.5		kΩ
IF section									
	IF amp gain	50Ω source		39.7			39.7		dB
	Limiter gain	50Ω source		62.5			62.5		dB
	Input limiting -3dB, R_{17} = 5.1k	Test at Pin 18		-113			-113		dBm
	AM rejection	80% AM 1kHz	30	34	42	29	34	43	dB
	Audio level, R_{10} = 100k	15nF de-emphasis	110	150	250	80	150	260	mV_{RMS}
	SINAD sensitivity	RF level -118dB		16			16		dB
THD	Total harmonic distortion		-35	-42		-34	-42		dB
S/N	Signal-to-noise ratio	No modulation for noise		73			73		dB
	IF RSSI output, R_9 = 100kΩ[1]	IF level = -118dBm	0	160	550	0	160	650	mV
		IF level = -68dBm	2.0	2.5	3.0	1.9	2.5	3.1	V
		IF level = -18dBm	4.1	4.8	5.5	4.0	4.8	5.6	V
	IF RSSI output rise time (10kHz pulse, no 455kHz filter) (no RSSI bypass capacitor)	IF frequency = 455kHz							
		RF level = -56dBm		1.2			1.2		µs
		RF level = -28dBm		1.2			1.2		µs
		IF frequency = 10.7MHz							
		RF level = -56dBm		1.2			1.2		µs
		RF level = -28dBm		1.1			1.1		µs
	IF RSSI output fall time (10kHz pulse, no 455kHz filter) (no RSSI bypass capacitor)	IF frequency = 455kHz							
		RF level = -56dBm		2.1			2.1		µs
		RF level = -28dBm		7.6			7.6		µs
		IF frequency = 10.7MHz							
		RF level = -56dBm		2.0			2.0		µs
		RF level = -28dBm		7.3			7.3		µs
	RSSI range	R_9 = 100kΩ Pin 16		90			90		dB
	RSSI accuracy	R_9 = 100kΩ Pin 16		±1.5			±1.5		dB
	IF input impedance		1.40	1.6		1.40	1.6		kΩ
	IF output impedance		0.85	1.0		0.85	1.0		kΩ
	Limiter input impedance		1.40	1.6		1.40	1.6		kΩ
	Limiter output impedance	Pin 10 or 11		300			300		Ω
	Limiter output level	Pin 10 or 11 with no load 3kΩ load (min)		280 250			280 250		mV_{RMS}

AC ELECTRICAL CHARACTERISTICS(Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNITS
			NE627			SA627			
			MIN	TYP	MAX	MIN	TYP	MAX	
IF section (continued)									
	Muted audio output resistance			58			58		kΩ
RF/IF section (Int LO)									
	System RSSI output	4.5V = V_{CC}, RF level = -27dBm		4.3			4.3		V

NOTE:
1. The generator source impedance is 50Ω, but the NE/SA627 input impedance at Pin 18 is 1500Ω. As a result, IF level refers to the actual signal that enters the NE/SA627 input (Pin 8) which is about 21dB less than the "available power" at the generator.

CIRCUIT DESCRIPTION

The NE/SA627 is an IF signal processing system suitable for second IF or single conversion systems with input frequency as high as 1GHz. The bandwidth of the IF amplifier is about 40MHz, with 39.7dB(v) of gain from a 50Ω source. The bandwidth of the limiter is about 28MHz with about 62.5dB(v) of gain from a 50Ω source. However, the gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 5dB, conversion gain of 13dB, and input third-order intercept of -10dBm. The oscillator will operate in excess of 1GHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

The output of the mixer is internally loaded with a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor can be added between the first IF output (Pin 16) and the interstage network.

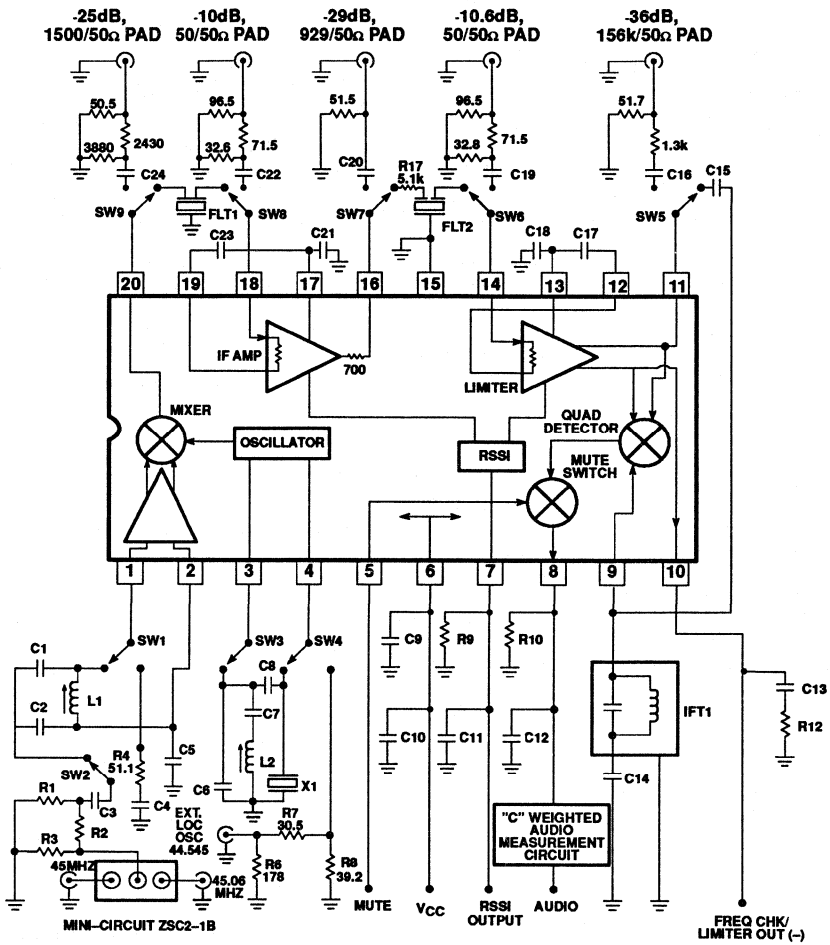
The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

Overall, the IF section has a gain of 90dB. For operation at intermediate frequencies greater than 455kHz, special care must be given to layout, termination, and interstage loss to avoid instability.

The demodulated output of the quadrature detector is available at two pins, one continuous and one with a mute switch. Signal attenuation with the mute activated is greater than 60dB. The mute input is very high impedance and is compatible with CMOS or TTL levels.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone.

NOTE: dB(v) = 20log V_{OUT}/V_{IN}

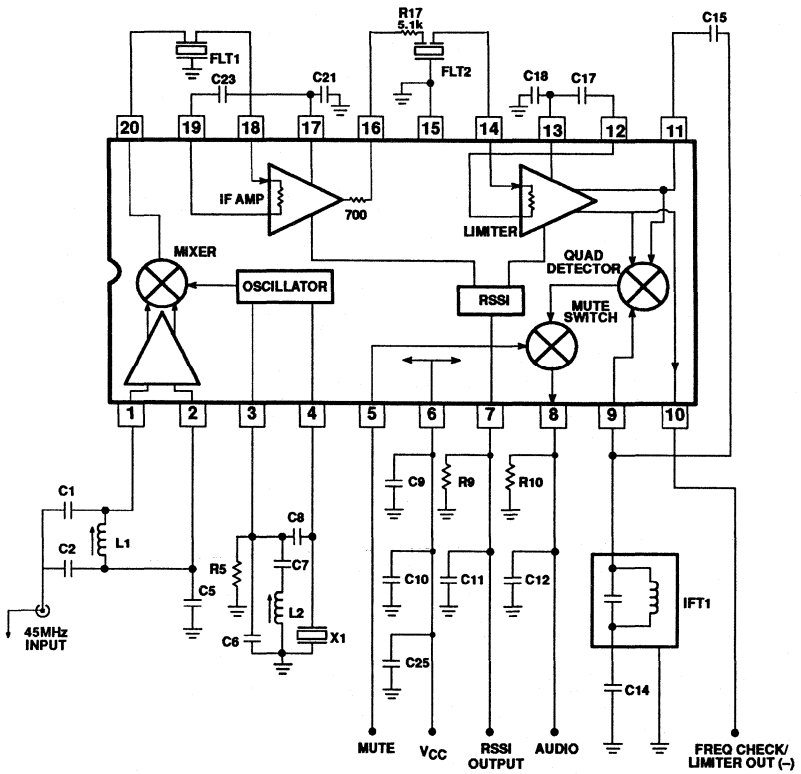


Automatic Test Circuit Component List

C1	100pF NPO Ceramic	C21	100nF ±10% Monolithic Ceramic
C2	390pF NPO Ceramic	C23	100nF ±10% Monolithic Ceramic
C5	100nF ±10% Monolithic Ceramic	C25	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic	Flt 1	Ceramic Filter Murata SFG455A3 or equiv
C7	1nF Ceramic	Flt 2	Ceramic Filter Murata SFG455A3 or equiv
C8	10.0pF NPO Ceramic	IFT 1	455kHz (Ce = 180pF) Toko RMC–2A6597H
C9	100nF ±10% Monolithic Ceramic	L1	147–160nH Coilcraft UNI–10/142–04J08S
C10	10μF Tantalum (minimum)	L2	0.8μH nominal Toko 292CNS–T1038Z
C11	100nF ±10% Monolithic Ceramic	X1	44.545MHz Crystal ICM4712701
C12	15nF ±10% Ceramic	R9	100k ±1% 1/4W Metal Film
C13	0.1μF ±10% Monolithic Ceramic	R17	5.1k ±5% 1/4W Carbon Composition
C14	100nF ±10% Monolithic Ceramic	R10	100k ±1% 1/4W Metal Film (optional)
C15	10pF NPO Ceramic	R11	100k ±1% 1/4W Metal Film (optional)
C17	100nF ±10% Monolithic Ceramic	R12	3kΩ ±5% 1/4W Metal Film (optional)
C18	100nF ±10% Monolithic Ceramic		

*NOTE: This value can be reduced when a battery is the power source.

Figure 1. NE/SA627 45MHz Test Circuit (Relays as shown)



Application Component List

C1	100pF NPO Ceramic
C2	390pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	10μF Tantalum (minimum) *
C11	100nF ±10% Monolithic Ceramic
C12	15nF ±10% Ceramic
C13	150pF ±2% N1500 Ceramic
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	455kHz (Ce = 180pF) Toko RMC–2A6597H
L1	147–160nH Coilcraft UNI–10/142–04J08S
L2	0.8μH nominal Toko 292CNS–T1038Z
X1	44.545MHz Crystal ICM4712701
R9	100k ±1% 1/4W Metal Film
R17	5.1k ±5% 1/4W Carbon Composition
R5	Not Used in Application Board (see Note 8)
R10	100k ±1% 1/4W Metal Film (optional)
R11	100k ±1% 1/4W Metal Film (optional)

*NOTE: This value can be reduced when a battery is the power source.

Figure 2. NE/SA627 45MHz Application Circuit

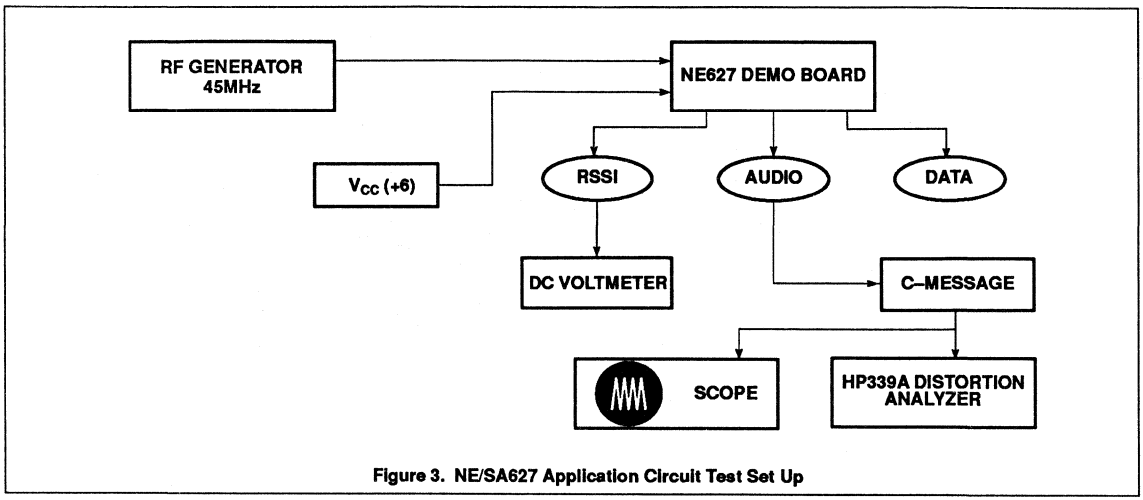


Figure 3. NE/SA627 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message filter has a peak gain of 100 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.22μV or -120dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 250mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10-15μF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1μF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2-3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 22kΩ, but should not be below 10kΩ.

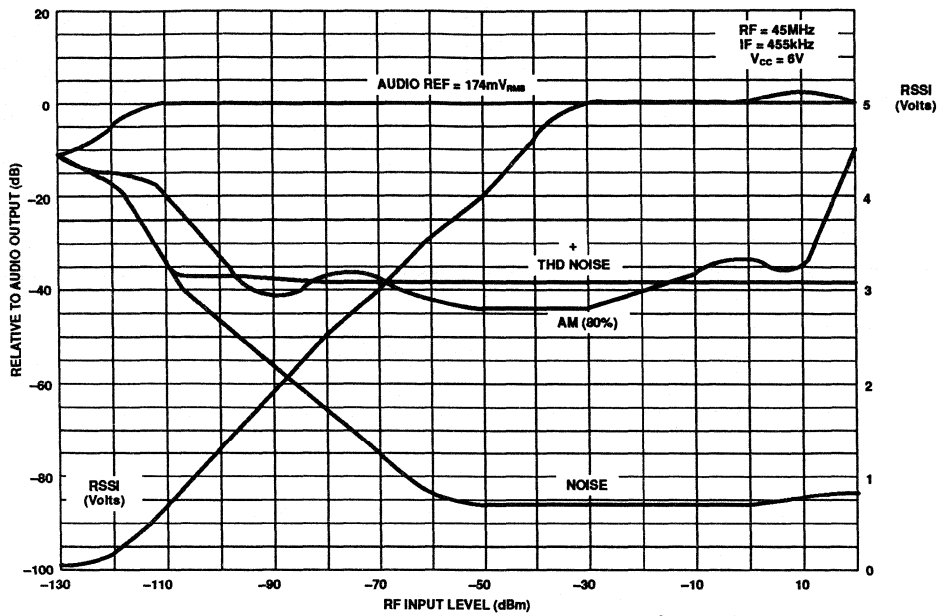


Figure 4. NE627 Application Board at 25°C

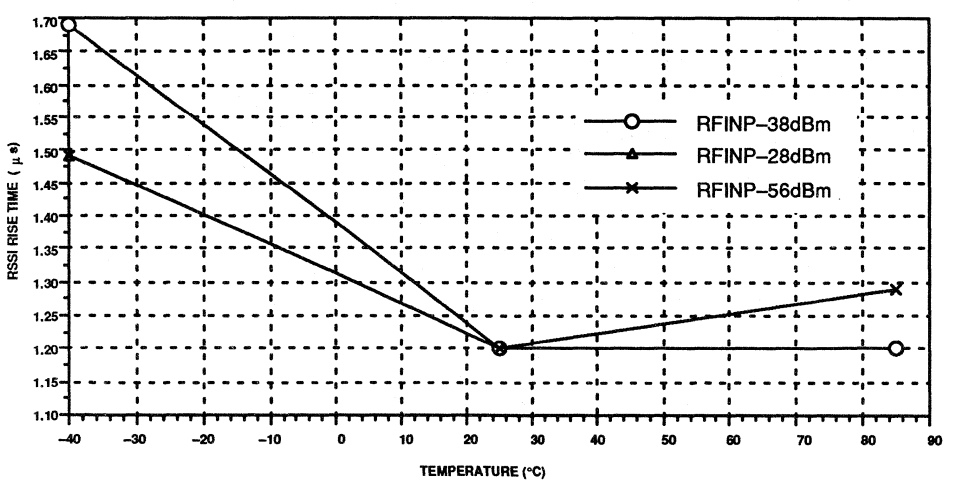


Figure 5. NE/SA627 Rise Time 455kHz IF Frequency

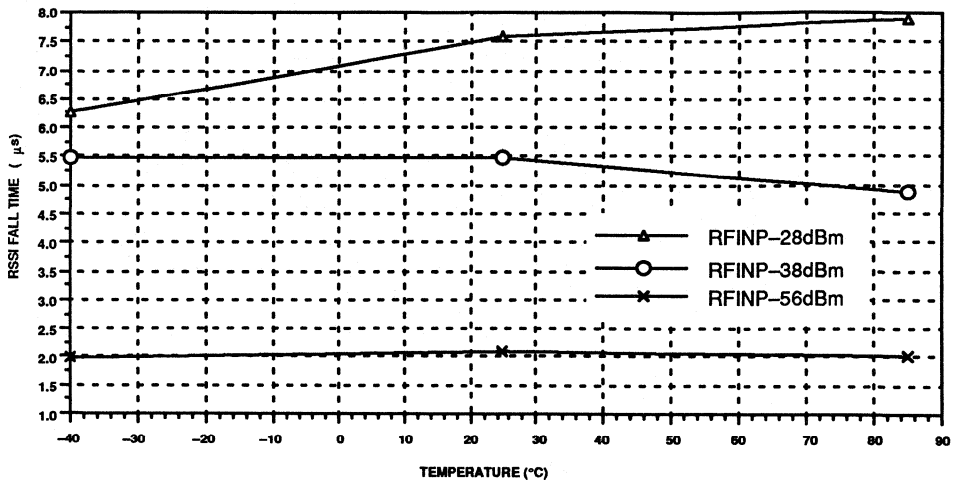


Figure 6. NE/SA627 Fall Time 455kHz IF Frequency

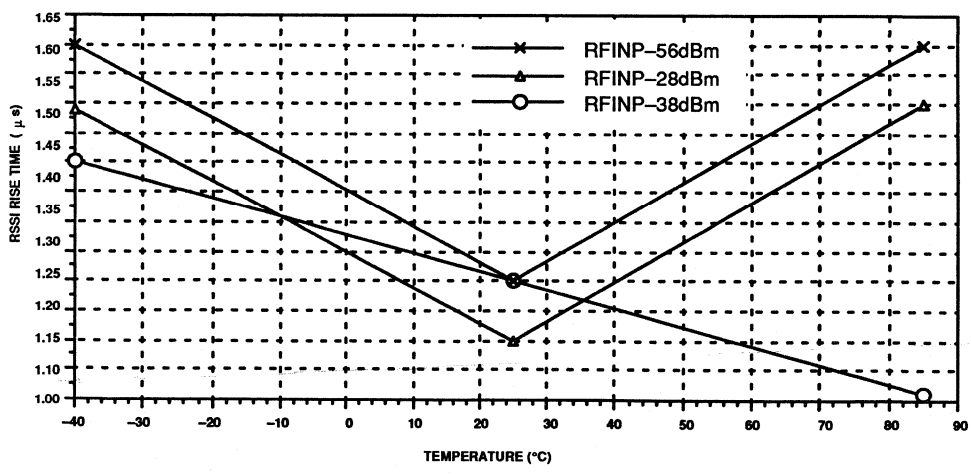


Figure 7. NE/SA627 Rise Time 10.7MHz IF Frequency

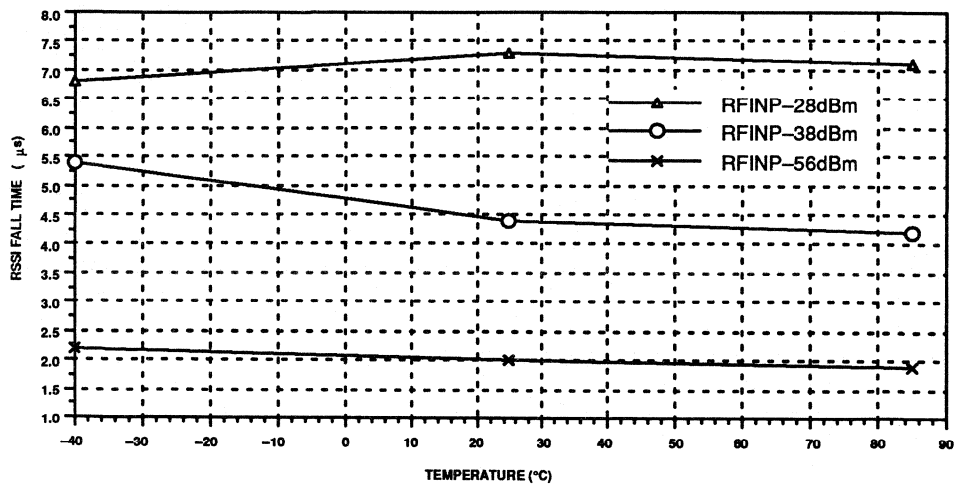


Figure 8. NE/SA627 Fall Time 10.7MHz IF Frequency

Single pole double throw (SPDT) switch

NE/SA630

DESCRIPTION

The NE630 is a wideband RF switch fabricated in BiCMOS technology and incorporating on-chip CMOS/TTL compatible drivers. Its primary function is to switch signals in the frequency range DC - 1GHz from one 50Ω channel to another. The switch is activated by a CMOS/TTL compatible signal applied to the enable channel 1 pin (ENCH1).

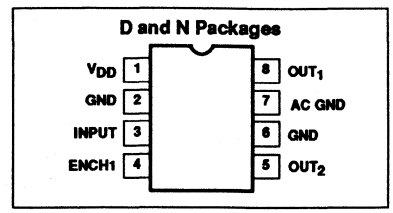
The extremely low current consumption makes the NE/SA630 ideal for portable applications. The excellent isolation and low loss makes this a suitable replacement for PIN diodes.

The NE/SA630 is available in an 8-pin dual in-line plastic package and an 8-pin SO (surface mounted miniature) package.

FEATURES

- Wideband (DC - 1GHz)
- Low through loss (1dB typical at 200MHz)
- Unused input is terminated internally in 50Ω
- Excellent overload capability (1dB gain compression point +18dBm at 300MHz)
- Low DC power (170μA from 5V supply)
- Fast switching (20ns typical)
- Good isolation (off channel isolation 60dB at 100MHz)
- Low distortion (IP_3 intercept +33dBm)
- Good 50Ω match (return loss 18dB at 400MHz)
- Full ESD protection
- Bidirectional operation

PIN CONFIGURATION



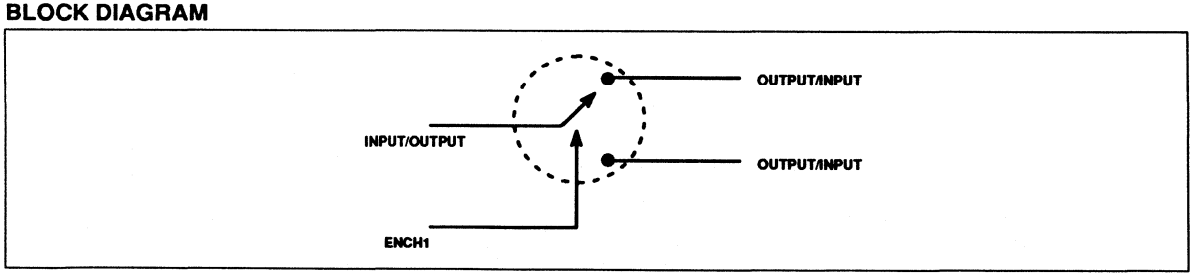
APPLICATIONS

- Digital transceiver front-end switch
- Antenna switch
- Filter selection
- Video switch
- FSK transmitter

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to 70°C	NE630N
8-Pin Plastic SO (Surface-mount)	0 to 70°C	NE630D
8-Pin Plastic DIP	-40 to +85°C	SA630N
8-Pin Plastic SO (Surface-mount)	-40 to +85°C	SA630D

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{DD}	Supply voltage	-0.5 to +5.5	V
P_D	Power dissipation, T_A = 25°C (still air)[1] 8-Pin Plastic DIP 8-Pin Plastic SO	 1160 780	 mW mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power input/output	+20	dBm
T_{STG}	Storage temperature range	-65 to +150	°C

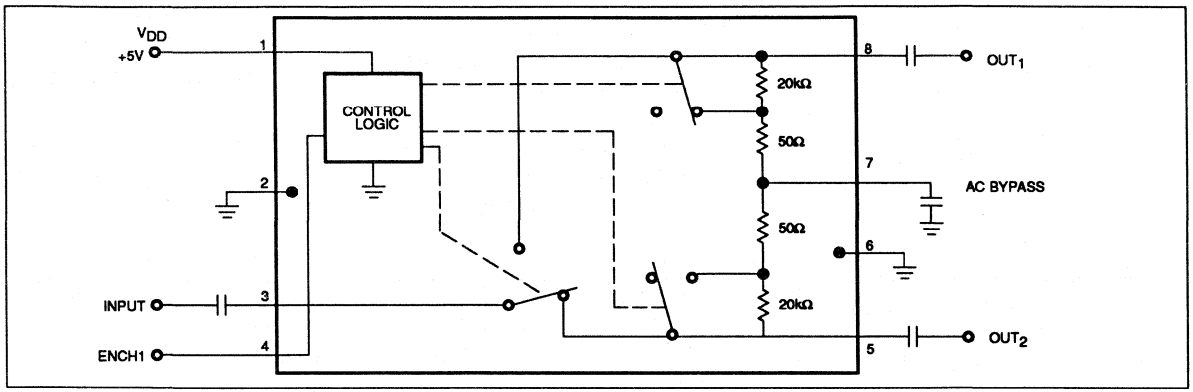
NOTES:

1. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}:
   8-Pin DIP: θ_{JA} = 108°C/W
   8-Pin SO: θ_{JA} = 158°C/W

Single pole double throw (SPDT) switch

NE/SA630

EQUIVALENT CIRCUIT



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{DD}	Supply voltage	3.0 to 5.5V	V
T_A	Operating ambient temperature range NE Grade SA Grade	 0 to +70 -40 to +85	 °C °C
T_J	Operating junction temperature range NE Grade SA Grade	 0 to +90 -40 to +105	 °C °C

DC ELECTRICAL CHARACTERISTICS

V_{DD} = +5V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA630			
			MIN	TYP	MAX	
I_{DD}	Supply current		40	170	300	µA
V_T	TTL/CMOS logic threshold voltage[1]		1.1	1.25	1.4	V
V_{IH}	Logic 1 level	Enable channel 1	2.0		V_{DD}	V
V_{IL}	Logic 0 level	Enable channel 2	-0.3		0.8	V
I_{IL}	ENCH1 input current	ENCH1 = 0.4V	-1	0	1	µA
I_{IH}	ENCH1 input current	ENCH1 = 2.4V	-1	0	1	µA

NOTE:
1. The ENCH1 input must be connected to a valid Logic Level for proper operation of the NE/SA630.

AC ELECTRICAL CHARACTERISTICS[1] - D PACKAGE

V_{DD} = +5V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS NE/SA630 MIN	LIMITS NE/SA630 TYP	LIMITS NE/SA630 MAX	UNITS
S_{21}, S_{12}	Insertion loss (ON channel)	DC - 100MHz 500MHz 900MHz		1 1.4 2	 2.8	dB
S_{21}, S_{12}	Isolation (OFF channel)[2]	10MHz 100MHz 500MHz 900MHz	70 24	80 60 50 30	 	dB
S_{11}, S_{22}	Return loss (ON channel)	DC - 400MHz 900MHz		20 12	 	dB
S_{11}, S_{22}	Return loss (OFF channel)	DC - 400MHz 900MHz		17 13	 	dB
t_D	Switching speed (on-off delay)	50% TTL to 90/10% RF		20		ns
t_r, t_f	Switching speeds (on-off rise/fall time)	90%/10% to 10%/90% RF		5		ns
	Switching transients			165		mV_{P-P}
P_{-1dB}	1dB gain compression	DC - 1GHz		+18		dBm
IP_3	Third-order intermodulation intercept	100MHz		+33		dBm
IP_2	Second-order intermodulation intercept	100MHz		+52		dBm
NF	Noise figure (Z_O = 50Ω)	100MHz 900MHz		1.0 2.0		dB

NOTE:
1. All measurements include the effects of the D package NE/SA630 Evaluation Board (see Figure 1B). Measurement system impedance is 50Ω.
2. The placement of the AC bypass capacitor is critical to achieve these specifications. See the applications section for more details.

AC ELECTRICAL CHARACTERISTICS[1] - N PACKAGE

V_{DD} = +5V, T_A = 25°C; all other characteristics similar to the D-Package, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS NE/SA630 MIN	LIMITS NE/SA630 TYP	LIMITS NE/SA630 MAX	UNITS
S_{21}, S_{12}	Insertion loss (ON channel)	DC - 100MHz 500MHz 900MHz		1 1.4 2.5		dB
S_{21}, S_{12}	Isolation (OFF channel)	10MHz 100MHz 500MHz 900MHz	58	68 50 37 15		dB
NF	Noise figure (Z_O = 50Ω)	100MHz 900MHz		1.0 2.5		dB

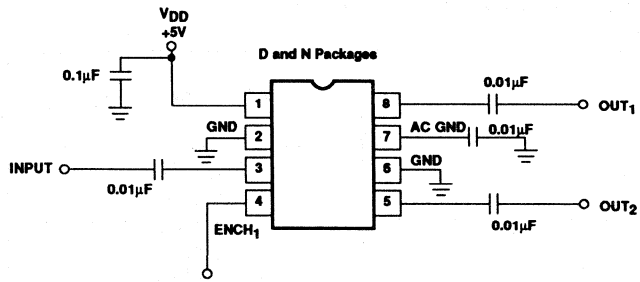
NOTE:
1. All measurements include the effects of the N package NE/SA630 Evaluation Board (see Figure 1C). Measurement system impedance is 50Ω.

APPLICATIONS

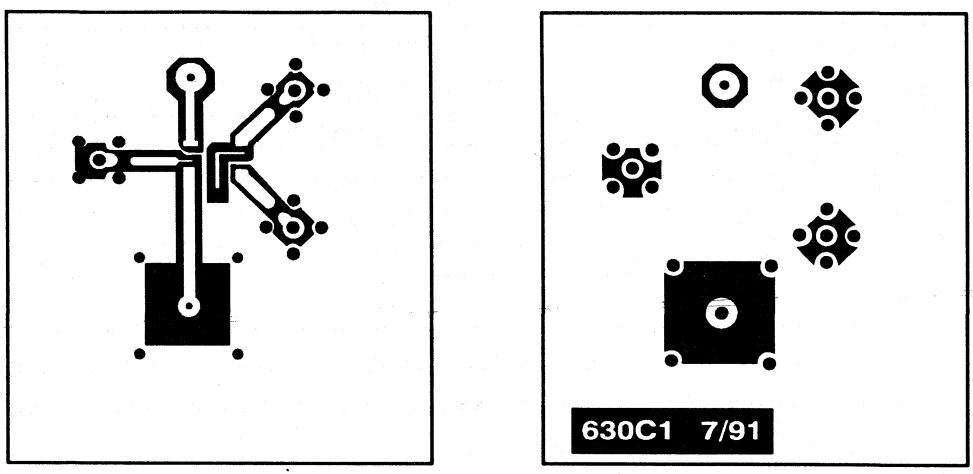
The typical applications schematic and printed circuit board layout of the NE/SA630 evaluation board is shown in Figure 1. The layout of the board is simple, but a few cautions need to be observed. The input and output traces should be 50Ω. The placement of the AC bypass capacitor is *extremely critical* if a symmetric isolation between the two channels is desired. The trace from Pin 7 should be drawn back towards the package and then be routed downwards. The capacitor should be placed straight down as close to the device as practical. For better isolation between the two channels at higher frequencies, it is also advisable to run the two output/input traces at an angle. This also minimizes any inductive coupling between the two traces. The power supply bypass capacitor should be placed close to the device. Figure 7 shows the frequency response of the NE/SA630. The loss matching between the two channels is excellent to 1.2GHz as shown in

Single pole double throw (SPDT) switch

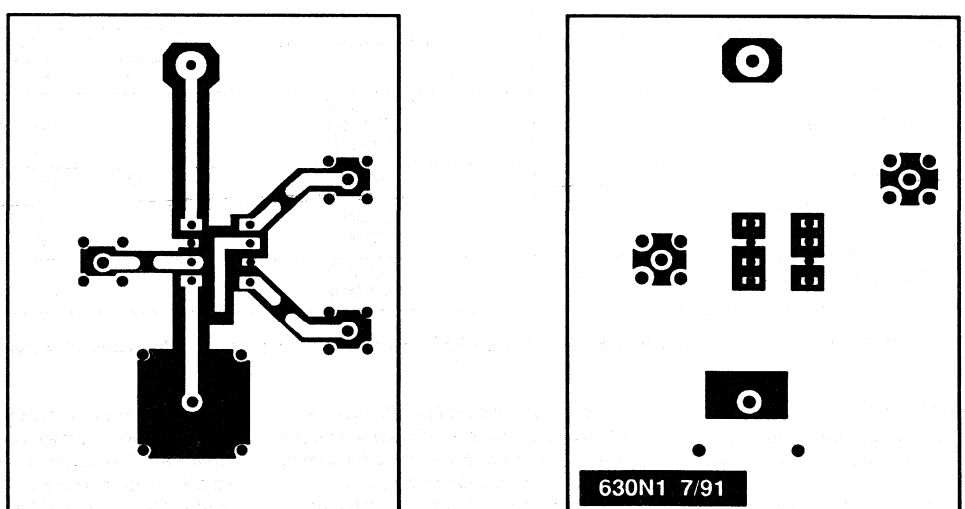
NE/SA630



a. NE/SA Evaluation Board Schematic



b. NE/SA630 D-Package Board Layout



c. NE/SA630 N-Package Board Layout

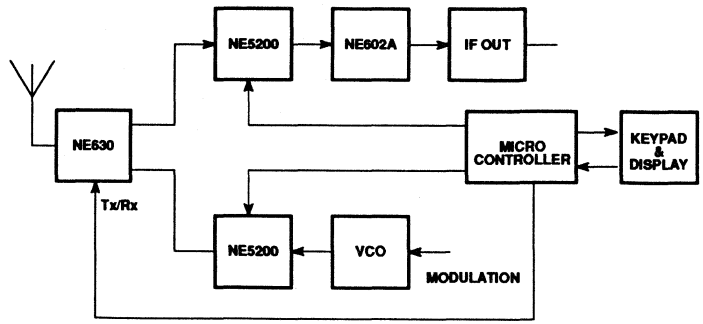
Figure 1

Figure 10. The isolation and matching of the two channels over frequency is shown in Figure 12 and Figure 14, respectively.

The NE630 is a very versatile part and can be used in many applications. Figure 2 shows a block diagram of a typical Digital RF transceiver front-end. In this application the NE630 replaces the duplexer which is typically very bulky and lossy. Due to the low power consumption of the device, it is ideally suited for handheld applications such as in CT2 cordless telephones. The NE630 can also be used to generate Amplitude Shift Keying (ASK) or On-Off Keying (OOK) and Frequency Shift Keying (FSK) signals for digital RF communications systems. Block diagrams for these applications are shown in Figure 3 and Figure 4, respectively.

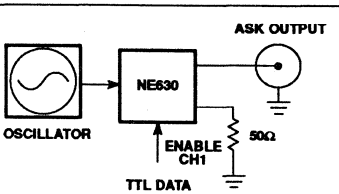
For applications that require a higher isolation at 1GHz than obtained from a single NE630, several NE630s can be cascaded as shown in Figure 5. The cascaded configuration will have a higher loss but greater than 35dB of isolation at 1GHz and greater than 65dB @ 500MHz can be obtained from this configuration. By modifying the enable control, an RF multiplexer/ de-multiplexer or antenna selector can be constructed. The simplicity of NE630 coupled with its ease of use and high performance lends itself to many innovative applications.

The NE/SA630 switch terminates the OFF channel in 50Ω. The 50Ω resistor is internal and is in series with the external AC bypass capacitor. Matching to impedances other than 50Ω can be achieved by adding a resistor in series with the AC bypass capacitor (e.g., 25Ω additional to match to a 75Ω environment).



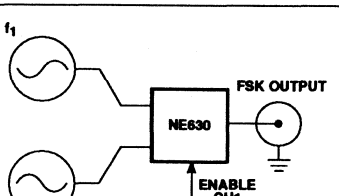
A TYPICAL TDMA/DIGITAL RF TRANSCEIVER SYSTEM FRONT-END

Figure 2



AMPLITUDE SHIFT KEYING (ASK) GENERATOR

Figure 3



FREQUENCY SHIFT KEYING (FSK) GENERATOR

Figure 4

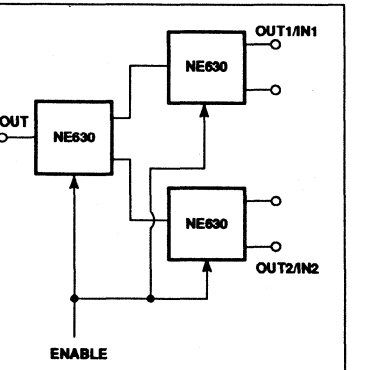


Figure 5

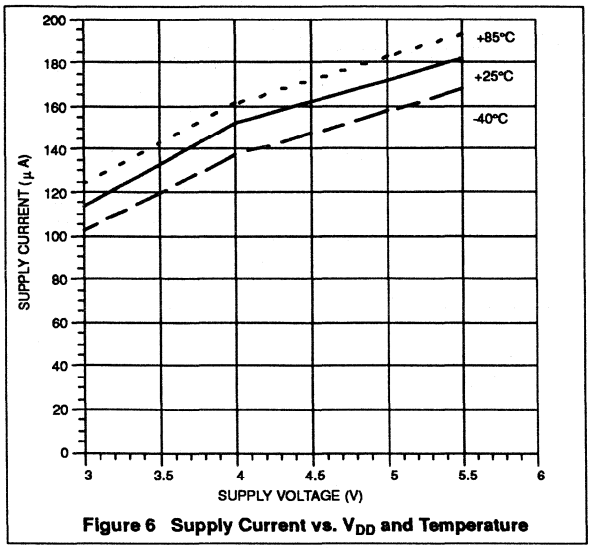


Figure 6 Supply Current vs. V_{DD} and Temperature

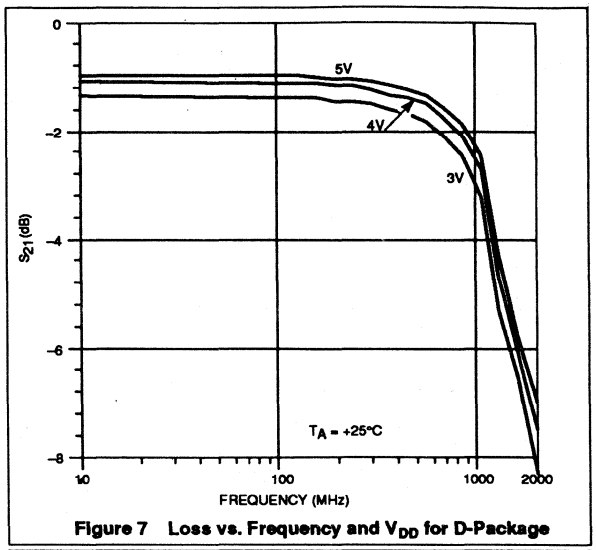


Figure 7 Loss vs. Frequency and V_{DD} for D-Package

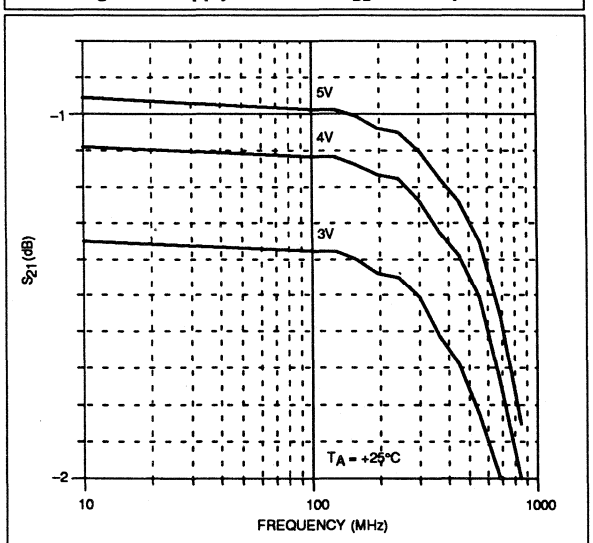


Figure 8 Loss vs. Frequency and V_{DD} for D-Package -Expanded Detail-

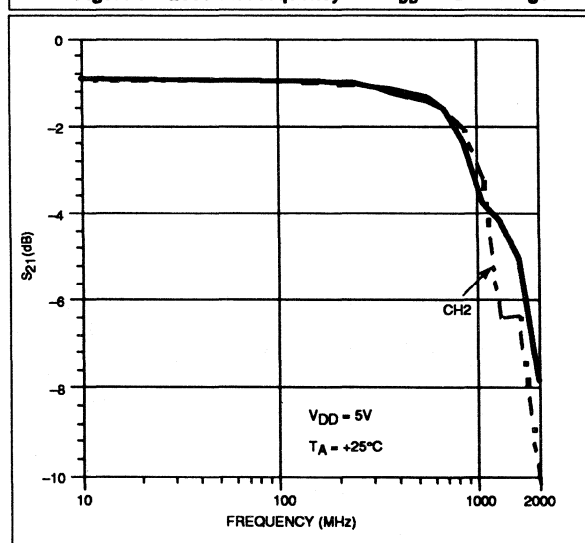


Figure 9 Loss Matching vs. Frequency for N-Package (DIP)

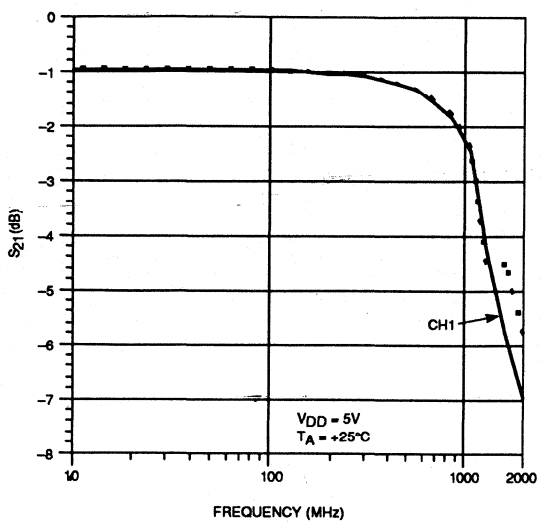


Figure 10 Loss Matching vs. Frequency; CH1 vs. CH2 for D-Pakage

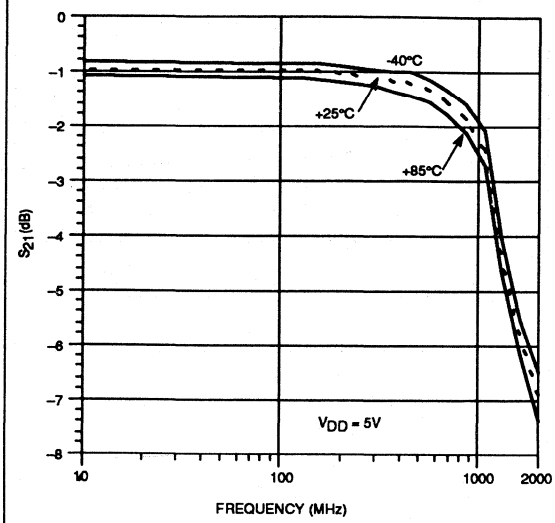


Figure 11 Loss vs. Frequency and Temperature for D-Package

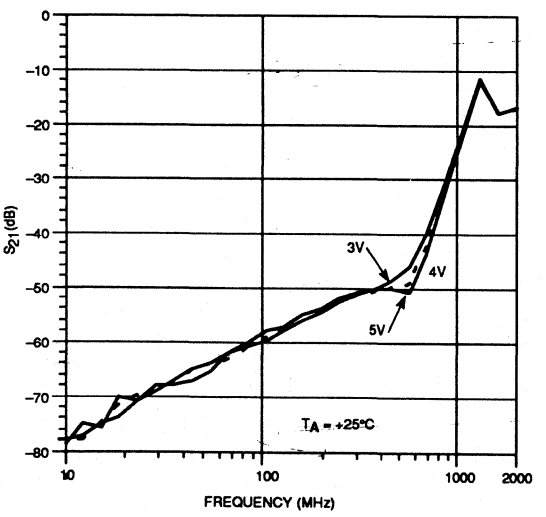


Figure 12 Isolation vs. Frequency and V_{DD} for D-Package

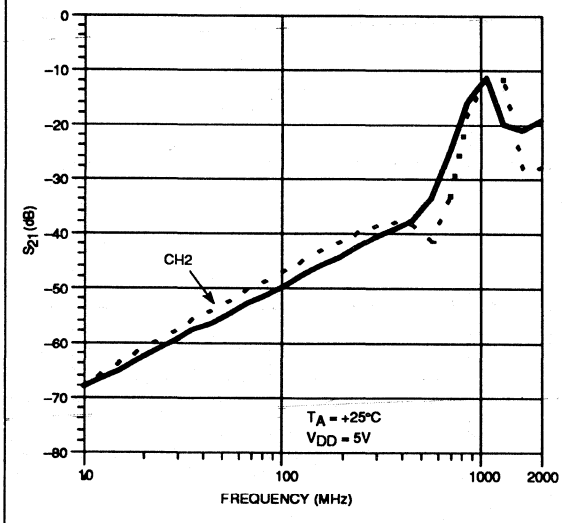


Figure 13 Isolation Matching vs. Frequency for N-Package (DIP)

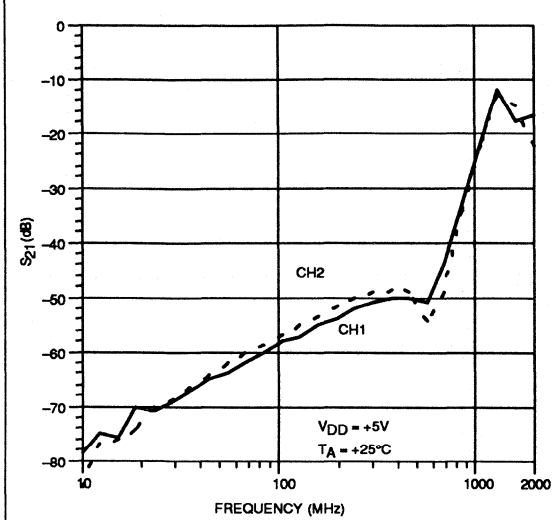


Figure 14 Isolation Matching vs. Frequency; CH1 vs. CH2 for D-Package

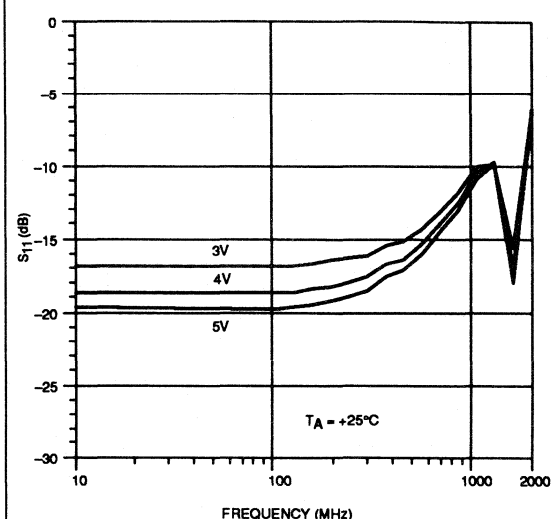


Figure 15 Input Match On-Channel vs. Frequency and V_{DD}

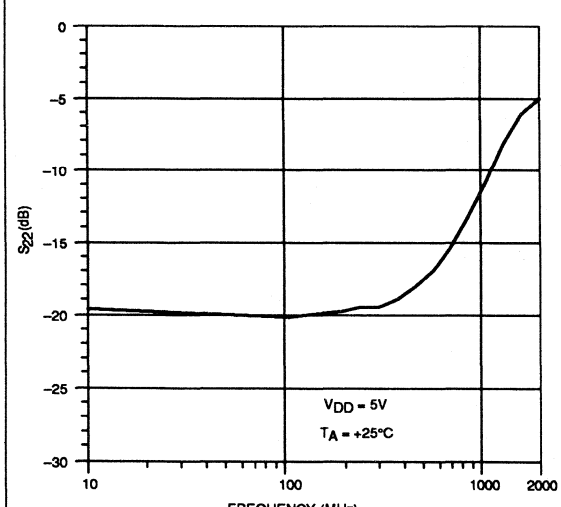


Figure 16 Output Match On-Channel vs. Frequency

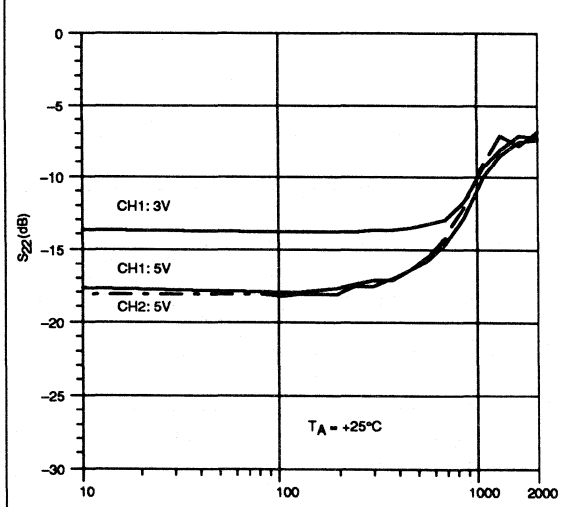


Figure 17 OFF-Channel Match vs. Frequency and V_{DD}

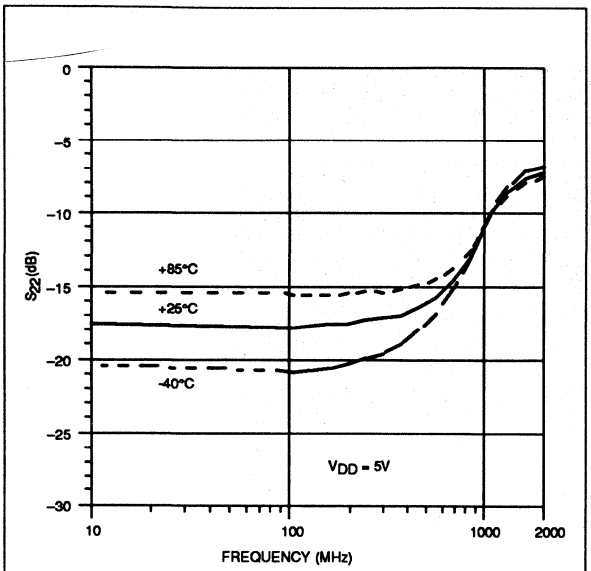


Figure 18 OFF Channel Match vs. Frequency and Temperature

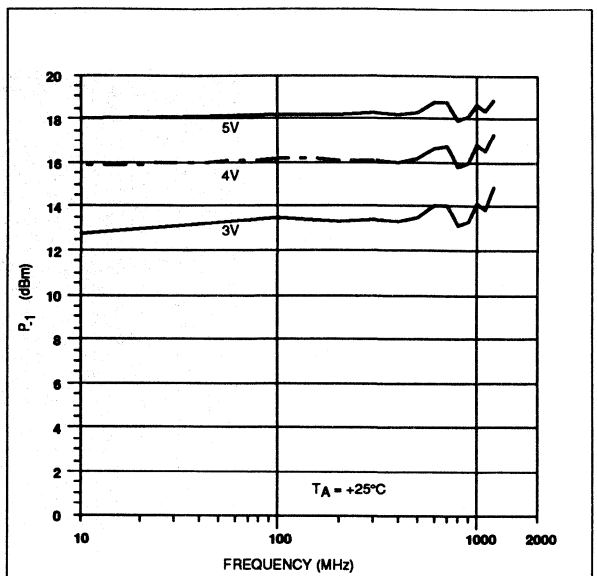


Figure 19 P_{-1} dB vs. Frequency and V_{DD}

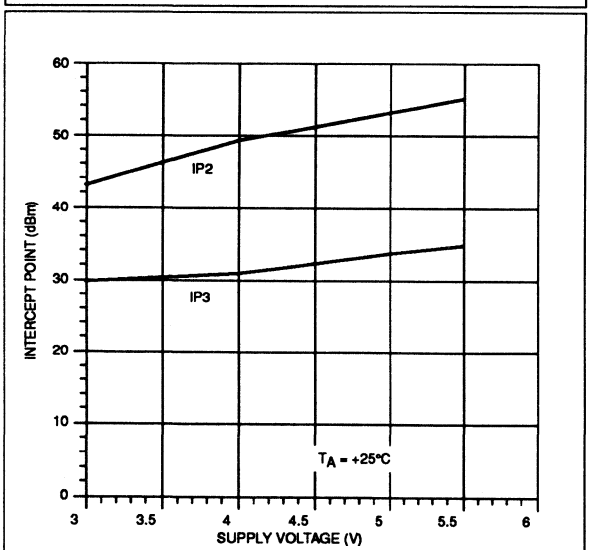


Figure 20 Intercept Points vs. V_{DD}

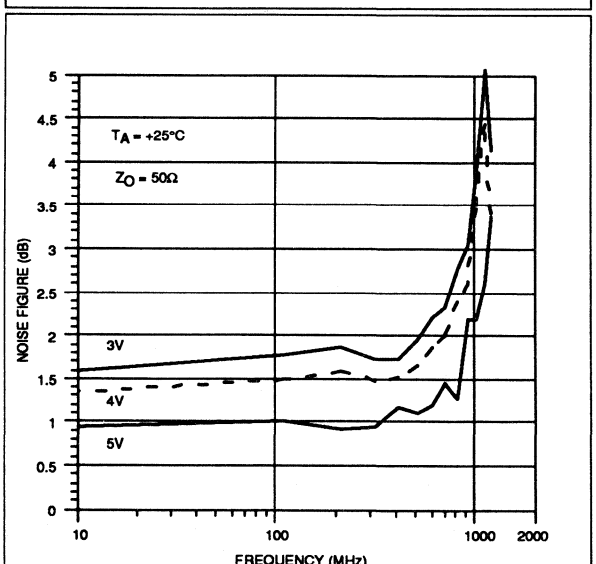


Figure 21 Noise Figure vs. Frequency and V_{DD} for D-Package

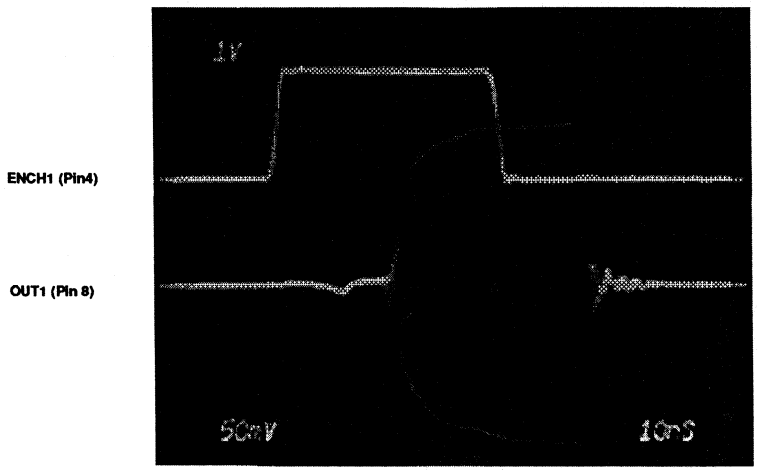


Figure 22 Switching Speed; f_{IN} = 100MHz at -6dBm, V_{DD} = 5V

Divide by: 128/129-64/65 dual modulus low power ECL prescaler

NE/SA701

DESCRIPTION

The NE701 is an advanced dual modulus (Divide By 128/129 or 64/65) low power ECL prescaler. The minimum supply voltage is 2.7V and is compatible with the new CMOS UMF1005 and UMF1009 synthesizers from Philips and other logic circuits. The low supply current allows application in battery operated low-power equipment. Maximum input signal frequency is 1.2GHz for cellular and other land mobile applications. There is no lower frequency limit due to a fully static design. The circuit is implemented in ECL technology on the QUBiC process. The circuit will be available in an 8-pin SO package with 150 mil package width and in 8-pin dual-in-line plastic package, and is pin compatible with Fujitsu MB501, Plessey SP8704 and Motorola MC12022.

FEATURES

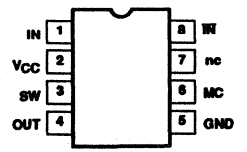
- Low voltage operation
- Low current consumption
- Operation up to 1.2GHz
- ESD hardened

APPLICATIONS

- Cellular phones
- Cordless phones
- RF LANs
- Test and measurement
- Military radio
- VHF/UHF mobile radio
- VHF/UHF hand-held radio

PIN CONFIGURATION

N, D Package



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	NE701N
8-Pin Plastic SO (Surface-mount)	0 to +70°C	NE701D
8-Pin Plastic DIP	-40 to +85°C	SA701N
8-Pin Plastic SO (Surface-mount)	-40 to +85°C	SA701D

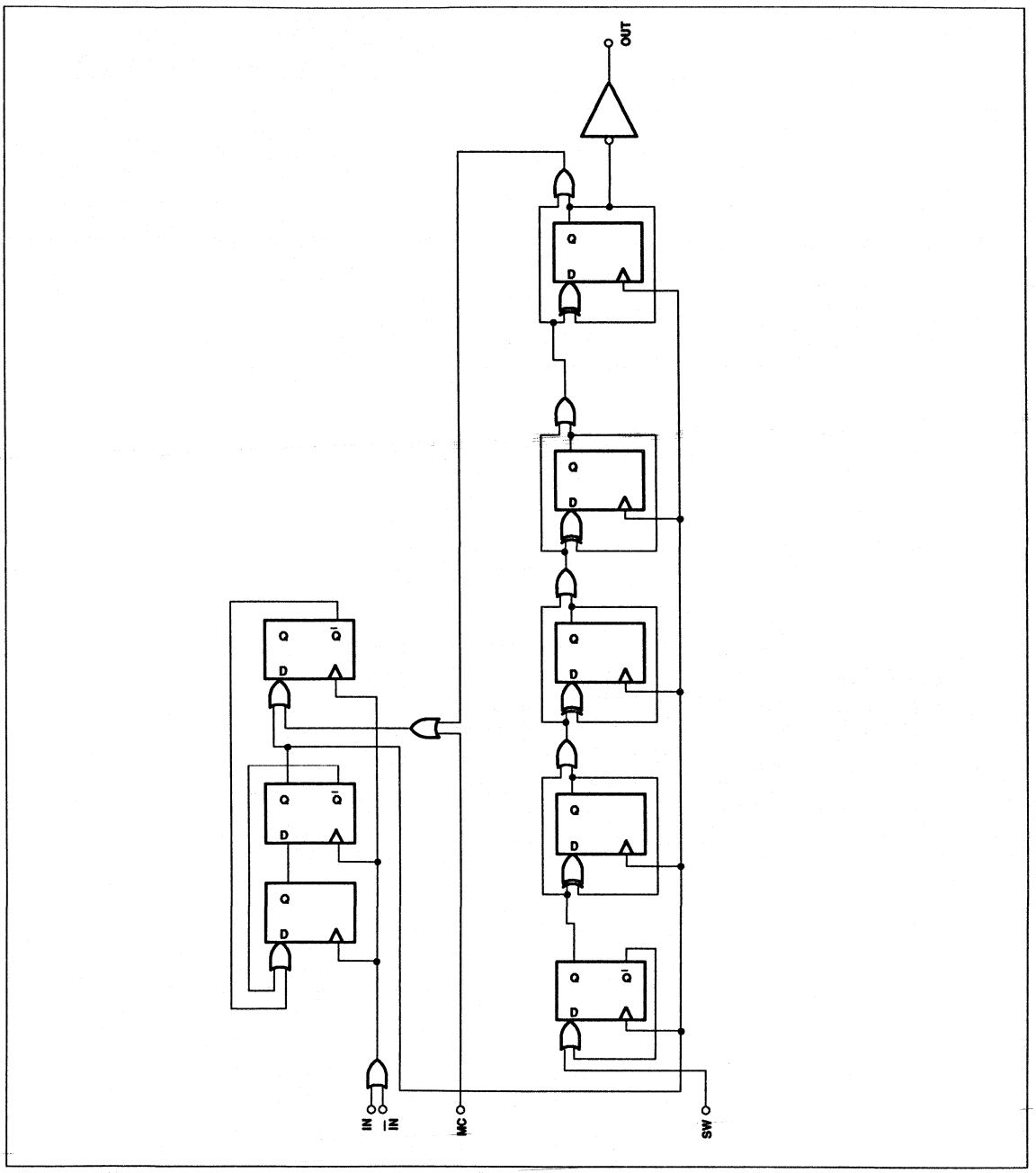
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	-0.3 to +7.0	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CC} + 0.3)	V
I_O	Output current	10	mA
T_{STG}	Storage temperature range	-65 to +125	°C
T_A	Operating ambient temperature range	-55 to +125	°C
θ_{JA}	Thermal impedance D package N package	158 108	°C/W

Divide by: 128/129-64/65 dual modulus low power ECL prescaler

NE/SA701

BLOCK DIAGRAM



Divide by: 128/129-64/65 dual modulus low power ECL prescaler

NE/SA701

DC ELECTRICAL CHARACTERISTICS

The following DC specifications are valid for T_A = 25°C and V_{CC} = 3.0V; unless otherwise stated. Test circuit Figure 1.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range	f_{IN} = 1GHz, input level = 0dBm	2.7		6.0	V
I_{CC}	Supply current	No load		4.5		mA
V_{OH}	Output high level	I_{OUT} = 1.2mA	V_{CC}-1.4			V
V_{OL}	Output low level			V_{CC}-2.6		V
V_{IH}	MC input high threshold		2.0		V_{CC}	V
V_{IL}	MC input low threshold		–0.3		0.8	V
V_{IH}	SW input high threshold		2.0		V_{CC}	V
V_{IL}	SW input low threshold		–0.3		0.8	V
I_{IH}	MC input high current	V_{MC} = V_{CC} = 6V		0.1	50	µA
I_{IL}	MC input low current	V_{MC} = 0V, V_{CC} = 6V	–100	–30		µA
I_{IH}	SW input high current	V_{SW} = V_{CC} = 6V		35	100	µA
I_{IL}	SW input low current	V_{SW} = 0V, V_{CC} = 6V	–50	–0.1		µA

AC ELECTRICAL CHARACTERISTICS

The following AC specifications are valid for V_{CC} = 3.0V, f_{IN} = 1GHz, input level = 0dBm, T_A = 25°C; unless otherwise stated. Test circuit Fig. 1.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{IN}	Input signal amplitude[1]	1000pF input coupling	0.05		2.0	V_{P-P}
f_{IN}	Input signal frequency	Direct coupled input[2]	0		1.2	GHz
		1000pF input coupling			1.2	GHz
R_{ID}	Differential input resistance	DC measurement		5		kΩ
V_O	Output voltage	V_{CC} = 5.0V		1.6		V_{P-P}
		V_{CC} = 3.0V		1.2		V_{P-P}
t_S	Modulus set-up time[1]				5	ns
t_H	Modulus hold time[1]				0	ns
t_{PD}	Propagation time			10		ns

NOTES:
1. Maximum limit is not tested, however, it is guaranteed by design and characterization.
2. For f_{IN} < 50MHz, minimum input slew rate of 32V/µs is required.

DESCRIPTION OF OPERATION

The NE701 comprises a frequency divider circuit implemented using a divide by 4 or 5 synchronous prescaler followed by a 5 stage synchronous counter, see BLOCK DIAGRAM. The normal operating mode is for SW (Modulus Set Switch) input to be set low and MC (Modulus Control) input to be set high in which case the circuit comprises a divide by 128. For divide by 129 the MC singal is forced low, causing the prescaler circuit to switch into divide by 5 operation for the last cycle of the synchronous counter. Similarly, for divide by 64 and 65 the NE701 will generate those respective moduli with the SW signal forced high, in which the fourth stage of the synchronous divider is bypassed.

A truth table for the modulus values is given below:

Table 1.

Modulus	MC	SW
128	1	0
129	0	0
64	1	1
65	0	1

For minimization of propagation delay effects, the second divider circuit is synchronous to the divide by 4/5 stage output.

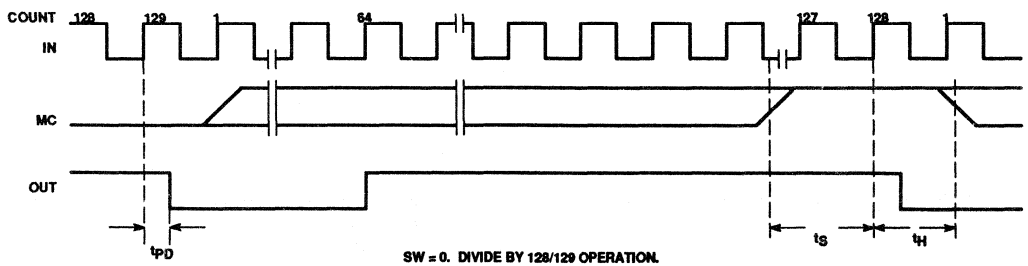
The prescaler input is positive edge sensitive, and the output at the final count is a falling edge with propagation delay t_{PD} relative to the input. The rising edge of the output occurs at the count 64 for modulus 128/129 or count 32 for modulus 64/65 with delay t_{PD}. The SW input is not designed for synchronous switching.

The MC and SW inputs are TTL compatible threshold inputs operating at a reduced input current. CMOS and low voltage interface capability are allowed. The SW input has an internal pull-down simplifying modulus group selection. With SW open the divide by 128/129 mode is selected and with SW connected to V_{CC} divide by 64/65 is selected.

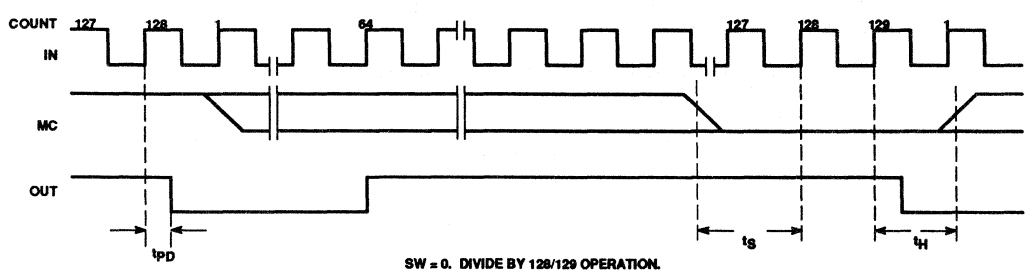
The prescaler input is differential and ECL compatible. The output is single-ended ECL compatible.

Divide by: 128/129-64/65 dual modulus low power ECL prescaler

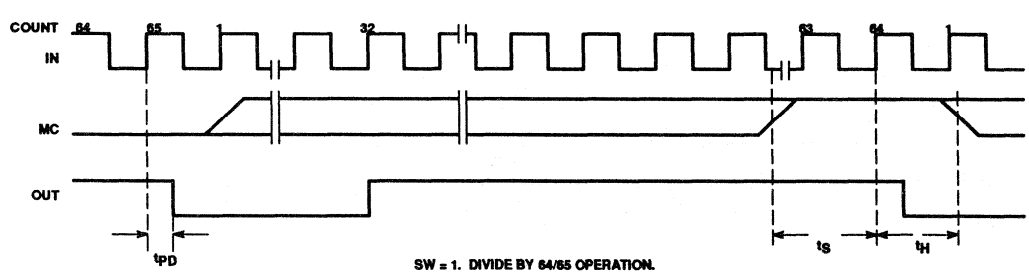
AC TIMING CHARACTERISTICS



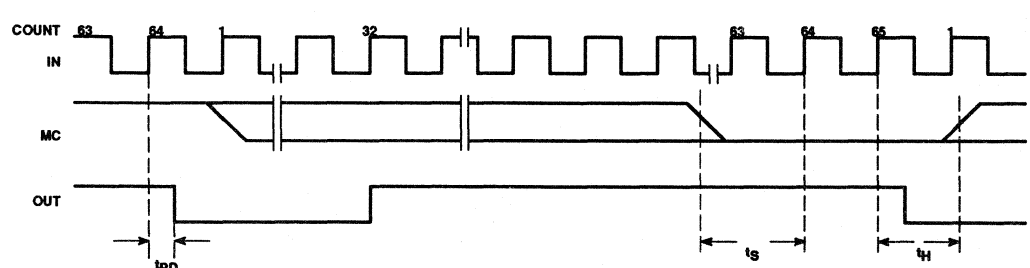
SW = 0. DIVIDE BY 128/129 OPERATION.



SW = 0. DIVIDE BY 128/129 OPERATION.



SW = 1. DIVIDE BY 64/65 OPERATION.



SW = 1. DIVIDE BY 64/65 OPERATION.

Divide by: 128/129-64/65 dual modulus low power ECL prescaler

NE/SA701

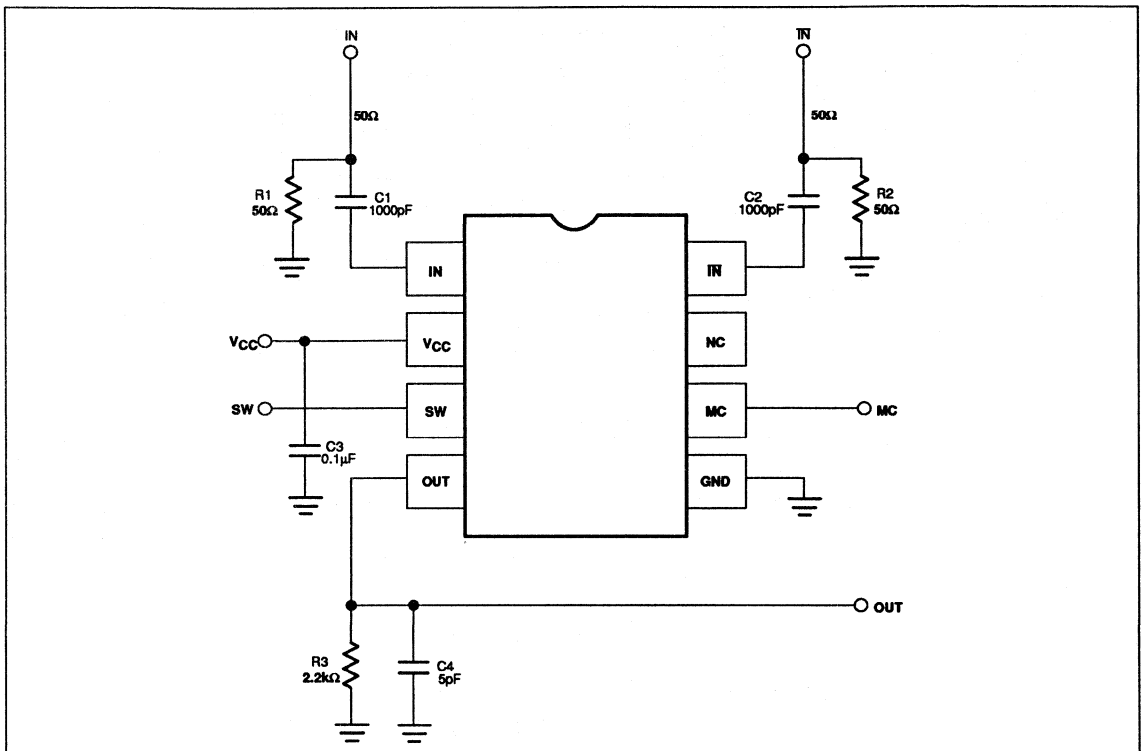


Figure 1. NE/SA701 Test Circuit

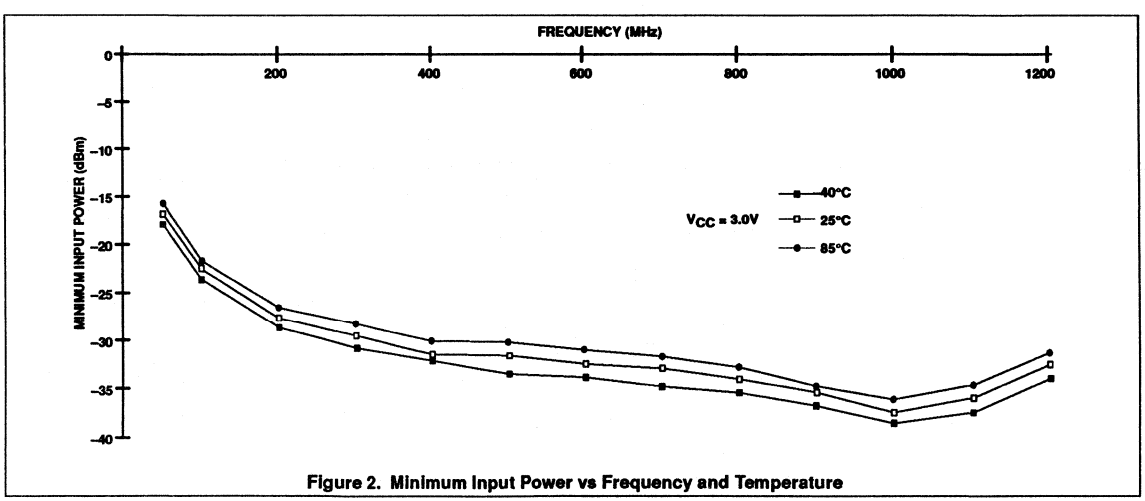


Figure 2. Minimum Input Power vs Frequency and Temperature

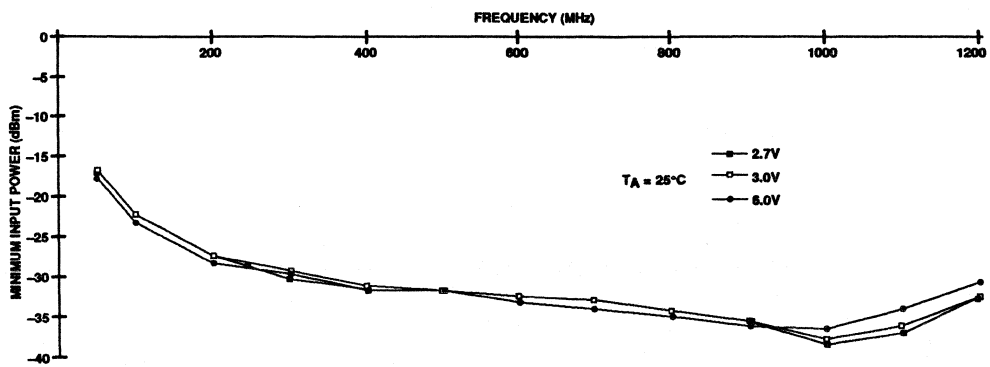


Figure 3. Minimum Input Power vs Frequency and V_{CC}

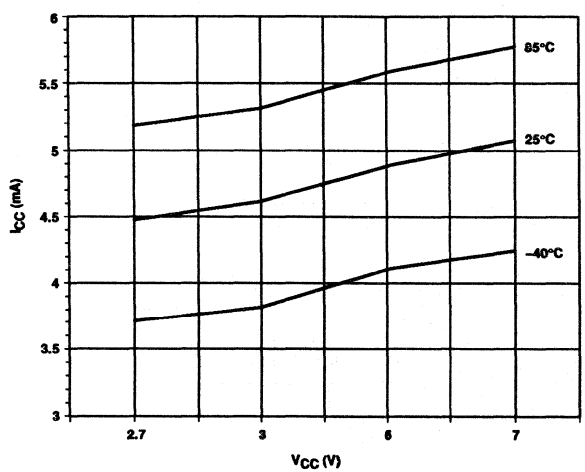
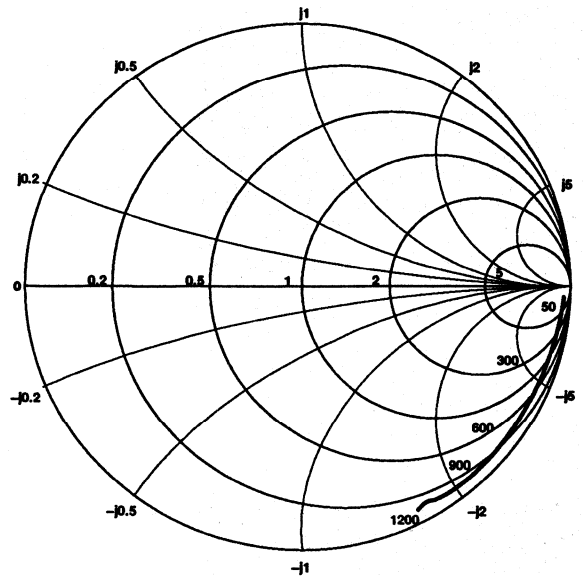


Figure 4. Supply Current vs Supply Voltage and Temperature With No Load

Divide by: 128/129-64/65 dual modulus low power ECL prescaler

NE/SA701



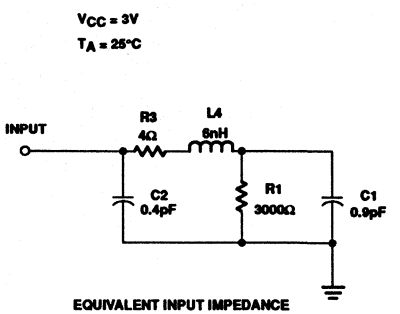
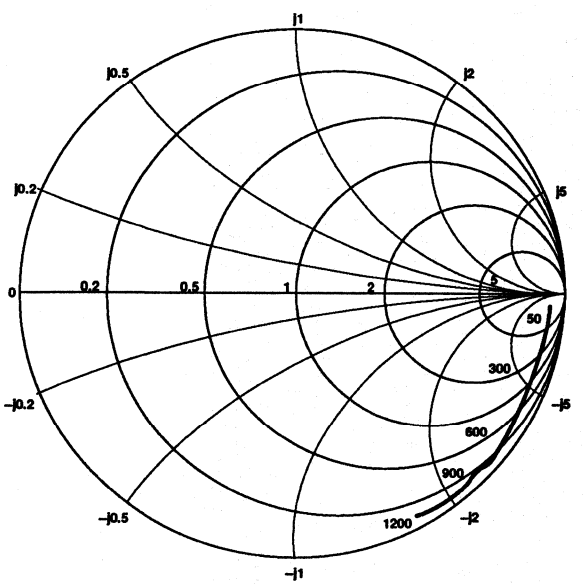


Figure 5. Typical N Package Input Impedance



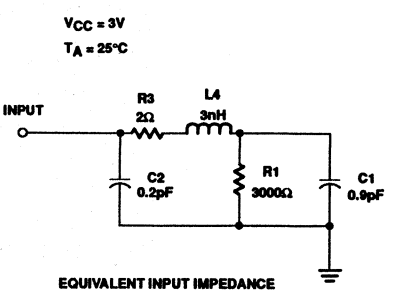


Figure 6. Typical D Package Input Impedance

Divide by: 64/65/72 triple modulus low power ECL prescaler

NE/SA702

DESCRIPTION

The NE702 triple modulus (Divide By 64/65/72) low power ECL prescaler is used in synthesizer systems to achieve low phase lock time, broad operating range, high reference frequency and small frequency step sizes. The minimum supply voltage is 2.7V and is compatible with the new CMOS UMF1005 and UMF1009 synthesizers from Philips and other logic circuits. The low supply current allows application in battery operated low-power equipment. Maximum input signal frequency is 1.2GHz for cellular and other land mobile applications. There is no lower frequency limit due to a fully static design. The circuit is implemented in ECL technology on the QUBiC process. The circuit will be available in an 8-pin SO package with 150 mil package width and in 8-pin dual-in-line plastic package.

FEATURES

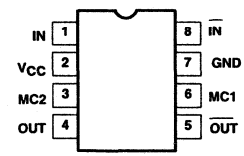
- Low voltage operation
- Low current consumption
- Operation up to 1.2GHz
- ESD hardened

APPLICATIONS

- Cellular phones
- Cordless phones
- RF LANs
- Test and measurement
- Military radio
- VHF/UHF mobile radio
- VHF/UHF hand-held radio

PIN CONFIGURATION

N, D Package



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic DIP	0 to +70°C	NE702N	0404
8-Pin Plastic SO (Surface-mount)	0 to +70°C	NE702D	0174
8-Pin Plastic DIP	-40 to +85°C	SA702N	0404
8-Pin Plastic SO (Surface-mount)	-40 to +85°C	SA702D	0174

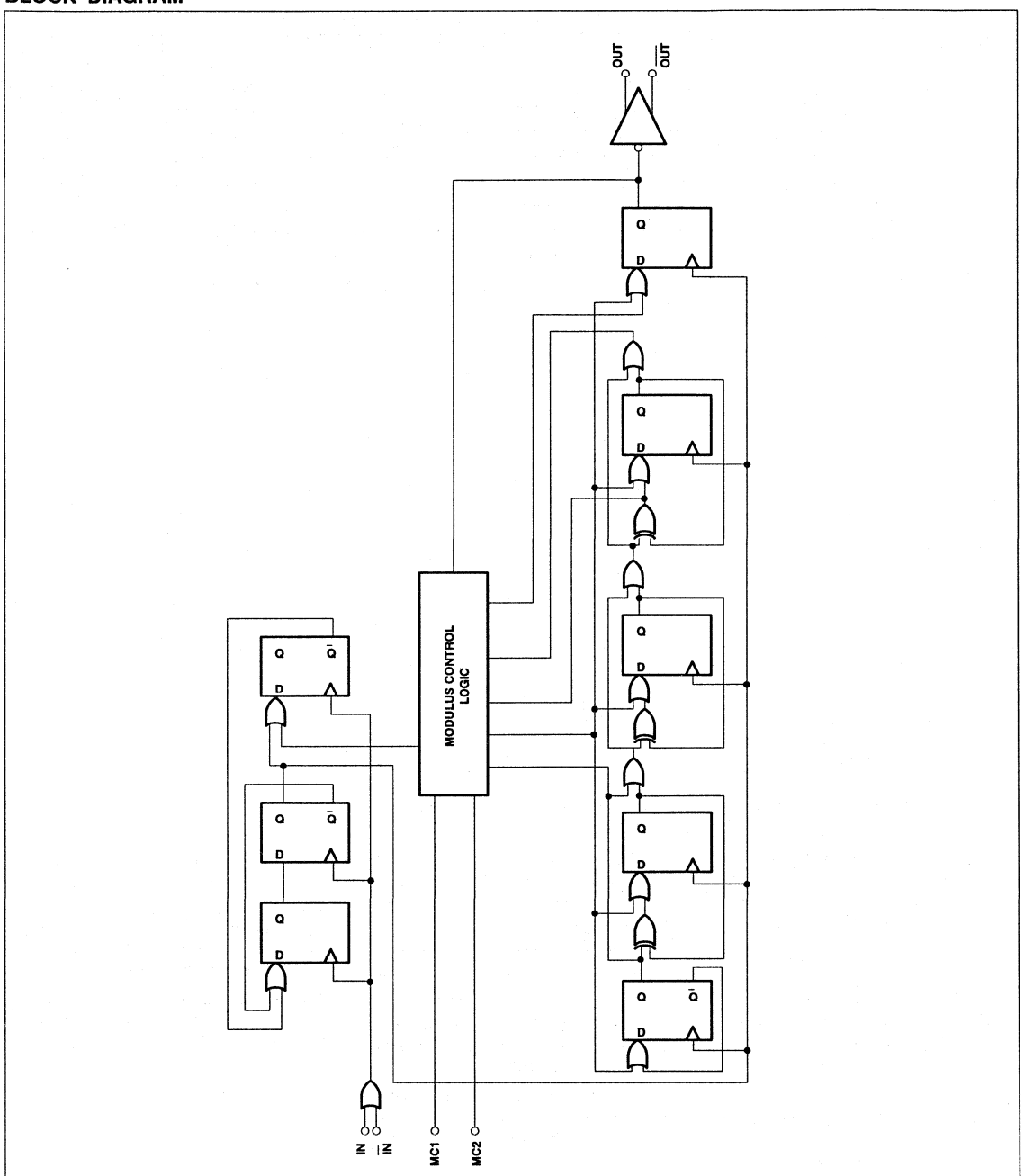
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		RATING	UNITS
V_{CC}	Supply voltage		-0.3 to +7.0	V
V_{IN}	Voltage applied to any other pin		-0.3 to (V_{CC} + 0.3)	V
I_O	Output current		10	mA
T_{STG}	Storage temperature range		-65 to +125	°C
T_A	Operating ambient temperature range		-55 to +125	°C
θ_{JA}	Thermal impedance	D package N package	158 108	°C/W

Divide by: 64/65/72 triple modulus low power ECL prescaler

NE/SA702

BLOCK DIAGRAM



Divide by: 64/65/72 triple modulus low power ECL prescaler

NE/SA702

DC ELECTRICAL CHARACTERISTICS

The following DC specifications are valid for $T_A = 25°C$ and $V_{CC} = 3.0V$; unless otherwise stated. Test circuit Figure 1.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range	f_{IN} = 1GHz, input level = 0dBm	2.7		6.0	V
I_{CC}	Supply current	No load		4.5		mA
V_{OH}	Output high level	I_{OUT} = 1.2mA	V_{CC}-1.4			V
V_{OL}	Output low level			V_{CC}-2.6		V
V_{IH}	MC1 input high threshold		2.0		V_{CC}	V
V_{IL}	MC1 input low threshold		–0.3		0.8	V
V_{IH}	MC2 input high threshold		2.0		V_{CC}	V
V_{IL}	MC2 input low threshold		–0.3		0.8	V
I_{IH}	MC1 input high current	$V_{MC1} = V_{CC} = 6V$		0.1	50	µA
I_{IL}	MC1 input low current	$V_{MC1} = 0V$, $V_{CC} = 6V$	–100	–30		µA
I_{IH}	MC2 input high current	$V_{MC2} = V_{CC} = 6V$		0.1	50	µA
I_{IL}	MC2 input low current	$V_{MC2} = 0V$, $V_{CC} = 6V$	–100	–30		µA

AC ELECTRICAL CHARACTERISTICS

These AC specifications are valid for f_{IN} = 1GHz, input level = 0dBm, $V_{CC} = 3.0V$ and $T_A = 25°C$; unless otherwise stated. Test circuit Fig. 1.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{IN}	Input signal amplitude[1]	1000pF input coupling	0.05		2.0	V_{P-P}
f_{IN}	Input signal frequency	Direct coupled input[2]	0		1.2	GHz
		1000pF input coupling			1.2	GHz
R_{ID}	Differential input resistance	DC measurement		5		kΩ
V_O	Output voltage	$V_{CC} = 5.0V$		1.6		V_{P-P}
		$V_{CC} = 3.0V$		1.2		V_{P-P}
t_S	Modulus set-up time[1]				5	ns
t_H	Modulus hold time[1]				0	ns
t_{PD}	Propagation time			10		ns

NOTES:
1. Maximum limit is not tested, however, it is guaranteed by design and characterization.
2. For f_{IN} < 50MHz, minimum input slew rate of 32V/µs is required.

DESCRIPTION OF OPERATION

The NE702 comprises a frequency divider circuit implemented using a divide by 4 or 5 synchronous prescaler followed by a 5 stage synchronous counter, see BLOCK DIAGRAM. The normal operating mode is for MC1 (Modulus Control) to be set high and MC2 input to be set low in which case the circuit comprises a divide by 64. For divide by 65 the MC1 singal is forced low, causing the prescaler circuit to switch into divide by 5 operation for the last cycle of the sunchronous counter. For divide by 72, MC2 is set high configuring the prescaler to divide by 4 and the counter to divide by 18. A truth table for the modulus values is given below:

Table 1.

Modulus	MC1	MC2
64	1	0
65	0	0
72	0	1
72	1	1

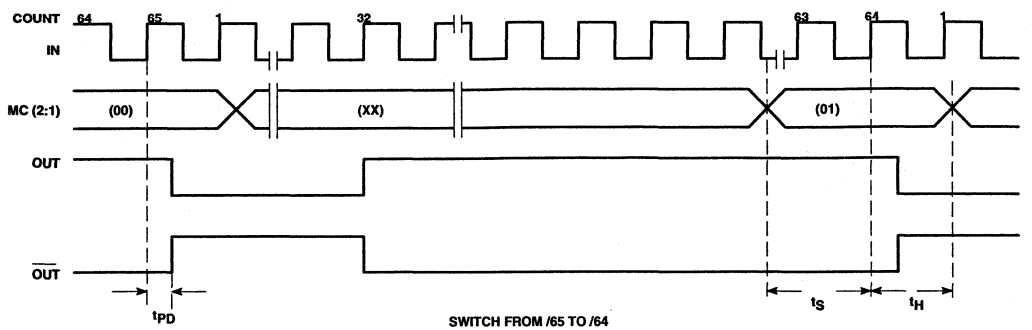
For minimization of propagation delay effects, the second divider circuit is synchronous to the divide by 4/5 stage output.

The prescaler input is positive edge sensitive, and the output at the final count is a falling edge with propagation delay t_{PD} relative to the input. The rising edge of the output occurs at the count 32 with delay t_{PD}.

The MC1 and MC2 inputs are TTL compatible threshold inputs operating at a reduced input current. CMOS and low voltage interface capability are allowed.

The prescaler input is differential and ECL compatible. The output is differential ECL compatible.

AC TIMING CHARACTERISTICS



Divide by: 64/65/72 triple modulus low power ECL prescaler

NE/SA702

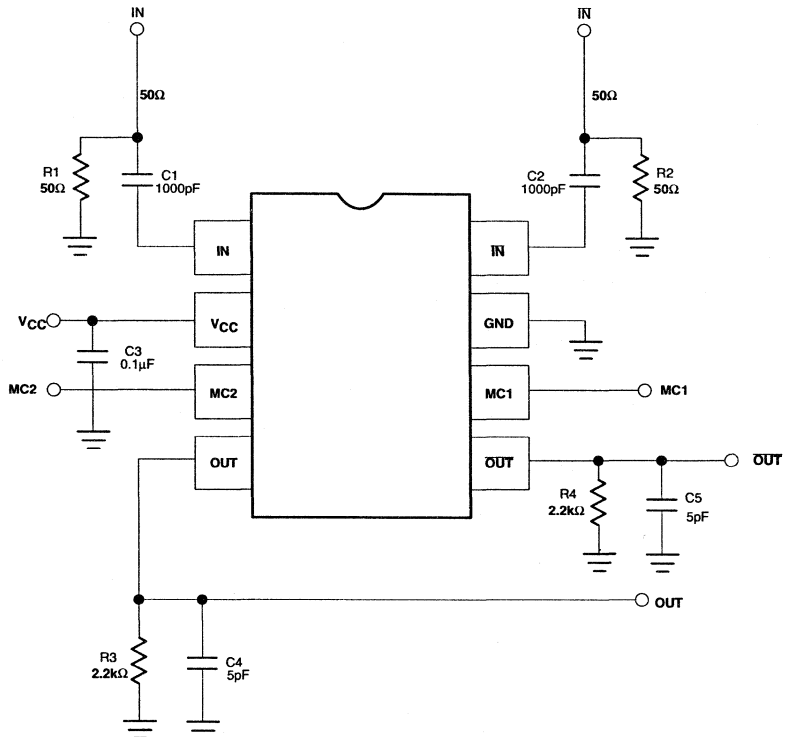


Figure 1. NE/SA702 Test Circuit

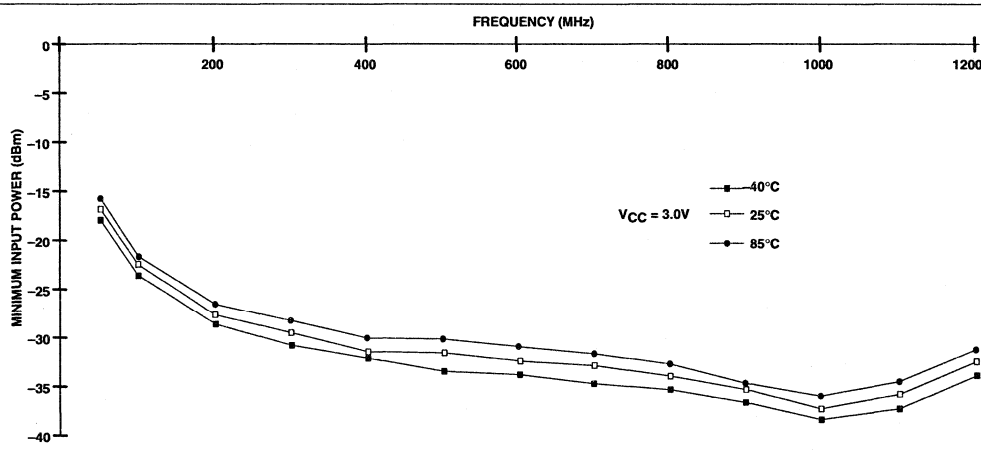


Figure 2. Minimum Input Power vs Frequency and Temperature

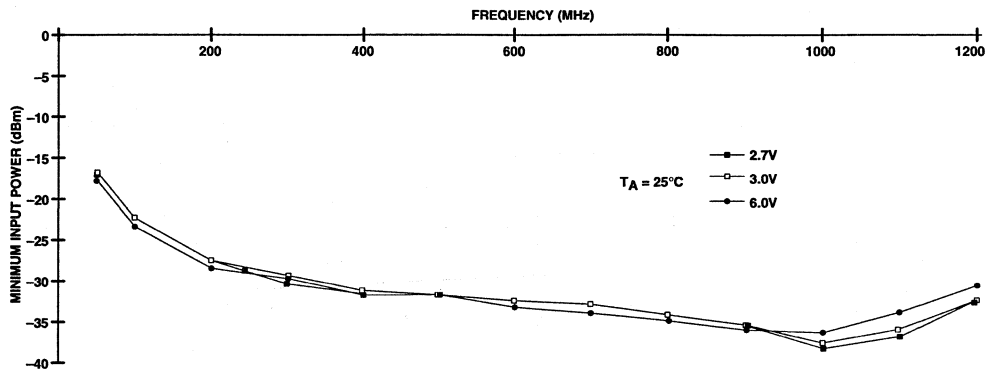


Figure 3. Minimum Input Power vs Frequency and V_{CC}

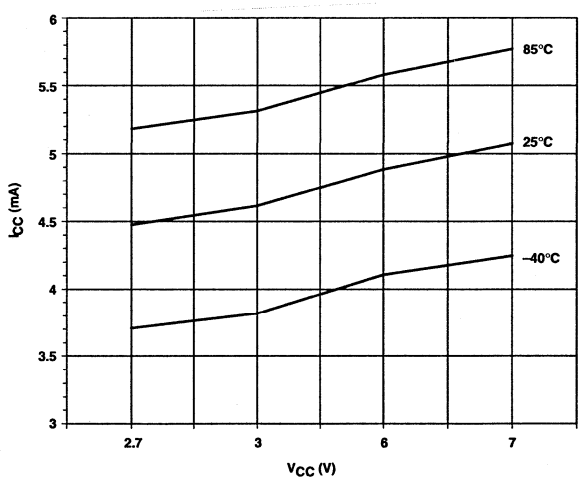
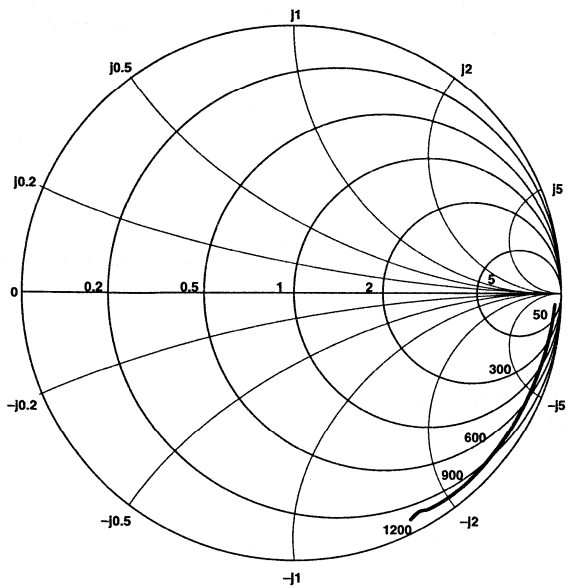


Figure 4. Supply Current vs Supply Voltage and Temperature With No Load



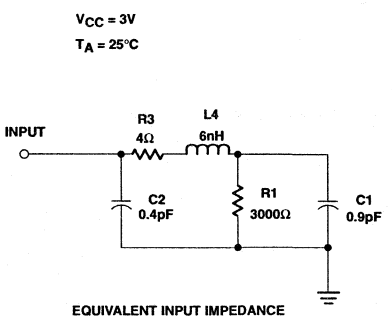
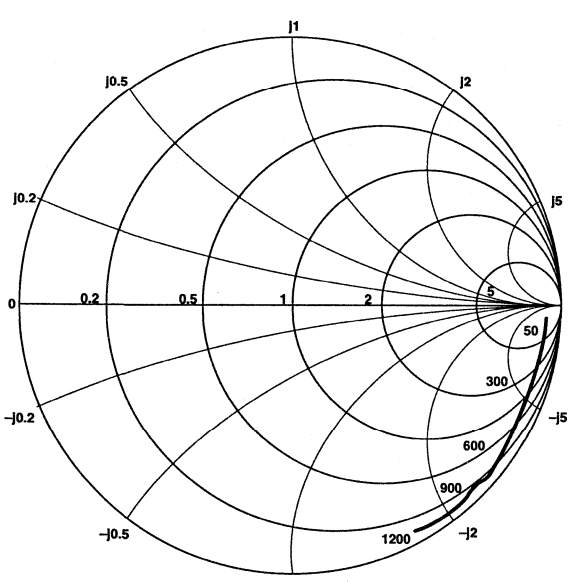


Figure 5. Typical N Package Input Impedance



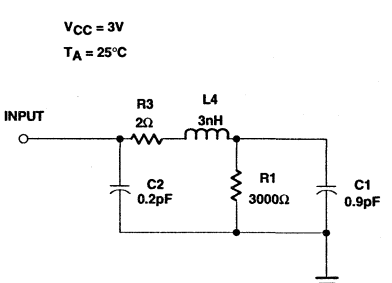


Figure 6. Typical D Package Input Impedance

Divide by: 128/129/144 triple modulus low power ECL prescaler

NE/SA703

DESCRIPTION

The NE703 triple modulus (Divide By 128/129/144) low power ECL prescaler is used in synthesizer systems to achieve low phase lock time, broad operating range, high reference frequency and small frequency step sizes. The minimum supply voltage is 2.7V and is compatible with the UMF1005 and UMF1009 synthesizers from Philips and other logic circuits. The low supply current allows application in battery operated low-power equipment. Maximum input signal frequency is 1.2GHz for cellular and other land mobile applications. There is no lower frequency limit due to a fully static design. The circuit is implemented in ECL technology on the QUBiC process. The circuit will be available in an 8-pin SO package with 150 mil package width and in 8-pin dual-in-line plastic package.

FEATURES

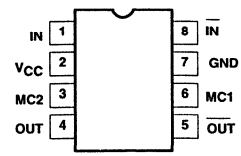
- Low voltage operation
- Low current consumption
- Operation up to 1.2GHz
- ESD hardened

APPLICATIONS

- Cellular phones
- Cordless phones
- RF LANs
- Test and measurement
- Military radio
- VHF/UHF mobile radio
- VHF/UHF hand-held radio

PIN CONFIGURATION

N, D Package



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic DIP	0 to +70°C	NE703N	0404
8-Pin Plastic SO (Surface-mount)	0 to +70°C	NE703D	0174
8-Pin Plastic DIP	-40 to +85°C	SA703N	0404
8-Pin Plastic SO (Surface-mount)	-40 to +85°C	SA703D	0174

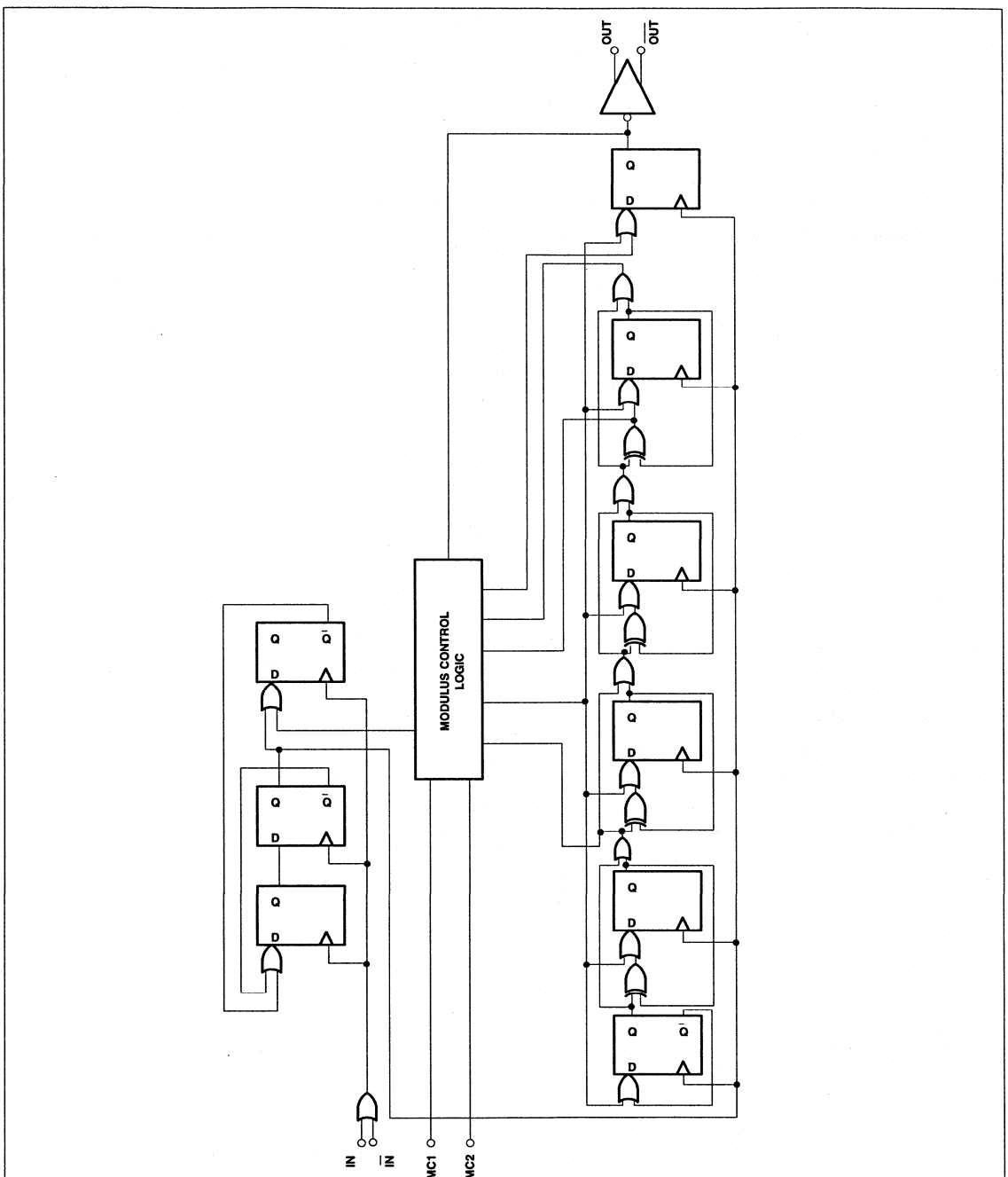
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	-0.3 to +7.0	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CC} + 0.3)	V
I_O	Output current	10	mA
T_{STG}	Storage temperature range	-65 to +125	°C
T_A	Operating ambient temperature range	-55 to +125	°C
θ_{JA}	Thermal impedance D package N package	158 108	°C/W

Divide by: 128/129/144 triple modulus low power ECL prescaler

NE/SA703

BLOCK DIAGRAM



Divide by: 128/129/144 triple modulus low power ECL prescaler

NE/SA703

DC ELECTRICAL CHARACTERISTICS

The following DC specifications are valid for $T_A = 25^{\circ}C$ and $V_{CC} = 3.0V$; unless otherwise stated. Test circuit Figure 1.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range	f_{IN} = 1GHz, input level = 0dBm	2.7		6.0	V
I_{CC}	Supply current	No load		4.5		mA
V_{OH}	Output high level	I_{OUT} = 1.2mA	V_{CC}-1.4			V
V_{OL}	Output low level			V_{CC}-2.6		V
V_{IH}	MC1 input high threshold		2.0		V_{CC}	V
V_{IL}	MC1 input low threshold		–0.3		0.8	V
V_{IH}	MC2 input high threshold		2.0		V_{CC}	V
V_{IL}	MC2 input low threshold		–0.3		0.8	V
I_{IH}	MC1 input high current	$V_{MC1} = V_{CC} = 6V$		0.1	50	µA
I_{IL}	MC1 input low current	$V_{MC1} = 0V, V_{CC} = 6V$	–100	–30		µA
I_{IH}	MC2 input high current	$V_{MC2} = V_{CC} = 6V$		0.1	50	µA
I_{IL}	MC2 input low current	$V_{MC2} = 0V, V_{CC} = 6V$	–100	–30		µA

AC ELECTRICAL CHARACTERISTICS

These AC specifications are valid for $V_{CC} = 3.0V$, f_{IN} = 1GHz, input level = 0dBm, $T_A = 25^{\circ}C$; unless otherwise stated. Test circuit Fig. 1.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{IN}	Input signal amplitude[1]	1000pF input coupling	0.05		2.0	V_{P-P}
f_{IN}	Input signal frequency	Direct coupled input[2]	0		1.2	GHz
		1000pF input coupling			1.2	GHz
R_{ID}	Differential input resistance	DC measurement		5		kΩ
V_O	Output voltage	$V_{CC} = 5.0V$		1.6		V_{P-P}
		$V_{CC} = 3.0V$		1.2		V_{P-P}
t_S	Modulus set-up time[1]				5	ns
t_H	Modulus hold time[1]				0	ns
t_{PD}	Propagation time			10		ns

NOTES:
1. Maximum limit is not tested, however, it is guaranteed by design and characterization.
2. For f_{IN} < 50MHz, minimum input slew rate of 32V/µs is required.

DESCRIPTION OF OPERATION

The NE703 comprises a frequency divider circuit implemented using a divide by 4 or 5 synchronous prescaler followed by a 5 stage synchronous counter, see BLOCK DIAGRAM. The normal operating mode is for MC1 (Modulus Control) to be set high and MC2 input to be set low in which case the circuit comprises a divide by 128. For divide by 129 the MC1 singal is forced low, causing the prescaler circuit to switch into divide by 5 operation for the last cycle of the sunchronous counter. For divide by 144, MC2 is set high configuring the prescaler to divide by 4 and the counter to divide by 36. A truth table for the modulus values is given below:

Table 1.

Modulus	MC1	MC2
128	1	0
129	0	0
144	0	1
144	1	1

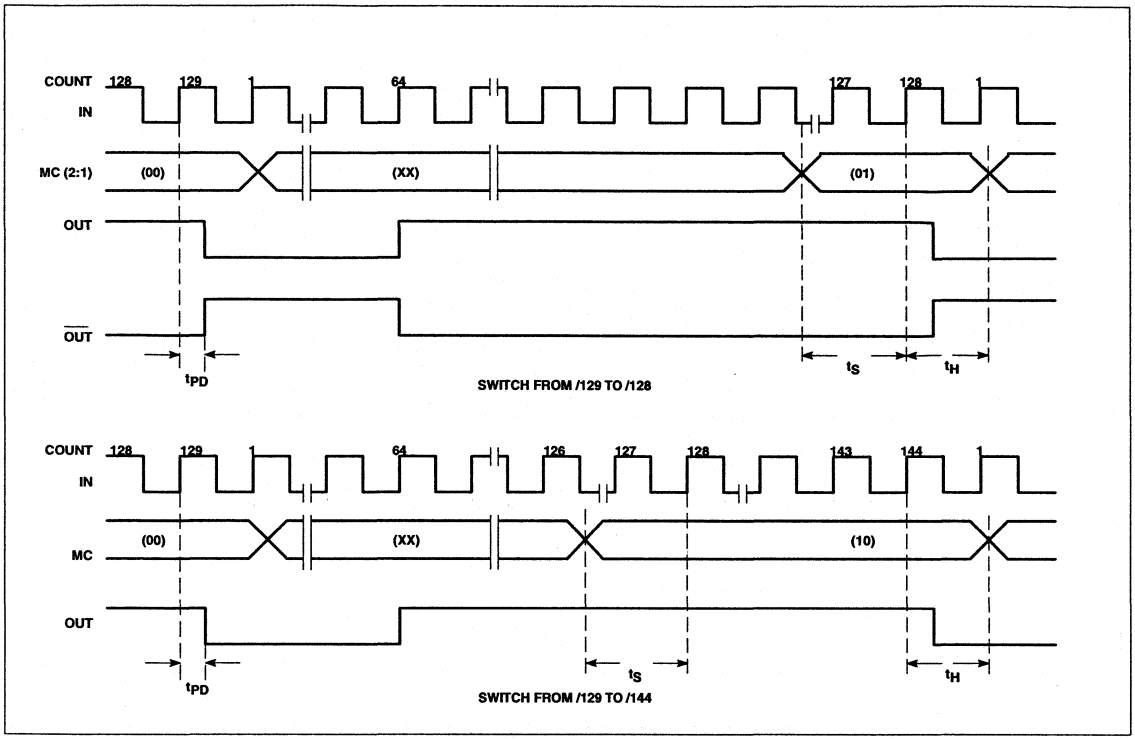
For minimization of propagation delay effects, the second divider circuit is synchronous to the divide by 4/5 stage output.

The prescaler input is positive edge sensitive, and the output at the final count is a falling edge with propagation delay t_{PD} relative to the input. The rising edge of the output occurs at the count 64 with delay t_{PD}.

The MC1 and MC2 inputs are TTL compatible threshold inputs operating at a reduced input current. CMOS and low voltage interface capability are allowed.

The prescaler input is differential and ECL compatible. The output is differential ECL compatible.

AC TIMING CHARACTERISTICS



Divide by: 128/129/144 triple modulus low power ECL prescaler

NE/SA703

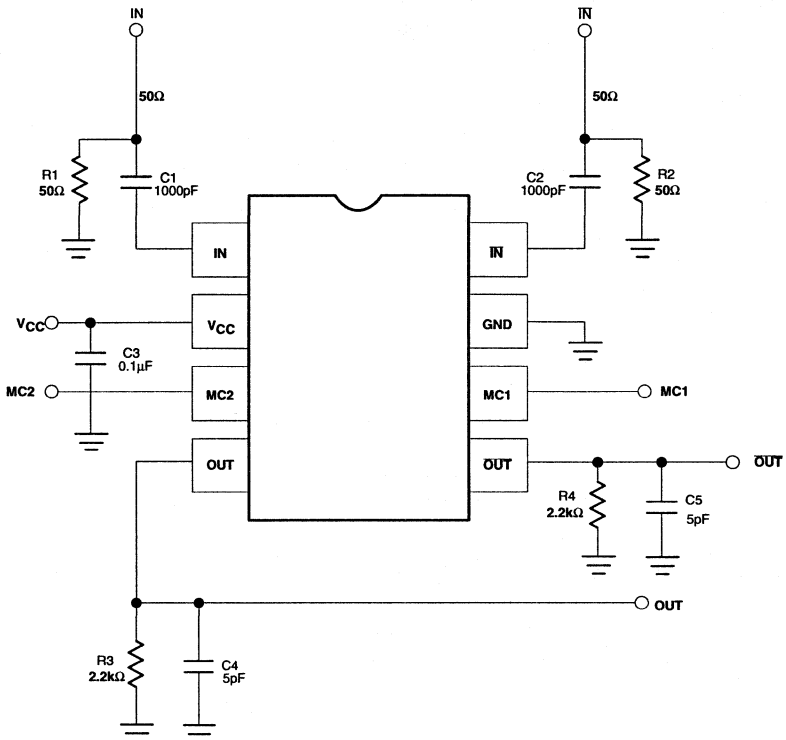


Figure 1. NE/SA703 Test Circuit

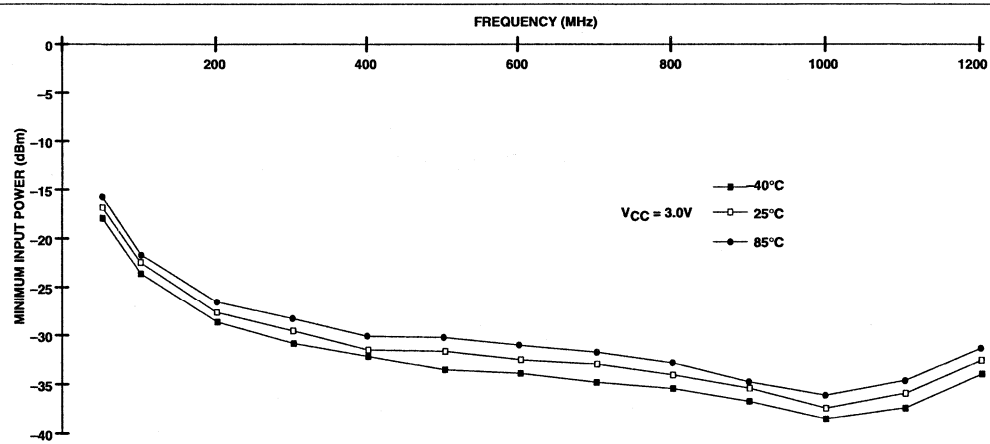


Figure 2. Minimum Input Power vs Frequency and Temperature

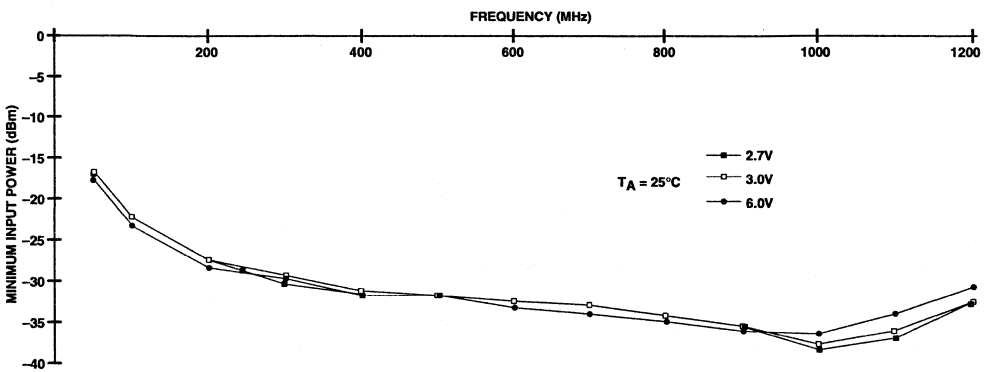


Figure 3. Minimum Input Power vs Frequency and V_{CC}

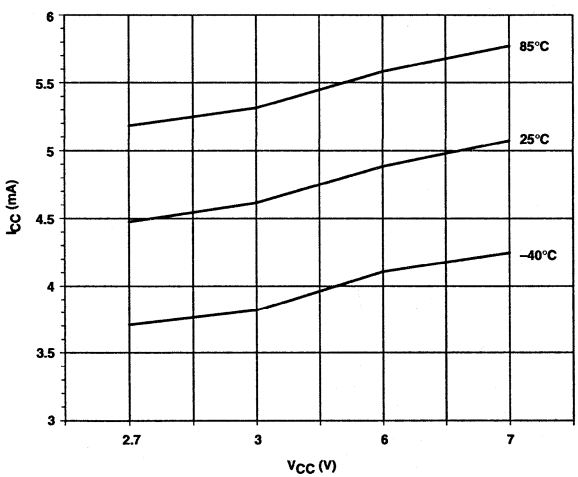
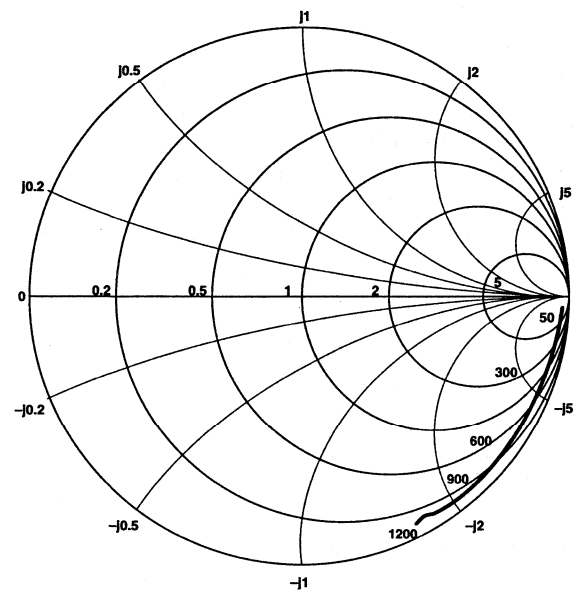


Figure 4. Supply Current vs Supply Voltage and Temperature With No Load

Divide by: 128/129/144 triple modulus low power ECL prescaler

NE/SA703



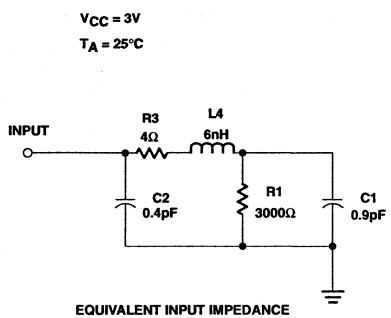
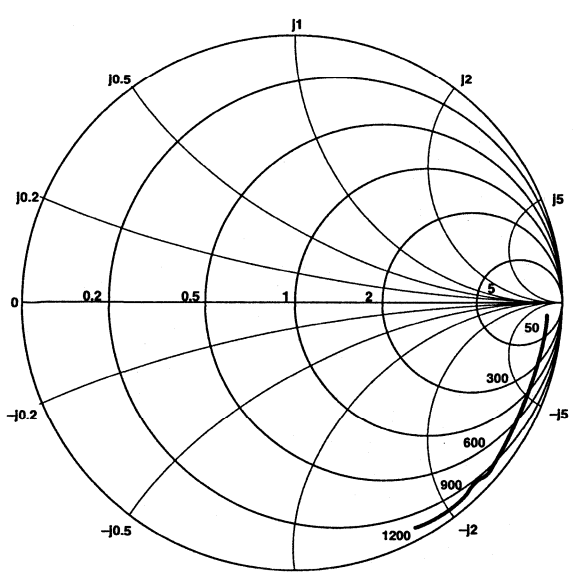


Figure 5. Typical N Package Input Impedance



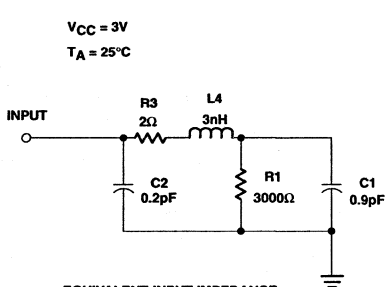


Figure 6. Typical D Package Input Impedance

RF dual gain-stage NE/SA5200

DESCRIPTION

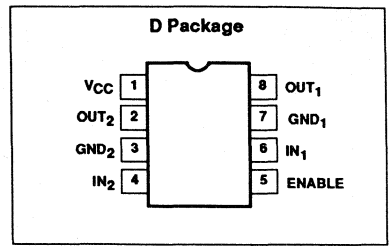
The NE/SA5200 is a dual amplifier with DC to 1200MHz response. Low noise (NF = 3.6dB) makes this part ideal for RF front-ends, and a simple power-down mode saves current for battery operated equipment. Inputs and outputs are matched to 50Ω.

The enable pin allows the designer the ability to turn the amplifiers on or off, allowing the part to act as an amplifier as well as an attenuator. This is very useful for front-end buffering in receiver applications.

FEATURES

- Dual amplifiers
- DC - 1200MHz operation
- Low DC power consumption (4.2mA per amplifier @ V_{CC} = 5V)
- Power-Down Mode (I_{CC} = 95µA typical)
- 3.6dB noise figure at 900MHz
- Unconditionally stable
- Fully ESD protected
- Low cost
- Supply voltage 4-9V
- Gain S_{21} = 7dB at f = 1GHz
- Input and output match S_{11}, S_{22} typically <–14dB

PIN CONFIGURATION



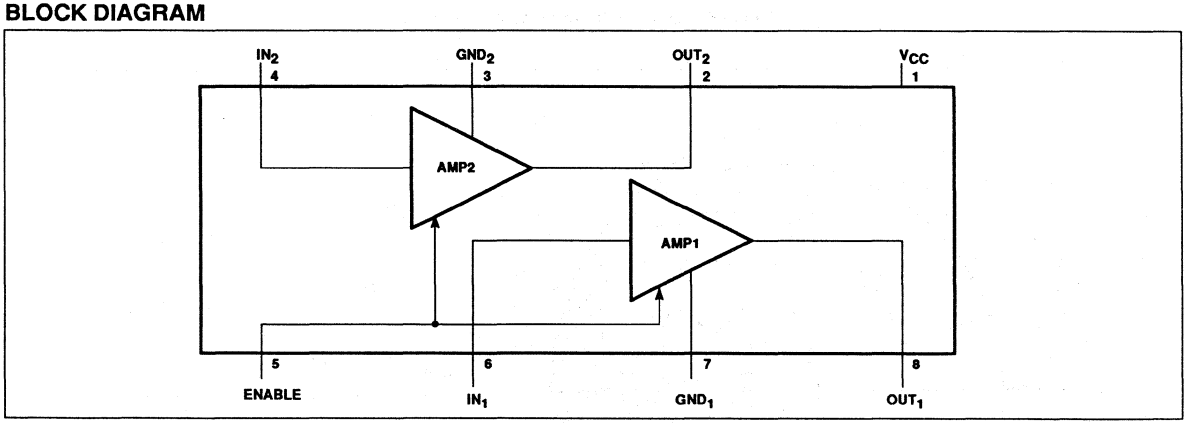
APPLICATIONS

- Cellular radios
- RF IF strips
- Portable equipment

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO (Surface–mount)	0-70°C	NE5200D
8-Pin Plastic SO (Surface–mount)	–40-+85°C	SA5200D

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage[1]	-0.5 to +9	V
P_D	Power dissipation, T_A = 25°C (still air)[2] 8-Pin Plastic SO	780	mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power input/output	+20	dBm
T_{STG}	Storage temperature range	–65 to +150	°C

NOTE:
1. Transients exceeding 10.5V on V_{CC} pin may damage product.
2. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}:
   8-Pin SO: θ_{JA} = 158°C/W

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	4.0 to 9.0	V
T_A	Operating ambient temperature range NE Grade SA Grade	 0 to +70 -40 to +85	 °C °C
T_J	Operating junction temperature NE Grade SA Grade	 0 to +90 -40 to +105	 °C °C

DC ELECTRICAL CHARACTERISTICS V_{CC} = +5V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{CC}	Supply voltage		4	5.0	9.0	V
I_{CC}	Total supply current	V_{CC} = 5V, ENABLE = High	6.4	8.4	10.4	mA
		V_{CC} = 5V, ENABLE = Low		95	255	µA
		V_{CC} = 9V, ENABLE = High		17.8	22.2	mA
		V_{CC} = 9V, ENABLE = Low		320	960	µA
V_T	TTL/CMOS logic threshold voltage[1]			1.25		V
V_{IH}	Logic 1 level	Power-up mode	2.0		V_{CC}	V
V_{IL}	Logic 0 level	Power-down mode	-0.3		0.8	V
I_{IL}	Enable input current	Enable = 0.4V	-1	0	1	µA
I_{IH}	Enable input current	Enable = 2.4V	-1	0	1	µA
$V_{IDC,ODC}$	Input and output DC levels		0.6	0.83	1.0	V

NOTE:
1. The ENABLE input must be connected to a valid logic level for proper operation of the NE/SA5200.

AC ELECTRICAL CHARACTERISTICS[1] V_{CC} = +5V, T_A = 25°C, either amplifier, enable = 5V; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
S21	Insertion gain	f = 100MHz	9.2	11	13.2	dB
		f = 900MHz	5.2	7.5		dB
S22	Output return loss	f = 900MHz		–14.3		dB
S12	Reverse isolation	f = 900MHz		–17.9		dB
S11	Input return loss	f = 900MHz		–16.5		dB
P-1	Output 1dB compression point	f = 900MHz		–4.3		dBm
NF	Noise figure in 50Ω	f = 900MHz		3.6		dB
IP_2	Input second-order intercept point	f = 900MHz		+4.3		dBm
IP_3	Input third-order intercept point	f = 900MHz		–1.8		dBm
ISOL	Amplifier-to-amplifier isolation[2]	f = 900MHz		–25		dB
P_{OUT}	Saturated output power	f = 900MHz		–1.7		dBm
S21	Insertion gain when disabled	f = 100MHz		–13		dB
		f = 900MHz		–13.5		dB

NOTE:
1. All measurements include the effects of the NE/SA5200 Evaluation Board (see Figure 2). Measurement system impedance is 50Ω.
2. Input applied to one amplifier, output taken at the other output. All ports terminated into 50Ω.

APPLICATIONS

NE/SA5200 is a user-friendly, wide-band, unconditionally stable, low power dual gain amplifier circuit. There are several advantages to using the NE/SA5200 as a high frequency gain block instead of a discrete implementation. First is the simplicity of use. The NE/SA5200 does not need any external biasing components. Due to the higher level of integration and small footprint (SO8) package it occupies less space on the printed circuit board and reduces the manufacturing cost of the system. Also the higher level of integration improves the reliability of the amplifier over a discrete implementation with several components. The power down mode in the NE/SA5200 helps reduce power consumption in applications where the amplifiers can be disabled. And last but not the least is the impedance matching at inputs and outputs. Only those who have toiled through discrete transistor implementations for 50Ω input and output impedance matching can truly appreciate the elegance and simplicity of the NE/SA5200 input and output impedance matching to 50Ω.

A simplified equivalent schematic is shown in Figure 1. Each amplifier is composed of an NPN transistor with an Ft of 13GHz in a classical series-shunt feedback configuration. The two wideband amplifiers are biased from the same bias generator. In normal operation each amplifier consumes about 4mA of quiescent current (at V_{CC} = 5V). In the disable mode the device consumes about 90μA of current, most of it is in the TTL enable buffer and the bias generator. The input impedance of the amplifiers is 50Ω. The amplifiers have typical gain of 11dB at 100MHz and 7dB of gain at 1.2GHz.

It can be seen from Figure 1 that any inductance between Pin 7, 3 and the ground plane will reduce the gain of the amplifiers at higher frequencies. Thus proper grounding of Pins 7 and 3 is essential for maximum gain and increased frequency response. Figure 2 shows the printed circuit board layout and the component placement for the NE/SA5200 evaluation board. The AC coupling capacitors should be selected such that at they are shorts at the desired frequency of operation. Since most low-cost large value surface mount capacitors cease to be simply capacitors in the UHF range and exhibit an inductive behavior, it is recommended that high frequency chip capacitors be utilized in the circuit. A good power supply bypass is also essential for the performance of the amplifier and should be as close to the device as practical.

Figure 3 shows the typical frequency response of the two channels of NE/SA5200. The low frequency gain is about 11dB at 100MHz and slowly drops off to 10dB at 500MHz. The gain is about 8dB at 900MHz and 7dB at 1.2 GHz which is typical of NE/SA5200 with a good printed circuit board layout. It can also be seen that both channels have a very well matched frequency response and matched gain to within 0.1dB at 100MHz and 0.2dB at 900MHz.

NE/SA5200 finds applications in many areas of RF communications. It is an ideal gain block for high performance, low cost, low power RF communications transceivers. A typical radio transceiver front-end is shown in Figure 4. This could be the front-end of a cellular phone, a VHF/ UHF hand-held transceiver, UHF cordless telephone or a spread spectrum system. The NE/SA5200 can be used in the receiver path of most systems as an LNA and pre-amplifier. The bandpass filter between the two amplifiers also minimize the noise into the first mixer. In the transmitter path, NE/SA5200 can be used as a buffer to the VCO and isolate the VCO from any load variations due to the power level changes in the power amplifier. This improves the stability of the VCOs. The NE/SA5200 can also be used as a pre-driver to the power amplifier modules.

The two amplifiers in NE/SA5200 can be easily cascaded to have a 13dB gain block at 900MHz. At 100MHz the gain will be 22dB and a noise figure of about 5.5dB. The NE/SA5200 can be operated at a higher voltage up to 9V for much improved 1dB output compression point and higher 3rd order intercept point.

Several stages of NE/SA5200 can also be cascaded and be used as an IF amplifier strip for DBS/TV/GPS receivers. Figure 5 shows a 60dB gain IF strip at 180MHz. The noise figure for the cascaded amplifier chain is given by equation 1.

NF (total) = NF1 + NF2/G1 + NF3/G1*G2 + NF4/G1*G2*G3 + ... (Equation. 1)

NOTE: The noise figure and gain should not be in dB in the above equation.

Since the noise figure for each stage is about 3.6dB and the gain is about 11dB, the noise figure for the 60dB gain IF strip will be about 6.4dB.

In applications where a single amplifier is required with a 7.5dB gain at 900MHz and current consumption is of paramount importance (battery powered receivers), the amplifier A1 can be used and amplifier A2 can be disabled by leaving GND2 (Pin 3) unconnected. This will reduce the total current consumption for the IC to a meager 4mA.

The ENABLE pin is useful for Time-Division-Duplex systems where the receiver can be disabled for a period of time. In this case the overall system supply current will be decreased by 8mA.

The ENABLE pin can also be used to improve the system dynamic range. For input levels that are extremely high, the NE/SA5200 can be disabled. In this case the input signal is attenuated by 13dB. This prevents the system from being overloaded as well as improves the system's overall dynamic range. In the disabled condition the NE/SA5200 IP_3 increases to nearly +20dBm.

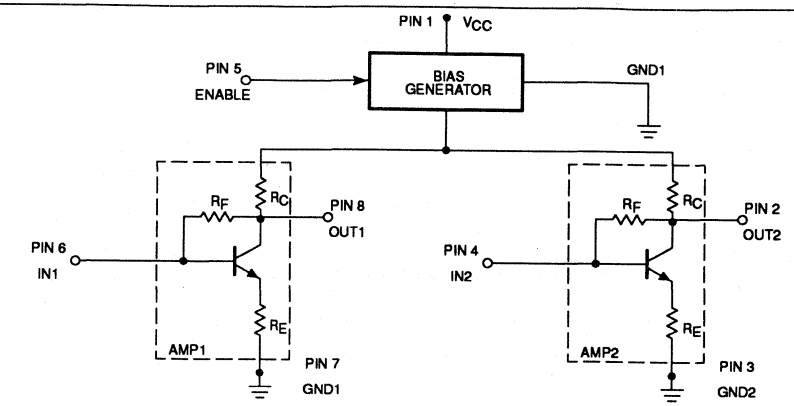
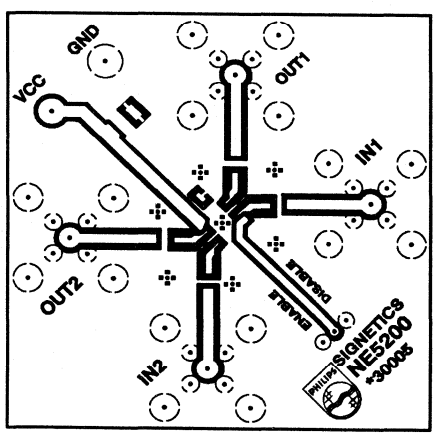
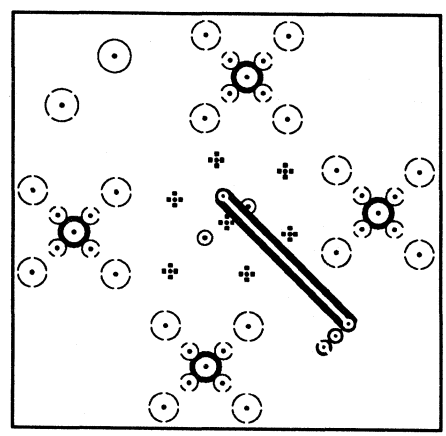


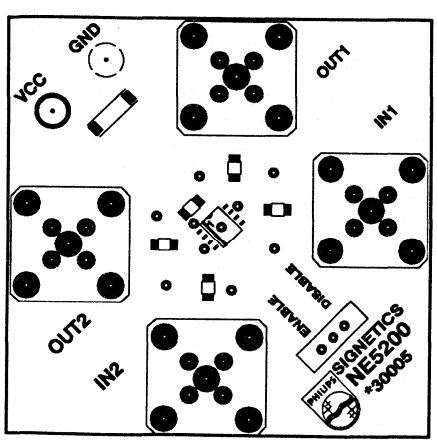
Figure 1. Simplified Equivalent Schematic of NE/SA5200



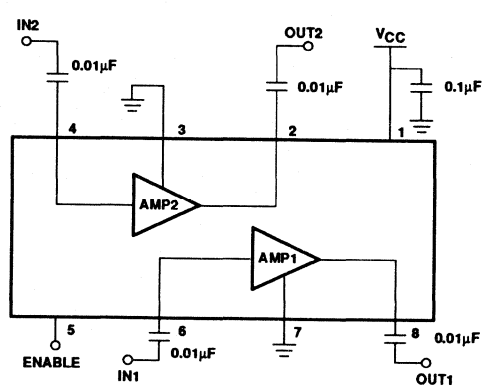
a. Top Side



b. Bottom Side



c. Top Silk Screen



d. NE/SA5200 Evaluation Board Schematic

Figure 2. Printed Circuit Board Layout of the NE/SA5200 Evaluation Board

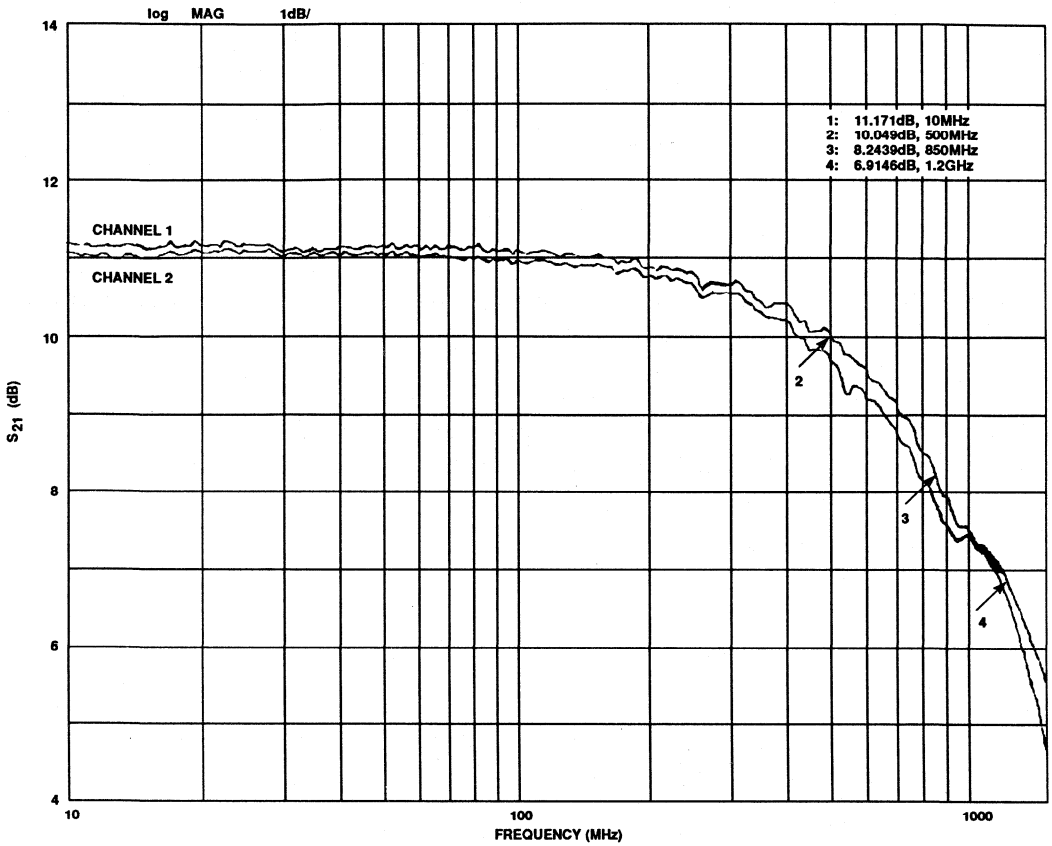


Figure 3. Typical Frequency Response of NE/SA5200 In a 50Ω System

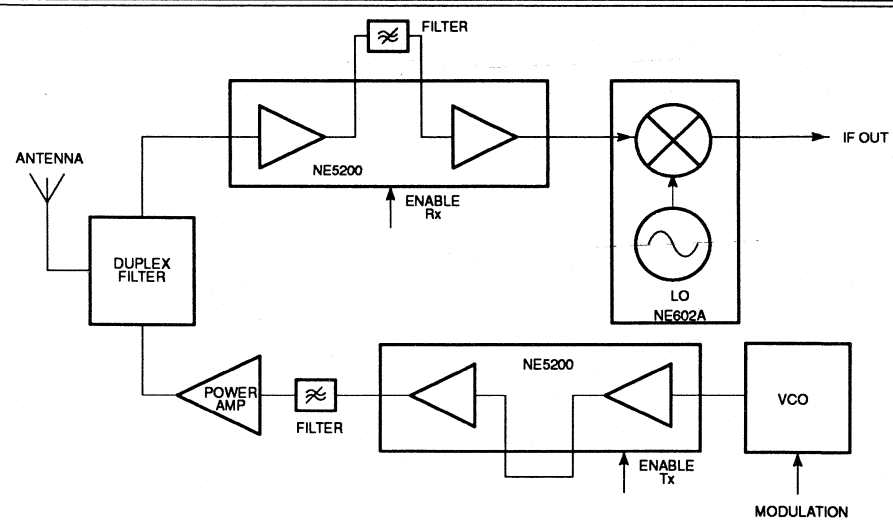


Figure 4. Typical Radio Transceiver Front-End

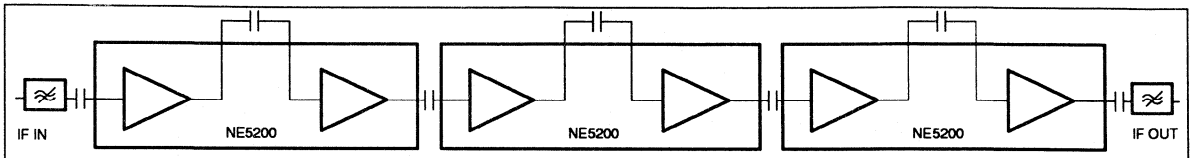


Figure 5. 60dB IF Gain Block for 100-300MHz IF for GPS/DBS Systems

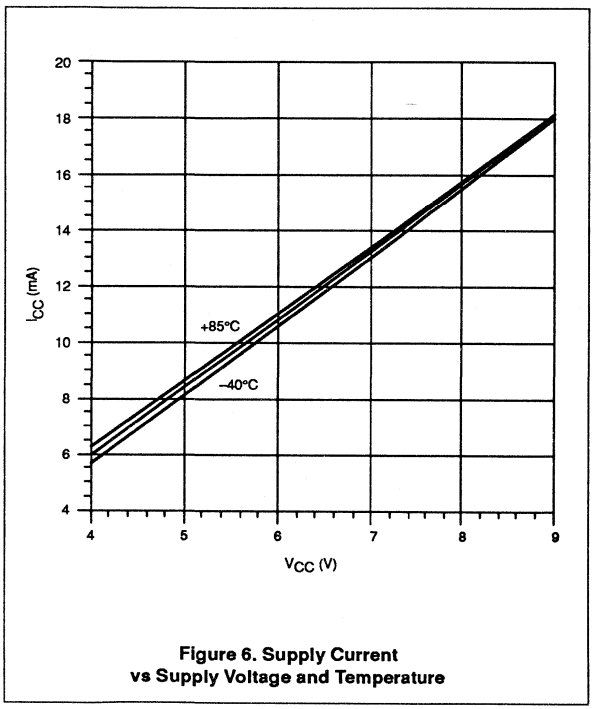


Figure 6. Supply Current vs Supply Voltage and Temperature

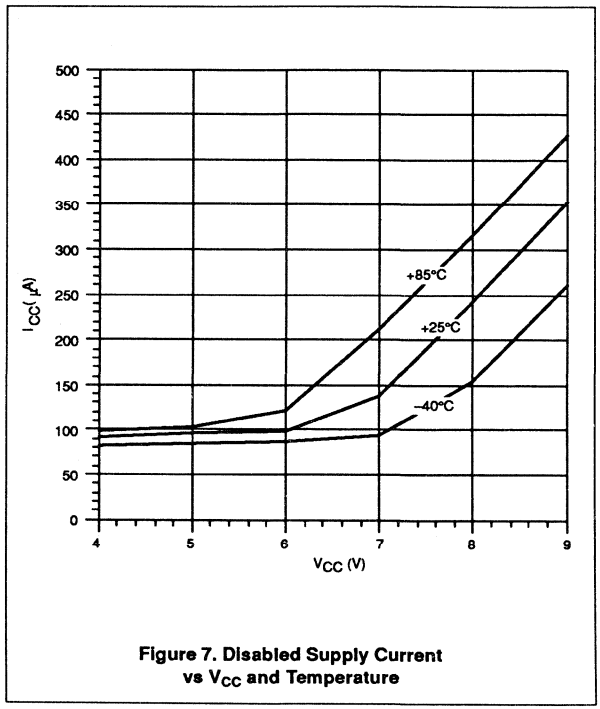


Figure 7. Disabled Supply Current vs V_{CC} and Temperature

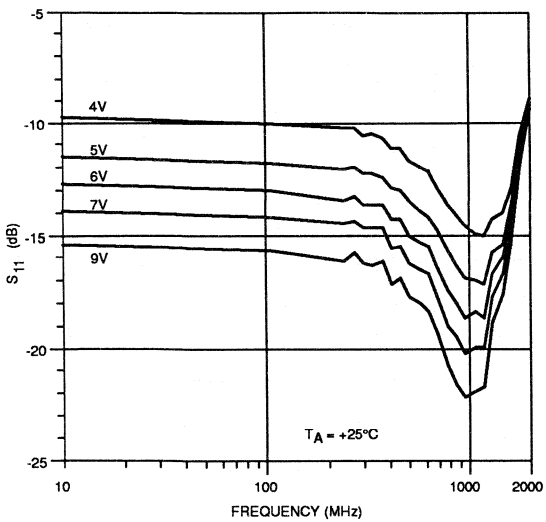


Figure 8. Input Match vs Frequency and V_{CC}

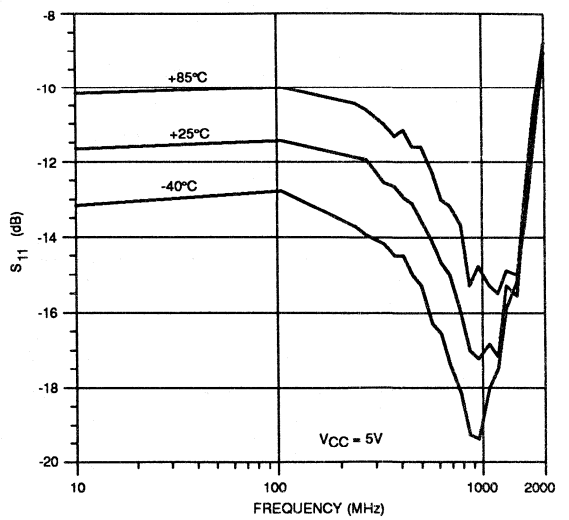


Figure 9. Input Match vs Frequency and Temperature

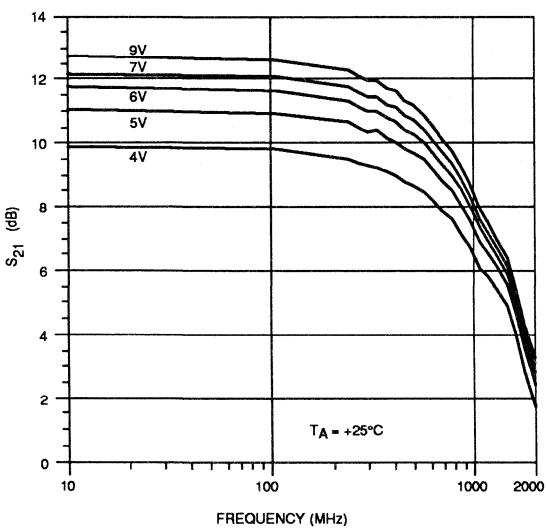


Figure 10. Insertion Gain vs Frequency and V_{CC}

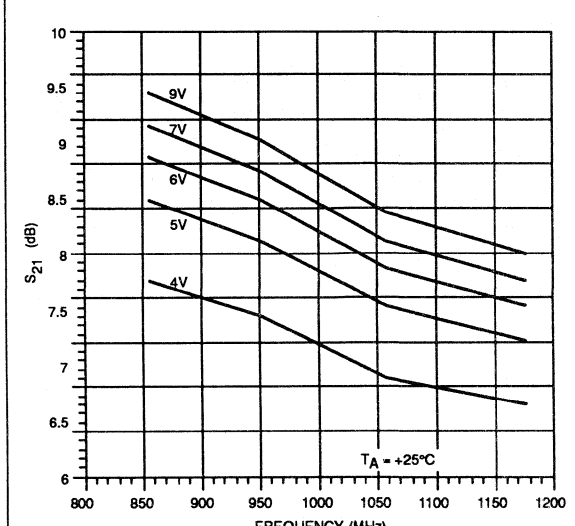


Figure 11. Insertion Gain vs Frequency and V_{CC} — Expanded Detail —

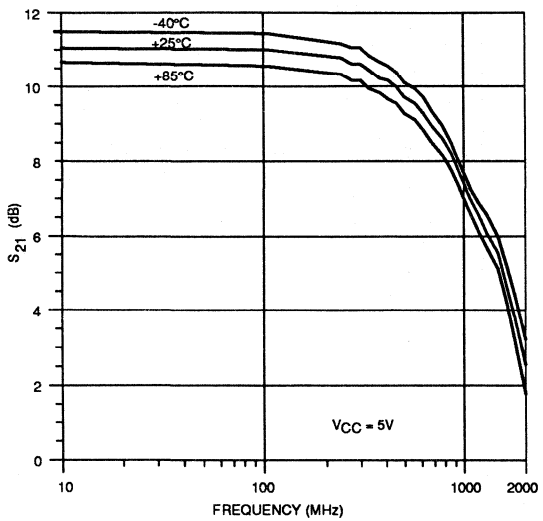


Figure 12. Insertion Gain vs Frequency and Temperature

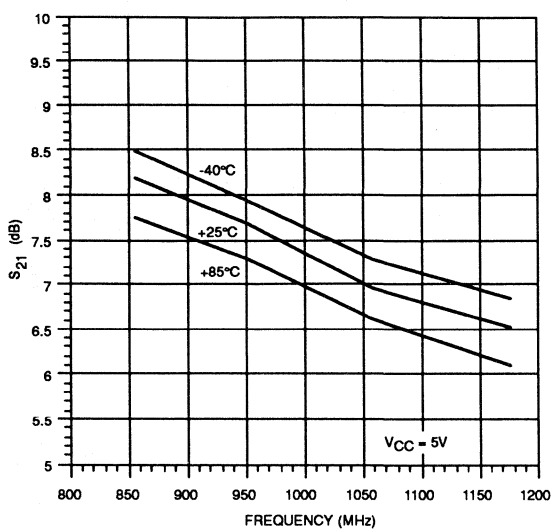


Figure 13. Insertion Gain vs Frequency and Temperature – Expanded Detail –

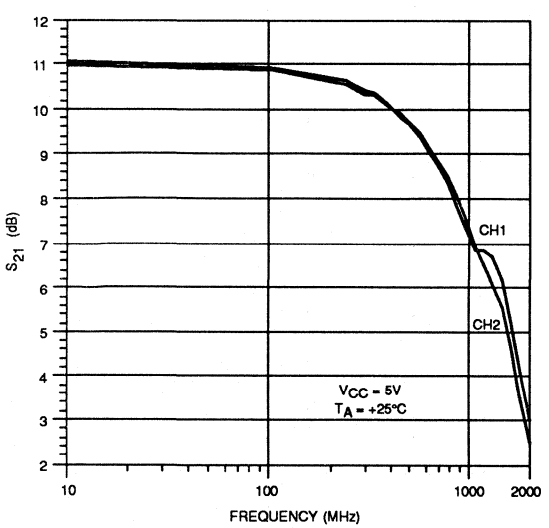


Figure 14. Insertion Gain Matching (CH1 vs CH2) vs Frequency

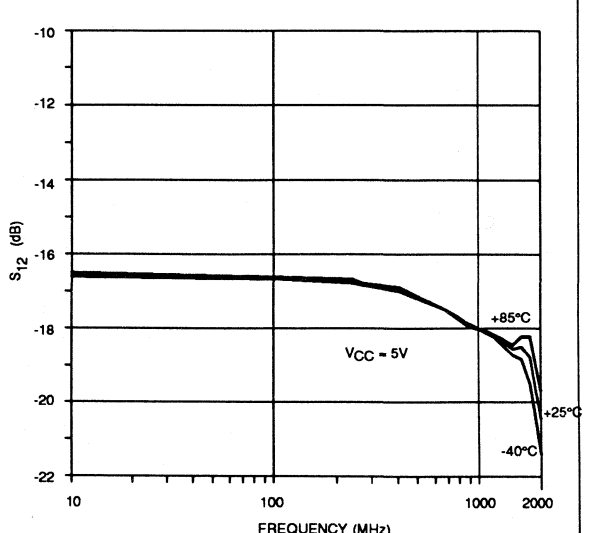


Figure 15. Reverse Insertion Gain vs Frequency and Temperature

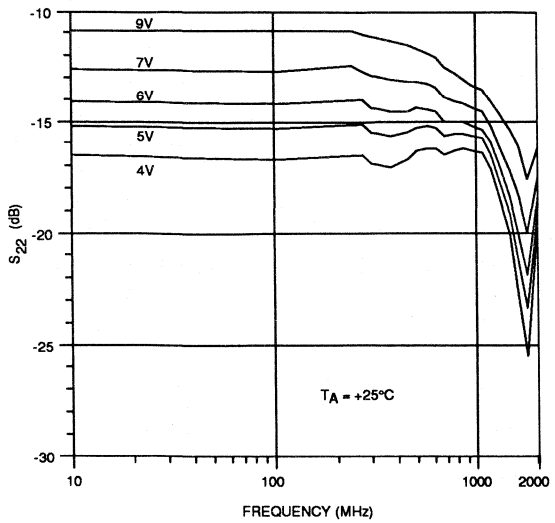


Figure 16. Output Match vs Frequency and V_{CC}

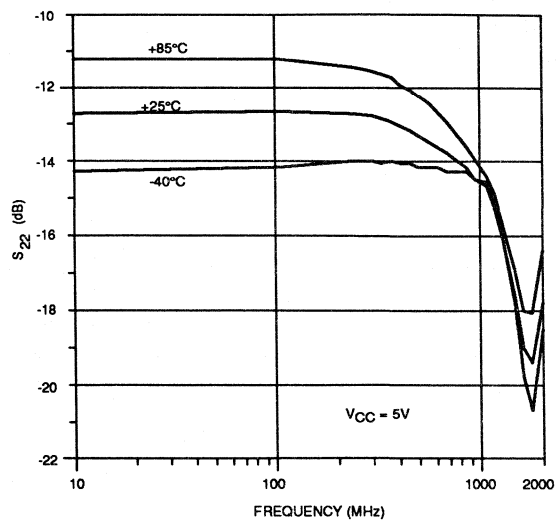


Figure 17. Output Match vs Frequency and Temperature

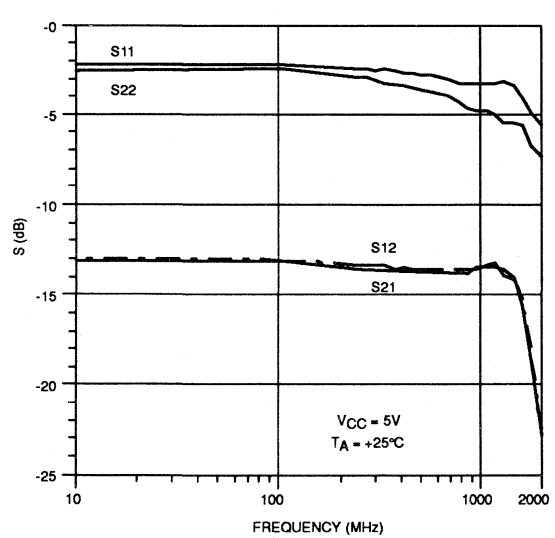


Figure 18. S-parameters vs Frequency for Disabled Amplifier

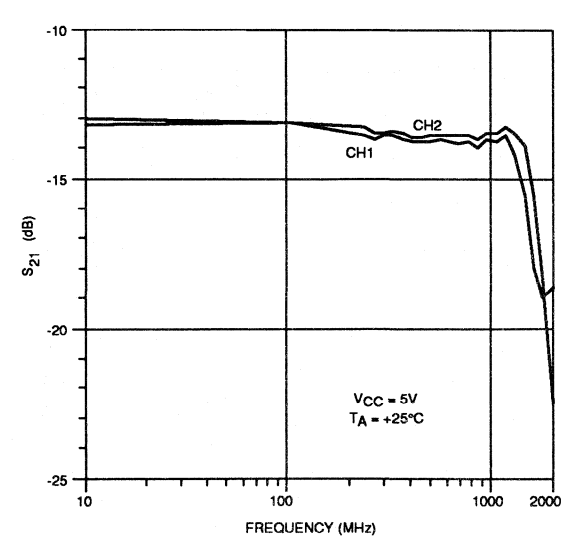


Figure 19. Insertion Gain Matching Disabled (CH1 vs CH2) vs Frequency

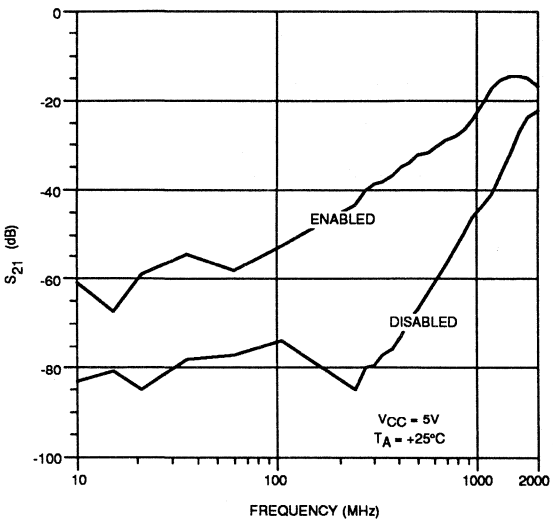


Figure 20. CH1 Input to CH2 Output Isolation vs Frequency

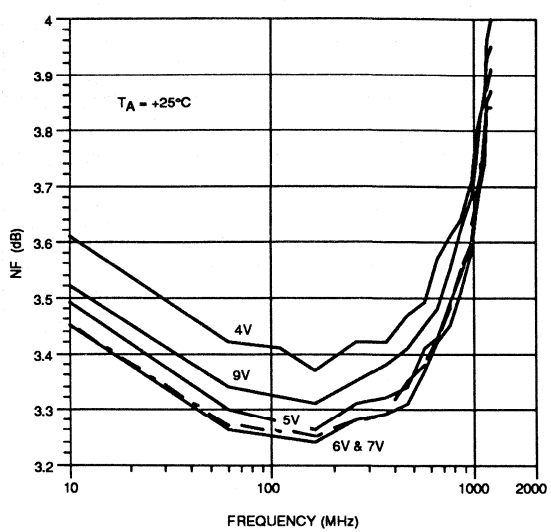


Figure 21. Noise Figure vs Frequency and V_{CC} in a 50Ω System

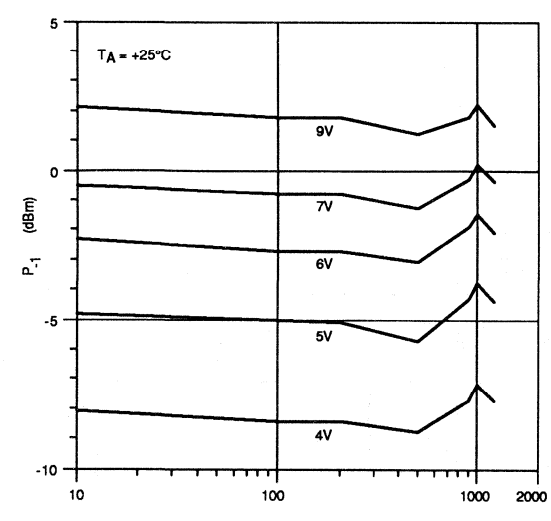


Figure 22. 1dB Output Compression Point vs Frequency and V_{CC}

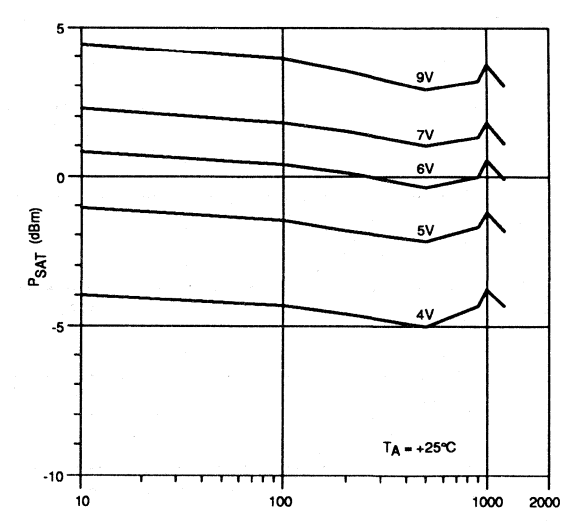


Figure 23. Saturated Output Power vs Frequency and V_{CC}

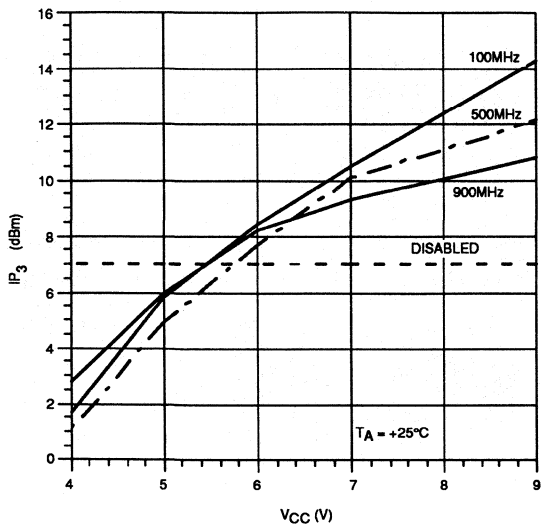


Figure 24. Third-Order Output Intercept vs Frequency and V_{CC}

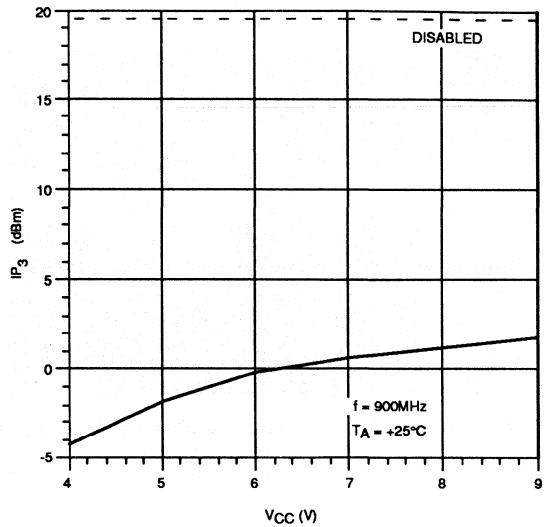


Figure 25. Third-Order Input Intercept vs Frequency and V_{CC}

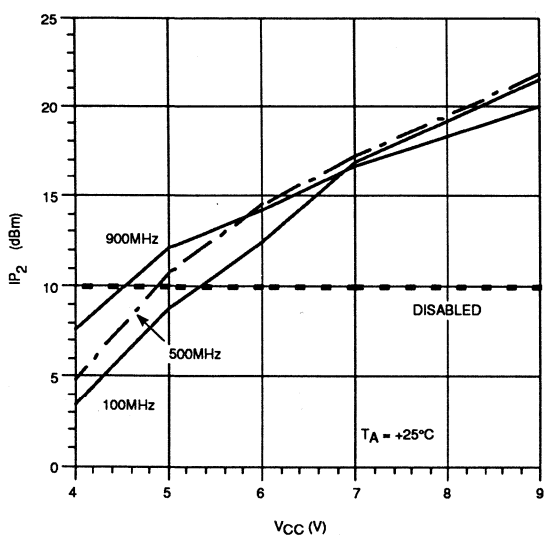


Figure 26. Second-Order Output Intercept vs Frequency and V_{CC}

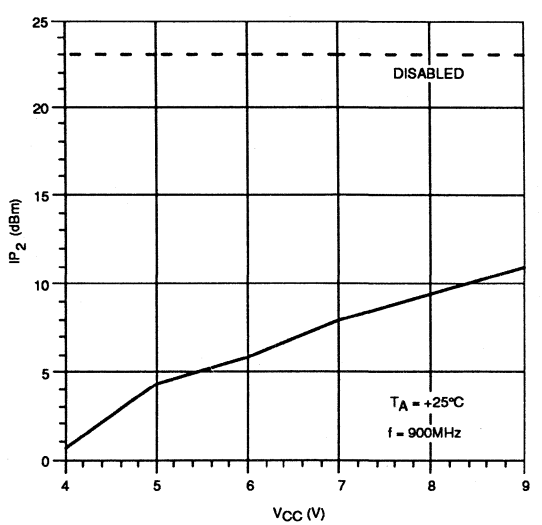


Figure 27. Second-Order Input Intercept vs Frequency and V_{CC}

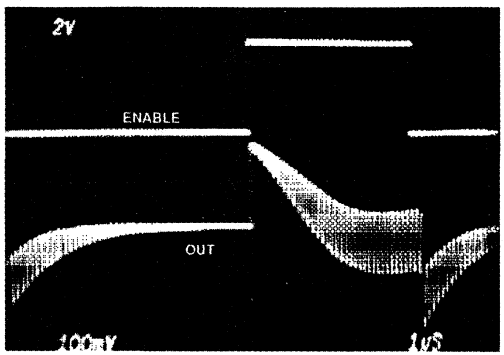


Figure 28. Switching Speed; f_{IN} = 10MHz at –26dBm, V_{DD} = 5V, Coupling Capacitors Set to 0.01μF

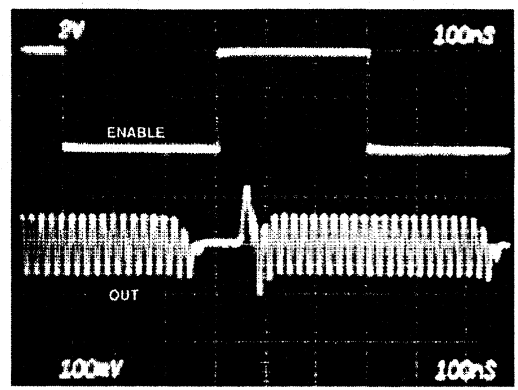


Figure 29. Switching Speed; f_{IN} = 50MHz at –26dBm, V_{DD} = 5V, Coupling Capacitors Set to 100pF

Wide-band high-frequency amplifier — NE/SA5204A

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC02 OR DATA SHEET

DESCRIPTION

The NE/SA5204A family of wideband amplifiers replaces the NE/SA5204 family. The 'A' parts are fabricated on a rugged 2µm bipolar process featuring excellent statistical process control. Electrical performance is nomically identical to the original parts.

The NE/SA5204A is a high-frequency amplifier with a fixed insertion gain of 20dB. The gain is flat to ±0.5dB from DC to 200MHz. The -3dB bandwidth is greater than 350MHz. This performance makes the amplifier ideal for cable TV applications. The NE/SA5204A operates with a single supply of 6V, and only draws 25mA of supply current, which is much less than comparable hybrid parts. The noise figure is 4.8dB in a 75Ω system and 6dB in a 50Ω system.

The NE/SA5204A is a relaxed version of the NE5205. Minimum guaranteed bandwidth is relaxed to 350MHz and the "S" parameter Min/Max limits are specified as typicals only.

Until now, most RF or high-frequency designers had to settle for discrete or hybrid solutions to their amplification problems. Most of these solutions required trade-offs that the designer had to accept in order to use high-frequency gain stages. These include high power consumption, large component count, transformers, large packages with heat sinks, and high part cost. The NE/SA5204A solves these problems by incorporating a wideband amplifier on a single monolithic chip.

The part is well matched to 50 or 75Ω input and output impedances. The standing wave ratios in 50 and 75Ω systems do not exceed 1.5 on either the input or output over the entire DC to 350MHz operating range.

Since the part is a small, monolithic IC die, problems such as stray capacitance are minimized. The die size is small enough to fit into a very cost-effective 8-pin small-outline (SO) package to further reduce parasitic effects.

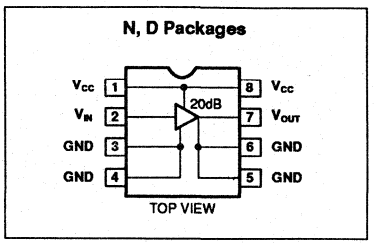
No external components are needed other than AC-coupling capacitors because the NE/SA5204A is internally compensated and matched to 50 and 75Ω. The amplifier has very good distortion specifications, with second and third-order intermodulation intercepts of +24dBm and +17dBm, respectively, at 100MHz.

The part is well matched for 50Ω test equipment such as signal generators, oscilloscopes, frequency counters, and all kinds of signal analyzers. Other applications at 50Ω include mobile radio, CB radio, and data/video transmission in fiber optics, as well as broadband LANs and telecom systems. A gain greater than 20dB can be achieved by cascading additional NE/SA5204As in series as required, without any degradation in amplifier stability.

FEATURES

- Bandwidth (min.)
  200 MHz, ±0.5dB
  350 MHz, -3dB
- 20dB insertion gain
- 4.8dB (6dB) noise figure ZO=75Ω (ZO=50Ω)
- No external components required
- Input and output impedances matched to 50/75Ω systems
- Surface-mount package available
- Cascadable
- 2000V ESD protection

PIN CONFIGURATION



APPLICATIONS

- Antenna amplifiers
- Amplified splitters
- Signal generators
- Frequency counters
- Oscilloscopes
- Signal analyzers
- Broadband LANs
- Networks
- Modems
- Mobile radio
- Security systems
- Telecommunications

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C –40 to +85°C	NE5204AN SA5204AN
8-Pin Plastic SO package	0 to +70°C –40 to +85°C	NE5204AD SA5204AD

Wide-band high-frequency amplifier — NE/SA/SE5205A

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC02 OR DATA SHEET

DESCRIPTION

The NE/SA/SE5205A family of wideband amplifiers replace the NE/SA/SE5205 family. The 'A' parts are fabricated on a rugged 2µm bipolar process featuring excellent statistical process control. Electrical performance is nominally identical to the original parts.

The NE/SA/SE5205A is a high-frequency amplifier with a fixed insertion gain of 20dB. The gain is flat to ±0.5dB from DC to 450MHz, and the -3dB bandwidth is greater than 600MHz in the EC package. This performance makes the amplifier ideal for cable TV applications. For lower frequency applications, the part is also available in industrial standard dual in-line and small outline packages. The NE/SA/SE5205A operates with a single supply of 6V, and only draws 24mA of supply current, which is much less than comparable hybrid parts. The noise figure is 4.8dB in a 75Ω system and 6dB in a 50Ω system.

Until now, most RF or high-frequency designers had to settle for discrete or hybrid solutions to their amplification problems. Most of these solutions required trade-offs that the designer had to accept in order to use high-frequency gain stages. These include high-power consumption, large component count, transformers, large packages with heat sinks, and high part cost. The NE/SA/SE5205A solves these problems by incorporating a wide-band amplifier on a single monolithic chip.

The part is well matched to 50 or 75Ω input and output impedances. The Standing Wave Ratios in 50 and 75Ω systems do not exceed 1.5 on either the input or output from DC to the -3dB bandwidth limit.

Since the part is a small monolithic IC die, problems such as stray capacitance are minimized. The die size is small enough to fit into a very cost-effective 8-pin small-outline (SO) package to further reduce parasitic effects.

No external components are needed other than AC coupling capacitors because the NE/SA/SE5205A is internally compensated and matched to 50 and 75Ω. The amplifier has very good distortion specifications, with second and third-order intermodulation intercepts of +24dBm and +17dBm respectively at 100MHz.

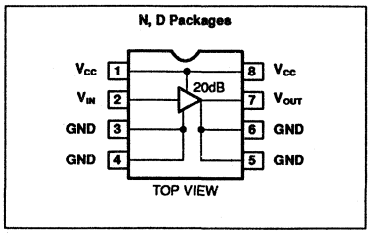
The device is ideally suited for 75Ω cable television applications such as decoder boxes, satellite receiver/decoders, and front-end amplifiers for TV receivers. It is also useful for amplified splitters and antenna amplifiers.

The part is matched well for 50Ω test equipment such as signal generators, oscilloscopes, frequency counters and all kinds of signal analyzers. Other applications at 50Ω include mobile radio, CB radio and data/video transmission in fiber optics, as well as broad-band LANs and telecom systems. A gain greater than 20dB can be achieved by cascading additional NE/SA/SE5205As in series as required, without any degradation in amplifier stability.

FEATURES

- 600MHz bandwidth
- 20dB insertion gain
- 4.8dB (6dB) noise figure ZO=75Ω (ZO=50Ω)
- No external components required
- Input and output impedances matched to 50/75Ω systems
- Surface mount package available
- MIL-STD processing available
- 2000V ESD protection

PIN CONFIGURATIONS



APPLICATIONS

- 75Ω cable TV decoder boxes
- Antenna amplifiers
- Amplified splitters
- Signal generators
- Frequency counters
- Oscilloscopes
- Signal analyzers
- Broad-band LANs
- Fiber-optics
- Modems
- Mobile radio
- Security systems
- Telecommunications

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO	0 to +70°C	NE5205AD
8-Pin Plastic DIP	0 to +70°C	NE5205AN
8-Pin Plastic SO	-40 to +85°C	SA5205AD
8-Pin Plastic DIP	-40 to +85°C	SA5205AN
8-Pin Plastic DIP	-55 to +125°C	SE5205AN

Document	853-1453
ECN No.	00223
Date of Issue	August 20, 1990
Status	Product Specification
RF Communications	

NE/SA5209

Wideband variable gain amplifier

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC11 OR DATA SHEET

DESCRIPTION

The NE5209 represents a breakthrough in monolithic amplifier design featuring several innovations. This unique design has combined the advantages of a high speed bipolar process with the proven Gilbert architecture.

The NE5209 is a linear broadband RF amplifier whose gain is controlled by a single DC voltage. The amplifier runs off a single 5 volt supply and consumes only 40mA. The amplifier has high impedance (1kΩ) differential inputs. The output is 50Ω differential. Therefore, the 5209 can simultaneously perform AGC, impedance transformation, and the balun functions.

The dynamic range is excellent over a wide range of gain setting. Furthermore, the noise performance degrades at a comparatively slow rate as the gain is reduced. This is an important feature when building linear AGC systems.

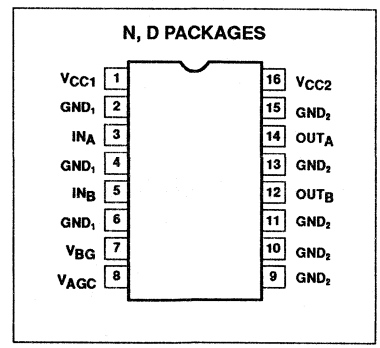
FEATURES

- Gain to 1.5GHz
- 850MHz bandwidth
- High impedance differential input
- 50Ω differential output
- Single 5V power supply
- 0 - 1V gain control pin
- >60dB gain control range at 200MHz
- 26dB maximum gain differential
- Exceptional $V_{CONTROL}$ / V_{GAIN} linearity
- 7dB noise figure minimum
- Full ESD protection
- Easily cascadable

APPLICATIONS

- Linear AGC systems
- Very linear AM modulator
- RF balun
- Cable TV multi–purpose amplifier
- Fiber optic AGC
- RADAR
- User programmable fixed gain block
- Video
- Satellite receivers
- Cellular communications

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic SO	0 to +70°C	NE5209D
16-Pin Plastic DIP	0 to +70°C	NE5209N
16-Pin Plastic SO	–40 to +85°C	SA5209D
16-Pin Plastic DIP	–40 to +85°C	SA5209N

Wideband variable gain amplifier — NE/SA5219

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC11 OR DATA SHEET

DESCRIPTION

The NE5219 represents a breakthrough in monolithic amplifier design featuring several innovations. This unique design has combined the advantages of a high speed bipolar process with the proven Gilbert architecture.

The NE5219 is a linear broadband RF amplifier whose gain is controlled by a single DC voltage. The amplifier runs off a single 5 volt supply and consumes only 40mA. The amplifier has high impedance (1kΩ) differential inputs. The output is 50Ω differential. Therefore, the 5219 can simultaneously perform AGC, impedance transformation, and the balun functions.

The dynamic range is excellent over a wide range of gain setting. Furthermore, the noise performance degrades at a comparatively slow rate as the gain is reduced. This is an important feature when building linear AGC systems.

FEATURES

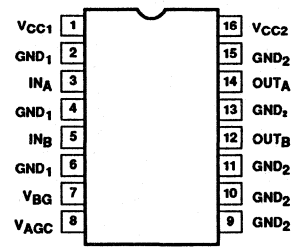
- 700MHz bandwidth
- High impedance differential input
- 50Ω differential output
- Single 5V power supply
- 0 - 1V gain control pin
- >60dB gain control range at 200MHz
- 26dB maximum gain differential
- Exceptional $V_{CONTROL}$ / V_{GAIN} linearity
- 7dB noise figure minimum
- Full ESD protection
- Easily cascadable

APPLICATIONS

- Linear AGC systems
- Very linear AM modulator
- RF balun
- Cable TV multi-purpose amplifier
- Fiber optic AGC
- RADAR
- User programmable fixed gain block
- Video
- Satellite receivers
- Cellular communications

PIN CONFIGURATION

N, D PACKAGES



ORDERING INFORMATION

Description	Temperature Range	Order Code	DWG #
16-Pin Plastic SO	0 to +70°C	NE5219D	0005
16-Pin Plastic DIP	0 to +70°C	NE5219N	0406
16-Pin Plastic SO	-40 to +85°C	SA5219D	0005
16-Pin Plastic DIP	-40 to +85°C	SA5219N	0406

Matched quad high-performance low-voltage operational amplifier

NE/SA5234

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC11 OR DATA SHEET

DESCRIPTION

The NE/SA5234 is a matched, low voltage, high performance quad operational amplifier. Among its unique input and output characteristics is the capability for both input and output rail-to-rail operation, particularly critical in low voltage applications. The output swings to less than 50mV of both rails across the entire power supply range. The NE/SA5234 is capable of delivering 5.5V peak-to-peak across a 600Ω load and will typically draw only 700μA per amplifier. The bandwidth is 2.5MHz and the 1% settling time is 1.4μs.

FEATURES

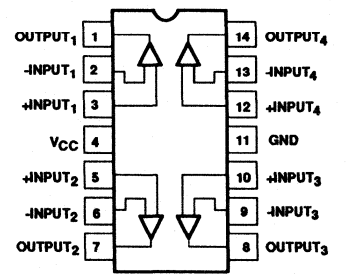
- Wide common-mode input voltage range: 250mV beyond both rails
- Output swing within 50mV of both rails
- Functionality to 1.8V typical
- Low current consumption: 700μA per amplifier
- ±15mA output current capability
- Unity gain bandwidth: 2.5MHz
- Slew rate: 0.8V/μs
- Low noise: 25nV/√Hz
- Electrostatic discharge protection
- Short-circuit protection
- Output inversion prevention

APPLICATIONS

- Automotive electronics
- Signal conditioning and sensing amplification
- Portable instrumentation
  - Test and measurement
  - Medical monitors and diagnostics
  - Remote meters
- Audio equipment
- Security systems
- Communications
  - Pagers
  - Cellular telephone
  - LAN
  - 5V Datacom bus
- Error amplifier in motor drives
- Transducer buffer amplifier

PIN CONFIGURATION

N, and D PACKAGES



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic SO	0 to +70°C	NE5234D
14-Pin Plastic DIP	0 to +70°C	NE5234N
14-Pin Plastic SO	-40 to +85°C	SA5234D
14-Pin Plastic DIP	-40 to +85°C	SA5234N

Document	853-1451
ECN No.	00210
Date of Issue	August 17, 1990
Status	Product Specification
RF Communications	

NE/SA5750

Audio processor – companding and amplifier section

special components for cellular radio

DESCRIPTION

The NE/SA5750 is a high performance low power audio signal processing system. The NE/SA5750 subsystems include a low noise microphone preamplifier with adustable gain, a noise cancellation switching amplifier with adjustable threshold, a voice operated transmitter (VOX) switch, VOX control, an audio compressor with buffered input, audio expandor, a unity gain power amplifier to drive a speaker, a summing power amplifier for sidetone attenuation and headphone (earpiece) drive, and an internal bandgap voltage regulator with power down capability. When used with Signetics' NE/SA5751, the complete audio processing function of an AMPS or TACS cellular telephone is easily implemented. The NE/SA5750 can also be used without the NE/SA5751 in a wide variety of radio communications applications.

FEATURES

- High performance
- 5V supply
- Adjustable VOX and noise cancellation threshold
- Adjustable gain preamplifier
- Audio companding
- ESD protected
- Open collector VOX output
- Logic inputs CMOS compatible
- Power down mode
- Built-in drivers for speaker and earpiece
- Few external components
- SOL and DIP packages

BENEFITS

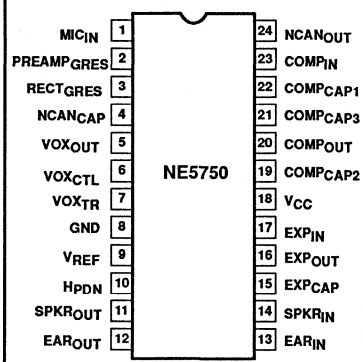
- Very compact applications
- Long battery life in portable equipment
- Complete cellular audio function with the SA5751

APPLICATIONS

- Cellular radio
- Mobile communications
- High performance cordless telephones
- 2-way radio

PIN CONFIGURATION

D[1] and N PACKAGE



NOTE:
1. Available only in SOL (large SO) package.

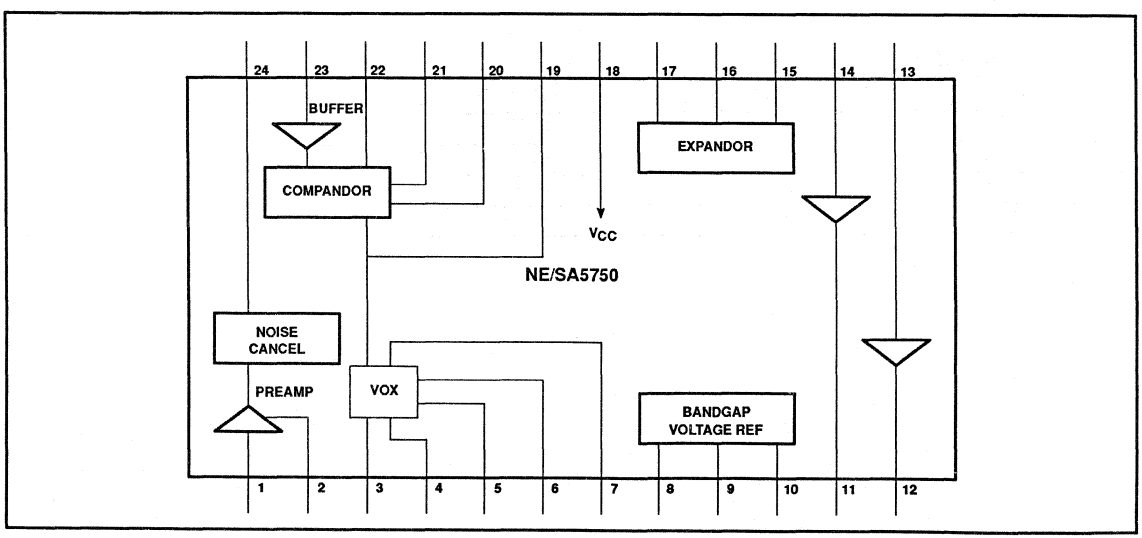
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
24-Pin Plastic DIP	0 to +70°C	NE5750N
24-Pin Plastic SOL	0 to +70°C	NE5750D
24-Pin Plastic DIP	–40 to +85°C	SA5750N
24-Pin Plastic SOL	–40 to +85°C	SA5750D

PIN DESCRIPTIONS

PIN NO.	SYMBOL	DESCRIPTION
1	MIC_{IN}	Microphone input
2	$PREAMP_{GRES}$	Preamplifier gain resistor
3	$RECT_{GRES}$	Reactifier gain resistor
4	$NCAN_{CAP}$	Noise cancellation timing capacitor
5	VOX_{OUT}	Voice operated transmission output
6	VOX_{CTL}	Voice operated transmission control
7	VOX_{TR}	Voice operated transmission threshold resistor
8	GND	Ground
9	V_{REF}	Reference voltage
10	H_{PDN}	Hardware power down
11	$SPKR_{OUT}$	Speaker output
12	EAR_{OUT}	Earpiece output
13	EAR_{IN}	Earpiece input, side tone input
14	$SPKR_{IN}$	Speaker input
15	EXP_{CAp}	Expandor timing capacitor
16	EXP_{OUT}	Expandor output
17	EXP_{IN}	Expandor input
18	V_{CC}	Positive supply
19	$COMP_{CAP2}$	Compressor timing capacitor 2
20	$COMP_{OUT}$	Compressor output
21	$COMP_{CAP3}$	Compressor timing capacitor 3
22	$COMP_{CAP1}$	Compressor timing capacitor 1
23	$COMP_{IN}$	Compressor input
24	$NCAN_{OUT}$	Noise cancellation output

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply voltage Voltage applied to any pin	6 –0.3 to (V_{CC} + 0.3)	V V
T_{STG}	Storage temperature	–65 to +150	°C
T_A	Ambient operating temperature NE5750 SA5750	 0 to 70 –40 to +85	°C

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = +5.0V, 0dB = 77.5mV_{RMS}. See test circuit, Figure 4.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
V_{CC}	Supply voltage		4.75	5.0	5.25	V
I_{CC}	Supply current	No signal Power down mode		8.4 1.8	12.0 3.0	mA mA
Z_L	Load impedance pins $NCAN_{OUT}$, EXP_{OUT}		50			kΩ
	$COMP_{OUT}$[1]		10			kΩ
Z_{IN}	Input impedance $COMP_{IN}$, MIC_{IN}, $SPKR_{IN}$		40	50	60	kΩ
	EXP_{IN}[2]		2.0	2.5		kΩ
	Noise cancellation current	Pin 7, grounded	40	50	60	µA
V_{OS}	DC offset $NCAN_{OUT}$[3]		–50		50	mV

NOTES:
1. Compressor is tested in production with 50kΩ load.
2. Not tested in production.
3. Offset values are identical for both gain states of noise reduction circuit.

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = +5.0V, 0dB level = 77.5mV_{RMS}. See test circuit, Figure 4.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
	Preamplifier gain range Preamplifier voltage gain 0dB Preamplifier voltage gain 40dB	 Pin 2 open Pin 2 AC ground	0 –1.0 39.0	 0 40	40 1.0 41.0	dB dB dB
	Preamplifier noise density	Pin 2 AC grounded RS = 0 – 50kΩ unweighted 20Hz–20kHz		7		$nV/\sqrt{Hz}$
		weighted CCIR DIN45405 20–20kHz		8		$nV/\sqrt{Hz}$
	Switch amplifier gain		9	10	11	dB
	Sidetone attenuation range				30	dB
Compandor 1kHz, all tests[1]						
$COMP_{OUT}$	Compressor error at –21dB output level	Input level = –42dB		0.38		dB
$COMP_{OUT}$	Compressor error at –10dB output level	Input level = –20dB	–1.0		1.0	dB
$COMP_{OUT}$	Compressor error at 0dB output level	Input level = 0dB	–1.5	0.12	1.5	dB
$COMP_{OUT}$	Compressor error at +5dB output level	Input level = +10dB	–1.0		1.0	dB
$COMP_{OUT}$	Compressor error at +12.3dB output level	Input level = +24.6dB	–1.0		1.0	dB
EXP_{OUT}	Expandor error at –42dB output level	Input level = –21dB		–0.41		dB
EXP_{OUT}	Expandor error at –21dB output level	Input level = –10.5dB	–1.0		1.0	dB

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = +5.0V$, 0dB level = $77.5mV_{RMS}$. See test circuit, Figure 4.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
EXP_{OUT}	Expandor error at –10dB output level	Input level = –5dB	–1.0		1.0	dB
EXP_{OUT}	Expandor error at 0dB output level	Input level = 0dB	–1.5	–0.18	1.5	dB
EXP_{OUT}	Expandor error at +10dB output level	Input level = +5dB	–1.0		1.0	dB
EXP_{OUT}	Expandor error at +24.6dB output level[2]	Input level = +12.3dB	–1.5		1.5	dB
EXP_{OUT}	Expandor V_{OS}	No signal	–50.0		50.0	mV
EXP_{OUT}	Expandor output DC shift	No signal to 0dB	–100		100	mV
	Timing capacitors compandor			2.2		µF
THD	Total harmonic distortion					
	Compressor	1kHz, 0dB		0.09	1	%
	Expandor	1kHz, 0dB		0.09	1	%
	$NCAN_{OUT}$	1kHz. Pin 2 open output level = 0dB		0.18	1	%
		1kHz, Pin 2 open output level = +25dB		0.13	1	%
	Speaker amplifier Drive capability				40	mA_{P-P}
	Output swing (<1% THD)	50Ω load	2	3.2		V_{P-P}
		100Ω load	3	4.1		V_{P-P}
		No load	4	4.9		V_{P-P}
	Ear amplifier Drive capability				10	mA_{P-P}
	Output swing (<1% THD)	300Ω load	3	4.3		V_{P-P}
		2000Ω load	4	4.9		V_{P-P}
		No load	4	4.9		V_{P-P}
VOX_{OUT}	Sink current				0.5	mA
	Low level High level	Open collector $I_L = 0.5mA$	 4	0.07 5	0.4	V V
VOX_{CTL}	Input current Low		–50	–21	0	µA
	High		–10		+10	µA
	Input level Low High		0 3.5		1.5 5	V V
H_{PDN}	Input current Low		–10		+10	µA
	High		–10		+10	µA
	Input level Low High		0 3.5		1.5 5	V V
	Reference filter capacitor			10		µF

NOTE:
1. Measurements are relative to 0dB output.
2. Measurement is absolute and indicative of the output dynamic range capability.

Audio processor – companding and amplifier section NE/SA5750

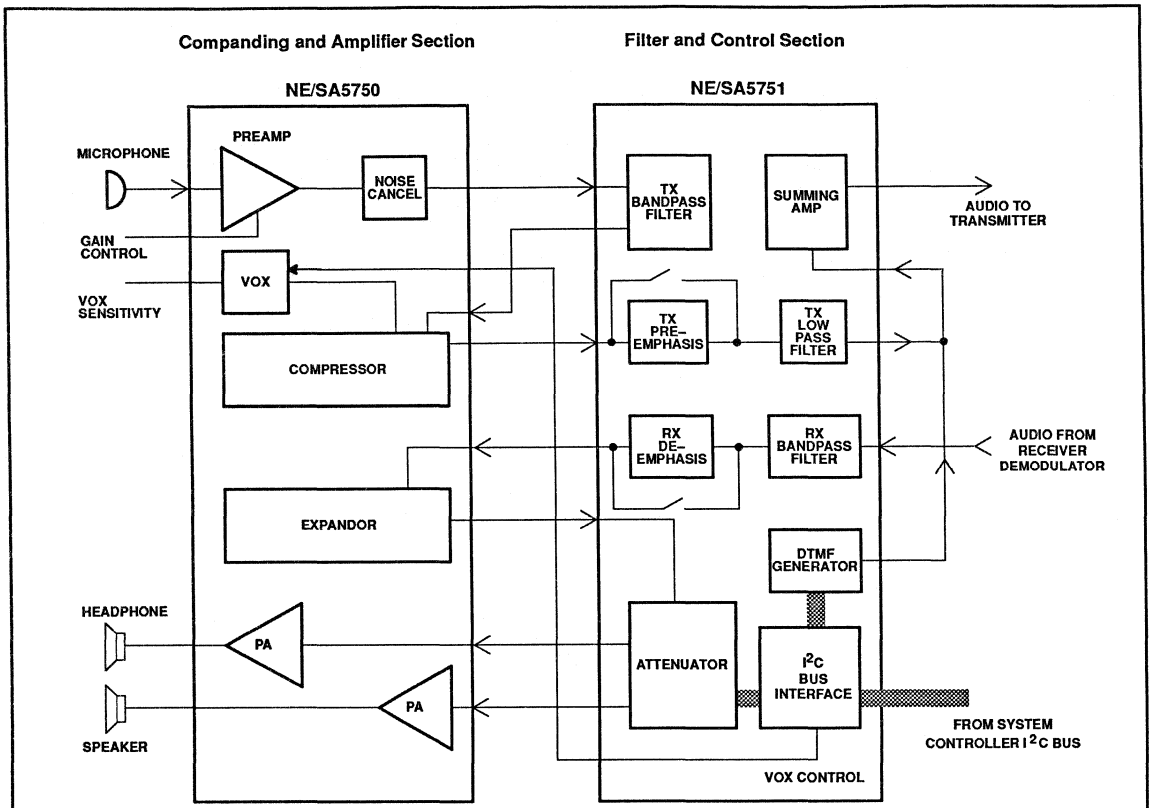


Figure 1. Typical Configuration of Audio Processor (APROC) System Chip Set

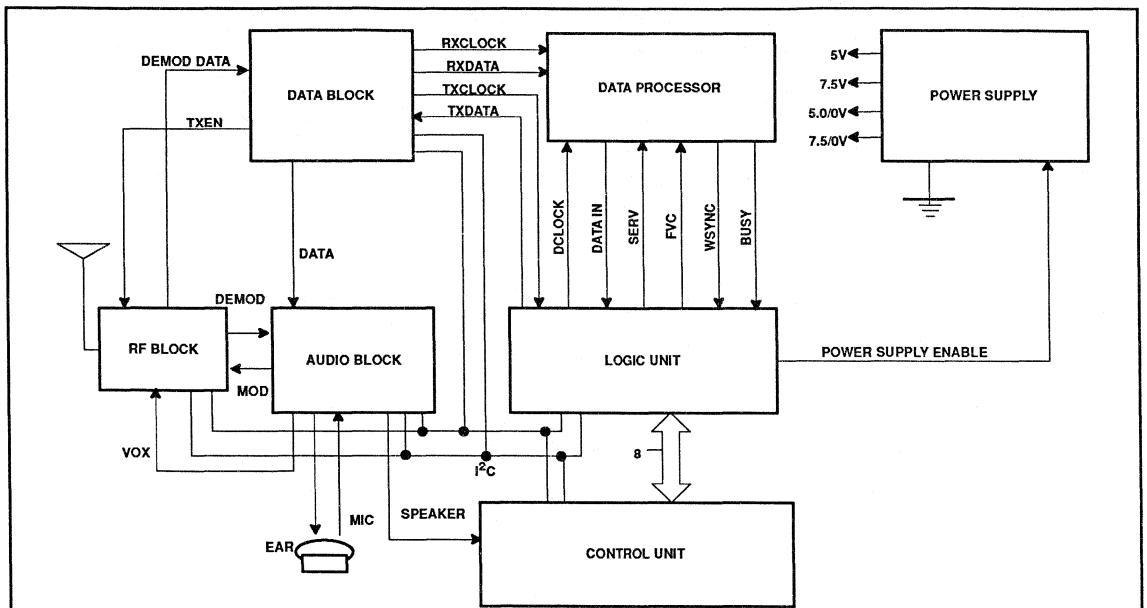


Figure 2. Cellular Radio System

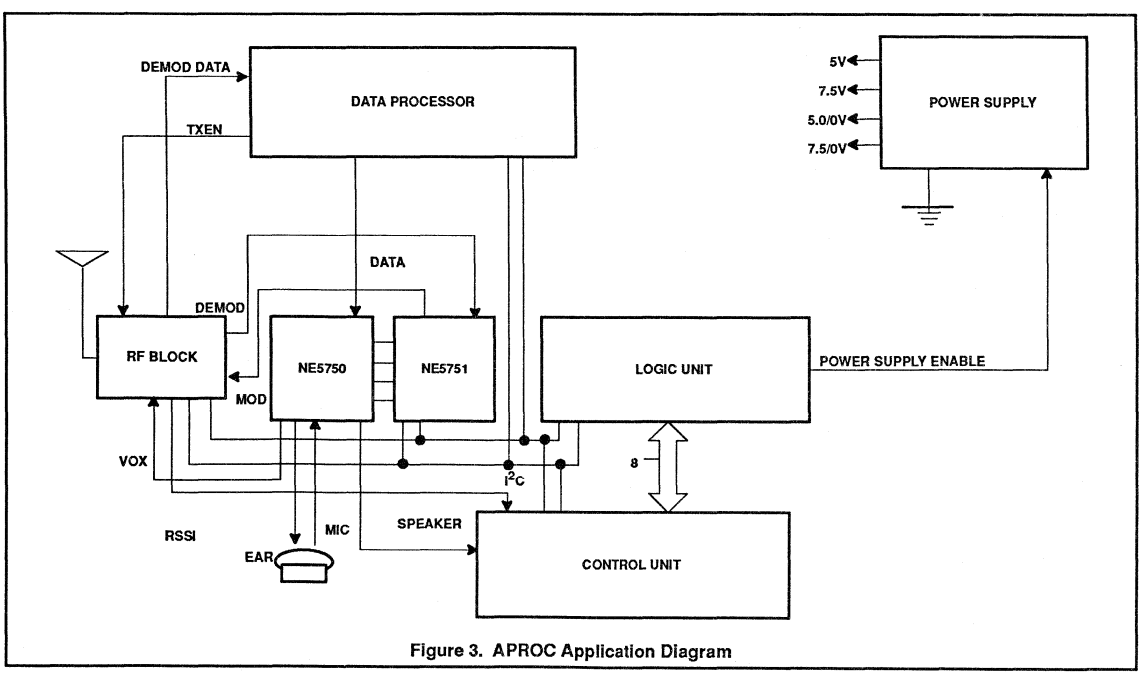


Figure 3. APROC Application Diagram

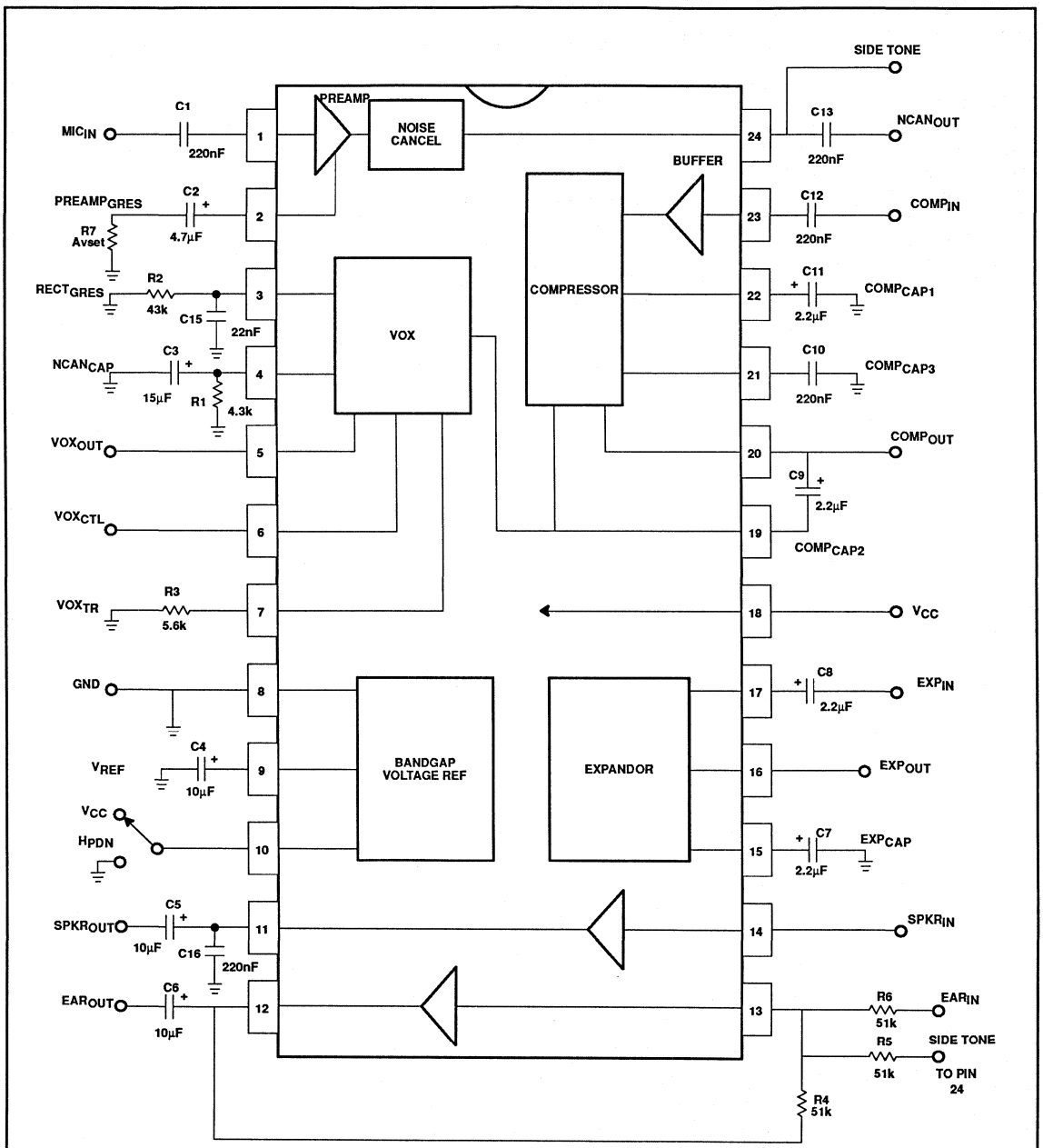


Figure 4. NE/SA5750 Test and Application Circuit

Philips Semiconductors

Document	853-1452
ECN No.	00211
Date of Issue	August 17, 1990
Status	Product Specification
RF Communications	

NE/SA5751

Audio processor – filter and control section

special components for cellular radio

DESCRIPTION

The NE/SA5751 is a high performance low power CMOS audio signal processing system. The NE/SA5751 subsystems include complementary transmit/receive voice band (300–3000Hz), switched capacitor bandpass filters with pre-emphasis and de-emphasis respectively, a transmit low pass filter, peak deviation limiter for transmit, a digitally controlled volume control with 30dB range (in 2dB steps), audio path mute switches, a programmable DTMF generator, power-down circuitry for low current standby, power-on reset capability, and an I²C interface. When the SA5751 is used with an SA5750 (companding function), the complete audio processing system of an AMPs or TACs cellular telephone is easily implemented.

FEATURES

- Low power
- High performance
- 5V supply
- Built-in programmable DTMF generator
- Built-in digitally controlled volume control
- Built-in peak-deviation limit
- I²C Bus controlled
- Power-on reset
- Power-down capability

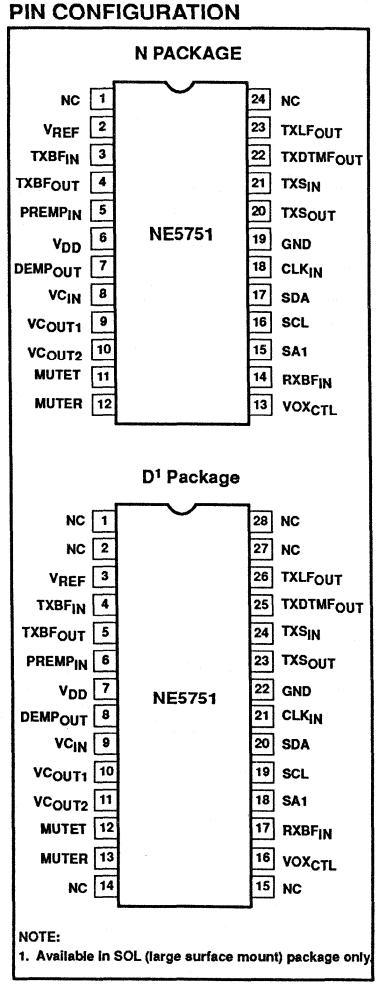
BENEFITS

- Very compact application
- Long battery life in portable equipment
- Complete cellular audio function with the SA5750

APPLICATIONS

- Cellular radio
- Mobile communications
- High performance cordless telephones
- 2-way radio

PIN CONFIGURATION



NOTE:
1. Available in SOL (large surface mount) package only.

ORDERING INFORMATION

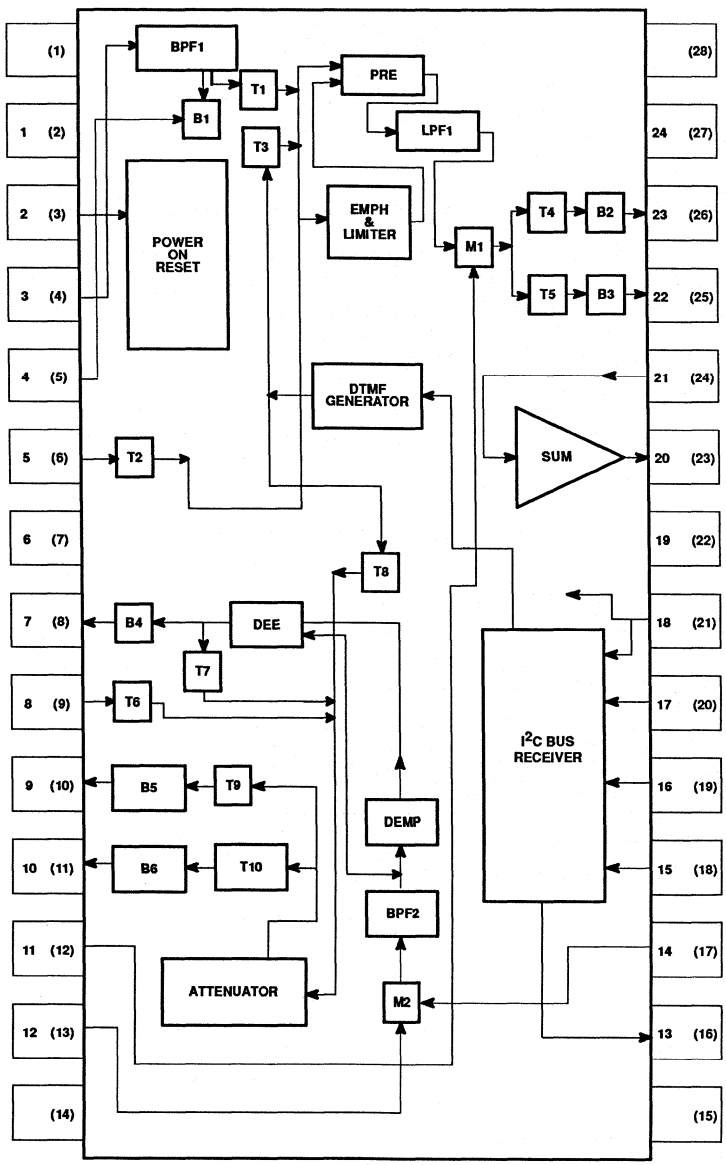
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
24-Pin Plastic DIP	0 to +70°C	NE5751N
28-Pin Plastic SOL	0 to +70°C	NE5751D
24-Pin Plastic DIP	–40 to +85°C	SA5751N
28-Pin Plastic SOL	–40 to +85°C	SA5751D

PIN DESCRIPTIONS

PIN NO.		SYMBOL	DESCRIPTION
	(1)	NC	Not connected
1	(2)	NC	Not connected
2	(3)	V_{REF}	Reference voltage
3	(4)	$TXBF_{IN}$	Transmit bandpass filter input
4	(5)	$TXBF_{OUT}$	Transmit bandpass filter output
5	(6)	$PREMP_{IN}$	Pre–emphasis input
6	(7)	V_{DD}	Positive supply
7	(8)	$DEMP_{OUT}$	De–emphasis output
8	(9)	VC_{IN}	Volume control input
9	(10)	VC_{OUT1}	Volume control output 1
10	(11)	VC_{OUT2}	Volume control output 2
11	(12)	MUTET	TX analog voice path mute input
12	(13)	MUTER	RX analog voice path mute input
	(14)	NC	Not connected
	(15)	NC	Not connected
13	(16)	VOX_{CTL}	Vox control output
14	(17)	$RXBF_{IN}$	Receive bandpass filter input
15	(18)	SA1	Serial bus address
16	(19)	SCL	Serial clock line
17	(20)	SDA	Serial data line
18	(21)	CLK_{IN}	Clock input
19	(22)	GND	Ground
20	(23)	TXS_{OUT}	Transmit summer output
21	(24)	TXS_{IN}	Transmit summer input
22	(25)	$TXDTMF_{OUT}$	Transmit DTMF output
23	(26)	$TXLF_{OUT}$	Transmit low–pass filter output
24	(27)	NC	Not connected
	(28)	NC	Not connected

NOTE:
1. Callouts are for N package; those in parentheses are for the D (SOL) package.

BLOCK DIAGRAM



NOTES:
1. T1 to T10 represent the signal path switches.
2. M1 and M2 represent the mute switches.
3. PRE and DEE represent the bypass switches for pre–emphasis and de–emphasis, respectively.
4. B1 to B6 represent the output buffers.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
	Power supply voltage[1]	6	V
T_{STG}	Storage temperature	–65 to +150	°C
T_A	Ambient operating temperature NE5751	0 to 70	°C
	SA5751	–40 to +85	°C

NOTE:
1. Voltage applied to any pin –0.3 to V_{DD} +0.3V

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{DD} = +5.0V, unless otherwise specified. See test circuit, Figure 4.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
V_{DD}	Power supply voltage range		4.75	5.0	5.25	V
I_{DD}	Supply current	Operating Standby		2.7 0.9	5.0 2.0	mA mA

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{DD} = +5.0V. See test circuit, Figure 4. Clock frequency = 1.2MHz; test level = 0dBV = 77.5mV_{RMS} = –20dBm, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
	RX BPF anti alias rejection			40		dB
	RX BPF input impedance	f= 1kHz		500		kΩ
	RX BPF gain with de–emphasis	f = 1kHz	–0.5	0	0.5	dB
	RX BPF gain with de–emphasis	f = 100Hz		–31	–29	dBm0
	RX BPF gain with de–emphasis	f = 300Hz	9.0	9.6	11.0	dBm0
	RX BPF gain with de–emphasis	f = 3kHz	–11.0	–10.0	–9.0	dBm0
	RX BPF gain with de–emphasis	f = 5.9kHz		–68	–50	dBm0
	RX BPF noise with de–emphasis	300Hz–3kHz		170		μV_{RMS}
	RX dynamic range	with deemphasis		80		dB
	$DEMP_{OUT}$ output impedance	f = 1kHz		40		Ω
	$DEMP_{OUT}$ output swing (1%)	2.3kΩ to V_{REF}; f = 1kHz	V_{DD} –3	3.5		V_{P-P}
	VC_{OUT1} ouput swing (1%)	50kΩ toV_{REF}; f = 1kHz	V_{DD} –1	4.5		V_{P-P}
	VC_{OUT2} output swing (1%)	50kΩ to V_{REF}; f = 1kHz	V_{DD} –1	4.5		V_{P-P}
	VC_{OUT1} noise	VC_{IN} grounded C – message		25		μV_{RMS}
	VC_{OUT2} noise	VC_{IN} grounded C – message		25		μV_{RMS}
	Mute threshold off		0		0.8	V
	Mute threshold on		2.0		5.0	V
	CLK1, 2 high		4.0		5.0	V
	CLK1, 2 low		0		1.0	V
	TX BPF anti alias rejection			40		dB
	TX BPF input impedance	f = 3kHz		500		KΩ

AC ELECTRICAL CHARACTERISTICS (continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
	TX BPF noise	300 – 3000kHz		90		μV_{RMS}
	TX LPF gain	f = 5.9kHz		–39	–36	dB
	TX LPF gain with pre–emphasis	f = 1kHz, 20dBV		12.06		dB
	TX LPF gain with pre–emphasis	f = 100Hz		–19		dBm0
	TX LPF gain with pre–emphasis	f = 300Hz		–10.45		dBm0
	TX LPF gain with pre–emphasis	f = 3kHz		9.14		dBm0
	TX LPF gain with pre–emphasis	f = 5900Hz		–39		dBm0
	TX LPF gain with pre–emphasis	f = 9kHz		–51		dBm0
	TX overall gain	1kHz	11.3	11.8	12.5	dB
	TX overall gain	100Hz		–47	–45	dBm0
	TX overall gain	300Hz	–11	–10.4	–9	dBm0
	TX overall gain	3kHz	8	9	9.6	dBm0
	TX overall gain	5.9kHz		–52	–45	dBm0
	TX BPF output impedance	f = 1kHz		360		Ω
	TX BPF output swing (1%THD)	50kΩ to V_{REF} f = 1kHz		4.5		V_{P-P}
	TX BPF dynamic range			90		dB
	$PREMP_{IN}$ input impedance	f = 3kHz		500		kΩ
	Summing op amp					
	Slew rate	C_L = 15pF		0.75		V/µs
	Output impedance	Unity gain; f = 3kHz		40		Ω
	Output swing (1% THD)	1kHz, 5kΩ load (25°C)		4.3		V_{P-P}
	Volume control accuracy	–30dB to 0dB	–1	0	+1	dB
	Analog switches					
	Insertion loss			60		dB
	On time transition	MUTET, MUTER 0.8V –>2.0V		3		µs
	Off time transition	MUTET, MUTER 2.0V –>0.8V		0.25		µs

I²C CHARACTERISTICS

The I²C bus is for 2–way, 2–line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both SDA and SCL are bidirectional lines connected to a positive supply voltage via a pull–up resistor. When the bus is free, both lines are high. Data transfer may be initiated only when the bus is not busy.

The output devices, or stages, connected to the bus must have an open drain or open collector output in order to perform the wired–AND function.

Data at the I²C bus can be transferred at a rate up to 100kbits/s. The number of devices connected to the bus is solely dependent on the maximum allowed bus capacitance of 400pF.

Due to the variety of different devices which can be connected to the I²C bus, the levels of the logical "0" and "1" are not fixed and depend on the appropriate level of V_{DD}. For the typical supply voltage of 5V which is chosen here, logical "1" and logical "0" are, however, fixed respectively on maximum input LOW voltage, 1.5V and minimum input HIGH voltage, 3.0V.

BIT TRANSFER

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock's cycle. If it does not remain HIGH, it may be interrupted as a control signal.

START AND STOP CONDITIONS

Both data and clock lines remain HIGH when the bus is not busy. A HIGH to LOW transition of the data line while the clock line is HIGH is defined as a start condition S. A LOW to HIGH transition of the data line while the clock is HIGH is defined as a stop condition.

SYSTEM CONFIGURATIONS

A device generating a message is a "transmitter"; a device receiving a message is the "receiver". The device that controls the message is the "master"; and devices which are controlled by the master are the "slaves".

ACKNOWLEDGE

The number of data bytes transferred between the start and the stop condition from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; set up and hold times must be taken into account.

I²C BUS DATA CONFIGURATIONS

The NE5751 is always a slave receiver in the I²C bus configuration (R/W bit–0). The slave address consists of seven bits in the serial mode where the least significant bit is selectable by hardware on input A0 and the other more significant bits are internally fixed.

POWER ON RESET

In order to avoid undefined states of the NE5751 when the power is switched on, a power on reset is supplied. The reset is active when Pin V_{REF} is held below 0.8V. The reset is off when Pin V_{REF} is above 2.0V. Pin V_{REF} is normally at 2.5V generated by a resistive divider from V_{DD}. Nominal impedance is 20kΩ. In a typical application a capacitor is connected to Pin V_{REF} to improve power supply rejection. The time delay of the network resets the internal registers when power is first applied. The signal paths are off in the reset condition. The NE5751 must be programmed via the I²C bus for normal operation. The Power Down mode is defined only when all register values are zero.

CONTROL REGISTERS

Register Map

The address register is as follows:

MSB							LSB
A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	0	0	0	SA1	0

SA1 is controlled by serial bus address pin.

Signal Path Register

MSB							LSB
T10	T9	T8	T6	VOX_{EN}	T4	T3T5	T2

T2 is the transmission gate between Pin $PREEMP_{IN}$ and the emphasis input.

T3T5 connects the output of the DTMF generator to the emphasis input and connects the output of the XMT LPF to Pin $TXDTMF_{OUT}$.

T4 connects the output of the XMT LPF to Pin $TXLF_{OUT}$.

VOX_{EN} enables the VOX function of NE5750.

T6 connects Pin VC_{IN} to the volume control.

T8 connects the output of the DTMF generator to the volume control.

T9 enables VC_{OUT1}.

T10 enables VC_{OUT2}.

Volume Control and Test Register

MSB							LSB
PDW	T1T7	DEE	PRE	V1	V2	V3	V4

V4 is volume control bit 4. This is the MSB. A zero is 16dB attenuation.

V3 is volume control bit 3. A zero is 8dB attenuation.

V2 is volume control bit 2. A zero is 4dB attenuation.

V1 is volume control bit 1. A zero is 2dB attenuation.

PRE is the bypass for the pre–emphasis.

DEE is the bypass for the de–emphasis.

T1T7 is the bypass for the compressor and expandor.

PDW is the control for power down mode.

This mode is defined only when all register values are reset to zero.

High Tone DTMF Register

MSB							LSB
HD7	HD6	HD5	HD4	HD3	HD2	HD1	HD0

The eight bits determine the output frequency by the following formula.:

High Frequency = 1200kHz/6/HD
where HD is the value of the register.

Low Tone DTMF Register

MSB							LSB
LD7	LD6	LD5	LD4	LD3	LD2	LD1	LD0

The eight bits determine the output frequency by the following formula.:

Low Frequency = 1200kHz/12/LD
where LD is the value of the register.

The operation of the 96ms DTMF timer is initiated by the loading of the low tone DTMF register. This timer terminates transmission of the tones as the generated tones cross the reference level after 96ms. The on time of the tones can thus vary by up to one cycle of the tones.

Continuous tones can be obtained by again loading the two DTMF registers before 96ms have elapsed.

Single tones can be obtained by loading 0, 1 or 2 into one of the registers to silence it.

Phase continuous frequency modulation can be produced by loading a new value into a DTMF register during operation.

Audio processor – filter and control section NE/SA5751

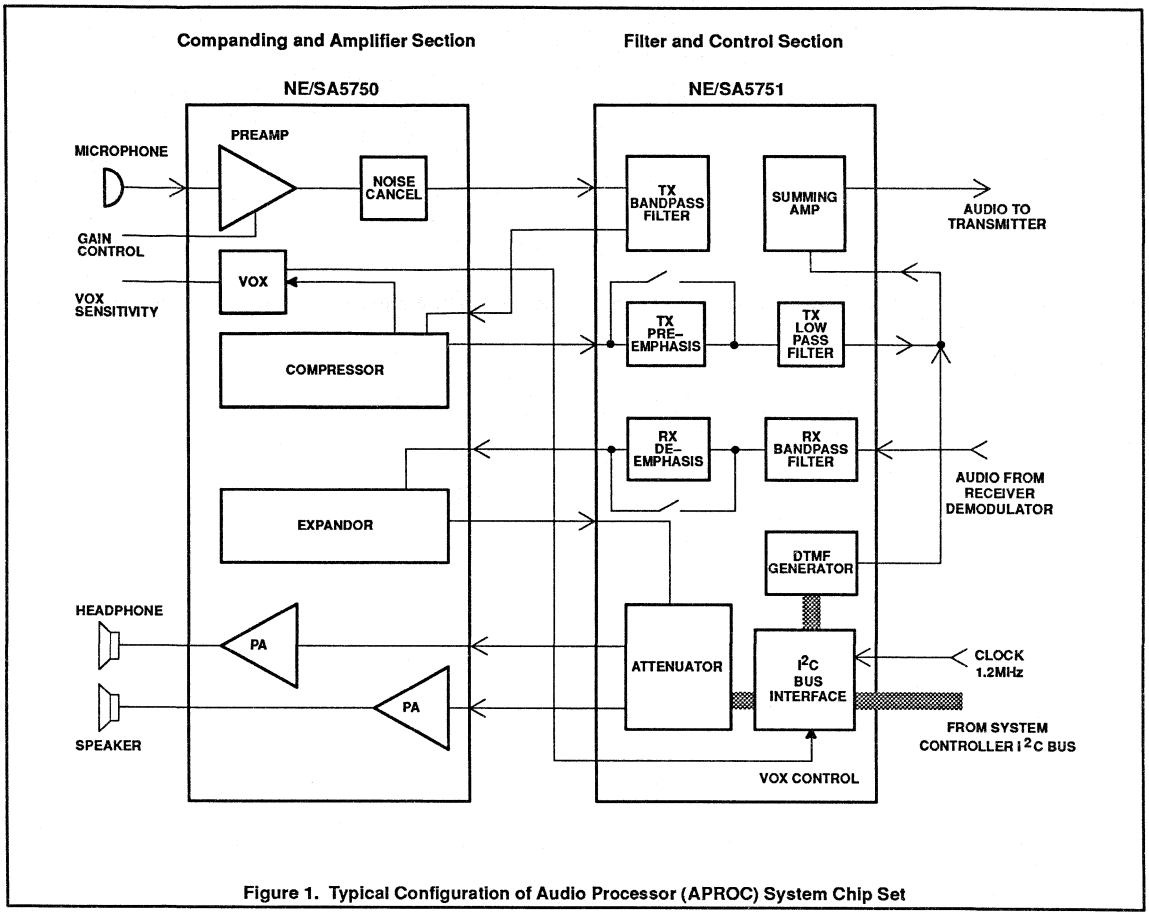


Figure 1. Typical Configuration of Audio Processor (APROC) System Chip Set

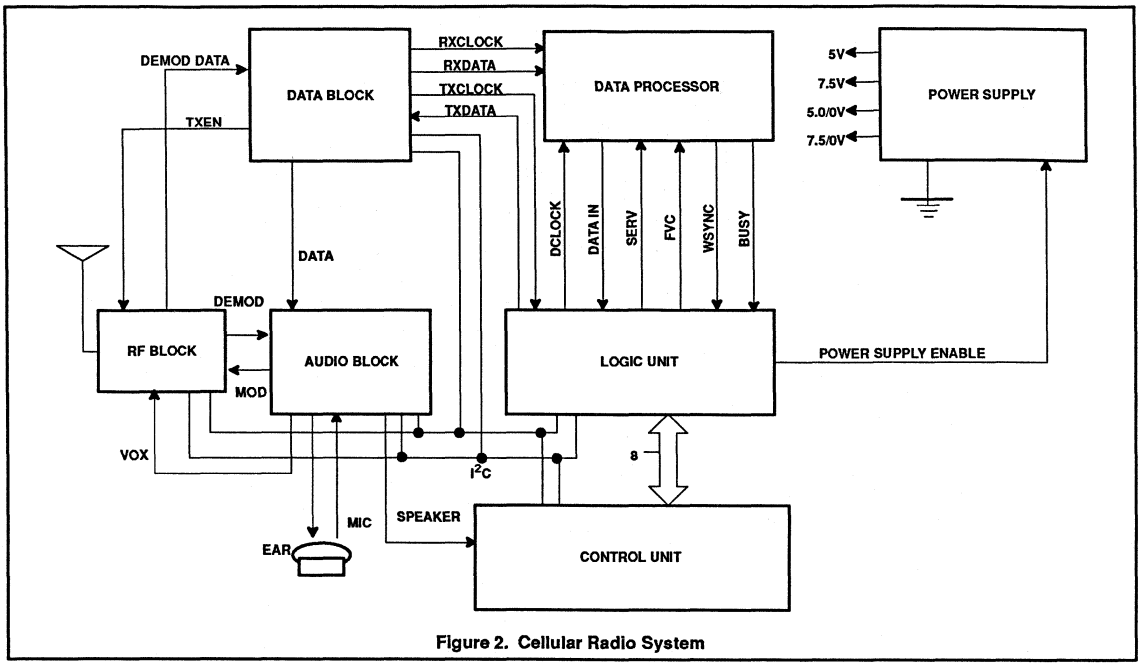


Figure 2. Cellular Radio System

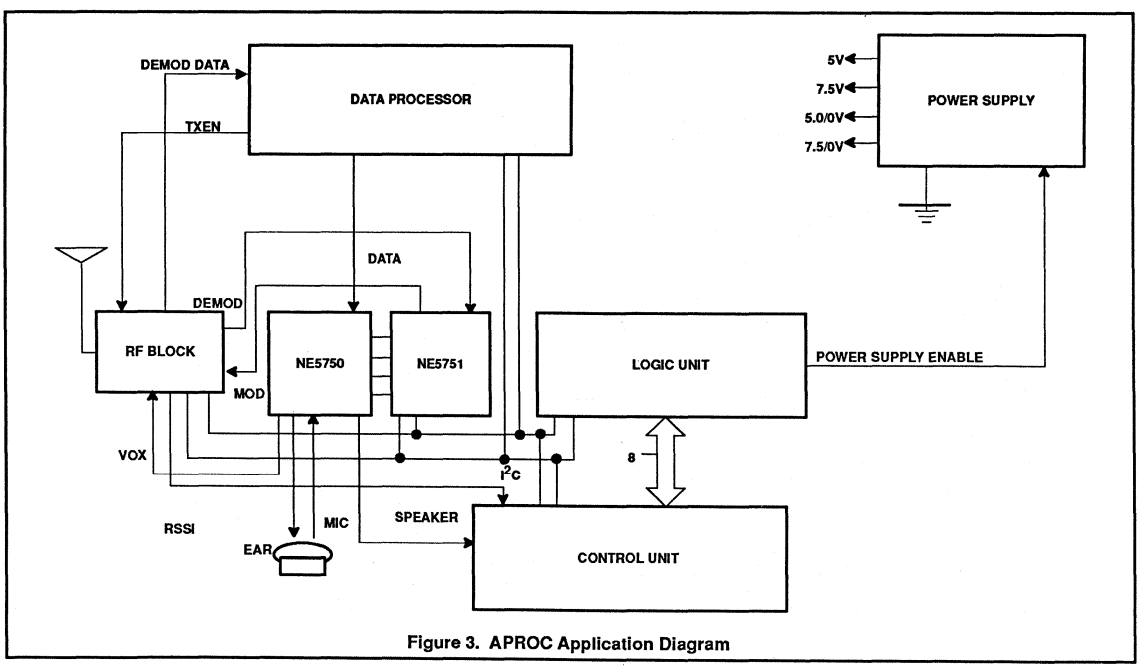


Figure 3. APROC Application Diagram

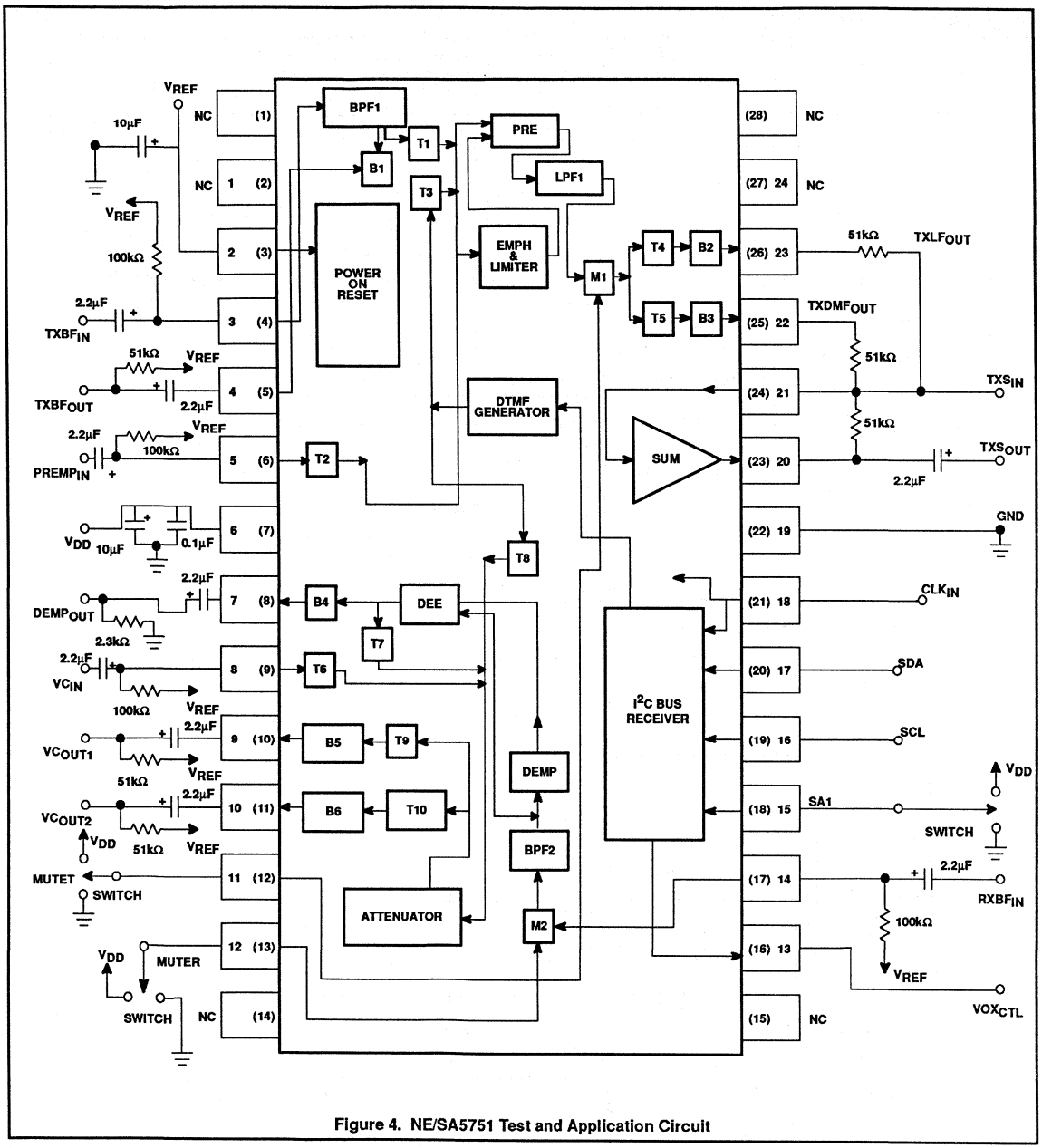
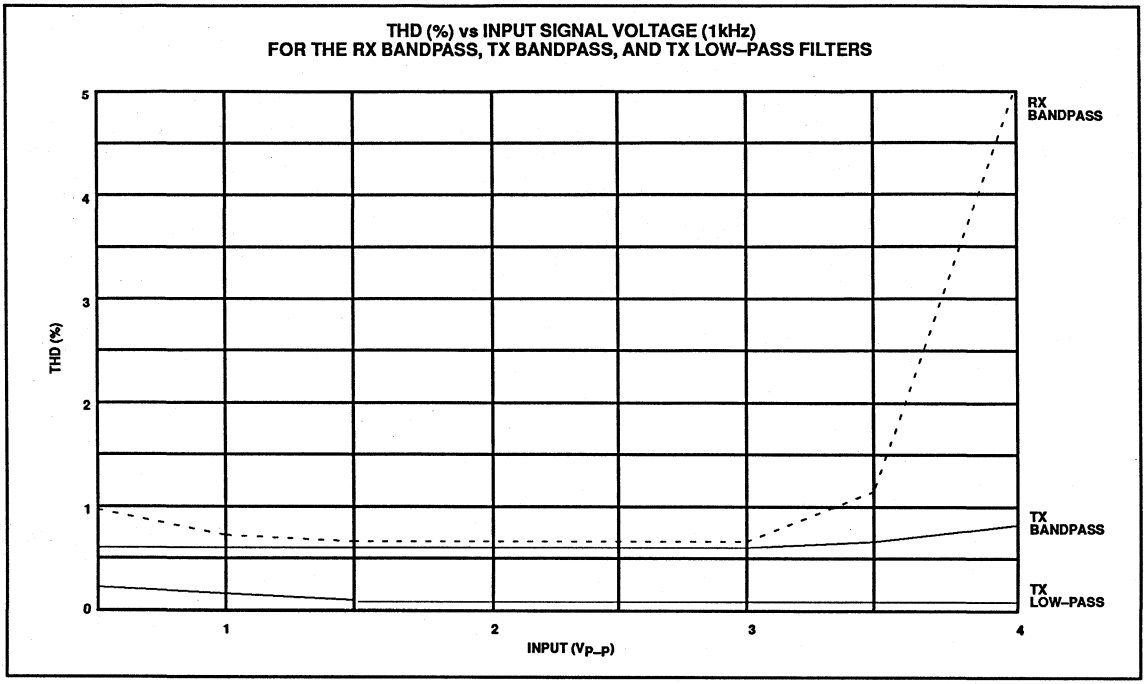


Figure 4. NE/SA5751 Test and Application Circuit

PERFORMANCE CHARACTERISTIC



Audio processor – companding, VOX and amplifier section

NE/SA5752

DESCRIPTION

The NE/SA5752 is a high performance low power audio signal processing system especially designed to meet the requirements for small size and low voltage operation of hand-held equipment. The NE/SA5752 subsystem includes a low noise microphone preamplifier with adustable gain, a noise cancellation switching amplifier with adjustable threshold, a voice operated transmitter (VOX) switch, VOX control, an audio compressor with buffered input, audio expandor, and an internal bandgap voltage regulator with power down capability. When used with Signetics' NE/SA5753, the complete audio processing function of an AMPS or TACS cellular telephone is easily implemented. The system also meets the requirements of the proposed NAMPS or NTACS specifications. The NE/SA5752 can also be used without the NE/SA5753 in a wide variety of radio communications applications.

FEATURES

- Low 3V supply
- Miniature SSOP and SO packages
- High performance
- Adjustable VOX and noise cancellation threshold
- Adjustable gain preamplifier
- Audio companding
- ESD protected
- Open collector VOX output
- Logic inputs CMOS compatible
- Power down mode
- Few external components
- Meets AMPS/TACS/NAMPS/NTACS requirements

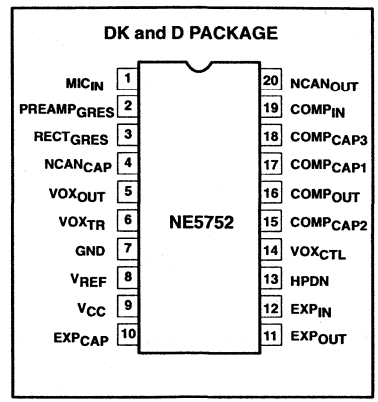
BENEFITS

- Very compact applications
- Long battery life in portable equipment
- Complete cellular audio function with the SA5753

APPLICATIONS

- Cellular radio
- Mobile communications
- High performance cordless telephones
- 2-way radio

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic SO	0 to +70°C	NE5752D
20-Pin Plastic SSOP	0 to +70°C	NE5752DK
20-Pin Plastic SO	-40 to +85°C	SA5752D
20-Pin Plastic SSOP	-40 to +85°C	SA5752DK

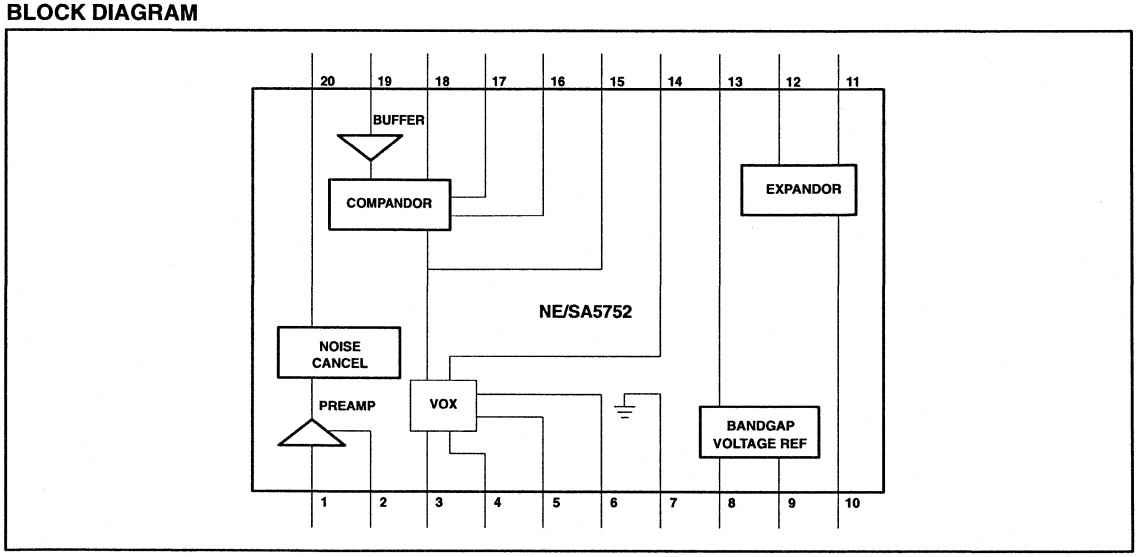
Audio processor – companding, VOX and amplifier section

NE/SA5752

PIN DESCRIPTIONS

PIN NO.	SYMBOL	DESCRIPTION
1	MIC_{IN}	Microphone input
2	$PREAMP_{GRES}$	Preamplifier gain resistor
3	$RECT_{GRES}$	Reactifier gain resistor
4	$NCAN_{CAP}$	Noise cancellation timing capacitor
5	VOX_{OUT}	Voice operated transmission output
6	VOX_{TR}	Voice operated transmission threshold resistor
7	GND	Ground
8	V_{REF}	Reference voltage
9	V_{CC}	Positive supply
10	EXP_{CAP}	Expandor timing capacitor
11	EXP_{OUT}	Expandor output
12	EXP_{IN}	Expandor input
13	HPDN	Hardware power-down
14	VOX_{CTL}	Voice operated transmission control
15	$COMP_{CAP2}$	Compressor timing capacitor 2
16	$COMP_{OUT}$	Compressor output
17	$COMP_{CAP1}$	Compressor timing capacitor 1
18	$COMP_{CAP3}$	Compressor timing capacitor 3
19	$COMP_{IN}$	Compressor input
20	$NCAN_{OUT}$	Noise cancellation output

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply voltage range	-0.3 to 6	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CC}+0.3)	V
T_{STG}	Storage temperature	-65 to +150	°C
T_A	Ambient operating temperature NE5752 SA5752	0 to 70 -40 to +85	°C

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = +3.0V, 0dB = 77.5mV_{RMS}. See test circuit, Figure 4.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
V_{CC}	Supply voltage		2.7	3.0	5.5	V
I_{CC}	Supply current	No signal Power down mode		5.0 200		mA µA
Z_L	Load impedance pins $NCAN_{OUT}$, EXP_{OUT}		50			kΩ
	$COMP_{OUT}$[1]		10			kΩ
Z_{IN}	Input impedance $COMP_{IN}$, MIC_{IN}		40	50	60	kΩ
	EXP_{IN}[2]		2.0			kΩ
	Noise cancellation current	Pin 6		25		µA
V_{OS}	DC offset $NCAN_{OUT}$[3]		-50		50	mV

NOTES:
1. Compressor is tested in production with 50kΩ load.
2. Not tested in production.
3. Offset values are identical for both gain states of noise reduction circuit.

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = +3.0V, 0dB level = 77.5mV_{RMS}. See test circuit, Figure 4.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
	Preamplifier gain range Preampliofer voltage gain 0dB Preamplifier voltage gain 40dB	 Pin 2 open Pin 2 AC ground	0 -1.0 39.0	 0 40	40 1.0 41.0	dB dB dB
	Preamplifier noise density	Pin 2 AC grounded RS = 50kΩ unweighted 20Hz-20kHz		7		nV/√Hz
		weighted CCIR DIN45405 20-20kHz		8		nV/√Hz
	Switch amplifier gain		9	10	11	dB
Compandor 1kHz, all tests[1]						
$COMP_{OUT}$	Compressor error at -21dB output level	Input level = -42dB	–1.0		1.0	dB
$COMP_{OUT}$	Compressor error at -10dB output level	Input level = -20dB	-1.0		1.0	dB
$COMP_{OUT}$	Compressor error at 0dB output level	Input level = 0dB	-1.5		1.5	dB
$COMP_{OUT}$	Compressor error at +5dB output level	Input level = +10dB	-1.0		1.0	dB
$COMP_{OUT}$	Compressor error at +12.3dB output level	Input level = +24.6dB	-1.0		1.0	dB
EXP_{OUT}	Expandor error at -42dB output level	Input level = -21dB	–1.0		1.0	dB

EXP_{OUT}	Expandor error at -21dB output level	Input level = -10.5dB	-1.0		1.0	dB
EXP_{OUT}	Expandor error at -10dB output level	Input level = -5dB	-1.0		1.0	dB

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = +3.0V, 0dB level = 77.5mV_{RMS}. See test circuit, Figure 4.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
EXP_{OUT}	Expandor error at 0dB output level	Input level = 0dB	-1.5		1.5	dB
EXP_{OUT}	Expandor error at +10dB output level	Input level = +5dB	-1.0		1.0	dB
EXP_{OUT}	Expandor error at +24.6dB output level[2]	Input level = +12.3dB	-1.0		1.0	dB
EXP_{OUT}	Expandor V_{OS}	No signal	-50.0		50.0	mV
EXP_{OUT}	Expandor output DC shift	No signal to 0dB	-100		100	mV
	Timing capacitors compandor			2200		nF
THD	Total harmonic distortion					
	Compressor	1kHz, 0dB			1	%
	Expandor	1kHz, 0dB			1	%
	$NCAN_{OUT}$	1kHz. Pin 2 open output level = 0dB			1	%
		1kHz, Pin 2 open output level = +25dB			1	%
VOX_{OUT}	Sink current				0.5	mA
	Low level High level	Open collector I_L = 0.5mA		 V_{CC}	0.4	V V
VOX_{CTL}	Input current Low		-50		0	µA
	High		-10		+10	µA
	Input level Low High		0 0.7V_{CC}		0.3V_{CC} V_{CC}	V V
H_{PDN}	Input current Low		-10		+10	µA
	High		-10		+10	µA
	Input level Low High		0 0.7V_{CC}		0.3V_{CC} V_{CC}	V V
	Reference filter capacitor			10		µF

NOTE:
1. Measurements are relative to 0dB output.
2. Measurement is absolute and indicative of the output dynamic range capability.

Audio processor – companding, VOX and amplifier section

NE/SA5752

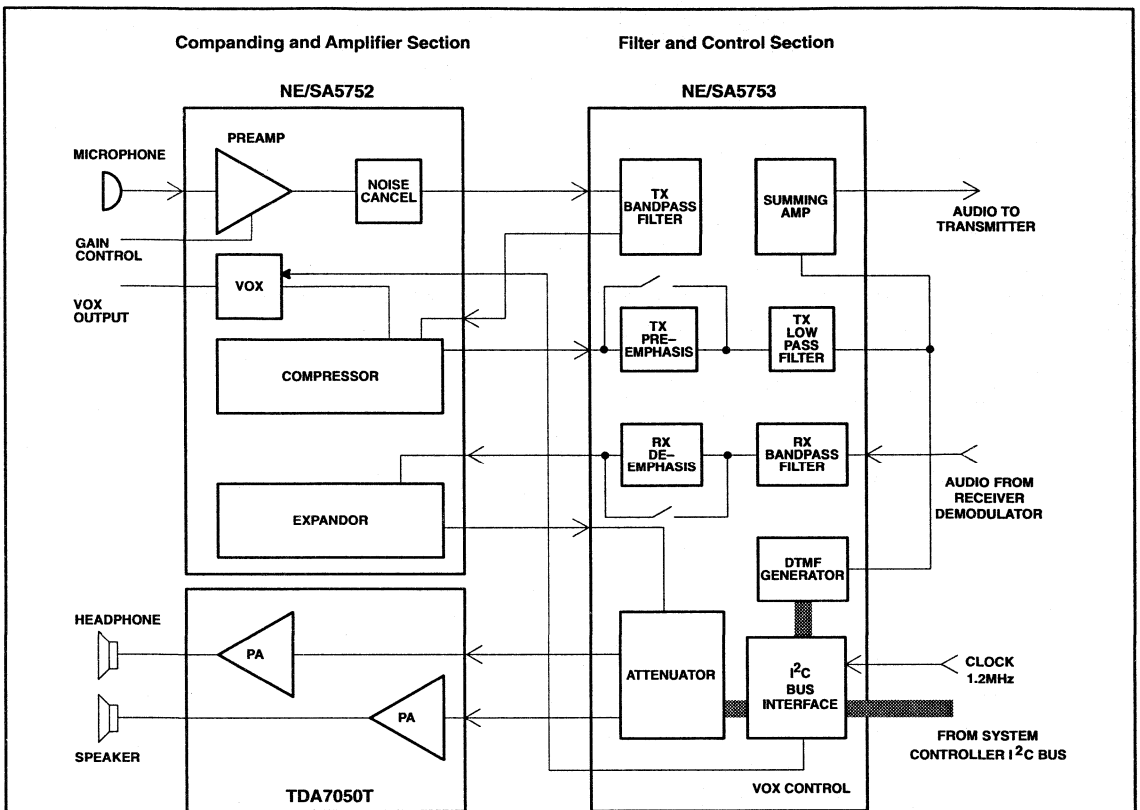


Figure 1. Typical Configuration of Audio Processor (APROC) System Chip Set

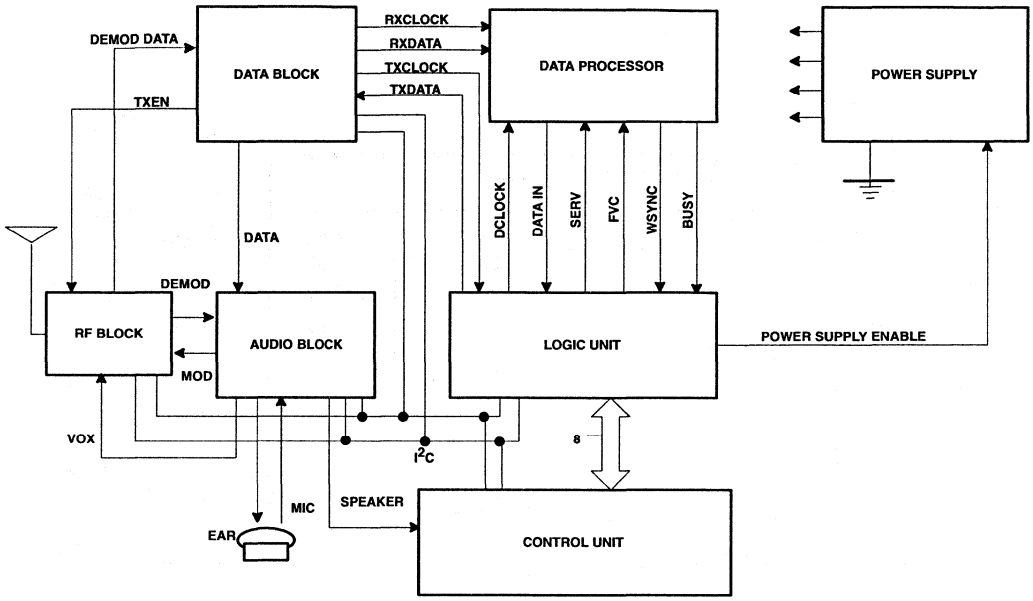


Figure 2. Cellular Radio System

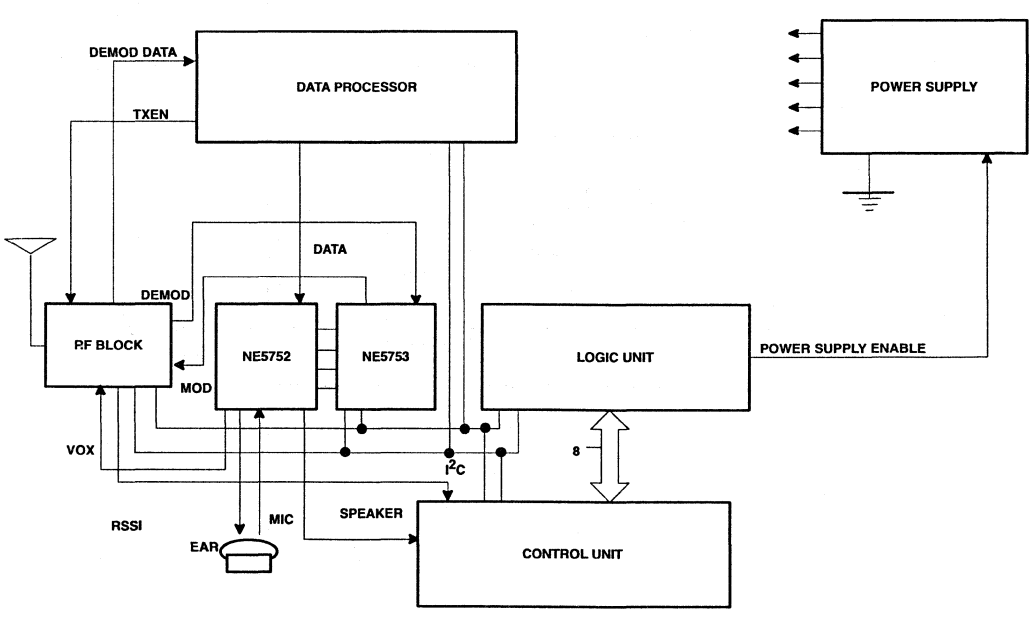


Figure 3. APROC Application Diagram

Audio processor – companding, VOX and amplifier section

NE/SA5752

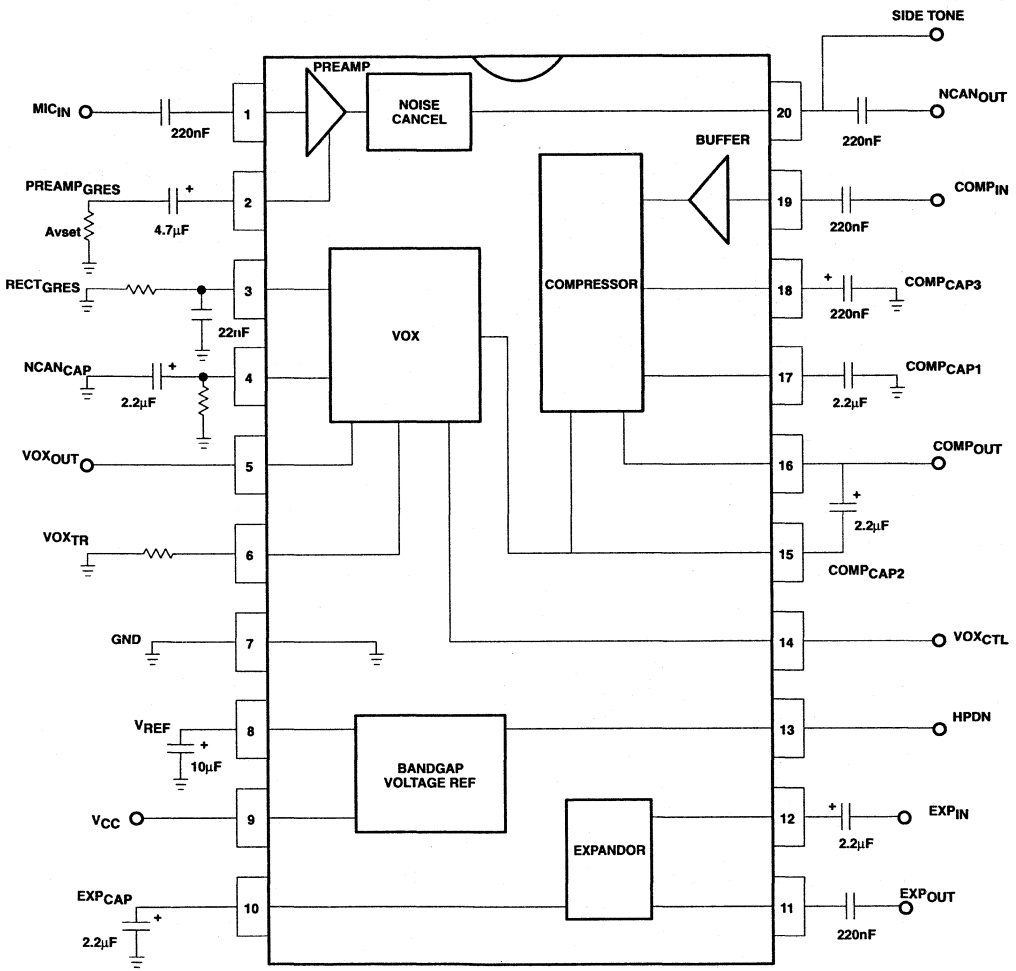


Figure 4. NE/SA5752 Test and Application Circuit

Audio processor – companding, VOX and amplifier section

NE/SA5752

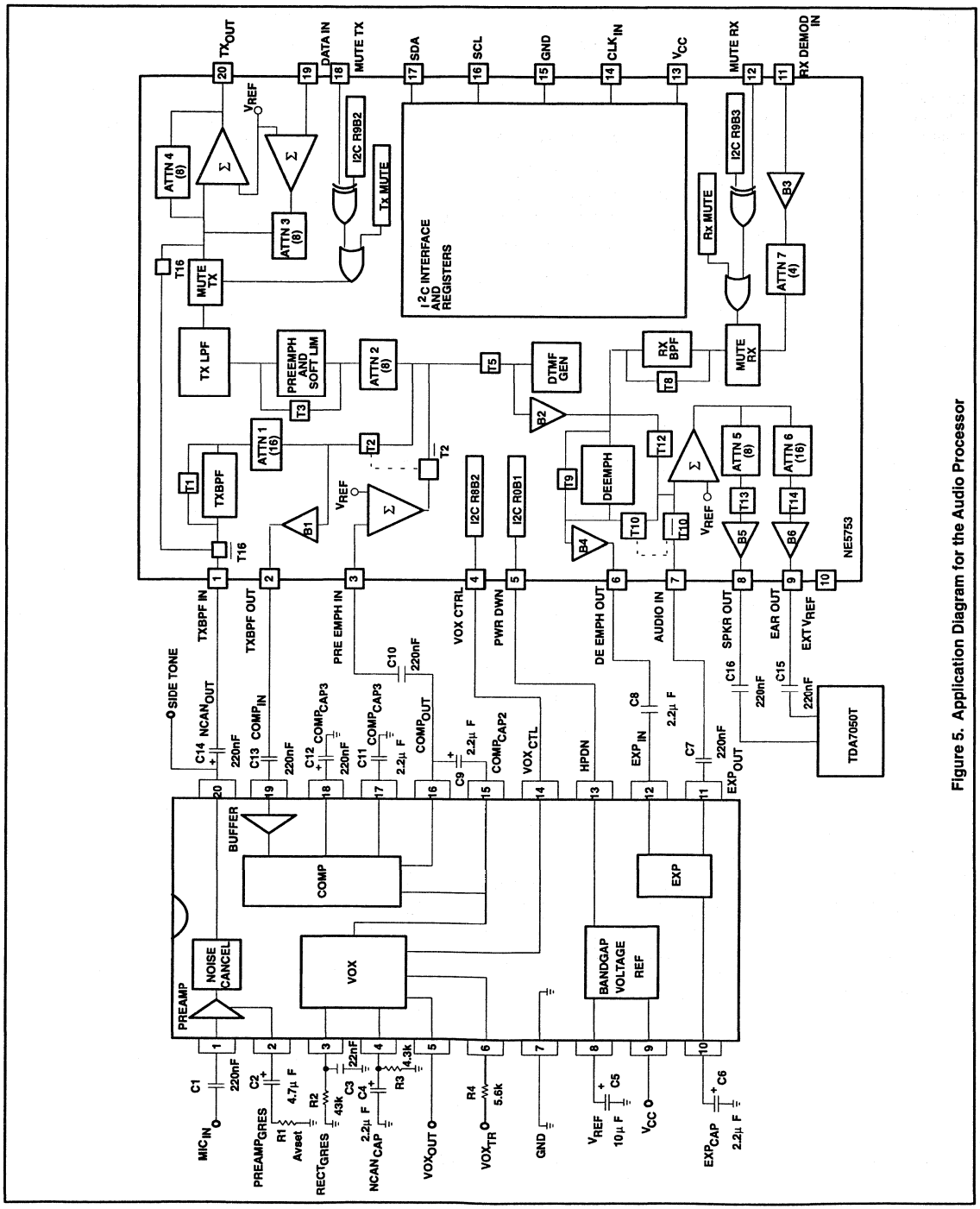


Figure 5. Application Diagram for the Audio Processor

Audio processor – filter and control section NE/SA5753

DESCRIPTION

The NE/SA5753 is a high performance low power CMOS audio signal processing system especially designed to meet the requirements for small size and low voltage operation of hand-held equipment. The NE/SA5753 subsystem includes complementary transmit/receive voice band (300-3000Hz), switched capacitor bandpass filters with pre-emphasis and de-emphasis respectively, a transmit low pass filter, peak deviation limiter for transmit, digitally controlled attenuators for signal level and volume control, audio path mute switches, a programmable DTMF generator, power-down circuitry for low current standby, power-on reset capability, and an I²C interface. When the NE/SA5753 is used with an NE/SA5752 (companding function), the complete audio processing system of an AMPS or TACS cellular telephone is easily implemented.

The system also meets the requirements of the proposed NAMPS or NTACS specification, and can be used in cordless telephone applications.

The NE5753 can be operated without the I²C bus interface by pulling DFT (Pin 13) HIGH.

FEATURES

- Low 3V supply
- Miniature SSOP package
- Low power
- High performance
- Built-in programmable DTMF generator
- Built-in digitally controlled attenuators for modulation and volume control
- Built-in peak-deviation limiter
- I²C Bus controlled
- Power-on reset
- Power down capability
- Programmable mute control
- Meets AMPS/TACS/NAMPS/NTACS requirements

BENEFITS

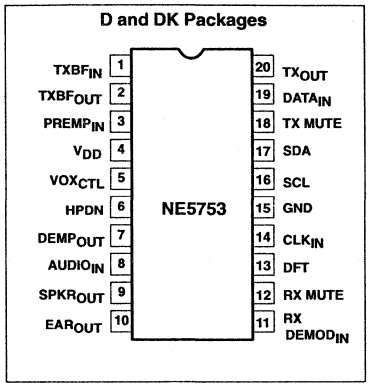
- Very compact application
- Long battery life in portable equipment
- Complete cellular audio function with the SA5752

APPLICATIONS

- Cellular radio
- Mobile communications
- High performance cordless telephones
- 2-way radio

PIN CONFIGURATION

D and DK Packages



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG NO.
20-Pin Plastic SOL	0 to +70°C	NE5753D	0172
20-Pin Plastic SOL	-40 to +85°C	SA5753D	0172
20-Pin Plastic SSOP	0 to +70°C	NE5753DK	1640
20-Pin Plastic SSOP	-40 to +85°C	SA5753DK	1640

PIN DESCRIPTIONS

PIN NO.	SYMBOL	DESCRIPTION
1	$TXBF_{IN}$	Transmit bandpass filter input
2	$TXBF_{OUT}$	Transmit bandpass filter output
3	$PREMP_{IN}$	Pre-emphasis input
4	V_{DD}	Positive supply
5	VOX_{CTL}	Vox control output
6	HPDN	Power-down I/O
7	$DEMP_{OUT}$	De-emphasis output
8	$AUDIO_{IN}$	Audio input
9	$SPKR_{OUT}$	Audio output to speaker
10	EAR_{OUT}	Audio output to earpiece
11	RX $DEMOD_{IN}$	Rx demodulated audio signal input
12	RX MUTE	RX audio signal mute input
13	DFT	Default input, non-I^2C or stand-alone operation
14	CLK_{IN}	Clock input (1.2MHz)
15	GND	Ground
16	SCL	I^2C serial clock line
17	SDA	I^2C serial data line
18	TX MUTE	Tx audio signal mute input
19	$DATA_{IN}$	Data input
20	TX_{OUT}	Transmit output

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Power supply voltage range	-0.3 to 6	V
V_{IN}	Voltage applied to any other pin	-0.3 to V_{DD}+0.3	V
	Storage temperature	-65 to +150	°C
T_A	Ambient operating temperature NE5753	0 to 70	°C
	SA5753	-40 to +85	°C

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{DD} = +3.0V, unless otherwise specified. See test circuit, Figure 4.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
V_{DD}	Power supply voltage range		2.7	3.0	5.5	V
I_{DD}	Supply current	Operating IDLE Power Down (PWDN)		2.7 600 200		mA µA µA
I_{IH}	Input current high TX MUTE, RX MUTE, HPDN DFT	$V_{IN} = V_{DD}$	 –10 0	 0 +10	 +10 +30	 µA µA
I_{IL}	Input current low TX MUTE, RX MUTE, HPDN, DFT	V_{IN} = GND	 –30 –10	 –10 0	 0 +10	 µA µA
V_{IH}	Input voltage high		0.7V_{DD}		V_{DD}	V
V_{IL}	Input voltage low		0		0.3V_{DD}	V

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{DD} = +3.0V. See test circuit, Figure 4. Clock frequency = 1.2MHz; test level = 0dBV = 77.5mV_{RMS} = -20dBm, unless otherwise specified. All gain control blocks (Attenuators) = 0dB gain, NAMPS and VCO bits set to 0.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
	RX BPF anti alias rejection			40		dB
	RX BPF input impedance	f= 1kHz		100		kΩ
	RX BPF gain with de-emphasis	f = 1kHz	-0.5	0	0.5	dB
	RX BPF gain with de-emphasis	f = 100Hz		-31	-29	dBm0
	RX BPF gain with de-emphasis	f = 300Hz	9.0	9.6	11.0	dBm0
	RX BPF gain with de-emphasis	f = 3kHz	-11.0	-10.0	-9.0	dBm0
	RX BPF gain with de-emphasis	f = 5.9kHz		-58	-50	dBm0
	RX BPF noise with de-emphasis	300Hz-3kHz				μV_{RMS}
	RX dynamic range	with deemphasis		80		dB
	$DEMP_{OUT}$ output impedance	f = 1kHz			40	Ω
	$DEMP_{OUT}$ output swing (1%)	2kΩ to $V_{DD/2}$; f = 1kHz		2.4		V_{P-P}
	$SPKR_{OUT}$ ouput swing (1%)	50kΩ to$V_{DD/2}$; f = 1kHz	V_{DD} -1	2.4		V_{P-P}
	EAR_{OUT} output swing (1%)	50kΩ to $V_{DD/2}$; f = 1kHz	V_{DD} -1	2.4		V_{P-P}
	$SPKR_{OUT}$ noise					μV_{RMS}
	$SPKR_{OUT}$ noise					μV_{RMS}
	CLK_{IN} high		2.1		3.0	V
	CLK_{IN} low		0		1.0	V
	TX BPF anti alias rejection	f > 50kHz		40		dB
	TX BPF input impedance	f = 3kHz		100		KΩ
	TX BPF noise	300 - 3000kHz				μV_{RMS}
	TX LPF gain	f = 5.9kHz		-39	-36	dBm0
	TX LPF gain with pre-emphasis	f = 1kHz, 0dBV		2.43		dB
	TX LPF gain with pre-emphasis	f = 100Hz		-19		dBm0
	TX LPF gain with pre-emphasis	f = 300Hz		-10.45		dBm0
	TX LPF gain with pre-emphasis	f = 3kHz		9.14		dBm0
	TX LPF gain with pre-emphasis	f = 5900Hz		-28		dBm0
	TX LPF gain with pre-emphasis	f = 9kHz		-51		dBm0
	TX overall gain	1kHz		2.43		dB
	TX overall gain	100Hz		-58	-45	dBm0
	TX overall gain	300Hz	-11	-10.4	-9	dBm0

AC ELECTRICAL CHARACTERISTICS (continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
	TX overall gain	3kHz	8	9	9.6	dBm0
	TX overall gain	5.9kHz		-52	-45	dBm0
	TX BPF dynamic range			TBD		dB
	$PREMP_{IN}$ input impedance	f = 3kHz		100		kΩ
	TX_{OUT} Slew rate	C_L = 15pF		0.75		V/µs
	Output impedance	f = 3kHz			40	Ω
	Output swing (limiting)			1.2		V_{P-P}
	Output swing (1% THD)	5kΩ load (25°C)		1.0		V_{P-P}
	Analog switches insertion loss			60		dB
	Time delay to mute from RX MUTE or TX MUTE transition	$V_{IN} = V_{IL}$ to V_{IH} $V_{IN} = V_{IH}$ to V_{IL}		0.5 0.5		µs µs

Table 1. Gain Control Blocks (Bit 0 is Least Significant Bit)

SYMBOL	Bits	TYPICAL STEP (dB)	TYPICAL GAIN (dB)	
			MIN	MAX
A1	4	–0.8	–12.0	0
A2a	5	±0.25	–3.75	+3.75
A2b	2	–6, (–12 on first)	–24.0	0
A3	4	–1.0	–15.0	0
A4	4	±0.5	–3.5	+3.5
A6	4	–2.0	–30.0	0
A7	4	±0.5	–3.5	+3.5
NAMPS	1		+1.9 in A2b –7.6 in A4	
VCO	1		+6.0 in A4	
For A2a, A4 and A7:		MSB sets the sign of the gain MSB = 0 for gain MSB = 1 for attenuation		
For all Gain Blocks:		All bits set to 0 = 0dB gain All bits set to 1 = maximum gain or attenuation		

FUNCTIONAL DESCRIPTION

The NE5753 is an audio signal processor designed to meet the requirements of compact low voltage radio telephone equipment. It includes transmit and receive bandpass filters for voiceband (300-3000Hz) with pre-emphasis and de-emphasis respectively, a transmit peak deviation limiter, voice channel mute switches and a data path which can be summed into the transmit channel. An I^2C interface is provided for software programmability of a DTMF generator, mute polarity, selection of different power down and operating modes and control of the gain in both the transmit and receive channels.

Software programmable gain control allows the device to be automatically optimized during equipment production and offers flexibility during normal operation.

Gain Blocks

The programmable gain blocks are shown in Table 1 and Figure 4. The purpose for each block is as follows:

a. A1 compensates for microphone gain variations in the transmit path.

b. A2a compensates for transmitter dynamic range variations due to manufacturing tolerances of the NE5753 and NE5752 compandor companion device. To meet AMPS requirements, the dynamic range between the zero crossing signal level of the compandor and the peak signal allowed by the deviation limiter is adjusted to 12.34dB.

c. A2b allows coarse attenuation to be inserted in the transmit path to eliminate positive feedback effects in hands-free speaker applications. First step is 12dB followed by two steps of 6dB.

d. A3 sets the gain between the $DATA_{IN}$ pin (Pin 19) and the TX_{OUT} pin (Pin 20) and should be adjusted after A2a and A4 have been previously optimized. The NE5753 will interface directly with the UMA1000T data processor (which produces a 2Vpk data signal). For NAMPS applications an additional 10 to 14dB resistive divider must be added at the $DATA_{IN}$ pin (Pin 19) for a 2V data signal.

e. A4 compensates for transmit gain variations due to manufacturing tolerances of the NE5753, NE5752 and VCO connected to TX_{OUT} (Pin 20). After A2a has been adjusted to set dynamic range then A4 is used to set the peak output

voltage at TX_{OUT} (Pin 20) such that a nominal 10kHz/V VCO produces a peak deviation of 12kHz to meet AMPS specifications.

f. A6 is the volume control for both the $SPKR_{OUT}$ and EAR_{OUT}.

g. A7 compensates for manufacturing tolerances in the NE5753 and preceeding demodulator. For AMPS requirements, a 1kHz tone with 2.9kHz deviation should produce an output signal at $DEMP_{OUT}$ (Pin 7) corresponding to the zero crossing signal level of the expandor.

NAMPS and VCO Offsets

For NAMPS applications, a '1' programmed into R5B3 (register 5, bit 3) will offset the transmit gain for NAMPS applications. It is recommended that A2a and A4 be programmed after the NAMPS option is set to compensate for manufacturing tolerances in the NAMPS offset, itself.

When the VCO bit of R5B2 is a '1', an extra gain of 6dB is provided at TX_{OUT} for direct interface to VCOs with a nominal gain of 5kHz/V.

Operation Using the I²C Communications Bus

The NE5753 includes on-chip gain blocks and options which can be programmed through an I²C interface bus. To use this capability, the DFT pin (Pin 13) must be pulled LOW. In this mode, all signal level adjustments can be made through software with no external potentiometers required.

With DFT pulled LOW, the HPDN pin (Pin 6) is an OUTPUT having the same value as the program bit in register 5 bit 1 (R5B1) of the control register bit map. The value at the VOX_{CTL} output (Pin 5) is the same as the program bit in R8B7. The HPDN and VOX_{CTL} outputs can be used to control the state of the NE5752 companion device.

Power On Reset and Power Down Modes

In order to avoid undefined states of the NE5753 when power is initially applied, a power-on-reset circuit is incorporated which defaults RxP and TxP such that the receive and transmit paths are muted if a 'high' voltage is applied to RX MUTE and TX MUTE (Pins 12 and 18). RX MUTE and TX MUTE include on-chip pull up resistors so, during power up, the user may apply a logic '1' to these pins or leave them floating. After power up, the registers can be programmed and the mutes removed by a quick access write to R0.

Three software controlled low power modes are provided on the NE5753. These are POWER DOWN (PWDN), IDLE and DENA and can be selected by programming a '1' into R6B2, R6B1 or R6B0 as follows. In PWDN mode (R6B2=1) both the voice and data channels are powered down with the respective I/O pins at a high impedance. In DENA mode (R6B1=1) the voice channels are powered down, but the data channel (from $DATA_{IN}$ and TX_{OUT}) is fully active. In IDLE mode (R6B1=1, R6B0=1) both voice and data channels are powered down. (See Table on page 8.)

The difference between selecting IDLE and PWDN is that the former maintains the normal operational bias voltages at all voice and data I/O pins and provides a glitch-free transfer from power down to a fully active mode and vice-versa.

Although the POWER DOWN mode exhibits lower power consumption, glitches may occur when transferring to an active mode because of the previous high impedance of the I/O pins.

The VOX_{CTL} and HPDN pins (Pins 5 and 6) still have the same value as R8B7 and R5B1 in all low power modes.

Operation Without Using the I²C Bus

The NE5753 can be operated in a default mode with the I²C bus bypassed. To use this mode, the DFT pin (Pin 13) is pulled HIGH. RxP and TxP are then defaulted such that a logic '1' is required at RX MUTE or TX MUTE to mute the appropriate path.

DTMF is disabled in the default mode. The HPDN pin (Pin 6) is now an INPUT which will put the NE5753 into POWER DOWN mode when pulled LOW. The VOX_{CTL} pin (Pin 5) will follow the value of the control bit in R8B7 prior to pulling DFT HIGH unless the device is programmed without using the I²C protocol, as described below.

Programming Without the I²C Protocol

In the default mode, with DFT (Pin 13) pulled HIGH, the registers in the control register bit map are chained together so that bit 0 of a register is connected to bit 7 of the preceeding register with R0B6, R0B7, R1B6 and R1B7 bypassed, i.e., R0B5 is connected to R1B0, R1B5 is connected to R2B0, R2B7 is connected to R3B0, etc. Bits can then be loaded as a serial stream through the SDA pin of the I²C bus by the negative edge of a shifting clock applied at the SCL pin of the I²C bus. When a bit is loaded at SDA it will load first into R0B0 and then will be shifted to R8B7 after 68 clock edges.

A total of 68 clock pulses (applied at SCL) are therefore required to completely load the registers.

In this mode of operation the contents of the register map are also shifted out from the VOX_{CTL} pin since it takes the same value as R8B7. After power up there is no reset within the registers so the first 68 bits clock out at the VOX_{CTL} pin will have an indeterminate value.

Summary: To use this capability, the DFT pin must be pulled HIGH, the serial bit stream loaded through SCL synchronous with the negative clock edge applied at SCL for 68 clock pulses, and then the DFT pin pulled LOW.

Cordless Telephone Applications

For cordless telephone applications, a switch S12 is provided (R5B0) to route data through the complete transmit path while inhibiting the voice channel. In the receive path, a quick access mode is provided through the I²C to disable both EAR_{OUT} and $SPKR_{OUT}$, by setting R0B0 and R0B1, when data is detected at the $DEMP_{OUT}$ pin (Pin 7).

I²C CHARACTERISTICS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both SDA and SCL are bidirectional lines connected to a positive supply voltage via a pull-up resistor. When the bus is free, both lines are HIGH. Data transfer may be initiated only when the bus is not busy (both lines HIGH).

The output devices, or stages, connected to the bus must have an open drain or open collector output in order to perform the wired-AND function.

Data at the I²C bus can be transferred at a rate up to 100kbits/s. The number of devices connected to the bus is solely dependent on the maximum allowed bus capacitance of 400pF.

For devices operating over a wide range of supply voltages, such as the NE5753, the following levels have been defined for a logical LOW and HIGH;

$V_{ILMAX} = 0.3V_{DD}$ (max. input LOW voltage)
$V_{IHMIN} = 0.7V_{DD}$ (min. input HIGH voltage)

Data Transfer

Data is transferred from a transmitting device to a receiving device with one data bit transferred during each clock pulse on the SCL line. The transmitter also generates the clock once arbitration has given it control of the SCL line. The data on the SDA line must remain stable during the HIGH period of the clock cycle, otherwise it may be interpreted as a control signal.

Start and Stop Conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH to LOW transition of the data line while the clock line is HIGH is defined as a start condition. A LOW to HIGH transition of the data line while the clock is HIGH is defined as a stop condition.

Acknowledgement

Following each byte of data transfered, the receiver must acknowledge successful reception. To do this the transmitter releases the SDA line (allowing it to go HIGH) at the end of each transmitted byte, and it is pulled LOW by the receiver. If this condition is maintained during the next HIGH period of the clock pulse (called the acknowledge clock pulse) then data transfer is resumed. If the receiver does not pull the SDA line LOW, the transmitter will abort the transfer.

I²C Bus Data Configurations

The NE5753 is always a slave receiver in the I²C bus configuration). The slave address consists of eight bits in the serial mode and is internally fixed.

Control Registers

The control register bit map is shown below. Either a quick access or normal address mode can be used, determined by the two MSB bits in the first word following the NE5753 address word. If the quick access mode is used, the registers R0 or R1 can be updated by sending only two bytes of information (address plus update). If R0 or R1 are updated using the address mode, then B7 and B6 of the data word are ignored. In all access modes, incremental register addressing is supported with following words updating the next register until a 'stop' bit is sent.

High Tone DTMF Register

MSB							LSB
HD7	HD6	HD5	HD4	HD3	HD2	HD1	HD0

The eight bits determine the output frequency by the following formula.:

High Frequency = 1200kHz/6/HD
where HD is the value of the register.

Low Tone DTMF Register

MSB							LSB
LD7	LD6	LD5	LD4	LD3	LD2	LD1	LD0

The eight bits determine the output frequency by the following formula.:

Low Frequency = 1200kHz/14/LD
where LD is the value of the register.

The operation of the 96ms DTMF timer is initiated by the loading of the low tone DTMF register. This timer terminates transmission of the tones as the generated tones cross the reference level after 96ms. The on time of the tones can thus vary by up to one cycle of the tones.

Continuous tones can be obtained by again loading DTC = 1 in R1, bit 5.

Single tones can be obtained by loading 2 into the unused tone register to silence it.

Loading a value of 1 or 0 into the registers will default the register value to 256 or 255, respectively.

Phase continuous frequency modulation can be produced by loading a new value into a DTMF register during continuous operation (DTC=1).

I²C Address and Access

S	A7 A6 A5 A4 A3 A2 A1 A0	ACK	F7 F6 F5 F4 F3 F2 F1 F0	ACK	...	P

S = start, A0 = 0, ACK = acknowledge, P = stop, A7–0 = NE5753 address fixed internally at 1000000.
Access mode is determined by F7, F6.

All access modes support incremental addressing.

Mode	F7	F6	Action
quick access	0	0	Load F5–F0 to R0B5 – R0B0
quick access	0	1	Load F5-F0 to R1B5 – R1B0
test mode	1	0	For test only. DO NOT USE.
address mode	1	1	F3–F0 point to register

Address Map

REG	Address				Register Bits							
	F3	F2	F1	F0	B7	B6	B5	B4	B3	B2	B1	B0
R0	0	0	0	0	Y	Y	RxM	TxM	A2bb1	A2bb0	S9	S10
R1	0	0	0	1	Y	Y	DTC	S4	S8	S13	S7	S2
R2	0	0	1	0	HD7	HD6	HD5	HD4	HD3	HD2	HD1	HD0
R3	0	0	1	1	LD7	LD6	LD5	LD4	LD3	LD2	LD1	LD0
R4	0	1	0	0	A1b3	A1b2	A1b1	A1b0	A4b3	A4b2	A4b1	A4b0
R5	0	1	0	1	A6b3	A6b2	A6b1	A6b0	NAMPS	VCO	HPDN	S12
R6	0	1	1	0	A2ab4	A2ab3	A2ab2	A2ab1	A2ab0	PWDN	IDLE 1	IDLE 0
R7	0	1	1	1	A3b3	A3b2	A3b1	A3b0	A7b3	A7b2	A7b1	A7b0
R8	1	0	0	0	VOX_{CTL}	S3	S5	S6	S11	RxP	TxP	S1

Y = ignored in address mode.
For all bits TRUE = '1'

A1b3–0 = program bits for gain block A1
A2ab4–0 = program bits for gain block A2a
A2bb1–0 = program bits for gain block A2b
A3b3–0 = program bits for gain block A3
A4b4–0 = program bits for gain block A4
A5b2–0 = program bits for gain block A5
A6b3–0 = program bits for gain block A6
A7b3–0 = program bits for gain block A7
HD7–0 = high tone DTMF
LD7–0 = low tone DTMF
NAMPS = program bit for NAMPS offset
VCO = 6dB higher TX_{OUT}
RxM = receive mute
TxM = transmit mute
RxP = receive mute polarity
TxP = transmit mute polarity
DTC = DTMF continuous
S1 = bypass TXBPF
S2 = bypass compressor in TX path, inhibit pre-emph input
S3 = bypass pre-emp and limiter in Tx path
S4 = enable DTMF to TX path and inhibit $PREMP_{IN}$ and S2.
S5 = bypass RXBPF
S6 = bypass de-emph in RX path
S7 = bypass expandor in RX path, inhibit audio input
S8 = enable DTMF to RX path and inhibit $AUDIO_{IN}$ and S7.
S9 = enable $SPKR_{OUT}$
S10 = enable EAR_{OUT}
S11 = bypass TXLPF
S12 = cordless data option established
S13 = enable data path
VOX_{CTL} = enable VOX of compandor/expander circuit. This bit appears at the VOX_{CTL} pin (Pin 5) of the NE5753.
HPDN = enable power down of compandor circuit. This bit appears at the HPDN pin (Pin 6) of the NE5753
PWDN, IDLE1, IDLE0 see Table below

Low Power Modes (R6B0 – R6B2)

PWDN	IDLE1	IDLE0	
1	X	X	(PWDN) Complete power down except I²C, I/Os high impedance.
0	1	0	(DENA) Low power, I/Os at $V_{DD}/2$, $DATA_{IN}$ to TX_{OUT} enabled.
0	1	1	(IDLE) Low power, I/Os at $V_{DD}/2$, $DATA_{IN}$ to TX_{OUT} disabled.
0	0	0	Normal operation.
0	0	1	$DATA_{IN}$ to TX_{OUT} disabled.

X = don't care.

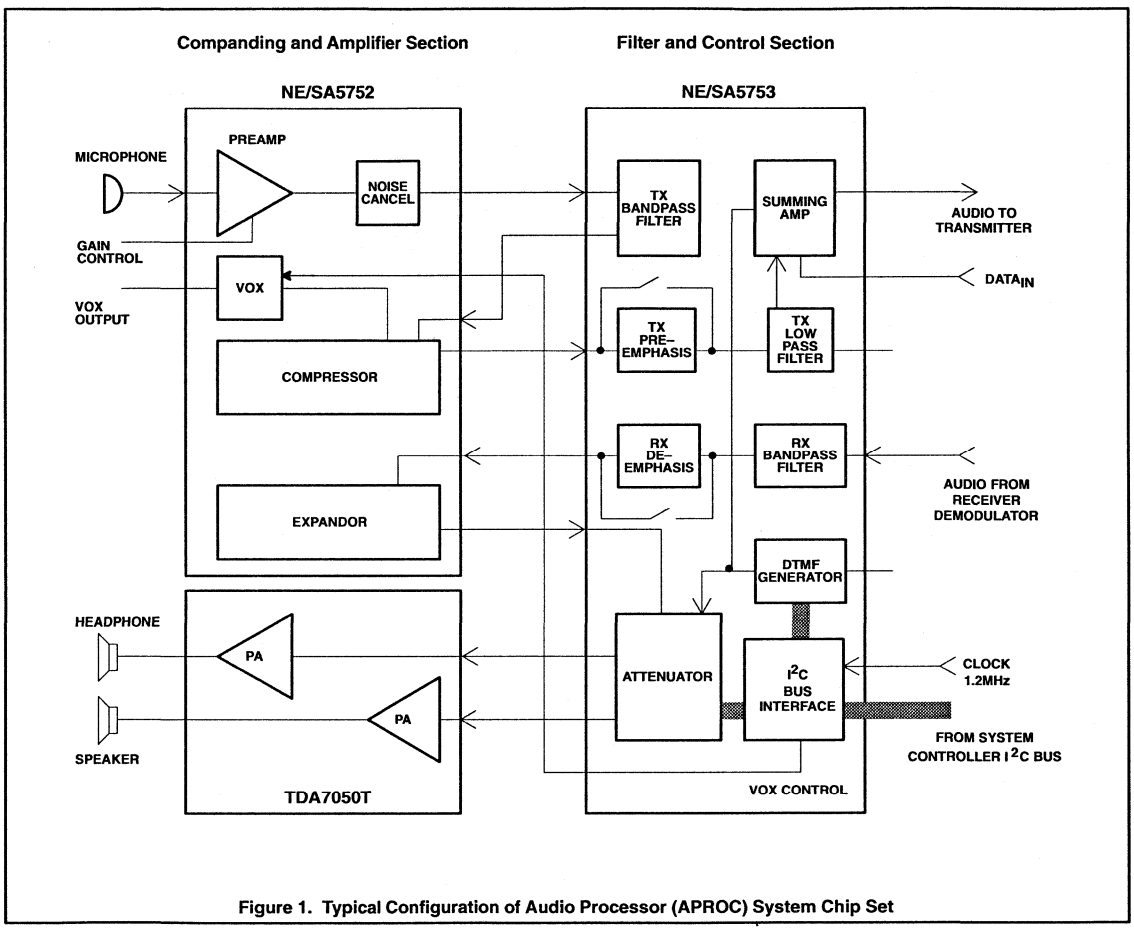


Figure 1. Typical Configuration of Audio Processor (APROC) System Chip Set

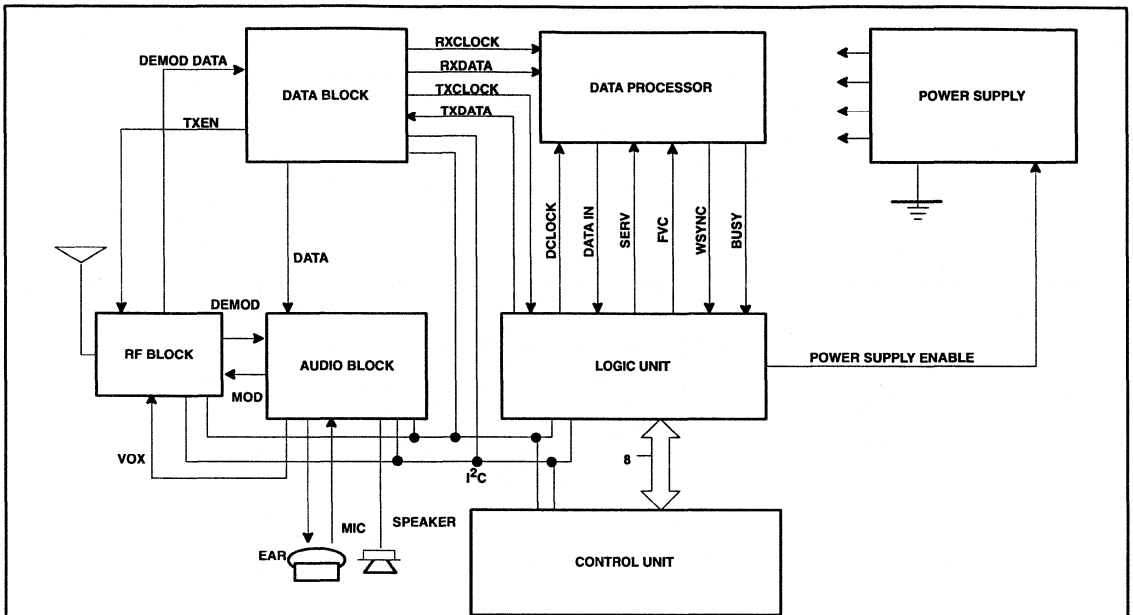


Figure 2. Cellular Radio System

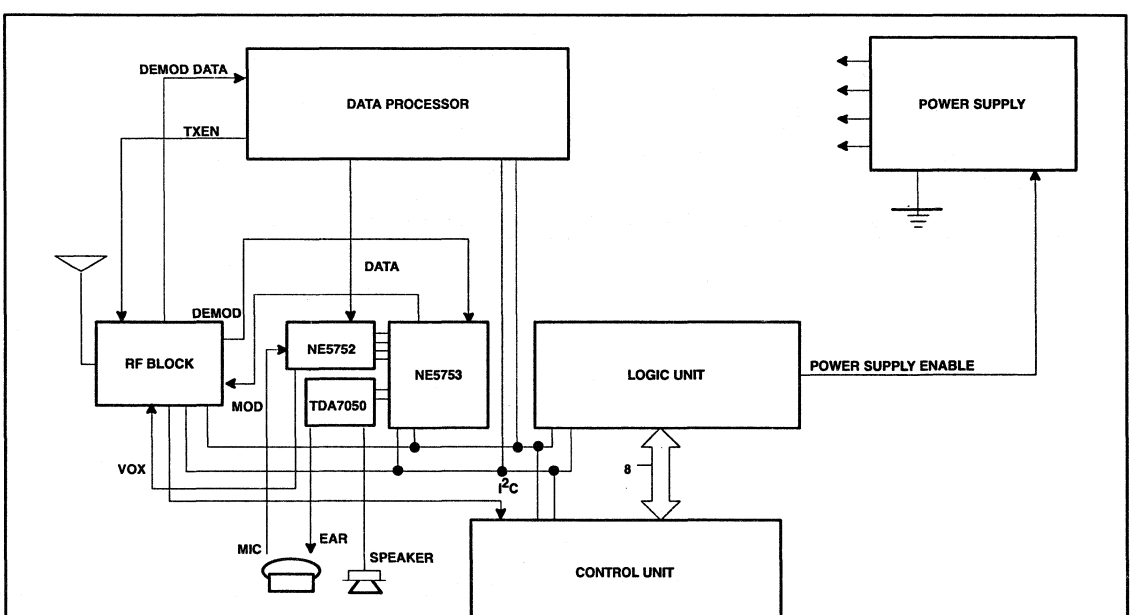


Figure 3. APROC Application Diagram

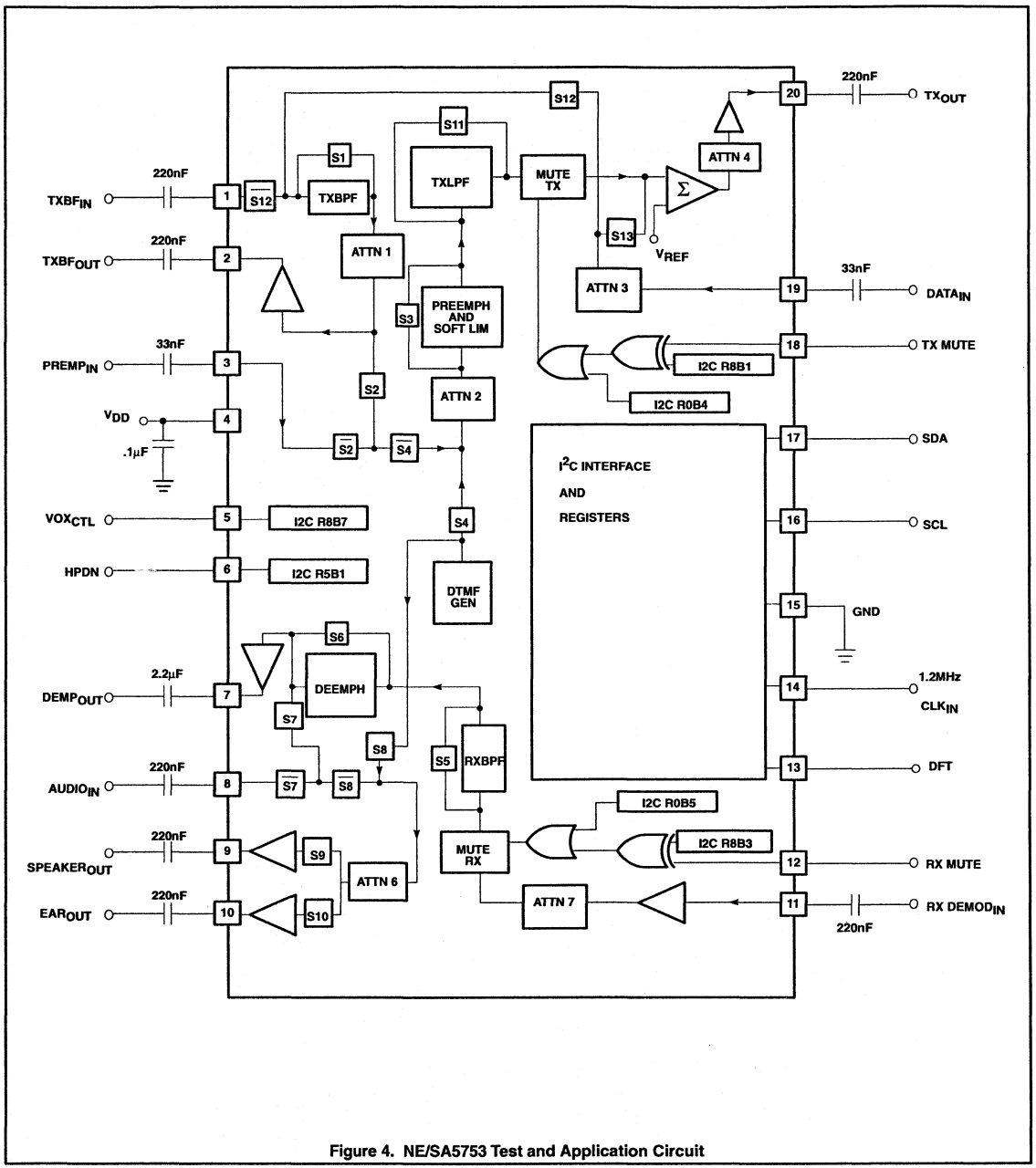


Figure 4. NE/SA5753 Test and Application Circuit

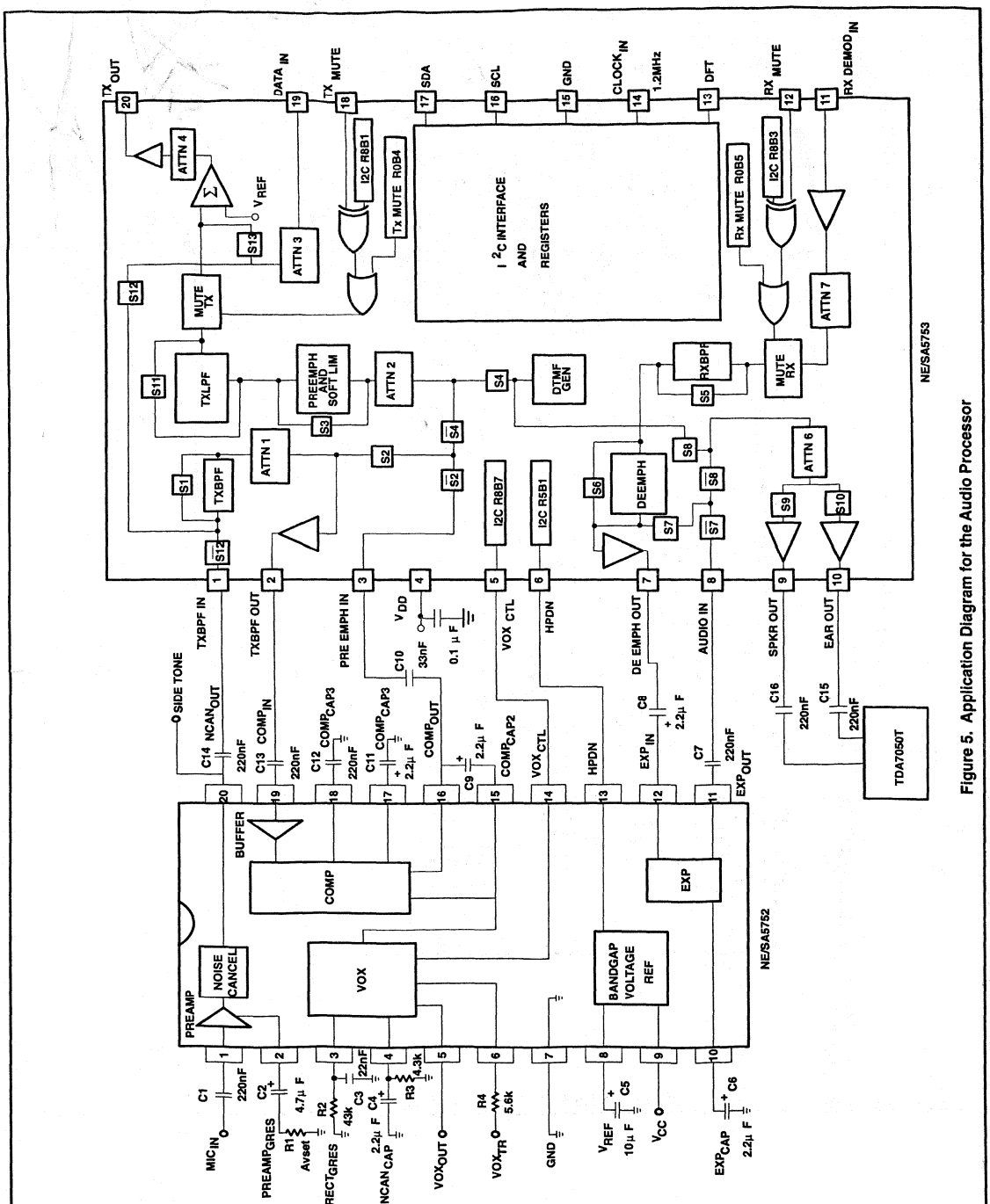


Figure 5. Application Diagram for the Audio Processor

Tone decoder/phase-locked loop

NE/SE567

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC11 OR DATA SHEET

DESCRIPTION

The NE/SE567 tone and frequency decoder is a highly stable phase-locked loop with synchronous AM lock detection and power output circuitry. Its primary function is to drive a load whenever a sustained frequency within its detection band is present at the self-biased input. The bandwidth center frequency and output delay are independently determined by means of four external components.

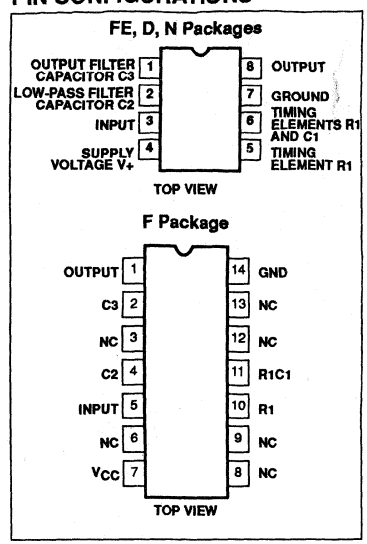
FEATURES

- Wide frequency range (.01Hz to 500kHz)
- High stability of center frequency
- Independently controllable bandwidth (up to 14%)
- High out-band signal and noise rejection
- Logic-compatible output with 100mA current sinking capability
- Inherent immunity to false signals
- Frequency adjustment over a 20-to-1 range with an external resistor
- Military processing available

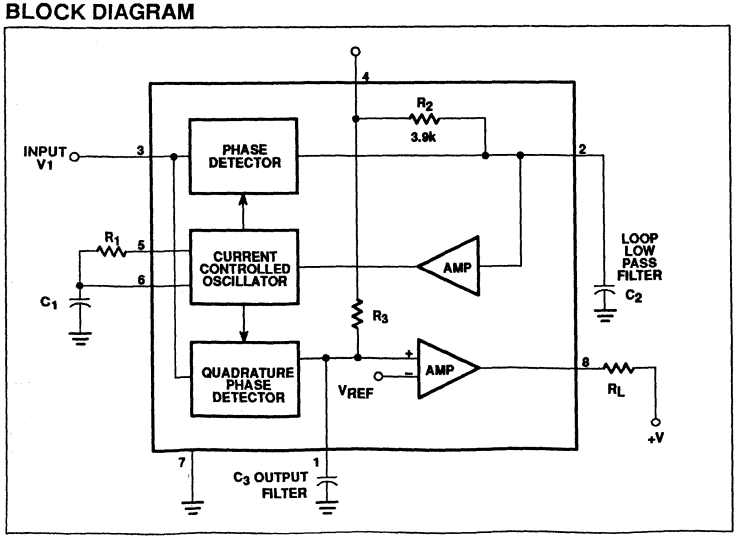
APPLICATIONS

- Touch-Tone® decoding
- Carrier current remote controls
- Ultrasonic controls (remote TV, etc.)
- Communications paging
- Frequency monitoring and control
- Wireless intercom
- Precision oscillator

PIN CONFIGURATIONS



BLOCK DIAGRAM



®Touch-Tone is a registered trademark of AT&T.

Low-voltage single-chip 8-bit microcontroller — 80CL51

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATA SHEET

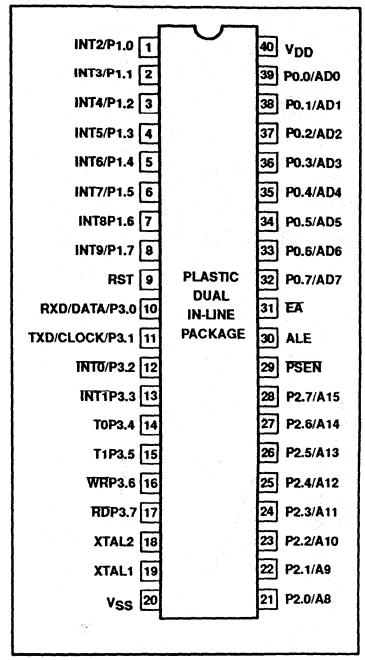
FEATURES

- Full static 80C51 CPU
- 8-bit CPU, ROM, RAM, 1/0 in a single 40-lead DIL / mini-pack
- 4K x 8 ROM, expandable externally to 64K bytes
- 128 bytes RAM, expandable externally to 64K bytes
- Four 8-bit ports, 321/0 lines
- Two 16-bit timer / event counters
- External memory expandable up to 128K, external ROM up to 64K and / or RAM up to 64K
- On-chip oscillator suitable for RC, LC, quartz crystal or ceramic resonator
- Thirteen source, thirteen vector interrupt structure with two priority levels
- Full duplex serial port (UART)
- Enhanced architecture with:
  - non-page oriented instructions
  - direct addressing
  - four eight byte RAM register banks
  - stack depth up to 128 bytes
  - multiply, divide, subtract and compare instructions
- Power-Down and IDLE instructions
- Wake-up via external interrupts at Port 1
- Single supply voltage of 1.8V to 6.0V
- Frequency range of 32 kHz to 12MHz
- Very low current consumption
- Operating temperature range: -40 to +85°C

DESCRIPTION

The 80CL51 is manufactured in an advanced CMOS technology. The instruction set of the 80CL51 is based on that of the 8051. The 80CL51 is a general purpose microcontroller especially suited for battery-powered application. The device has low power consumption and a wide range of supply voltage. For emulation purposes, the 85CL000 (Piggy-back version) with 256 bytes of RAM is recommended. The 80CL51 has two software selectable modes of reduced activity for further power reduction: Idle and Power-down. The 80CL51 also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 46 two-byte, and 16 three-byte.

PIN CONFIGURATIONS



ORDERING INFORMATION

ROMLESS	ROM	TEMPERATURE RANGE °C AND PACKAGE	DRAWING NUMBER
P80CL31HFP	P80CL51HFP	40-lead Plastic Dual In-line Package	SOT129
P80CL31HFT	P80CL51HFT	40-lead Plastic Small Outline Package	SOT158A

CMOS single-chip 8-bit microcontroller with A/D and watchdog timer

80C550/83C550/87C550

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATA SHEET

DESCRIPTION

The Philips 8XC550 is a high-performance microcontroller fabricated with Philips high-density CMOS technology. This Philips CMOS technology combines the high speed and density characteristics of HMOS with the low power attributes of CMOS. Philips epitaxial substrate minimizes latch-up sensitivity. The CMOS 8XC550 has the same instruction set as the 80C51.

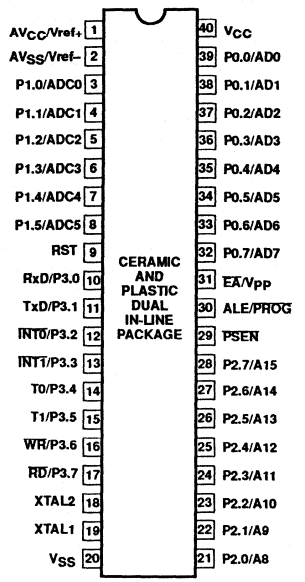
The 8XC550 contains a 4k × 8 EPROM (87C550)/ROM (83C550)/ROMless (80C550 has no program memory on-chip), a 128 × 8 RAM, 8 channels of 8-bit A/D, four 8-bit ports (port 1 is input only), a watchdog timer, two 16-bit counter/timers, a seven-source, two-priority level nested interrupt structure, a serial I/O port for either multi-processor communications, I/O expansion or full duplex UART, and an on-chip oscillator and clock circuits.

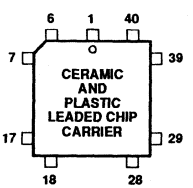
In addition, the 8XC550 has two software selectable modes of power reduction — idle mode and power-down mode. The idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

FEATURES

- 80C51 based architecture
  - 4k × 8 EPROM (87C550)/ ROM (83C550)
  - 128 × 8 RAM
  - Eight channels of 8-bit A/D
  - Two 16-bit counter/timers
  - Watchdog timer
  - Full duplex serial channel
  - Boolean processor
- Memory addressing capability
  - 64k ROM and 64k RAM
- Power control modes:
  - Idle mode
  - Power-down mode
- CMOS and TTL compatible
- One speed range at V_{CC} = 5V ±10%
  - 3.5 to 16MHz
- Four package styles
- Extended temperature ranges
- OTP package available

PIN CONFIGURATIONS





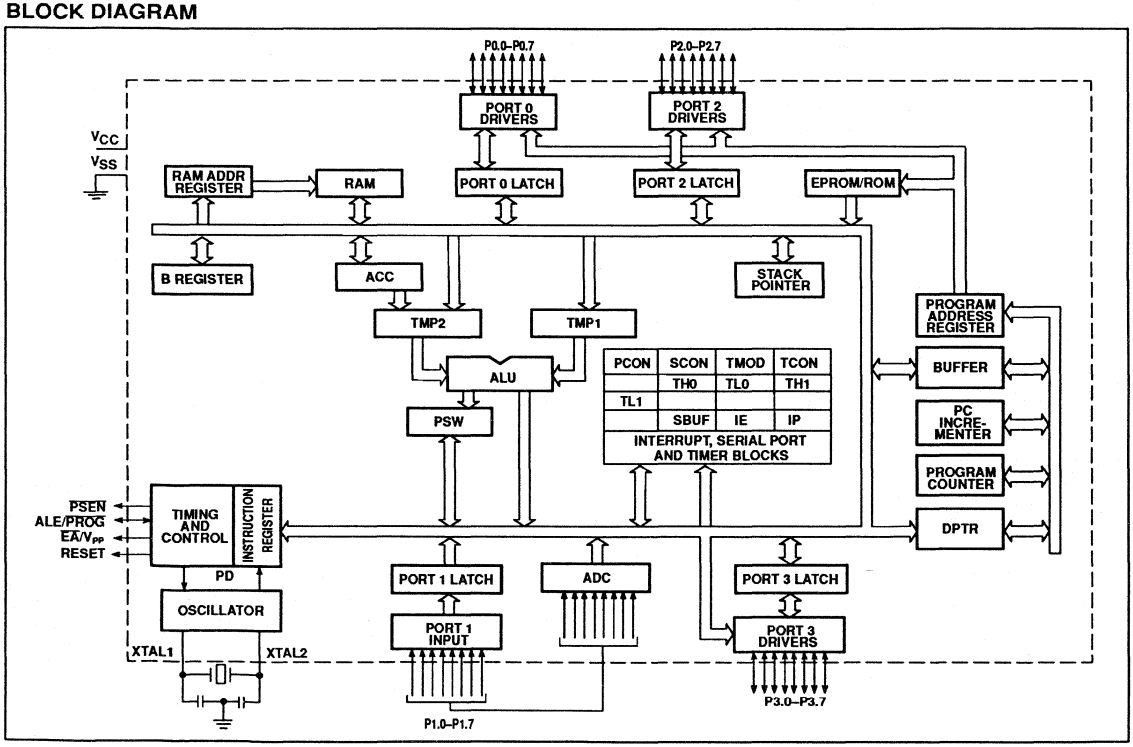
Pin	Function	Pin	Function	Pin	Function
1	AV_{CC}	16	P3.2/INT0	31	P2.6/A14
2	Vref+	17	P3.3/INT1	32	P2.7/A15
3	Vref–	18	P3.4/T0	33	PSEN
4	AV_{SS}	19	P3.5/T1	34	ALE/PROG
5	P1.0/ADC0	20	P3.6/WR	35	EA/V_{PP}
6	P1.1/ADC1	21	P3.7/RD	36	P0.7/AD7
7	P1.2/ADC2	22	XTAL2	37	P0.6/AD6
8	P1.3/ADC3	23	XTAL1	38	P0.5/AD5
9	P1.4/ADC4	24	V_{SS}	39	P0.4/AD4
10	P1.5/ADC5	25	P2.0/A8	40	P0.3/AD3
11	P1.6/ADC6	26	P2.1/A9	41	P0.2/AD2
12	P1.7/ADC7	27	P2.2/A10	42	P0.1/AD1
13	RST	28	P2.3/A11	43	P0.0/AD0
14	P3.0/RxD	29	P2.4/A12	44	V_{CC}
15	P3.1/TxD	30	P2.5/A13		

ORDERING INFORMATION

ROMless	ROM	EPROM	TEMPERATURE RANGE °C AND PACKAGE [1]	FREQ MHz	DRAWING NUMBER
		P87C550EBF FA	0 to +70, Ceramic Dual In-Line Package, UV	3.5 to 16	0590B
		P87C550EBL KA	0 to +70, Ceramic Leaded Chip Carrier, UV	3.5 to 16	1472A
P80C550EBP N	P83C550EBP N	P87C550EBP N	0 to +70, Plastic Dual In-Line Package, OTP	3.5 to 16	0415C
P80C550EBA A	P83C550EBA A	P87C550EBA A	0 to +70, Plastic Leaded Chip Carrier, OTP	3.5 to 16	0403G
P80C550EFP N	P83C550EFP N	P87C550EFP N	–40 to +85, Plastic Dual In-Line Package, OTP	3.5 to 16	0415C
P80C550EFA A	P83C550EFA A	P87C550EFA A	–40 to +85, Plastic Leaded Chip Carrier, OTP	3.5 to 16	0403G
		P87C550EFL KA	–40 to +85, Ceramic Leaded Chip Carrier, UV	3.5 to 16	1472A
		P87C550EFF FA	–40 to +85, Ceramic Dual In-Line Package, UV	3.5 to 16	0590B

NOTES:
1. OTP = One Time Programmable EPROM. UV = UV Erasable EPROM.

BLOCK DIAGRAM



Low voltage/low power single-chip 8-bit microcontroller with I²C

80CL410/83CL410

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATA SHEET

DESCRIPTION

The 80CL410/83CL410 (hereafter generically referred to as 8XCL410) is manufactured in an advanced CMOS process that allows the part to operate at supply voltages down to 1.8V and oscillator frequencies down to DC. The 8XCL410 has the same instruction set as the 80C51.

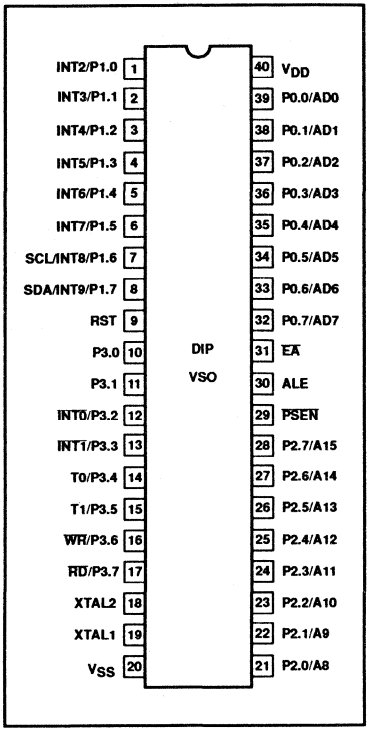
The 8XCL410 features a 4k byte ROM (83CL410), 128 bytes RAM (both ROM and RAM are externally expandable to 64k bytes), four 8-bit ports, two 16-bit timer/counters, an I²C serial interface, a thirteen source, two priority level nested interrupt structure, and on-chip oscillator circuitry suitable for quartz crystal, ceramic resonator, RC, or LC.

The 8XCL410 has two reduced power modes that are the same as those on the standard 80C51. The special reduced power feature of this part is that it can be stopped and then restarted. Running from an external clock source, the clock can be stopped and after a period of time restarted. The 8XCL410 will resume operation from where it was when the code stopped with no loss of internal state, RAM contents, or Special Function Register contents. If the internal oscillator is used the part cannot be stopped and started, but the power-down mode, which can be terminated via an interrupt, can be used to achieve similar power savings and then restart without loss of on-chip RAM and Special Function Register values.

FEATURES

- Supply voltage from 1.8 to 6.0V
- Operating frequency from 32kHz to 12MHz (see Note 1)
- 80C51 based architecture
  - 4k × 8 ROM (64k external)
  - 128 × 8 RAM (64k external)
  - Four 8-bit I/O ports
  - Two 16-bit timer/counters
  - A thirteen-source, two-level, nested priority interrupt structure
  - 10 external interrupts
- Fully static 80C51 CPU
- I²C Serial Interface
- Two power control modes
  - Idle mode
  - Power-down mode – can be terminated by reset or external interrupt
- Wake-up via external interrupts at port 1
- On-chip oscillator (quartz crystal, ceramic resonator, RC, LC)
- Very low power consumption
- Operating temperature range: –40 to +85°C

PIN CONFIGURATION



NOTE:
1. The currently available product is guaranteed up to 12MHz at 4.5V. A 16MHz device will be made available during 1992.

ORDERING CODE

PHILIPS PART ORDER NUMBER PART MARKING		SIGNETICS PART ORDER NUMBER[1]		TEMPERATURE (°C) AND PACKAGE	FREQUENCY
ROMless	ROM	ROMless	ROM		
P80CL410HFP	P83CL410HFP	P80CL410HF N	P83CL410HF N	–40 to +85, plastic DIP	32kHZ to 12MHz
P80CL410HFT	P83CL410HFT	P80CL410HF D	P83CL410HF D	–40 to +85, plastic VSO	32kHZ to 12MHz

NOTE:
1. Parts ordered by the Signetics part number will be marked with the Philips part marking.

For emulation purposes, the P85CL000 (Piggyback version) with 256 bytes of RAM is recommended.

Low-voltage 8-bit microcontroller P83CL411

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATA SHEET

FEATURES

- 80C51 central processing unit (CPU)
- 4 k x 8 ROM, externally expandable to 64 k bytes
- 256 bytes RAM, externally expandable to 64 k bytes
- Four 8-bit ports, 32 I/O lines
- Two 16-bit timer/event counters
- External memory expandable up to 128 k, external ROM up to 64 k and/or RAM up to 64 k
- On-chip oscillator suitable for RC, LC, quartz crystal or ceramic resonator
- 13 source, 13 vector interrupt structure with 2 priority levels
- Full-duplex serial UART facilities
- Enhanced architecture with:
  - non page oriented instructions
  - direct addressing
  - 4 x 8 byte RAM register banks
  - stack depth limited only by available internal RAM (maximum 256 bytes)
  - multiply, divide, subtract and compare instructions
- STOP and IDLE instructions
- Wake-up via external interrupts at Port 1
- Single supply voltage range 1.8 V to 6.0 V
- XTAL frequency range 32 kHz to 12 MHz
- Very low current consumption
- Operating ambient temperature range: T_{amb} = −40 to +85 °C

GENERAL DESCRIPTION

The P83CL411 is manufactured in an advanced CMOS technology. The instruction set of the P83CL411 is based on that of the 8051. The P83CL411 is an 8-bit general purpose microcontroller especially suited for cordless telephone applications. The device has low power consumption and a wide range of supply voltage. For emulation purposes, the P85CL781 (Piggy-back version) with 256 bytes of RAM is recommended.

The P83CL411 has two software selectable modes of reduced activity for further power reduction: Idle and Power-down. The P83CL411 also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set comprises over 100 instructions: 49 one-byte, 46 two-byte and 16 three byte.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
P83CL411HFP	40	DIL	plastic	SOT129
P83CL411HFH	44	QFP	plastic	SOT205AG

Low-voltage single-chip 8-bit microcontroller

P83CL580

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATA SHEET

FEATURES

- Full static 80C51 CPU
- 8-bit CPU, ROM, RAM, I/O in a single 56-lead mini-pack
- 6K x 8 ROM, expandable externally to 64K bytes
- 256 bytes RAM, expandable externally to 64K bytes
- Five 8-bit ports, 40 I/O lines
- Three 16-bit timer / event counters
- External memory expandable up to 128K, external ROM up to 64K and / or RAM up to 64K
- On-chip oscillator suitable for RC, LC, quartz crystal or ceramic resonator
- Fifteen source, fifteen vector interrupt structure with two priority levels
- Full duplex serial UART
- I²C-bus interface for serial transfer on two lines
- A/D converter with power-down mode (8-bit, 4 inputs)
- Pulse width modulated output (8-bit resolution)
- Watchdog timer
- Enhanced architecture with:
  - non-page oriented instructions
  - direct addressing
  - four eight byte RAM register banks
  - stack depth limited only by available internal RAM (max. 256 bytes)
  - multiply, divide, subtract and compare instructions
- STOP and IDLE instructions
- Wake-up via external interrupts at Port 1
- Single supply voltage of 2.5 V to 6.0 V
- Frequency range of 32 kHz to 16 MHz *
- Very low current consumption: typically 5 mA (3 V, 8 MHz)
- Operating temperature range: –40 to +85 °C

* The currently available product is guaranteed up to 12 MHz at 4.5 V. A device covering the range up to 16 MHz at 4.5 V will be available later in 1992.

GENERAL DESCRIPTION

The P83CL580 is manufactured in an advanced CMOS technology. The instruction set of the P83CL580 is based on that of the 8051. The P83CL580 is an 8-bit general purpose microcontroller especially suited for "cordless phones" and mobile communication applications. The device has low power consumption and a wide range of supply voltage. For emulation purposes, the P85CL000 (Piggy-back version) with 256 bytes of RAM is recommended. The P83CL580 has two software selectable modes of reduced activity for further power reduction: Idle and Power-down. The P83CL580 also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 46 two-byte, and 16 three-byte.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
P83CL580HFT	56	mini-pack	plastic	SOT190

Low-voltage 8-bit microcontroller P83CL782

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATA SHEET

FEATURES

- 80C51 central processing unit (CPU)
- 16 k x 8 ROM, externally expandable to 64 k bytes
- 256 bytes RAM, externally expandable to 64 k bytes
- Four 8-bit ports, 32 I/O lines
- Three 16-bit timer/event counters
- External memory expandable up to 128 k, external ROM up to 64 k and/or RAM up to 64 k
- On-chip oscillator suitable for RC, LC, quartz crystal or ceramic resonator
- 15 source, 15 vector interrupt structure with 2 priority levels
- Full-duplex serial UART facilities
- I²C-bus interface for serial transfer on two lines
- Enhanced architecture with:
  - non page oriented instructions
  - direct addressing
  - 4 x 8 byte RAM register banks
  - stack depth limited only by available internal RAM (maximum 256 bytes)
  - multiply, divide, subtract and compare instructions
- STOP and IDLE instructions
- Wake-up via external interrupts at Port 1
- Single supply voltage range 1.8 V to 6.0 V
- XTAL frequency range 32 kHz to 12 MHz (12 MHz at 3.0 V)
- Very low current consumption
- Operating ambient temperature range: T_{amb} = –25 to +55 °C

GENERAL DESCRIPTION

The P83CL782 is manufactured in an advanced CMOS technology. The instruction set of the P83CL782 is based on that of the 8051. The P83CL782 is an 8-bit general purpose microcontroller especially suited for cordless telephone applications. The device has low power consumption and a wide range of supply voltage. For emulation purposes, the P85CL781 (Piggy-back version) with 256 bytes of RAM is recommended.

The P83CL782 has two software selectable modes of reduced activity for further power reduction: Idle and Power-down. The P83CL782 also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set comprises over 100 instructions: 49 one-byte, 46 two-byte and 16 three byte.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
P83CL782HDP	40	DIL	plastic	SOT129
P83CL782HDH	44	QFP	plastic	SOT205AG

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 358 10011.

16/32-bit microcontrollers P9xC1xx Family

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC21 OR DATA SHEET

1. FEATURES

- CHMOS technology
- 32-bit internal structure
- Maximum internal clock frequency: 15 MHz
- 8 programmable interrupt inputs
- Choice of on-chip memory (RAM, ROM and EPROM)
- Built-in clock generators - maximum 30 MHz crystal
- Reset control circuitry
- On-chip address decoder
- 16-bit input/output General Purpose Port
- 8-bit input/output Auxiliary Port
- 16-bit input/output Secondary Port
- I²C serial bus interface
- UART serial interface
- 16-bit timer/counter
- Two 16-bit match/count/capture registers
- Full 68000 software compatibility
- 68000-compatible bus interface
- 56 powerful instruction types
- 5 basic data types
- 2 M byte addressing range
- 14 addressing modes
- Memory-mapped I/O
- Auto-vectored interrupts
- 7 interrupt levels
- Reduced power modes
- 80C51 bus interface compatible
- 84-pin PLCC or 80-pin QFP package
- Supply voltage of 3.3 to 6.0 V (9xC101 only)

2. GENERAL DESCRIPTION

This document gives an overview of the basic functions, internal structure and electrical characteristics of the P9xC1xx family of microcontrollers. The family comprises the 90C100, 93C100, 97C100; 90C101 and the 93C101 in this data sheet the term 90C100 refers to any one of the family members. The 90C100 is a highly integrated 16/32-bit microcontroller for use in a large variety of applications and is fully software compatible with the 68000. By integrating standard as well as advanced peripheral functions on the 90C100, system costs are dramatically reduced.

The internal architecture of the 90C100 is built around a bus interconnecting the CPU and the various on-chip peripheral functions. Each function has several dedicated connections to the external circuitry. The 90C100 has powerful programmable interrupt processing circuitry for interrupts generated by internal and external sources. An on-chip clock generator provides a 15 MHz clock signal for CPU and peripheral interfaces.

The I²C-bus interface allows easy and low-cost addition of peripherals (master and slave devices). The 90C100 also includes a UART interface. Expansion of memory (up to 2 M bytes) and catering for additional peripherals is possible using dedicated 8051 and 68000 compatible buses. A built-in timer/counter with two independently programmable match/count/capture registers means that the 90C100 can be programmed with any two of the following options simultaneously:

- pulse generator
- external event counter
- reference timer

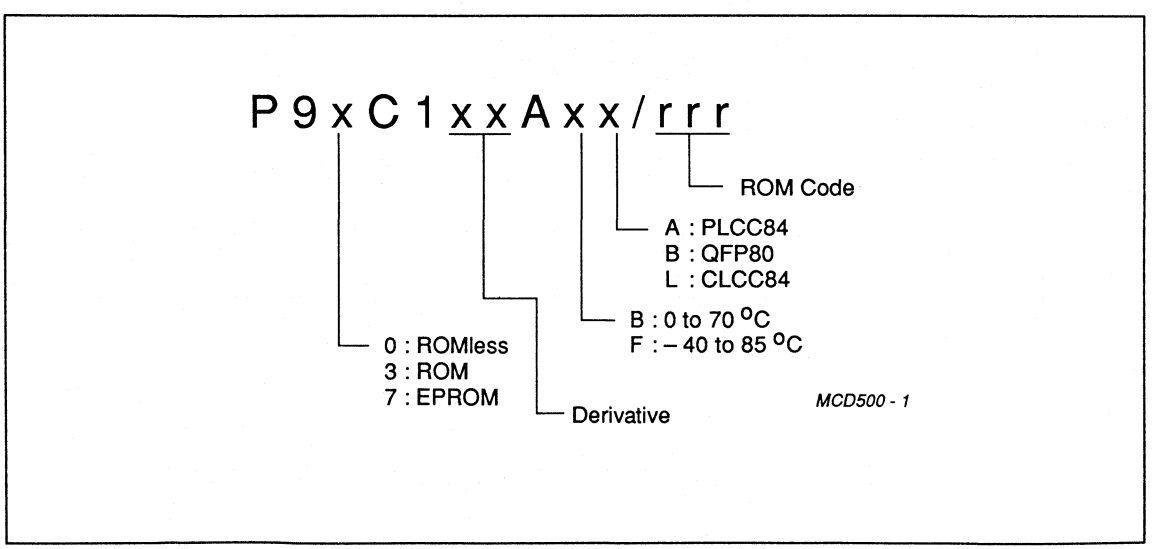
A choice of memory configurations is possible with this family of microcontrollers; these are shown in Table 1. A total of 40 input/output pins are available having standard or quasi-bidirectional features.

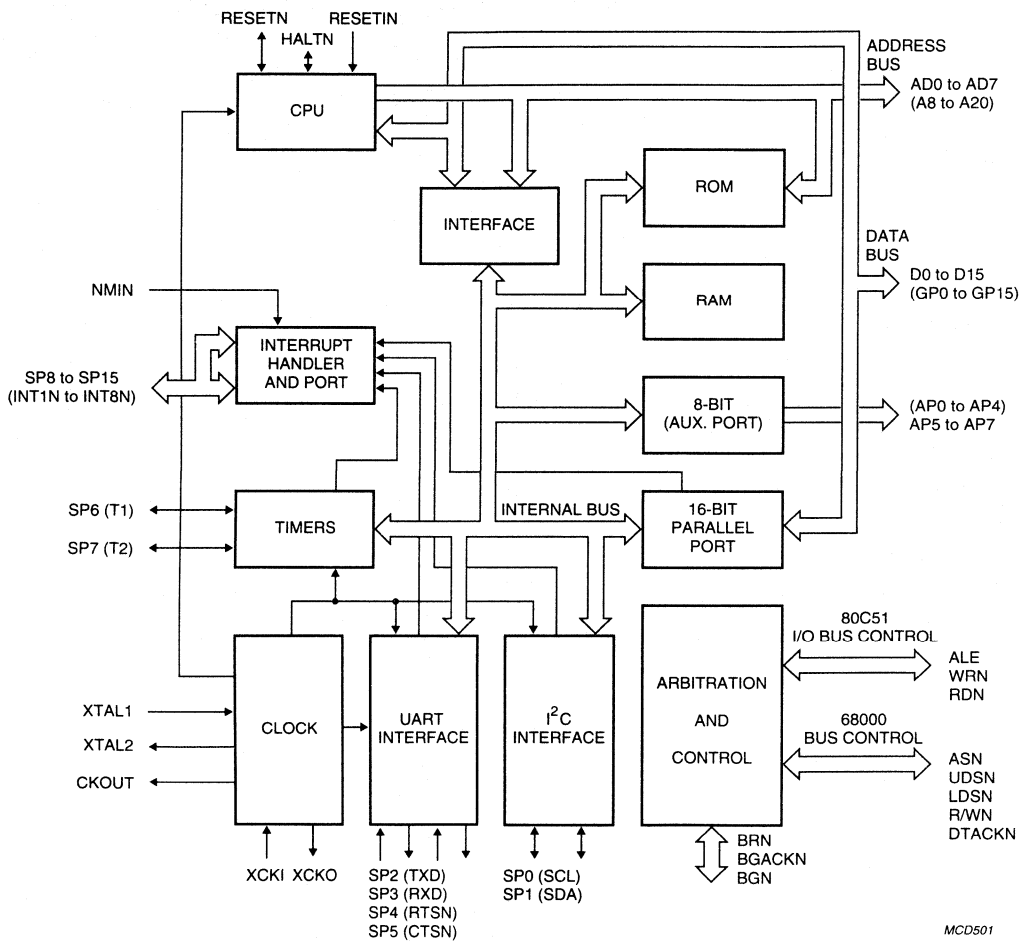
Table 1 Memory configurations

DEVICE	RAM	ROM	EPROM
90C100	512 bytes	–	–
93C100	512 bytes	34 K bytes	–
97C100	512 bytes	–	32 K bytes
90C101	512 bytes	–	–
93C101	512 bytes	34 K bytes	–

3. ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE				TEMPERATURE RANGE (°C)
	PINS	PIN POSITION	MATERIAL	CODE	
P90C100ABA	84	PLCC	plastic	SOT189	0 to 70
P90C100ABB	80	QFP	plastic	SOT318	0 to 70
P90C100AFA	84	PLCC	plastic	SOT189	–40 to 85
P90C100AFB	80	QFP	plastic	SOT318	–40 to 85
P93C100ABA	84	PLCC	plastic	SOT189	0 to 70
P93C100ABB	80	QFP	plastic	SOT318	0 to 70
P93C100AFA	84	PLCC	plastic	SOT189	–40 to 85
P93C100AFB	80	QFP	plastic	SOT318	–40 to 85
P97C100ABA	84	PLCC	plastic	SOT189	0 to 70
P97C100AFA	84	PLCC	plastic	SOT189	–40 to 85
P97C100ABL	84	CLCC	ceramic	NO331B	0 to 70
P97C100AFL	84	CLCC	ceramic	NO331B	–40 to 85
P90C101ABA	84	PLCC	plastic	SOT189	0 to 70
P90C101ABB	80	QFP	plastic	SOT318	0 to 70
P90C101AFA	84	PLCC	plastic	SOT189	–40 to 85
P90C101AFB	80	QFP	plastic	SOT318	–40 to 85
P93C101ABA	84	PLCC	plastic	SOT189	0 to 70
P93C101ABB	80	QFP	plastic	SOT318	0 to 70
P93C101AFA	84	PLCC	plastic	SOT189	–40 to 85
P93C101AFB	80	QFP	plastic	SOT318	–40 to 85





1. AP7, BGACKN, BRN and BGN not available with the QFP80 package.

Fig.1 Block diagram.

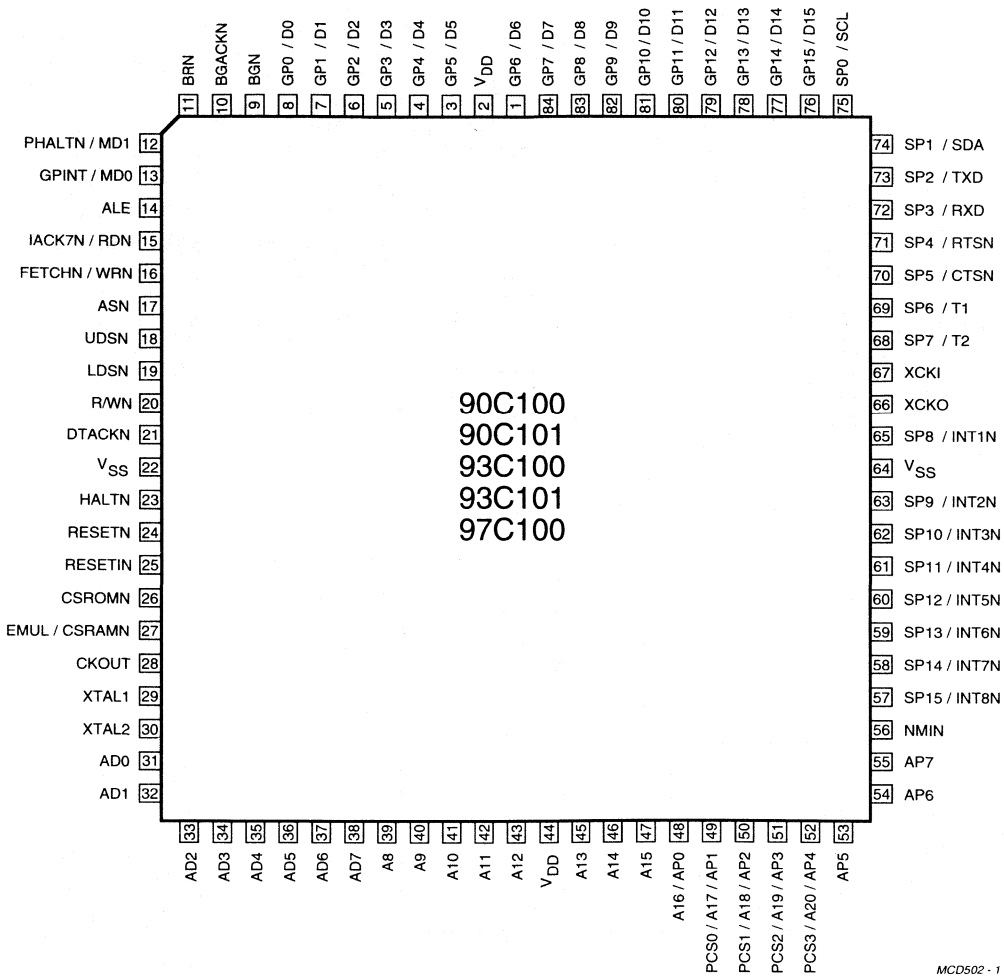


Fig.2 Pinning diagram for PLCC84.

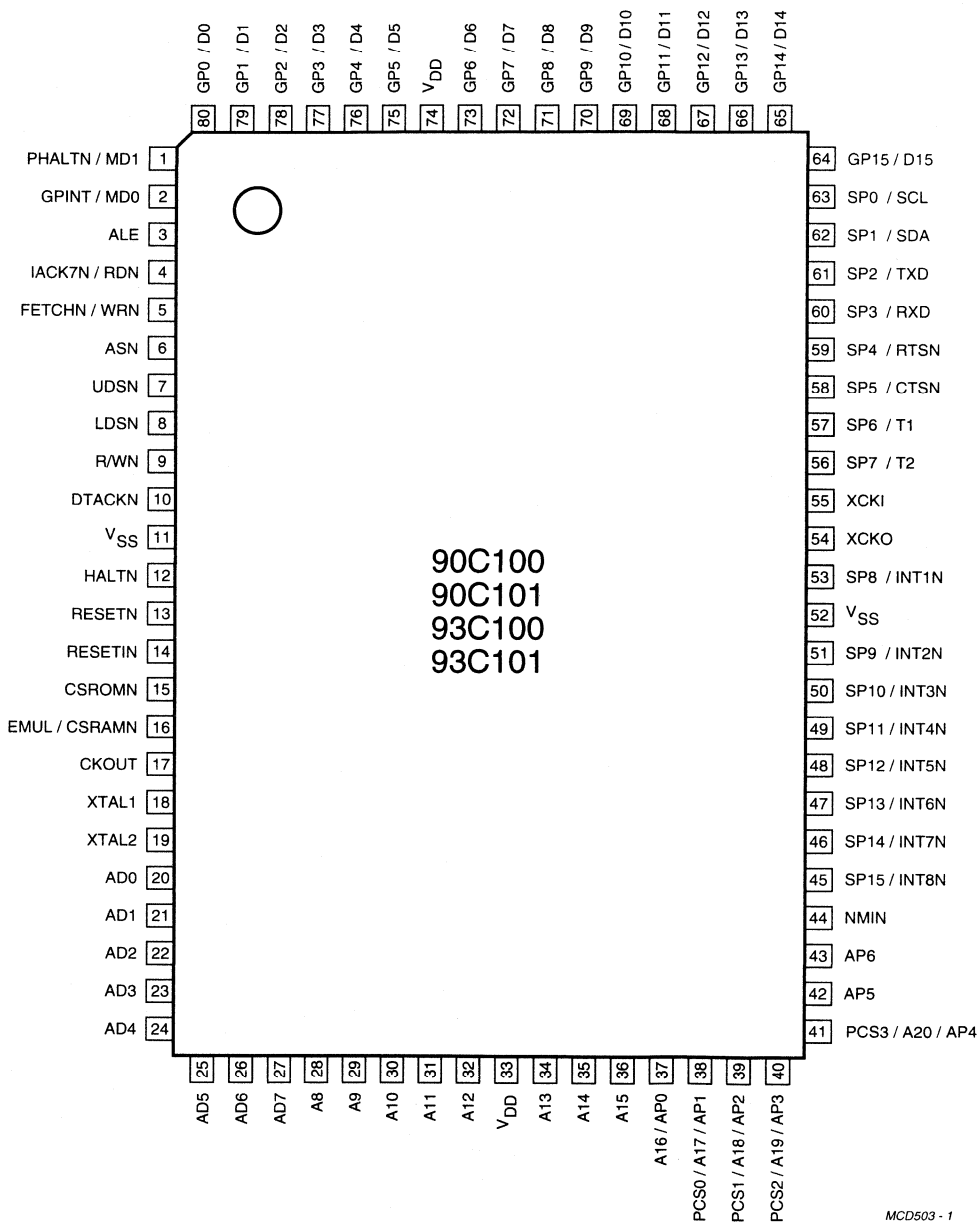


Fig.3 Pinning diagram for QFP80.

4. SIGNAL DESCRIPTION

MNEMONIC	TYPE	PLCC84	QFP80	FUNCTION
AD0 to AD7	I/O	31-38	20–27	**Address/Data bus** (active HIGH, 3-state). Multiplexed bus for peripheral extension (8051), these are the LSBs for the address bus during memory extension cycles (68000).
A8 to A15	O	39-43, 45-47	28–32, 34–36	**Address lines** (active HIGH, 3-state). Used as the MSBs for peripheral extension cycles and as the middle part of address bus for memory extension cycles.
AP0 to AP4 (A16 to A20) (PCS0 to PCS3)	I/O	48-52	37–41	**Auxiliary I/O port**. Either the MSBs of the address in Memory extension cycles or Chip selects.
GP0 to GP15 (D0 to D15)	I/O	8-3 1, 84-76	80–75, 73–64	**General Purpose port** (active HIGH, 3-state). Alternative function 16-bit bidirectional Data bus for the 68000 memory.
ASN	O	17	6	**Address Strobe** (active LOW, 3-state). Indicates a valid address on the bus.
LDSN	O	19	8	**Lower Data Strobe** (active LOW, 3-state). For a WRITE cycle, the data is valid on the lower half of the data bus (D0 to D7). For a READ cycle, the data is to be placed on the lower half of the bus (D0 to D7).
UDSN	O	18	7	**Upper Data Strobe** (active LOW, 3-state). For a WRITE cycle, the data is valid on the upper half of the data bus (D8 to D15). For a READ cycle, the data is to be placed on the upper half of the bus (D8 to D15).
R/WN	O	20	9	**Read** (active HIGH)/**Write** (active LOW, 3-state). Controls the direction of the data flow of the memory bus cycle.
DTACKN	I	21	10	**Data Transfer Acknowledge** (active LOW). Asserted by the peripheral during CPU bus cycles when data is either received from or placed on the bus. If not asserted punctually it causes the CPU to insert wait states.
BRN	I	11	n.a.	**Bus Request** (active LOW). Asserted by wire-ORed external DMA devices that request bus ownership. (PLCC package only). See note 1.
BGN	O	9	n.a.	**Bus Grant** (active LOW). A daisy chain output which is asserted by the 90C100 when the bus is granted by the CPU. (PLCC package only).
BGACKN	I/O	10	n.a.	**Bus Grant Acknowledge** (active LOW, open drain). Asserted by any external DMA device that has control of the bus or by the internal 80C51 bus controller. As long as this line is held LOW externally, the 90C100 will hold the bus signals in the high impedance state. When BGACKN is released, the 90C100 will have access to the bus. (PLCC package only). See note 1.
RESETN	I/O	24	13	**Reset** (active LOW, open drain, bidirectional). If asserted externally together with the HALTN line, it will cause the processor to enter the Reset state. It is driven LOW by the processor when the Reset instruction resets external hardware or on-chip peripherals. See note 1.

MNEMONIC	TYPE	PLCC84	QFP80	FUNCTION
HALTN	I/O	23	12	**Halt** (active LOW, open drain, bidirectional). If asserted externally together with RESETN, it causes the 90C100 to enter the Reset state. If asserted alone, it will cause the CPU to stop after completion of the current bus cycle. As long as HALTN is held LOW, all control signals are inactive (except BGACKN) and all 3-state lines are placed in the high-impedance state. When the processor has stopped executing instructions (e.g. after a double bus fault), the processor drives this line LOW. See note 1.
NMIN	I	56	44	**Non-Maskable Interrupt (level 7)** (active LOW). While the other interrupts may be masked (disabled), this interrupt is always enabled. The LOW level must be maintained until the interrupt acknowledge cycle is performed.
SP8 to SP15 (INT1N to INT8N)	I/O	65, 63-57	53, 51–45	**Latched Interrupt Inputs** (active LOW). A LOW level for ≥ 1 clock pulse will be stored as a pending interrupt request. Priority levels are programmable. These 8-bits may also be used as an Input/Output port. See note 1.
RESETIN	I	25	14	**Reset Input Line** (active HIGH). Connected to an external capacitor in order to provide the correct reset sequence at power-up.
V_{DD}	-	44, 2	33, 74	**Supply voltage** + 5 V nominal.
V_{SS}	-	22, 64	11, 52	**Ground.**
XTAL1, XTAL2	I	29, 30	18, 19	**External Crystal Inputs.** XTAL1 can be used as a clock-input if an external clock generator is used. The crystal or external clock frequency is divided by 2 to obtain the internal clock and CKOUT signals.
CKOUT	O	28	17	**Clock Out.** This is the reference from the internal system clock.
MD0/GPINT MD1/PHALTN	I	13, 12	2, 1	**Input lines.** These signals define the memory map to be used and the activation of the 16-bit parallel port or the 16-bit data bus. These pins are combined with signals used in emulator mode: GPINT is the Interrupt coming from the external logic used to emulate the GP port. PHALTN is used to freeze the state of the on chip peripherals.
ALE	O	14	3	**Address Latch Enable.** Used to latch the low byte of address (AD0-AD7) during access to external 8051 bus compatible peripheral circuits.
WRN/FETCHN	O	16	5	**External Peripheral Write Strobe** (active LOW). In emulator mode, this pin serves also as the FETCHN output.
RDN/IACK7N	O	15	4	**External Peripheral Read Strobe** (active LOW). In emulator mode, this pin serves also as IACK7N output.

MNEMONIC	TYPE	PLCC84	QFP80	FUNCTION
CSROMN	O	26	15	**ROM Chip Select** (active LOW). Decodes a size of 512 K bytes mapped from 0 to 512 K bytes (available in the Modes 1 to 3). CSROMN is asserted during the read cycles of the Reset Vector.
CSRAMN/EMUL	O	27	16	**RAM Chip Select** (active LOW). Decodes a size of 512 K bytes mapped from 512 K bytes to 1 M bytes (available in the Modes 1 to 3). This pin is also used during Reset, to enter Emulator mode. See notes 1 and 2.
AP5 to AP7	I/O	53–55	42, 43, n.a.	**Auxiliary I/O Port** (always available). AP7 is not available in the QFP package.
SCL (SP0)	I/O	75	63	**Serial Clock** (open drain). SCL is the clock signal for the I²C-bus operation. It is driven either by the 90C100 when the I²C interface is in the master mode, or it becomes the clock input when I²C interface is in the slave mode.
SDA (SP1)	I/O	74	62	**Serial Data** (open drain). SDA is the data signal for the I²C-bus.
T1 (SP6), T2 (SP7)	I/O	69, 68	57, 56	**Timers 1 and 2** (3-state). These are I/O signals for the capture timers of Channels 1 and 2 respectively. They can be programmed as either outputs for pulses or inputs for count cycles and events.
RXD (SP3)	I/O	72	60	**Receive Data**. RXD is the data input for the UART serial interface.
TXD (SP2)	I/O	73	61	**Transmit Data**. TXD is data output for the UART serial interface.
RTSN (SP4)	I/O	71	59	**Request To Send** (active LOW). This output of the UART serial interface indicates that the receiver is ready to accept data on the RXD line.
CTSN (SP5)	I/O	70	58	**Clear To Send** (active LOW). This input to the UART serial interface indicates that the remote receiving device is ready. RTSN and CTSN can be connected to each other if no control lines are required.
XCKI	I	67	55	**External Clock**. When selected, XCKI is the clock input for the UART serial interface. This signal can be used to either: - generate special baud rates. - or when a crystal frequency other than 29.491 MHz is used by the 90C100, an external clock of 9.8304 MHz may be connected to this input to generate the standard baud rates.
XCKO	O	66	54	**Auxiliary Oscillator Output**. To be connected along with XCKI, to a crystal in order to generate the auxiliary clock for the UART or the CPU. Can be used as a low-cost RC oscillator for stand-by function.
SP0 to SP7	I/O	75-68	63–56	**Input/Output** port if the alternate function is not used.

Notes

1. Pin with high impedance pull-up resistor
2. The pull-up on CSRAMN/EMUL is activated during the RESET to avoid floating level at power-on.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC06 OR DATA SHEET

DIGITAL PHASE-LOCKED-LOOP FILTER

FEATURES

- **Digital design avoids analog compensation errors**
- **Easily cascadable for higher order loops**
- **Useful frequency range: DC to 55 MHz typical (K-clock) DC to 35 MHz typical (I/D-clock)**
- **Dynamically variable bandwidth**
- **Very narrow bandwidth attainable**
- **Power-on reset**
- **Output capability: standard/bus driver**
- **I_{CC} category: MSI**

GENERAL DESCRIPTION

The 74HC/HCT297 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT297 are designed to provide a simple, cost-effective solution to high-accuracy, digital, phase-locked-loop applications. These devices contain all the necessary circuits, with the exception of the divide-by-n counter, to build first order phase-locked-loops.

Both EXCLUSIVE-OR (XORPD) and edge-controlled (ECPD) phase detectors are provided for maximum flexibility. The input signals for the EXCLUSIVE-OR phase detector must have a 50% duty factor to obtain the maximum lock-range.

Proper partioning of the loop function, with many of the building blocks external to the package, makes it easy for the designer to incorporate ripple cancellation (see Fig. 7) or to cascade to higher order phase-locked-loops.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay I/D_{CP} to I/D_{OUT} ϕA_1, ϕB to $XORPD_{OUT}$ ϕB, ϕA_2 to $ECPD_{OUT}$	C_L = 15 pF V_{CC} = 5 V	 15 13 19	 18 13 19	ns
f_{max}	maximum clock frequency K_{CP} I/D_{CP}		 63 41	 68 40	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	18	19	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

16-lead DIL; plastic (SOT38Z).

16-lead mini-pack; plastic (SO16; SOT109A).

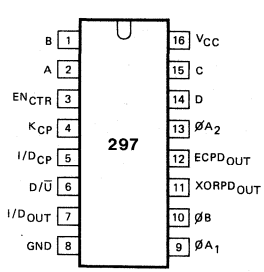


Fig. 1 Pin configuration.

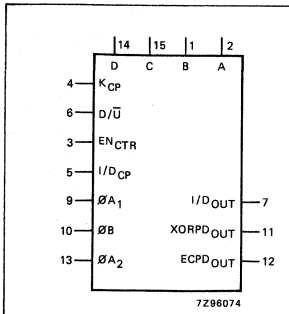


Fig. 2 Logic symbol.

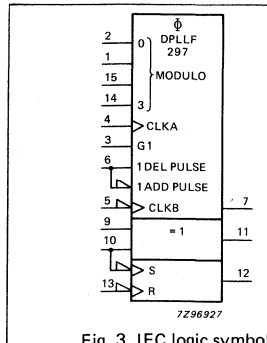


Fig. 3 IEC logic symbol.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC06 OR DATA SHEET

PHASE-LOCKED-LOOP WITH VCO

FEATURES

- **Low power consumption**
- **Centre frequency of up to 17 MHz (typ.) at V_{CC} = 4.5 V**
- **Choice of three phase comparators: EXCLUSIVE-OR; edge-triggered JK flip-flop; edge-triggered RS flip-flop**
- **Excellent VCO frequency linearity**
- **VCO-inhibit control for ON/OFF keying and for low standby power consumption**
- **Minimal frequency drift**
- **Operating power supply voltage range: VCO section 3.0 to 6.0 V digital section 2.0 to 6.0 V**
- **Zero voltage offset due to op-amp buffering**
- **Output capability: standard**
- **I_{CC} category: MSI**

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
f_o	VCO centre frequency	C1 = 40 pF R1 = 3 kΩ V_{CC} = 5 V	19	19	MHz
C_I	input capacitance (pin 5)		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	24	24	pF

GND = 0 V; T_{amb} = 25 °C

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. Applies to the phase comparator section only (VCO disabled). For power dissipation of the VCO and demodulator sections see Figs 22, 23 and 24.

PACKAGE OUTLINES

16-lead DIL; plastic (SOT38Z).
16-lead mini-pack; plastic (SO16; SOT109A).

GENERAL DESCRIPTION

The 74HC/HCT4046A are high-speed Si-gate CMOS devices and are pin compatible with the "4046" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4046A are phase-locked-loop circuits that comprise a linear voltage-controlled oscillator (VCO) and three different phase comparators (PC1, PC2 and PC3) with a common signal input amplifier and a common comparator input.

The signal input can be directly coupled to large voltage signals, or indirectly coupled (with a series capacitor) to small voltage signals. A self-bias input circuit keeps small voltage signals within the linear region of the input amplifiers. With a passive low-pass filter, the "4046A" forms a second-order loop PLL. The excellent VCO linearity is achieved by the use of linear op-amp techniques.

(continued on next page)

APPLICATIONS

- **FM modulation and demodulation**
- **Frequency synthesis and multiplication**
- **Frequency discrimination**
- **Tone decoding**
- **Data synchronization and conditioning**
- **Voltage-to-frequency conversion**
- **Motor-speed control**

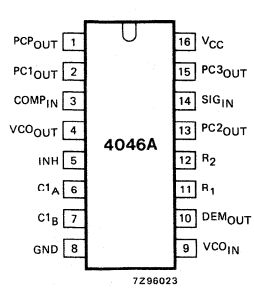


Fig. 1 Pin configuration.

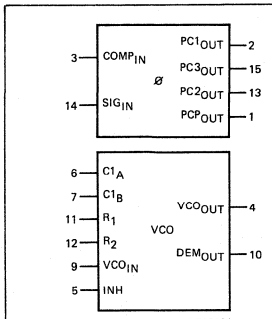


Fig. 2 Logic symbol.

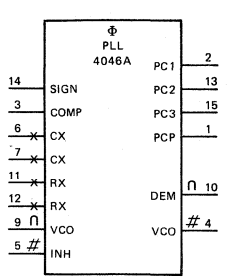


Fig. 3 IEC logic symbol.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC06 OR DATA SHEET

PHASE-LOCKED-LOOP WITH LOCK DETECTOR

FEATURES

- Low power consumption
- Centre frequency up to 17 MHz (typ.) at V_{CC} = 4.5 V
- Choice of two phase comparators: EXCLUSIVE-OR; edge-triggered JK flip-flop;
- Excellent VCO frequency linearity
- VCO-inhibit control for ON/OFF keying and for low standby power consumption
- Minimal frequency drift
- Operation power supply voltage range: VCO section 3.0 to 6.0 V digital section 2.0 to 6.0 V
- Zero voltage offset due to op-amp buffering
- Output capability: standard
- I_{CC} category: MSI

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
f_o	VCO centre frequency	C1 = 40 pF R1 = 3 kΩ V_{CC} = 5 V	19	19	MHz
C_I	input capacitance (pin 5)		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	24	24	pF

GND = 0 V; T_{amb} = 25 °C

Notes

1. Applies to the phase comparator section only (VCO disabled).
   For power dissipation of VCO and demodulator sections see Figs 20, 21 and 22.
2. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V

PACKAGE OUTLINES

16-lead DIL; plastic (SOT38CP).
16-lead mini-pack; plastic (SO16; SOT109A).

GENERAL DESCRIPTION

The 74HC/HCT7046 are high-speed Si-gate CMOS devices and are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT7046 are phase-locked-loop circuits that comprise a linear voltage-controlled oscillator (VCO) and two different phase comparators (PC1 and PC2) with a common signal input amplifier and a common comparator input.

A lock detector is provided and this gives a HIGH level at pin 1 (LD) when the PLL is locked. The lock detector capacitor must be connected between pin 15 (C_{LD}) and pin 8 (GND). The value of the C_{LD} capacitor can be determined, using information supplied in Fig. 32

The input signal can be directly coupled to large voltage signals, or indirectly coupled (with a series capacitor) to small voltage signals. A self-bias input circuit keeps small voltage signals within the linear region of the input amplifiers. With a passive low-pass filter, the "7046" forms a second-order loop PLL. The excellent VCO linearity is achieved by the use of linear op-amp techniques.

(continued on next page)

APPLICATIONS

- FM modulation and demodulation
- Frequency synthesis and multiplication
- Frequency discrimination
- Tone decoding
- Data synchronization and conditioning
- Voltage-to-frequency conversion
- Motor-speed control

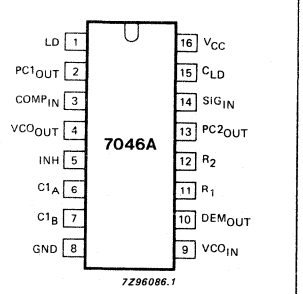


Fig. 1 Pin configuration.

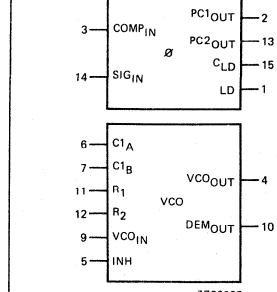


Fig. 2 Logic symbol.

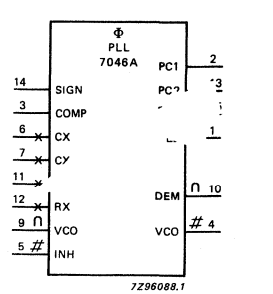


Fig. 3 IEC logic symbol.

Programmable analog CMOS transmission IC

PCA1070

FEATURES

- Line interface with:
  Voltage regulator with programmable DC voltage drop
  Programmable set impedance
  Output to control an external switching MOS transistor for pulse dialling
  Programmable DC voltage duting pulse dialling
  Circuitry for fast DC start-up
- Interface to peripheral circuits with:
  Supply for microcontroller and DTMF diallers
  Input to sense supply voltage of microcontroller and output for reset of microcontroller
  I²C-bus (programming of parameters, control of all logic signals)
  DTMF signal input
  Input for external oscillator signal
  Power down via I²C-bus
  Stabilized supply for electret microphones
- Microphone amplifier:
  Suitable for various types of microphones
  Symmetrical high impedance inputs
  Programmable gain
  Sending mute via I²C-bus to disable microphone amplifier and enable DTMF amplifier
  Sending mute also to be used as privacy switch
  Dynamic limiting (speech controlled) to prevent distortion of line signal and sidetone; programmable maximum sending level
- Receive amplifier
  Suitable for various types of earpieces (including piezo)
  Programmable gain and hearing protection level
  Receive mute via I²C-bus to disable receive amplifier and enable DTMF confidence tone
  On-chip anti-sidetone circuit with programmable sidetone balance
  Confidence tone in the earpiece during DTMF dialling
- Faciltity to regulate parameters with line current:
  Value of DC line current (bit code) readable via I²C-bus
  Line loss compensation with fully software programmable characteristics (control range, stop current) of microphone/earpiece/DTMF amplifiers
  Fully software programmable control of sidetone balance and DC voltage drop as a function of line length

APPLICATIONS

- Requires few external components
- Programming via I²C-bus

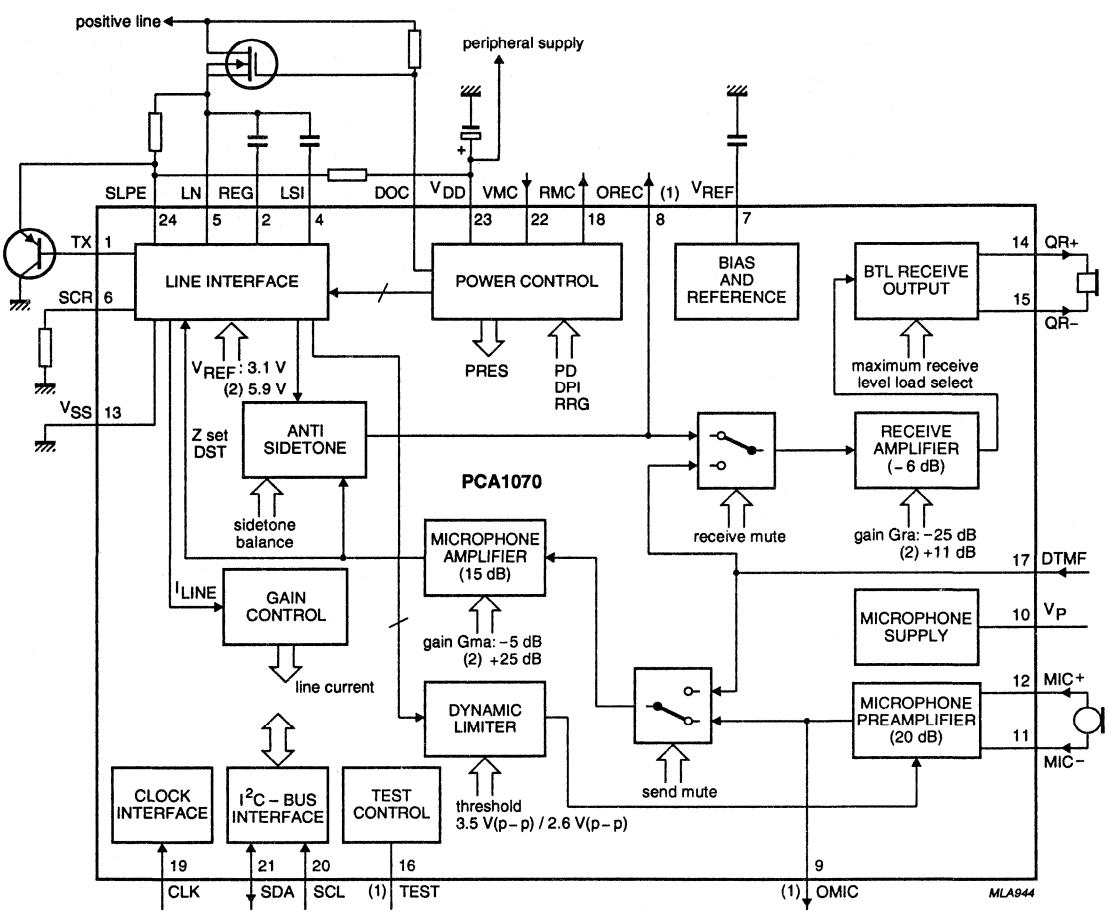
GENERAL DESCRIPTION

The PCA1070 is a CMOS integrated circuit performing all speech and line interface functions in fully electronic telephone sets. The device requires a minimum of external components. The transmission parameters are programmable via the I²C-bus.

The values are stored in the EEPROM of a microcontroller and are loaded in the PCA1070 during the start-up phase of the transmission IC after hook-off.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCA1070P	24	DIL	plastic	SOT101
PCA1070T	24	mini-pack	plastic	SO24; SOT137A



(1) Test pins.
(2) Default value.

Fig.1 Block diagram.

Programmable analog CMOS transmission IC

PCA1070

PINNING

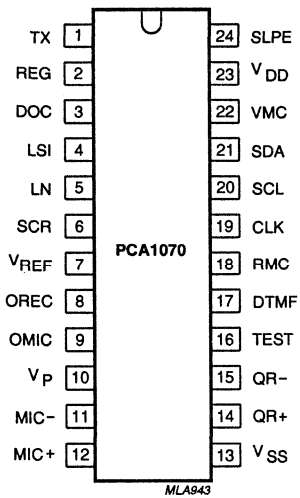


Fig.2 Pin configuration.

SYMBOL	PIN	DESCRIPTION
TX	1	drive output
REG	2	voltage regulator decoupling
DOC	3	dial output connection
LSI	4	line signal input
LN	5	positive line terminal
SCR	6	sending current resistor
V_{REF}	7	voltage reference decoupling
OREC	8	output for receive preamplifier; to be left open-circuit in application
OMIC	9	output for microphone preamplifier; to be left open-circuit in application
V_P	10	supply for electret microphones
MIC–	11	inverting microphone input
MIC+	12	non-inverting microphone input
V_{SS}	13	negative line terminal
QR+	14	non-inverting output for receiving amplifier
QR–	15	inverting output for receiving amplifier
TEST	16	test pin; to be connected to V_{SS} in application
DTMF	17	dual tone multi-freqency input
RMC	18	reset output for microcontroller
CLK	19	clock signal input
SCL	20	serial clock line; I²C-bus
SDA	21	serial data line; I²C-bus
VMC	22	input to sense supply voltage microcontroller
V_{DD}	23	positive supply decoupling
SLPE	24	slope (DC resistance) adjustment

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

SUPERSEDES DATA OF MAY 1990

PAGING DECODER

GENERAL DESCRIPTION

The PCA5000AT is a fully integrated decoder for the CCIR Radio Paging Code number 1 (POCSAG-code). It supports two basic modes of operation:

Alert-Only-Pager. This is a stand-alone mode in which the PCA5000AT scans inputs from three external switches that relate to the states ON, OFF and SILENT. Only a few external components are required to build an Alert-Only pager.

Display-Pager. In this mode, received calls and messages are transferred via the IC's serial communication interface to an external microcontroller. A built-in voltage converter can double the supply voltage output and perform level shifting on the interface signals.

Call-alert cadences are generated when valid calls and messages are received, and status cadences to indicate the present state of the decoder are generated following a status interrogation. An on-chip 5 x 9-bit static RAM with battery back-up is provided for programming two user-addresses and for special functions. Synchronization of the input data stream is achieved by the built-in ACCESS algorithm which allows data to be synchronized without preamble detection and minimizes battery power consumption by receiver-enable control. One of three error correction algorithms is applied to received code words to optimize the call success rate.

The PCA5000AT is fabricated in SACMOS-technology to ensure low power consumption at low supply voltages. Typical applications are alert-only pagers, numeric/alphanumeric display pagers, cellular radio and data/telemetry decoders.

Features

- Wide operating supply voltage range (1.7 to 6.0 V)
- Very low supply current (15 μA typ.)
- Decodes CCIR Radio Paging Code number 1
- Data rate: 512 bits/s
- Powerful 'ACCESS' synchronisation algorithm
- Supports two user addresses
- Four cadences per user address
- Silent call storage, up to four different calls
- Interfaces directly to the UAA2033 digital paging receiver
- Directly drives a 2 kHz bleeper
- High-level alert facility requires only a single external transistor
- Receiver-enable control for battery economy
- On-chip static RAM, non-volatile with battery back-up
- On-chip voltage converter
- Level-shifted microcontroller interface
- Battery-low alert
- Out-of-range indication (optional)

PACKAGE OUTLINE

28-lead mini-pack; plastic (SO28; SOT136A.)

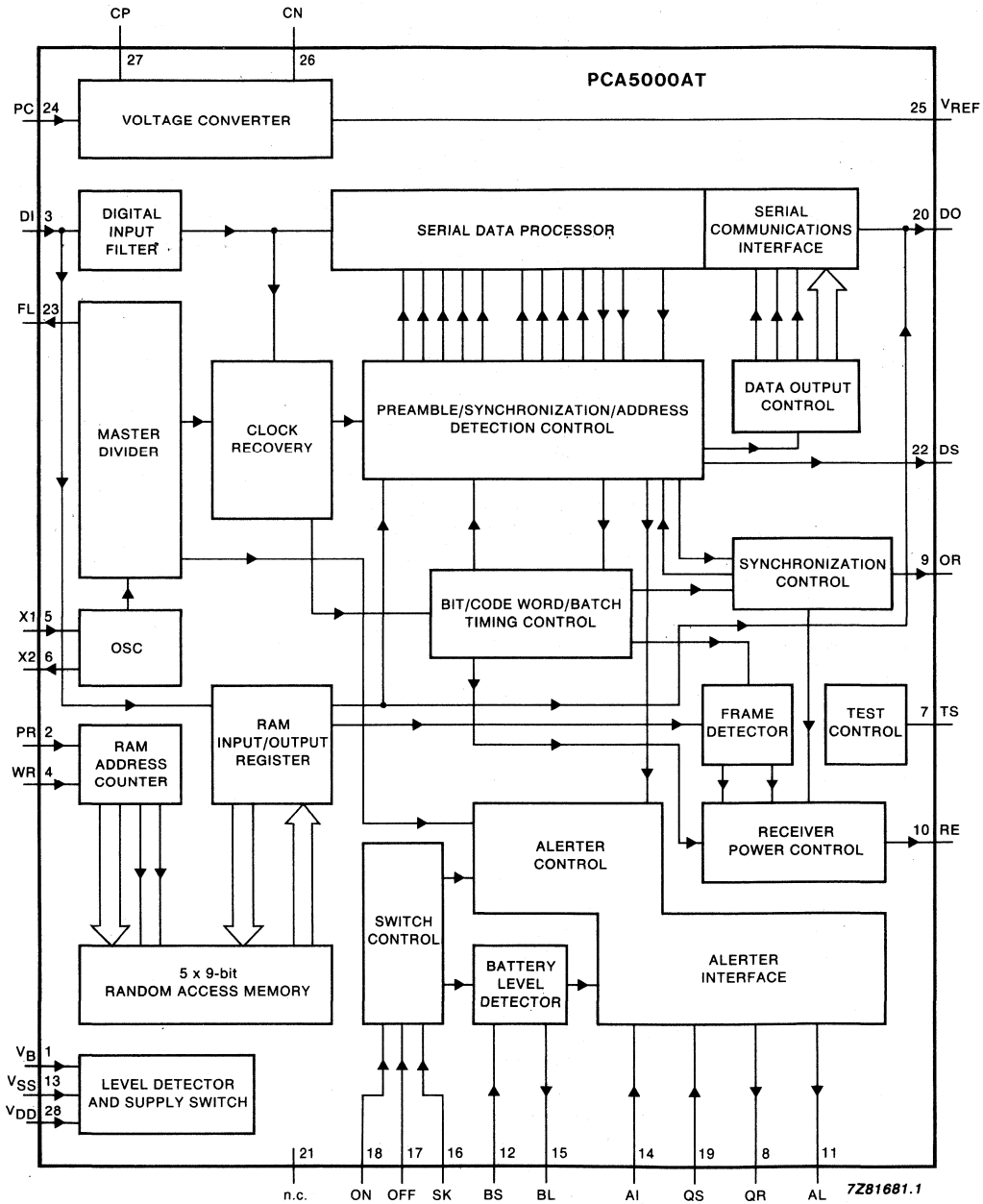


Fig. 1 Block diagram.

DEVELOPMENT DATA

PINNING

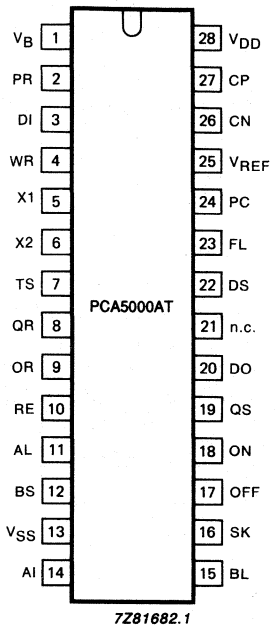


Fig. 2 Pinning diagram.

pin	mnemonic	description
1	V_B	RAM back-up negative supply voltage
2	PR	programming enable input
3	DI	serial data input
4	WR	programming WRITE input
5	X1	oscillator input
6	X2	oscillator output
7	TS	test mode enable input
8	QR	alert high-level output/vibrator output
9	OR	out-of-range output
10	RE	receiver enable output
11	AL	alert low-level output
12	BS	battery sense input
13	V_{SS}	negative supply voltage
14	AI	alarm input
15	BL	battery-low output
16	SK	silent key/mute input
17	OFF	off key/reset input
18	ON	on key/on-off input
19	QS	vibrator enable input
20	DO	received data output
21	n.c.	not connected
22	DS	received data strobe output
23	FL	frequency reference output
24	PC	power control input to voltage converter
25	V_{REF}	microcontroller interface negative reference voltage
26	CN	voltage converter external capacitor (negative)
27	CP	voltage converter external capacitor (positive)
28	V_{DD}	positive supply voltage (common)

FUNCTIONAL DESCRIPTION

Operating modes

The decoder has two basic operating modes; alert-only-pager and display-pager. There is also a programming mode in which the contents of the internal RAM are programmed or verified. The RAM holds two user-addresses and special function bits.

Alert-Only-Pager

No external microcontroller is required in this mode.

Tone-alert cadences are generated when valid calls are received. Four different alert cadences are available and are called by combinations of the function bits. The voltage doubler is disabled in this mode.

The decoder continually scans the inputs ON, OFF and SK from the external switches ON, OFF and SILENT that determine the internal operating status. Operating one of the switches first causes the cadence of the existing internal status to be generated and then, after 1.5 s switch operation, generation of a cadence to indicate the new internal status of the decoder.

Display-Pager

In this mode the decoder receives calls/messages and directs those addressed to one of the two stored user addresses to an external microcontroller for post-processing and display. Tone-alert cadences are generated when valid calls are received.

The decoder provides a doubled supply voltage output to the microcontroller and associated hardware, and the interface signals are level-shifted to allow direct coupling to the microcontroller.

The internal state of the decoder is determined by the logic levels on the static inputs ON and SK.

Internal states

If the decoder is in one of the two operating modes, its internal status is always one of the following:

OFF state. This is the power-saving inactive state in which no decoding takes place and the paging receiver is disabled. Scanning of the ON, OFF and SK inputs is maintained to allow state-changes to be effected.

ON state. This is the normal active state of the decoder. Received calls and messages are compared with the two user addresses stored in the RAM. When the validity of incoming calls is confirmed, appropriate cadences are generated and data is shifted out via the serial microcontroller interface.

SILENT state. This is the same as the ON state except that alert cadences are not generated following valid calls. Instead, if programmed as an alert-only pager, the decoder stores up to four different calls. The appropriate alert cadences are generated after the decoder has been returned to the ON-state. However, special silent override calls will cause generation of alert cadences.

DEVELOPMENT DATA

POCSAG code structure

A transmission using the CCIR Radio Paging Code No. 1 (POCSAG code) is structured according to the following rules (see Fig. 3)

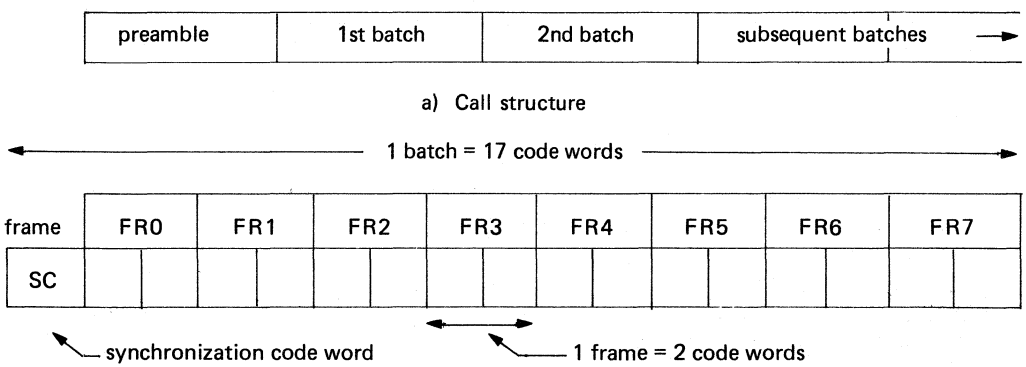
The transmission is started by sending a preamble which is a sequence of at least 576 continually alternating bits (01010101 . . .). The preamble precedes a number of batch blocks. The transmission is terminated after the last batch.

Every batch comprises a synchronisation code word with a fixed 32-bit pattern followed by eight frames (numbered 0 to 7). Only complete batches are transmitted.

A frame comprises two code words, each 32 bits long. A code word is either an address, message or an idle code word. Idle code words are transmitted to fill empty batches or to separate messages.

An address code word is coded as shown in Fig. 3; 18 bits of the 21-bit user address are coded in the code word and are protected against transmission errors by a CRC check word (bits 22 to 31). The other three bits of the user address are coded in the number of the frame in which the address code word is transmitted. Two function bits (bits 20 and 21) allow distinction between four different calls to one user address.

A message code word contains 20 bits of any information, these are also protected by a check word.



bit	1	2 to 19	20	21	22 to 31	32
	0	user address	FC	FC	parity check	

c) Address code word structure (FC are function code bits)

bit	1	2 to 21	22 to 31	32
	1	message	parity check	

d) Message code word structure

Fig. 3 POCSAG coding structure.

FUNCTIONAL DESCRIPTION (continued)

Decoding

The POCSAG-coded input data is first noise-filtered by a digital filter. A sampling clock, synchronous to the 512 bits/s data rate, is derived from the filtered data.

Synchronization is performed on the POCSAG code structure using the ACCESS algorithm, which is a five-stage state mechanism.

The decoder first searches the data stream for preamble or synchronization code word patterns. Before synchronism can be achieved, the decoder must ascertain that synchronization code words are correctly positioned at the beginning of each batch. When the correct structure is detected, the decoder switches to the 'receive mode'. (The receiver enable output (RE) is active before input data is required.) Error correction algorithms are applied to the data.
If synchronization is lost (i.e. no synchronization code word found at the beginning of the next batch) the decoder enters a two-step recovery mechanism. In the first step, over the next 15 batches, the decoder attempts to resynchronize by bit-wise shifting its frame window. A 'carrier off' state is entered in the second step, in this the data stream is tested convolutionally for a preamble or synchronization code word at every effective bit position within a continuous stream of at least 17 batches. When synchronization is regained, the decoder returns to the 'receive mode'.

In the 'receive mode', the input data stream is sampled at the frame position pointed to by the RAM program and the sampled code words are error-corrected. If they are address code words, they are compared with the two user addresses from the RAM. If the result of this comparison is 'true', the following actions take place:

- a store is set for a call-alert cadence. The cadence will relate to the combination of the function bits in the accepted code word but will not be generated until the call has been terminated;
- the receiver enable output (RE) is held active so that reception of the call can continue. This condition remains until
  - another address code word or an IDLE instruction is received
  - the error-correction algorithm fails to generate a code word
  - synchronisation is lost;
- message code words attached to the validated address code word are transferred via the serial communication interface to the external microcontroller.

Programming

The on-chip RAM is organized in five 9-bit words (Fig. 4). It is used to store two user addresses (receiver identification codes) and six programmed special function bits. A lithium back-up battery maintains data retention when the main power supply is removed.

	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
word 0	A08	A07	A06	A05	A04	A03	A02	A01	A00
word 1	A17	A16	A15	A14	A13	A12	A11	A10	A09
word 2	B08	B07	B06	B05	B04	B03	B02	B01	B00
word 3	B17	B16	B15	B14	B13	B12	B11	B10	B09
word 4	FR2	FR1	FR0	SP6	SP5	SP4	SP3	SP2	SP1

where:

AXX are 18 bits of user address 'A'
BXX are 18 bits of user address 'B'
FR2 to FR0 are frame number bits common to both addresses 'A' and 'B'
SP6 to SP1 are special function bits.

Fig. 4 RAM organization.

A user address in POCSAG code comprises 21 bits, three of which are coded in the frame number. In the PCA5000AT the frame number is common to both user addresses.

The special function bits are programmable to select from the following:

bit SP1: 0 alert-only-pager mode; silent override enabled on address 'B'
1 display-pager mode

SP2: 0 enable voltage converter (SP1 = 1)
1 disable voltage converter (SP1 = 1); cadence 1 also for FC = 11

SP3: 0 1-bit error-correction on message code words
1 4-bit burst error-correction on message code words on address 'B' (FC = 00 or 11)

SP4: free for user-application

SP5: 0 silent override enabled on address 'B' (FC = 01 or 10)
1 silent override enabled on address 'B' (FC = 00 or 11)

SP6: 0 silent override disabled on address 'A' (FC = 10)
1 silent override enabled on address 'A' (FC = 10)

The programming mode is entered by holding input PR at V_{DD} during power-on; exit from the programming mode is made by removing the main power supply. The back-up battery must remain connected to the PCA5000AT to keep the RAM contents when the main power supply is removed. During programming, inputs ON, OFF and SK must not all be '1' at the same time.

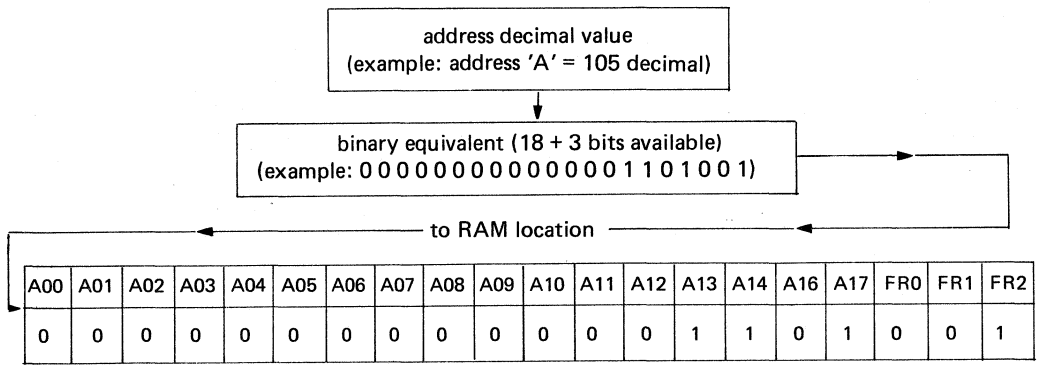
Programming of the RAM and verifying its contents is performed in a sequence starting with word 0, bit 0 and progressing through each of the five words in turn. Input and output is a serial operation; X1 is the shift clock input and DI, DO are respectively the data input and output.

During the RAM programming operation, a negative-going pulse first on WR and then on PR copies the 9 bits just shifted in into the RAM and switches to the next word (see Fig. 10).

During the RAM verify operation, reading the first word is triggered by a negative-going pulse on PR, which also switches to the next word in the sequence after 9 bits have been read (see Fig. 11).

Exit from the programming mode should be made after programming or verification of the RAM contents has been performed on all five words.

FUNCTIONAL DESCRIPTION (continued)



A00	A01	A02	A03	A04	A05	A06	A07	A08	A09	A10	A11	A12	A13	A14	A16	A17	FR0	FR1	FR2
0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	1

Fig. 5 Example of bit conversion in user address programming.

Generation of output signals

Alerter interface

The alerter interface provides for the acoustic signalling of calls received (Fig. 8) and of changes of pager status (Fig. 9).

When valid calls are received and the pager is in the ON state, the decoder generates 2 kHz squarewave output signals to produce tone alert cadences via a magnetic or piezoceramic 2 kHz bleeper. The cadence signals differ in modulation according to the two function bits FC in the address code word (Fig. 6b). The PCA5000AT supports two levels of alerter loudness: during the first four seconds, cadences are generated at low intensity (output AL active, output QR inactive); during the following twelve seconds, the intensity is increased (outputs AL and QR both active).

The alert tone generation is automatically terminated after sixteen seconds. Alert cadences are also terminated by an ON, OFF or SILENT input when in alert-only-pager mode, or by pulsing the status/reset input in display-pager mode.

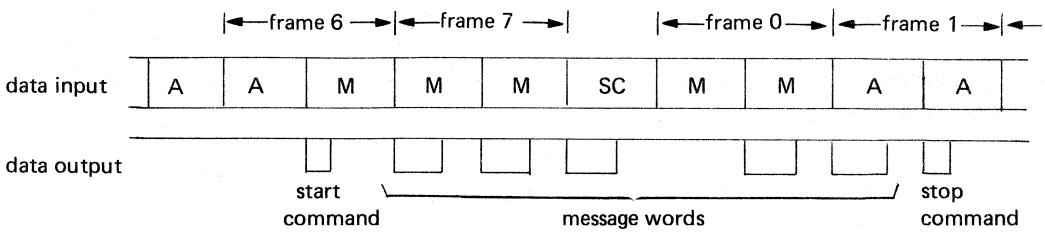
If the call is a message with subsequent message code words, alert cadence generation begins after the message has been terminated.

The alerter generates cadences to indicate the present internal status when interrogated and, when the main supply is low, gives a battery-low indicator output and generates an alarm tone.

Serial communication interface

This interface facilitates communication with an external microcontroller. Data is transmitted serially in the format shown in Fig. 6.

After receiving a valid address code word, transmission commences by sending a start command. The start command contains function data from the RAM, user address called (A or B) and function control bits FC from the address code word. The transmission continues with message words that contain the data from the received message code words. The end of a message transfer is marked by the sending of a stop command or another start command. In a stop command, bit 2 indicates that the call was successfully terminated.



a) Message format

bit

0	1	2	3	4	5	6	7
0	1	SP3	SP6	SP5	user address A or B	address bit 20 (FC)	address bit 21 (FC)

b) Start command format

bit

0	1	2	3	
1	1	1	1	message code word bits 2 to 21 as received

c) Message word format

bit

0	1	2	3	4	5	6	7
0	0	successful termination	$\overline{QS}$ input	SP4	SP2	not used	not used

d) Stop command format

Fig. 6 Serial communication interface.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
V_{DD} is referred to as 0 V (ground)

parameter	symbol	min.	max.	unit
Supply voltage	$V_{SS} = V_{13-28}$	+ 0.5	−7.0	V
RAM back-up supply voltage	V_B	V_{SS} + 0.8	−6.0	V
Input voltage on pins ON, OFF, SK, AI, PC, FL, BL, DS, DO	V_I	0.8	V_{REF}−0.8	V
Input voltage on any other pin	V_I	0.8	V_{SS}−0.8	V
Power dissipation per output	P_O	–	100	mW
Total power dissipation	P_{tot}	–	250	mW
Operating ambient temperature range	T_{amb}	−10	+ 60	°C
Storage temperature range	T_{stg}	−55	+ 125	°C

CHARACTERISTICS: Alert-Only-Pager (SP1 = 0)

V_{DD} = 0 V; V_{SS} = −2.7 V; V_{REF} = −2.7 V; V_B = −3.0 V; T_{amb} = 25 °C; quartz crystal f = 32.768 kHz, R_{Smax} = 40 kΩ, C1 (Fig. 12) = 8 to 40 pF

parameter	conditions	symbol	min.	typ.	max.	unit
Operating supply voltage range		V_{SS}	−1.7	−2.7	−6.0	V
Operating supply current	all outputs open; all inputs at V_{SS}; voltage converter off	I_{SS}	–	–	−22.0	μA
Level at which RAM switches to V_B		$V_{SS(sw)}$	−1.0	–	−1.7	V
Supply current; peak value	AL = LOW	I_{SSM}	–	–	−45.0	mA
Input voltage LOW						
PR, DI, BS, QS, WR, TS		V_{IL}	0.7 V_{SS}	–	–	V
AI, ON, OFF, SK, PC		V_{IL}	0.7 V_{REF}	–	–	V
Input voltage HIGH						
PR, DI, BS, QS, WR, TS		V_{IH}	–	–	0.3 V_{SS}	V
AI, ON, OFF, SK, PC		V_{IH}	–	–	0.3 V_{REF}	V

CHARACTERISTICS: Alert-Only-Pager (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Input current						
PR, TS, BS	$V_I = V_{DD}$	I_I	7.0	–	18.0	μA
WR	$V_I = V_{SS}$	I_I	–9.0	–	–28.0	μA
DI	$V_I = V_{DD}$; $V_{RE} = V_{SS}$	I_I	6	–	16	μA
PR, TS, BS, DI, QS, PC	$V_I = V_{SS}$	I_I	–	–	–0.1	μA
WR, QS, PC	$V_I = V_{DD}$	I_I	–	–	0.1	μA
AI, ON, OFF, SK,	$V_I = V_{DD}$	I_I	6.0	–	16.0	μA
AI, ON, OFF, SK	$V_I = V_{SS}$	I_I	–	–	–0.1	μA
Input capacitance						
BS, DI, PR, WR, QS, TS		C_I	–	–	5	pF
AI, ON, OFF, SK, PC		C_I	–	–	5	pF
X1		C_I	–	–	5	pF
Output current LOW						
RE, OR, QR	$V_{OL} = -1.35$ V	I_{OL}	10.0	–	–	μA
DO, DS, BL, FL	$V_{OL} = -1.35$ V	I_{OL}	10.0	–	–	μA
AL	$V_{OL} = -1.5$ V	I_{OL}	17.5	–	41.5	mA
Output current HIGH						
RE	$V_{OH} = -1.35$ V	$-I_{OH}$	10.0	–	–	μA
OR, QR	$V_{OH} = -1.35$ V	$-I_{OH}$	10.0	540	750	μA
DO, DS, BL, FL	$V_{OH} = -1.35$ V	$-I_{OH}$	10.0	–	–	μA
AL	AL = high impedance	$-I_{OH}$	–	–	0.2	μA
Output capacitance						
X2		C_O	19	–	23	pF

CHARACTERISTICS: Display-pager; alphanumeric mode (SP1 = 1, SP2 = 1)

CN and CP open circuit;
$V_{DD} = 0$ V; $V_{SS} = -3.0$ V; $V_{REF} = -6.0$ V; $T_{amb} = 25$ °C; quartz crystal f = 32.768 kHz,
$R_{Smax} = 40$ kΩ, C1 (Fig. 13) = 8 to 40 pF

parameter	conditions	symbol	min.	typ.	max.	unit
Operating supply voltage range		V_{SS}	–1.7	–	–3.0	V
Microcontroller interface negative reference		V_{REF}	V_{SS}	–	–6.0	V
Input current AI, ON, OFF, SK	$V_I = V_{REF}$ or V_{DD}	I_I	–	–	0.1	μA

DEVELOPMENT DATA

CHARACTERISTICS: Display-pager; numeric mode (SP1 = 1, SP2 = 0)

220 nF capacitor connected to CN, CP;
V_{DD} = 0 V; V_{SS} = −3.0 V; T_{amb} = 25 °C;
quartz crystal f = 32.768 kHz, R_{Smax} = 40 kΩ, C1 (Fig. 13) = 8 to 40 pF

parameter	conditions	symbol	min.	typ.	max.	unit
Operating supply voltage range		V_{SS}	−1.7	–	−3.0	V
Voltage converter V_{REF} output: output voltage	V_{SS} = −3.0 V; no load	V_{REF}	−5.95	–	−6.0	V
	V_{SS} = −2.0 V; I_{VREF} = 150 μA; PC = 0	V_{REF}	−2.7	–	–	V
	V_{SS} = −2.0 V; I_{VREF} = 45 μA; PC = 1	V_{REF}	−2.7	–	–	V
output current	V_{SS} = −2.0 V; PC = 0	I_{VREF}	−150	–	–	μA
	V_{SS} = −2.0 V; PC = 1	I_{VREF}	−45	–	–	μA
Input current AI, ON, OFF, SK	V_I = V_{REF} or V_{DD}	I_I	–	–	0.1	μA

TIMING: Display-pager (SP1 = 1)

V_{DD} = 0 V; V_{SS} = −2.7 V; T_{amb} = 25 °C;
quartz crystal f = 32.768 kHz, R_{Smax} = 40 kΩ, C1 (Fig. 13) = 8 to 40 pF

parameter	conditions	symbol	min.	typ.	max.	unit
Oscillator frequency		f_{osc}	–	32.768	–	kHz
Alerter frequency		f_{alert}	–	2048	–	Hz
Data input rate		f_{DI}	–	512	–	bits/s
Frequency reference FL output		f_{FL}	–	16.384	–	kHz
Data input transition time		t_{TDI}	–	–	100	μs
Preamble duration			1125	–	–	ms
Batch duration		t_{BAT}	–	1062.5	–	ms
Bit period		t_{BIT}	–	1.9531	–	ms
Data output rate		f_{DO}	–	512	–	bit/s
Data output transition time	C_L = 5 pF	t_{DTO}	–	–	100	ns
Data strobe clock period		t_{DS}	–	1.9531	–	ms
Data output set-up time		t_{DOS}	–	1.77	–	ms
Data strobe pulse width		t_{DSW}	61	122	–	μs
Data hold time		t_{DH}	30.5	61	–	μs
Call alert period		t_{ALT}	–	16	–	s
Call alert (low level) AL output only		t_{ALL}	–	4.0	–	s
Call alert (high level) QR and AL outputs		t_{ALH}	–	12.0	–	s

parameter	conditions	symbol	min.	typ.	max.	unit
Call alert cycle period		t_{ALC}	–	1.0	–	s
Call alert pulse period		t_{ALP}	–	125	–	ms
Status pulse set-up time		t_{STP}	10.0	330	–	μs
Status pulse duration		t_{STD}	10.0	330	–	μs
Status alert period		t_{STON}	–	62.5	–	ms
Status alert delay		t_{STOF}	–	62.5	–	ms
Receiver control RE transition time	C_L = 5 pF	t_{RXT}	–	–	100	ns
RE establishment time		t_{RXON}	–	31.2	–	ms
Programming: data clock period		t_{PDC}	–	100	–	μs
data settling time		t_{PDS}	20.0	–	–	μs
write set-up time		t_{WSU}	20.0	–	–	μs
write pulse width		t_{WP}	10.0	–	–	μs
program input pulse width		t_{PR}	10.0	–	–	μs
program input settling time		t_{PRS}	20	–	–	μs
Power-on reset pulse width		t_{POR}	7.5	–	–	μs
Program start delay time		t_{CSU}	20.0	–	–	μs
Program data hold time		t_{PDE}	10.0	–	–	μs
Data clock period LOW		t_{X1}	10.0	50.0	–	μs

DEVELOPMENT DATA

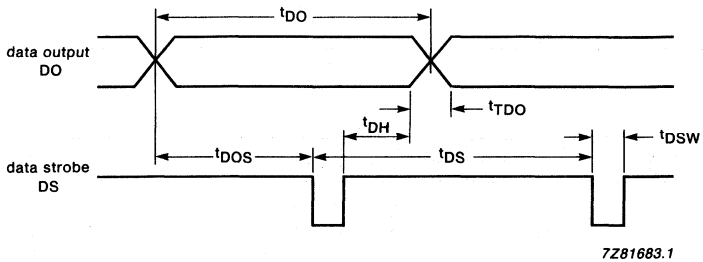


Fig. 7 Serial communications interface timing.

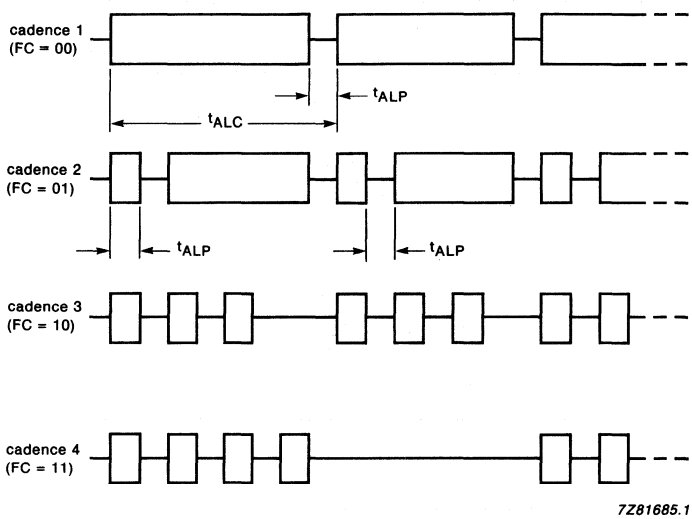


Fig. 8 Call alert cadences; FC refers to function control bits 20 and 21 in the address code word.

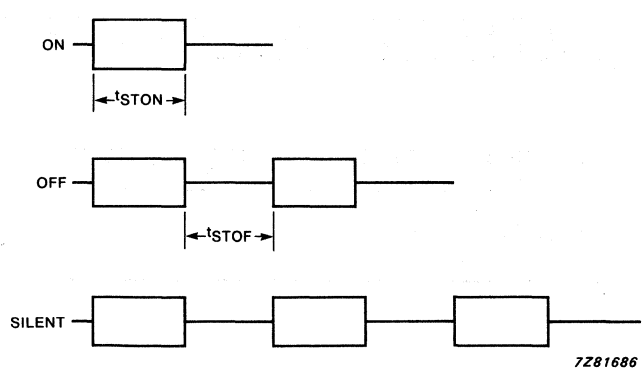


Fig. 9 Status indication cadences.

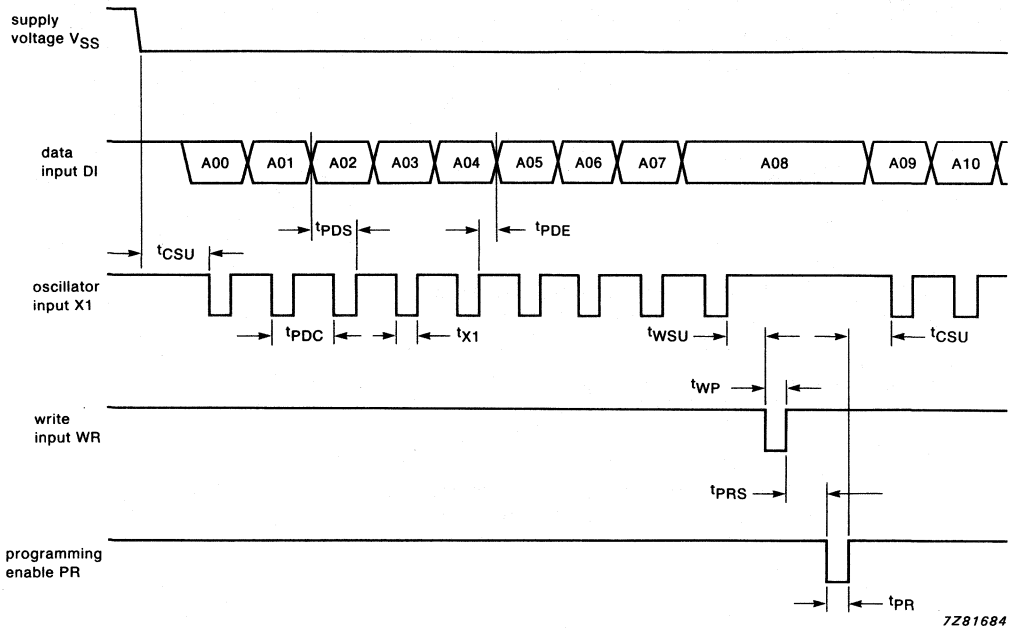


Fig. 10 Timing of RAM programming operation.

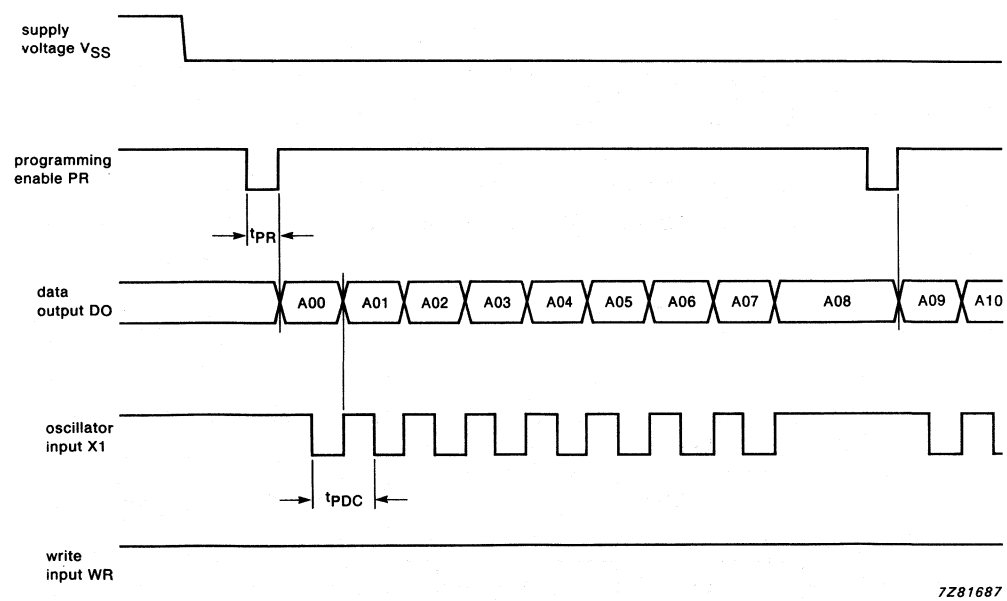


Fig. 11 Timing of RAM verify operation.

DEVELOPMENT DATA

APPLICATION INFORMATION

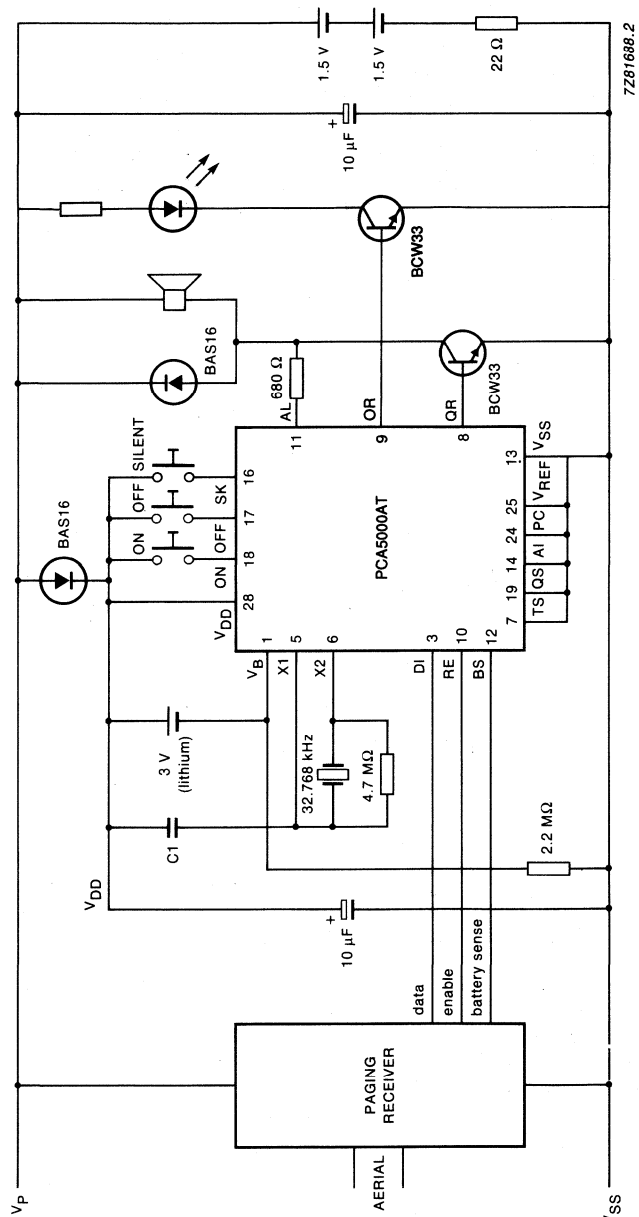


Fig. 12 Example of alert-only pager.

DEVELOPMENT DATA

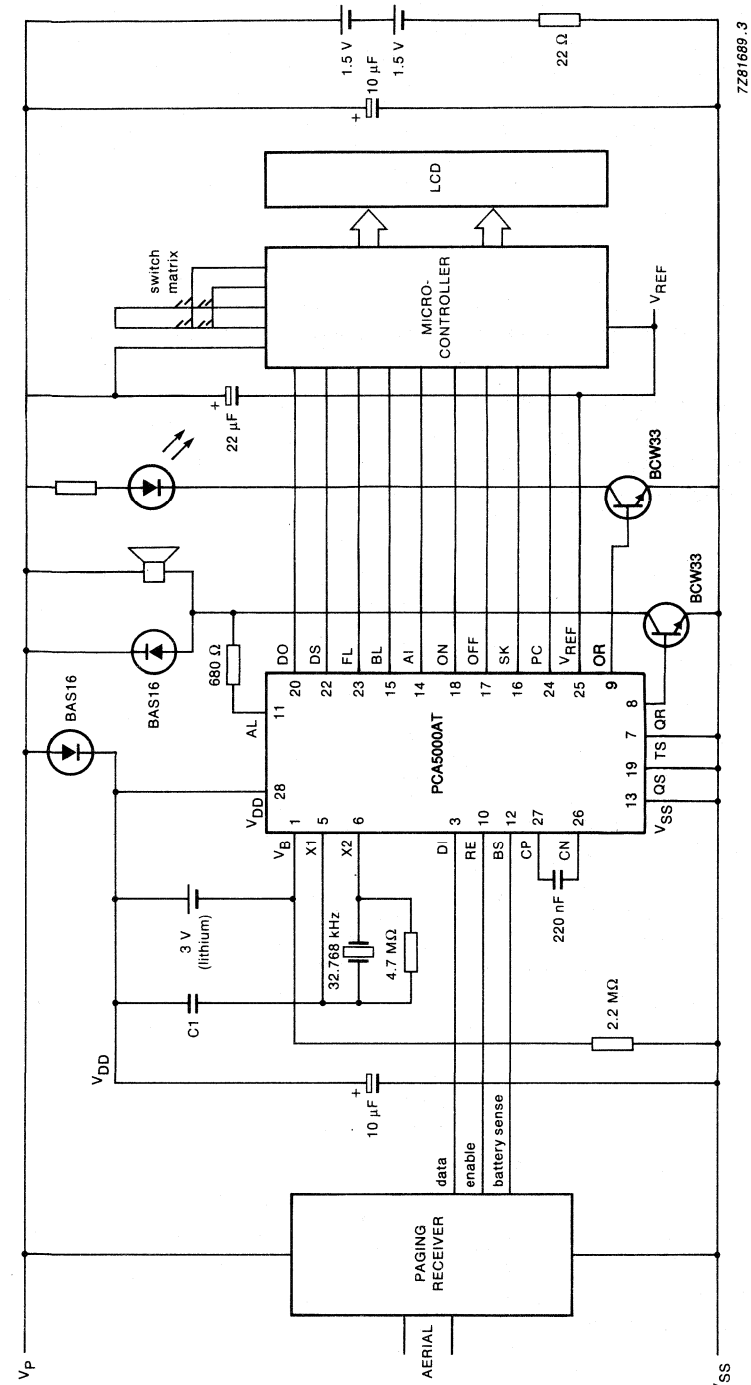


Fig. 13 Example of display-pager in alphanumeric mode with voltage converter enabled.

Application notes

Input pins

The programming control inputs have internal biasing resistors of sufficiently low impedance to provide safe operation even if the pins are left open circuit.

Pin 1 (V_B): RAM back-up battery negative supply. Connect this pin to the negative terminal of a lithium battery and connect the positive battery terminal to V_{DD}. This battery supply ensures data retention when the main supply voltage is removed.

Pin 2 (PR): programming enable, normally LOW. To enter the programming mode, pull this input HIGH when connecting the main supply voltage.

Pin 3 (DI): serial data input. During normal operation, POCSAG-coded data is received via this pin. When in programming mode, data to be stored in the internal RAM is read from this input whenever a pulse on X1 occurs.

Pin 4 (WR): programming write input, normally HIGH. A positive edge on this pin copies the preceding word shifted into the internal RAM. Keep this pin HIGH during RAM-read operations.

Pin 5 (X1): oscillator input. Connect a 32 kHz crystal to this pin during normal operation. When in programming write mode, a positive edge on X1 shifts the data present on DI to the internal register. When in programming read mode, a positive edge on X1 moves the next bit from the internal register to DO.

Pin 6 (X2): oscillator output. Return connection to the 32 kHz crystal.

Pin 7 (TS): test mode enable input, **always** LOW.

Pin 12 (BS): battery sense input. The decoder samples this input when it is in the ON state and the receiver is enabled. Every single sample is copied to the BL output. A continuous high-level alert tone is generated if four sequential samples are HIGH.

Pin 13 (V_{SS}): main negative supply voltage. Remove the voltage from this pin to leave the programming mode. The RC combination of 22 Ω and 10 μF (Figs 12 and 13) should remain connected; disconnect the battery only.

Pin 14 (AI): alarm input, normally LOW. A HIGH on this input causes a continuous high-level alert tone to be generated. The input may be pulsed to modulate the output tone.

Pin 16 (SK): silent key/mute input.
Alert-Only-Pager: push-button switch input, pushing the switch selects SILENT state.
Display-Pager: static input, when HIGH no calls are stored and no alert tones are generated for calls received.

Pin 17 (OFF): off key/reset input.
Alert-Only-Pager: push-button switch input, pushing the switch selects OFF state.
Display-Pager: static input, normally LOW. A positive-going pulse on this input causes (a) status indication cadences to be generated if the decoder is not alerting or (b) resetting an alert call or a battery-low alert if active.

Pin 18 (ON): on key/on-off input.
Alert-Only-Pager: push-button switch input. Pushing the switch selects ON state.
Display-pager: static input. LOW level selects OFF state, HIGH level selects ON state.

Pin 19 (QS): vibrator enable input, normally LOW. A HIGH level enables the vibrator output logic and switches QR to vibrator output.

Pin 24 (PC): voltage converter power control. The level on this pin determines the output impedance of the voltage converter. LOW selects low impedance, HIGH selects high impedance.

Pin 26 (CN): voltage converter external capacitor, negative connection.

Input pins (continued)

Pin 27 (CP): voltage converter external capacitor, positive connection.

Pin 28 (V_{DD}): main positive supply input. This pin is common to all supply voltages and is referred to as GROUND.

Output pins

Pin 8 (QR): alert high-level output/vibrator output. This output can directly drive an external bipolar transistor to control a vibrator-type alerter if QS is set HIGH, or supports high-level alerting in conjunction with AL.

Pin 9 (OR): out-of-range output, active HIGH. If the decoder detects 'carrier-off', an output is generated for the duration of the synchronization scan period. Connecting OR to QR provides alert tone generation during 'carrier-off'.

Pin 10 (RE): receiver enable output, active HIGH. Connect the radio paging receiver power control input to this pin to minimize power consumption. Whenever no input data is required, the PCA5000AT will disable the paging receiver to conserve power.

Pin 11 (AL): alert low-level output, active LOW. The low-level alert tone is generated via this output; the alert becomes high-level in conjunction with QR.

Pin 15 (BL): battery-low output, active HIGH. Every time the PCA5000AT samples the BS input, data sensed is output on this pin.

Pin 20 (DO): received data output. During normal operation, accepted calls and possibly subsequent message code words are output via this pin at a rate of 512 bits/s. When in programming read mode, data read from the internal RAM is presented bit-by-bit on this pin.

Pin 22 (DS): received data strobe output, active LOW. In normal operation, every time this output goes LOW, the next bit on the DO output is valid.

Pin 23 (FL): frequency reference output. If the decoder is programmed as a Display-Pager, a 16 kHz squarewave reference is output from this pin.

Pin 25 (V_{REF}): microcontroller interface negative reference voltage. The LOW level of pins FL, BL, DO, DS, AI, ON, OFF, SK and PC is related to the voltage on V_{REF}.

Alert-Only-Pager: Connect V_{REF} output to V_{SS}.

Display-Pager: The doubled negative supply voltage generated by the internal voltage converter is output from V_{REF}. The V_{REF} pin may also be driven from an external supply if the capacitor across CN/CP is removed and CN/CP are left open circuit.

Single-chip 8-bit microcontroller 83C552-5; 80C552-5

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATA SHEET

1. FEATURES

- 80C51 central processing unit
- 8 K x 8 ROM, expandable externally to 64 kbytes
- 256 x 8 RAM, expandable externally to 64 kbytes
- Two standard 16-bit timer/counters
- An additional 16-bit timer/counter coupled to four capture registers and three compare registers
- A 10-bit ADC with 8 multiplexed analog inputs
- Two 8-bit resolution, Pulse Width Modulated outputs
- Five 8-bit I/O ports plus one 8-bit input port shared with analog inputs
- I²C-bus serial I/O port with byte orientated master and slave functions
- Full-duplex UART compatible with the standard 80C51
- On-chip watchdog timer
- Three frequency ranges: 1.2 to 16 MHz; 1.2 to 24 MHz; 1.2 to 30 MHz
- Three operating ambient temperature ranges:

  PCB83C552-5: 0 to +70 °C (XTAL frequency max. 30 MHz)

  PCF83C552-5: –40 to +85 °C (XTAL frequency max. 24 MHz)

  PCA83C552-5: –40 to +125 °C (XTAL frequency max. 16 MHz)

2. GENERAL DESCRIPTION

The 80C552-5/83C552-5 (hereafter generally referred to as 8XC552) single-chip 8-bit microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family. The 8XC552 has the same instruction set as the 80C51. Two versions of the derivative exist:

- 83C552-5: 8 kbytes mask-programmable ROM
- 80C552-5: ROMless version of the 83C552-5.

This I/O intensive device provides architectural enhancements to function as a controller in the field of automotive electronics, specifically engine management and gear box control.

The 8XC552 contains a non-volatile 8 K x 8 read-only program memory, a volatile 256 x 8 read/write data memory, six 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), an additional 16-bit timer coupled to capture and compare latches, a fifteen-source, two-priority-level, nested interrupt structure, an 8-input ADC, a dual DAC with pulse width modulated outputs, two serial interfaces (UART and I²C-bus), a 'watchdog' timer and on-chip oscillator and timing circuits. For systems that require extra capability, the 8XC552 can be expanded using standard TTL compatible memories and logic.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte and 17 three-byte. With a 16 MHz (24 MHz; 30 MHz) crystal, 58% of the instructions are executed in 0.75 µs(0.5µs; 0.4µs) and 40% in 1.5 µs (1 µs; 0.8 µs). Multiply and divide instructions require 3 µs (2 µs; 1.6 µs).

3. ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			FREQUENCY RANGE (MHz)	TEMPERATURE RANGE (°C)
	PINS	PIN POSITION	CODE		
ROMless					
PCA80C552-5-16WP	68	PLCC	SOT188CG	1.2 to 16	–40 to +125
PCB80C552-5-16WP	68	PLCC	SOT188CG	1.2 to 16	0 to +70
PCF80C552-5-16WP	68	PLCC	SOT188CG	1.2 to 16	–40 to +85
PCA80C552-5-16H	80	QFP	SOT318	1.2 to 16	–40 to +125
PCB80C552-5-16H	80	QFP	SOT318	1.2 to 16	0 to +70
PCF80C552-5-16H	80	QFP	SOT318	1.2 to 16	–40 to +85
PCB80C552-5-24WP	68	PLCC	SOT188CG	1.2 to 24	0 to +70
PCF80C552-5-24WP	68	PLCC	SOT188CG	1.2 to 24	–40 to +85
PCB80C552-5-24H	80	QFP	SOT318	1.2 to 24	0 to +70
PCF80C552-5-24H	80	QFP	SOT318	1.2 to 24	–40 to +85
PCB80C552-5-30WP	68	PLCC	SOT188CG	1.2 to 30	0 to +70
PCB80C552-5-30H	80	QFP	SOT318	1.2 to 30	0 to +70
ROM coded					
PCA83C552-5WP/XXX	68	PLCC	SOT188CG	1.2 to 16	–40 to +125
PCB83C552-5WP/XXX	68	PLCC	SOT188CG	1.2 to 16	0 to +70
PCF83C552-5WP/XXX	68	PLCC	SOT188CG	1.2 to 16	–40 to +85
PCA83C552-5H/XXX	80	QFP	SOT318	1.2 to 16	–40 to +125
PCB83C552-5H/XXX	80	QFP	SOT318	1.2 to 16	0 to +70
PCF83C552-5H/XXX	80	QFP	SOT318	1.2 to 16	–40 to +85
PCB83C552-5WP/XXX	68	PLCC	SOT188CG	1.2 to 24	0 to +70
PCF83C552-5WP/XXX	68	PLCC	SOT188CG	1.2 to 24	–40 to +85
PCB83C552-5H/XXX	80	QFP	SOT318	1.2 to 24	0 to +70
PCF83C552-5H/XXX	80	QFP	SOT318	1.2 to 24	–40 to +85
PCB83C552-5WP/XXX	68	PLCC	SOT188CG	1.2 to 30	0 to +70
PCB83C552-5H/XXX	80	QFP	SOT318	1.2 to 30	0 to +70

Note

1. XXX = ROM code number; to be defined.

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	October 1990

PCD3310 family

Pulse and DTMF dialler with redial

This Data sheet has been changed, see footnote !

FEATURES

- Pulse and DTMF dialling
- 23-digit capacity for redial operation (cursor method)
- Memory clear and electronic notepad
- Mixed-mode dialling: start with PD and end with DTMF dialling
- Dual redial buffers for PABX and public calls
- Four extra function keys; program, flash, redial, PD to DTMF (mixed dialling)
- DTMF timing:
  manual dialling - minimum duration for bursts and pauses
  re-dialling - calibrated timing
- On-chip voltage reference for supply and temperature independent tone output
- On-chip filtering for low output distortion (CEPT CS 203 compatible)
- On-chip oscillator uses low-cost 3.58 MHz (tv colour burst) crystal or piezo resonator
- Uses standard single-contact or double-contact (common left open) keyboard
- Keyboard entries fully debounced
- Flash (register recall) output

GENERAL DESCRIPTION

The PCD3310 family are single-chip silicon gate CMOS integrated circuits with on-chip oscillators suitable for use with 3.58 MHz crystals. They are dual-standard dialling circuits for either pulse dialling (PD) or dual tone multi-frequency (DTMF) dialling.

Input data is derived from any standard matrix keyboard for dialling in either DP or DTMF mode. Numbers of up to 23 digits can be retained in RAM for redial and notepad facilities.

In DTMF mode bursts as well as pauses are timed to a minimum, in manual dialling the maximum depends on the key depression time. For data communication mix mode dialling is also possible.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	operating supply voltage		2.5	-	6.0	V
V_{DDO}	standby supply voltage		1.8	-	6.0	V
I_{DDO}	low standby current (on hook)	V_{DDO} = 1.8 V	-	-	2	µA
	operating currents	V_{DD} = 3.0 V				
I_{DDC}	conversation mode		-	-	150	µA
I_{DDP}	pulse dialling mode		-	-	200	µA
I_{DDF}	DTMF dialling mode		-	-	0.9	µA
	DTMF output voltage level		-	192	-	mV
$V_{HG(rms)}$	HIGH group		-	150	-	mV
$V_{LG(rms)}$	LOW group					
ΔV_G	pre-emphasis of group		-	2.1	-	dB
THD	total harmonic distortion		-	–25	-	dB
Tamb	operating ambient temperature range		–25	-	+ 70	°C

Note:

the PCD3310C, PCD3310E, PCD3310F and PCD3310H are not to be used for new design-ins.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCD3310XP*	20	DIL	plastic	SOT146
PCD3310XT*	28	SO28	plastic	SO28; SOT136A

* When ordering 'X' is replaced by one of the letters A, C, E, F, G, H or nothing.

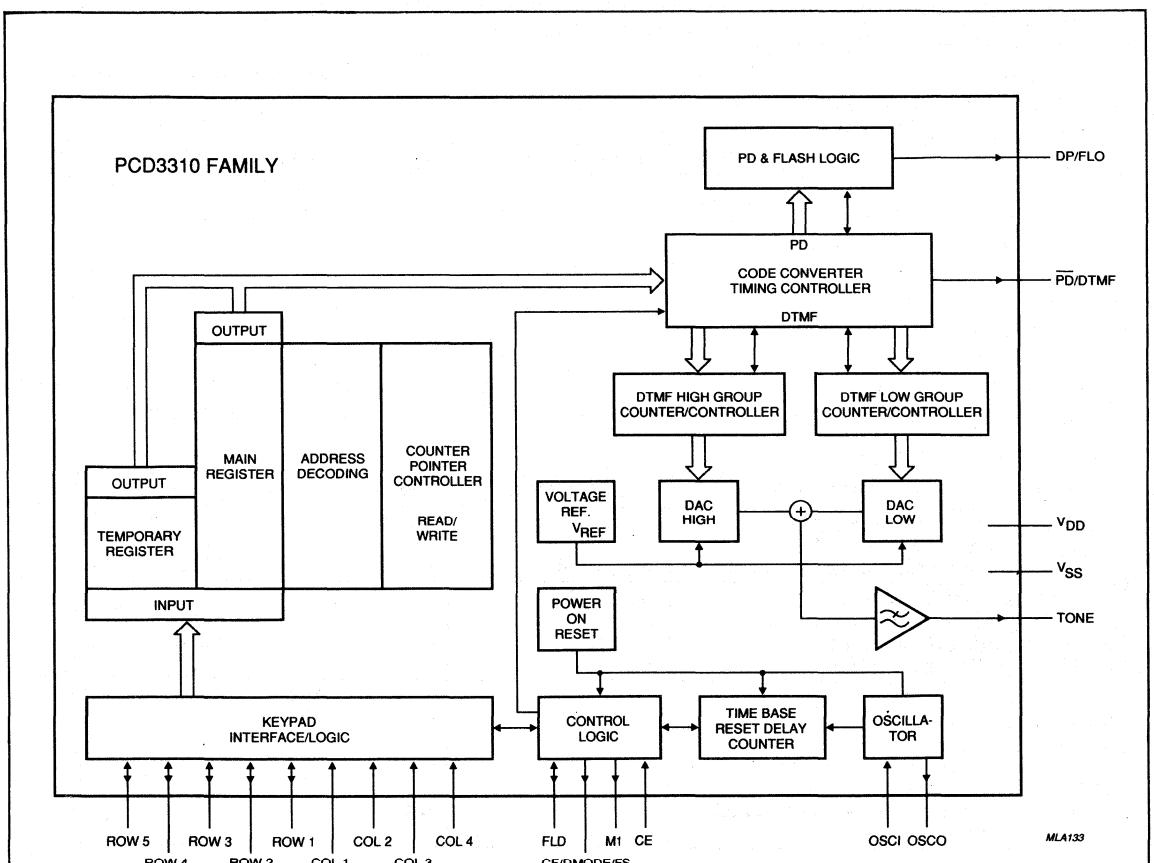


Fig.1 Block diagram.

Table 1 The PCD3310 family of ICs.

PCD3310	P/T dialler with redial, notepad, 4 x 5 keypad, flash, mark/space ratio 2:1, PABX register, automatic access pause control access to the cursor method.
PCD3310A	item PCD3310 with 3:2 mark/space ratio
PCD3310C	item PCD3310 with dialling mode output
PCD3310E	item PCD3310 with also 20 Hz pulse dialling
PCD3310F	item PCD3310 with DTMF timing of 60/90 ms
PCD3310G	item PCD3310 during switch over to data mode the '*' and '#' keys do not send out their corresponding tones
PCD3310H	item PCD3310 M1 replaced by M2

PCD3310 FAMILY SURVEY

FUNCTION	PCD3310	PCD3310A	PCD3310C	PCD3310E	PCD3310F	PCD3310G	PCD3310H
Redial key	R	R	R	R	R	R	R
Notepad keys; note 1	P/R	P/R	P/R	P/R	P/R	P/R	P/R
Mixed mode entry PD-DTMF + tone PD-DTMF no tone	 * # A-D >	 * # A-D >	 * # A-D >	 * # A-D >	 * # A-D >	 A-D > * #	 * # A-D >
Keypad (4x5, A-D)	3 x 5	3 x 5	3 x 5	3 x 5	3 x 5	3 x 5	3 x 5
Pulse dial; break/make 10 Hz, t_{id} = 840 ms 20 Hz, t_{id} = 504 ms	67, 33	60, 40	67, 33	67, 33 34, 17	67, 33	67, 33	67, 33
DTMF dial: tone/pause (ms) mute hold-over	 70, 70 80	 70, 70 80	 70, 70 80	 70, 70 80	 60, 90 100	 70, 70 80	 70, 70 80
Flash (ms)	100+	100+	100+	100+	100+	100+	100+
Pin 15 (SOT146) Pin 20 (SO28; SOT136A)	CF CF	CF CF	DMODE DMODE	FS FS	CF CF	CF CF	CF CF
Memory main, data Memory PABX	23 5	23 5	23 5	23 5	23 5	23 5	23 5
SOT146 package SO28/SOT136A package	20 28	20 28	20 28	20 28	20 28	20 28	20 -

Notes to the Family survey

1. P = program, R = dial.
2. PCD3310H only available in DIL package.

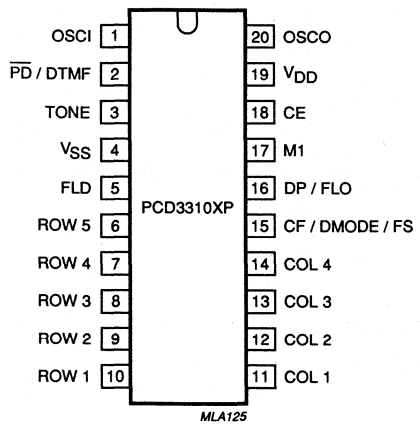


Fig.2 Pinning diagram; PCD3310XP.

PINNING

SYMBOL	PIN	DESCRIPTION
OSCI	1	oscillator input
$\overline{PD}$/DTMF	2	select pin; pulse or DTMF dialling
TONE	3	single or dual tone frequency output
V_{SS}	4	negative supply
FLD	5	flash duration control input/output
ROW 5	6	scanning row keyboard input/output
ROW 4	7	scanning row keyboard input/output
ROW 3	8	scanning row keyboard input/output
ROW 2	9	scanning row keyboard input/output
ROW 1	10	scanning row keyboard input/output
COL 1	11	sense column keyboard input
COL 2	12	sense column keyboard input
COL 3	13	sense column keyboard input
COL 4	14	sense column keyboard input
CF/DMODE/FS	15	confidence tone output, dialling mode output, frequency select
DP/FLO	16	dialling pulse and flash output
M1	17	muting output
CE	18	chip enable input
V_{DD}	19	positive supply
OSCO	20	oscillator output

Note: COL1 to COL4 have internal pull-ups.

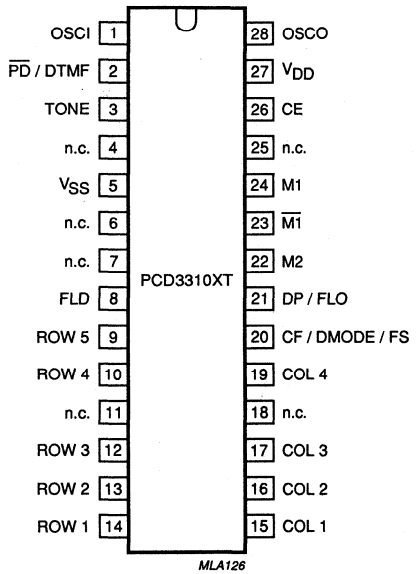


Fig.3 Pinning diagram for PCD3310XT.

PINNING

SYMBOL	PIN	DESCRIPTION
OSCI	1	oscillator input
$\overline{PD}$/DTMF	2	select pin; pulse or DTMF dialling
TONE	3	single or dual tone frequency output
n.c.	4	not connected
V_{SS}	5	negative supply
n.c.	6	not connected
n.c.	7	not connected
FLD	8	flash duration control input/output
ROW 5	9	scanning row keyboard input/output
ROW 4	10	scanning row keyboard input/output
n.c.	11	not connected
ROW 3	12	scanning row keyboard input/output
ROW 2	13	scanning row keyboard input/output
ROW 1	14	scanning row keyboard input/output
COL 1	15	sense column keyboard input
COL 2	16	sense column keyboard input
COL 3	17	sense column keyboard input
n.c.	18	not connected
COL 4	19	sense column keyboard input
CF/DMODE/FS	20	confidence tone output, dialling mode output, frequency select
DP/FLO	21	dialling pulse and flash output
M2	22	strobe; active HIGH during transmission
$\overline{M1}$	23	inverted mute output
M1	24	muting output
n.c.	25	not connected
CE	26	chip enable input
V_{DD}	27	positive supply
OSCO	28	oscillator output

Note: COL1 to COL4 have internal pull-ups.

FUNCTIONAL DESCRIPTION

Power supply (V_{DD}; V_{SS})

The positive supply of the circuit (V_{DD}) must meet the voltage requirements as indicated in the DC characteristics. To avoid undefined states of the device when powered-on, an internal reset circuit clears the control logic and counters. If V_{DD} drops below the minimum standby supply voltage of 1.8 V the power-on reset circuit inhibits re-dialling after hook-off. The power-on reset signal has the highest priority; it blocks and resets the complete circuit without delay regardless of the state of chip enable input (CE).

Clock oscillator (OSCI, OSCO)

The time base for the circuit for both PD and DTMF modes is a crystal controlled on-chip oscillator which is completed by connecting a 3.58 MHz crystal or ceramic resonator between the OSCI and OSCO pins.

Recommended resonator type:

- 3.58 MHz PXE - Murata; CSA 3.58MG310VA.

Chip Enable (CE)

The CE input enables the circuit and is used to initialize the device.

CE = LOW provides the static standby condition. In this state the clock oscillator is disabled, all registers and logic are reset with the exception of the Write Address Counter (WAC) and Temporary WriteAddress Counter (TWAC) which point to the last entered digit (see Fig.6). The keyboard input is inhibited, but data previously entered is saved in the redial register as long as V_{DD} is higher than $V_{DDO\ (min)}$. The current drawn is I_{DDO} (standby current) and serves to retain data in the redial register during hook-on.

CE = HIGH activates the clock oscillator and the circuit changes from static standby condition to the conversation mode. The current consumption is I_{DDC} until the first digit is entered from the keyboard. Then a dialling or re-dialling operation starts. The operating current is I_{DDP} if in the pulse dialling mode, or I_{DDF} if the DTMF dialling mode is selected.

If the CE input is taken to a LOW level for longer than time period t_{rd} (see Fig.10a, Fig.10b and timing data) an internal reset pulse will be generated at the end of the t_{rd} period. The system changes to the static standby state. Short CE pulses of $< t_{rd}$ will not affect the operation of the circuit and reset pulses are not produced.

Mode selection ($\overline{PD}$/DTMF)

PD mode

If $\overline{PD}$/DTMF = V_{SS} the pulse mode is selected. Entries of non-numeric keys are neglected, they are neither stored in the redial register nor transmitted.

DTMF mode

If $\overline{PD}$/DTMF = V_{DD} the dual tone multi-frequency dialling mode is selected. Each non-function key activated corresponds to a combination of two tones, each one out of four possible LOW and HIGH group frequencies. The frequencies are transmitted with a constant amplitude, regardless of power supply variations. Harmonic content is filtered out thus meeting the CEPT CS 203 recommendations.

The transmission time is calibrated for redial. In manual operation the duration of bursts and pauses is the actual key depression time, but not less than the minimum transmission time (t_t) or minimum pause time (t_p).

Mixed mode

When the $\overline{PD}$/DTMF pin is open-circuit the mixed mode is selected. After activation of CE or FL (Flash) the circuit starts as a pulse dialler and remains in this state until a non-numeric key (A, B, C, D, *, # or >) is activated. The circuit then changes to DTMF dialling for data communication and remains in this state until FL is activated or after a static standby condition when CE is re-activated.

A connection between the $\overline{PD}$/DTMF pin and V_{DD} also initiates DTMF dialling. Chip enable, FL or a connection of $\overline{PD}$/DTMF pin to V_{SS} sets the circuit back to pulse dialling.

Keyboard inputs/outputs

The sense column inputs COL 1 to COL 4 and the scanning row outputs ROW 1 to ROW 5 of the circuit are connected to the keyboard as shown in Fig.4. All keyboard entries are debounced on both the leading and trailing edges for approximately time period t_e as shown in Fig.11. Each entry is tested for validity. When a key is depressed, keyboard scanning starts and only returns to the sense mode after release of that key.

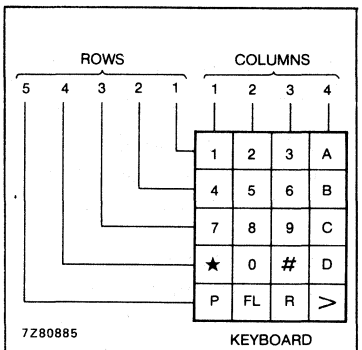


Fig.4 Keyboard organization.

Row 5 of the keyboard contains the following special function keys:

- P memory clear and programming (notepad)
- FL flash or register recall
- R redial
- > change of dial mode from PD to DTMF in mixed dialling mode

In pulse dialling mode the valid keys are the 10 numeric keys (0 to 9). The non-numeric keys (A, B, C, D, *, #) have no effect on the dialling or the redial storage. Valid function keys are P, R and FL.

In DTMF mode all non-function keys are valid. They are transmitted as a dual tone combination and at the same time stored in the redial register. Valid function keys are P, L and R.

In mixed mode all key entries are valid and executed accordingly.

Flash duration control (FLD)

Flash (or register recall) is activated by the FL key and can be used in DTMF and pulse dialling modes. Pressing the FL key will produce a timed line-break of 100 ms (min.) at the DP/FLO output. During the conversation mode this flash pulse entry will act as a chip enable. The flash pulse duration (t_{FL}) is calibrated and can be prolonged with an external resistor and capacitor connected to the FLD input/output (see Fig.5). The flash pulse resets the Read Address Counter (RAC). Later redial is possible (see redial procedure with the "Flash" inserted telephone number). The counter of the reset delay time is held during the period of t_{FL}.

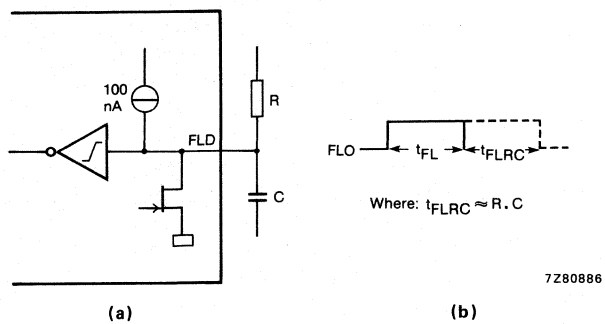


Fig.5 Flash pulse duration setting.

TONE output (DTMF mode)

The single and dual tones which are provided at the TONE output are filtered by an on-chip switched-capacitor filter, followed by an on-chip active RC low-pass filter. Hence, the total harmonic distortion of the DTMF tones meets the CEPT CS 203 recommendations. The tone output has following states:

- tone OFF; 3-state
- tone ON; the associated frequencies are superimposed on a DC level of 1/2 V_{DD}.

When the DTMF mode is selected output tones are timed in manual dialling with a minimum duration of bursts and pauses, and in redial with a calibrated timing. Single tones may be generated for test purposes (CE = HIGH). Each row and column has one corresponding frequency. High group frequencies are generated by connecting the column to V_{SS} and Low group frequencies are generated by forcing the row to V_{DD}. The single tone frequency will be transmitted during activation time, but it is neither calibrated nor stored.

An on-chip reference voltage provides output-tone levels independent of the supply voltage. Table 1 shows the frequency tolerance of the output tones for DTMF signalling.

Table 1 Frequency tolerance of the output tones for DTMF signalling; f_{XTAL} = 3.579545 MHz.

ROW/ COLUMN	STANDARD FREQUENCY (Hz)	TONE OUTPUT FREQUENCY (Hz)	FREQUENCY DEVIATION	
			%	Hz
Row 1	697	607.90	+ 0.13	+ 0.90
Row 2	770	770.46	+ 0.06	+ 0.46
Row 3	852	850.45	–0.18	–1.55
Row 4	941	943.23	+ 0.24	+ 2.23
Col 1	1209	1206.45	–0.21	–2.55
Col 2	1336	1341.66	+ 0.42	+ 5.66
Col 3	1477	1482.21	+ 0.35	+ 5.21
Col 4	1633	1638.24	+ 0.32	+ 5.25

Dial pulse and flash output (DP/FLO)

This is a combined output which provides control signals for timing in pulse dialling or for a calibrated break in both dialling modes (flash or register recall).

Mute output (M1)

During pulse dialling the mute output becomes active HIGH for the period of the inter-digit pause, break time and make time. It remains at this level until the last digit is pulsed out.

During DTMF dialling the mute output becomes active HIGH for the period of tone transmission and remains at this level until the end of hold-over time. It is also active HIGH during flash and flash hold-over time.

Mute output ($\overline{M1}$)

Inverted output of M1. In the PCD3310P it is only available as a bonding option of M1.

Strobe output (M2)

Active HIGH output during actual dialling; i.e. during break or make time in pulse dialling, or during tone ON/OFF in DTMF dialling. It is an open drain p-channel output.

DIALLING PROCEDURES
(see Figs.8 to 10)

Dialling

After CE has risen to V_{DD} the oscillator starts running and the Read Address Counter (RAC) is set to the first address (see Fig.6). By entering the first valid digit, the Temporary Write Address Counter (TWAC) will be set to the first address, the decoded digit will be stored in the register and the TWAC incremented to the next address. Any subsequent keyboard entry will be decoded and stored in the redial register after validation. The first 5 valid entries have no effect on the main register and its associated Write Address Counter. After the sixth valid digit is entered TWAC indicates an overflow condition. The data from the temporary register will be copied into the 5 least significant places of the main register and TWAC into the WAC. All following digits (including the sixth digit) will be stored in the main register (a total of not more than 23). If more than 23 digits are entered redial will be inhibited. If not more than 5 digits are entered only the temporary register and the associated TWAC are affected. Allentries are debounced on both the leading and trailing edges for at least time period t_e as shown in Fig.11. Each entry is tested for validity before being stored in the redial register.

- In DTMF mode all non-function keys are valid
- In PD mode only numeric keys are valid

Simultaneous to their acceptance and corresponding to the selected mode (PD, DTMF or mixed), the entries are transmitted as PD pulse-trains or as DTMF frequencies in accordance with postal requirements. Non-numeric entries are neglected during pulse dialling, they are neither stored nor transmitted.

Re-dialling

After CE has risen to V_{DD} the oscillator starts running and the Read Address Counter (RAC) is set to the first address to be sent. The circuit is in the conversation mode. If "R" is the first keyboard entry the circuit starts re-dialling the contents of the temporary register. If the overflow flag of the TWAC was set in the previous dialling, the re-dialling continues in the main register. If the flag was not set, the number residing in the temporary register will only be redialled until the temporary read and write registers are equal.

Before pressing "R" a dialling sequence with up to 4 digits is possible. If the digits are equal to the corresponding ones in the main register, then redial starts in the main register until the last digit stored is transmitted.

Timing in the DTMF mode is calibrated for both tone bursts and pauses.

In mixed mode only the first part entered (the pulse dialled part of the stored number) can be redialled.

During redial keyboard entries (function or non-function) are not accepted until the circuit returns to the conversation mode after completion of re-dialling. No redial activity takes place if one of the following events occur:

- Power-on reset
- Memory clear ("P" without successive data entry)
- Memory overflow (more than 23 valid data entries)

Notepad

The redial register can also be used as a notepad. In conversation mode a number with up to 23 digits can be entered and stored for re-dialling. By activating the program key (P) the WAC and TWAC pointers are reset. This acts like a memory clear (redial is inhibited). Afterwards, by entering and storing any digits, re-dialling will be possible after flash or hook on and off.

During notepad programming the numbers entered will neither be transmitted nor is the mute active, only the confidence tone is generated.

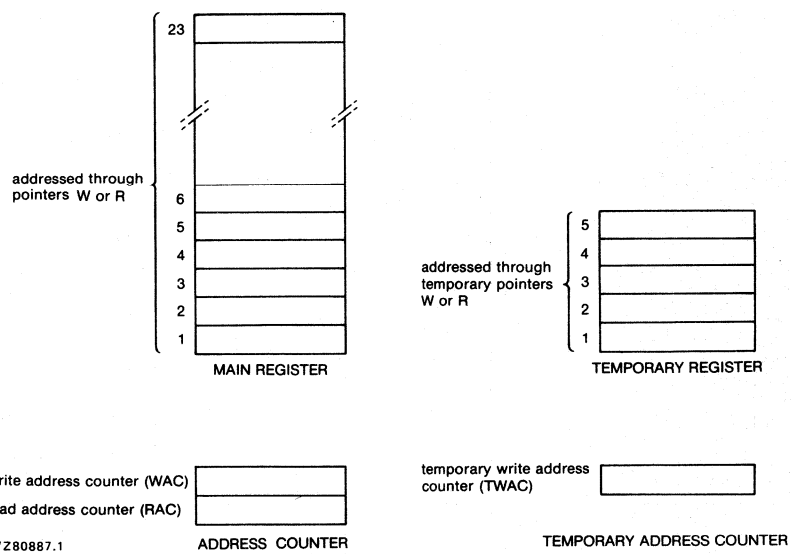


Fig.6 Program memory map.

Note to Fig.6

(1). If [access digit(s) + external number] ≤ 23 digits.

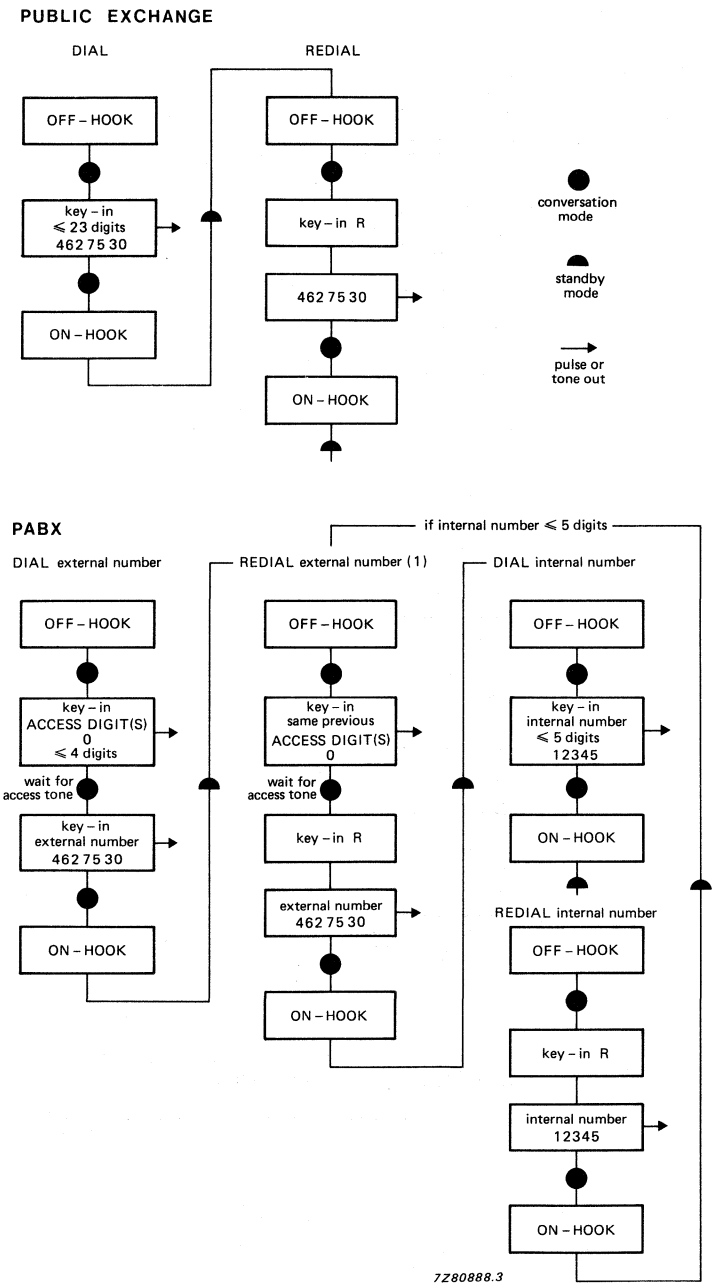


Fig.7 PD or DTMF dialling mode.

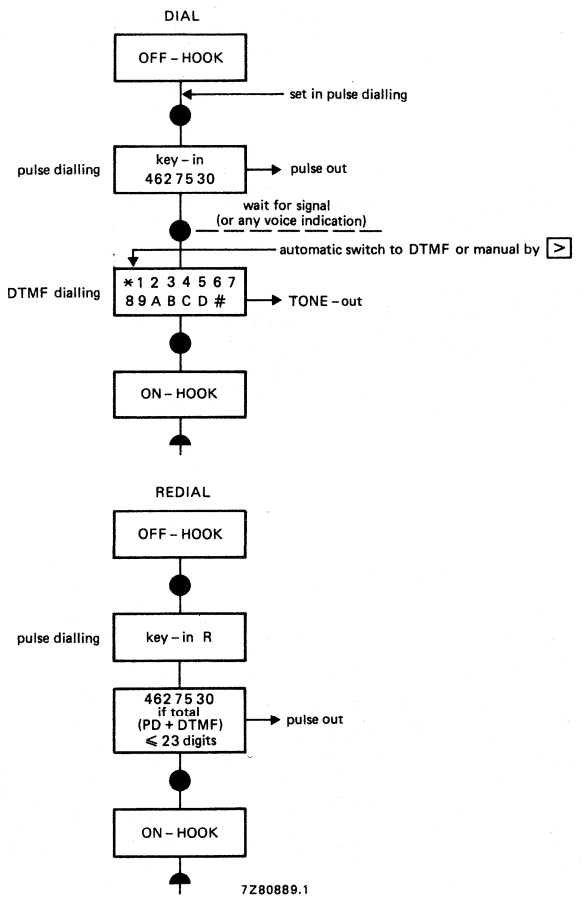


Fig.8 PD/DTMF mixed-mode dialling.

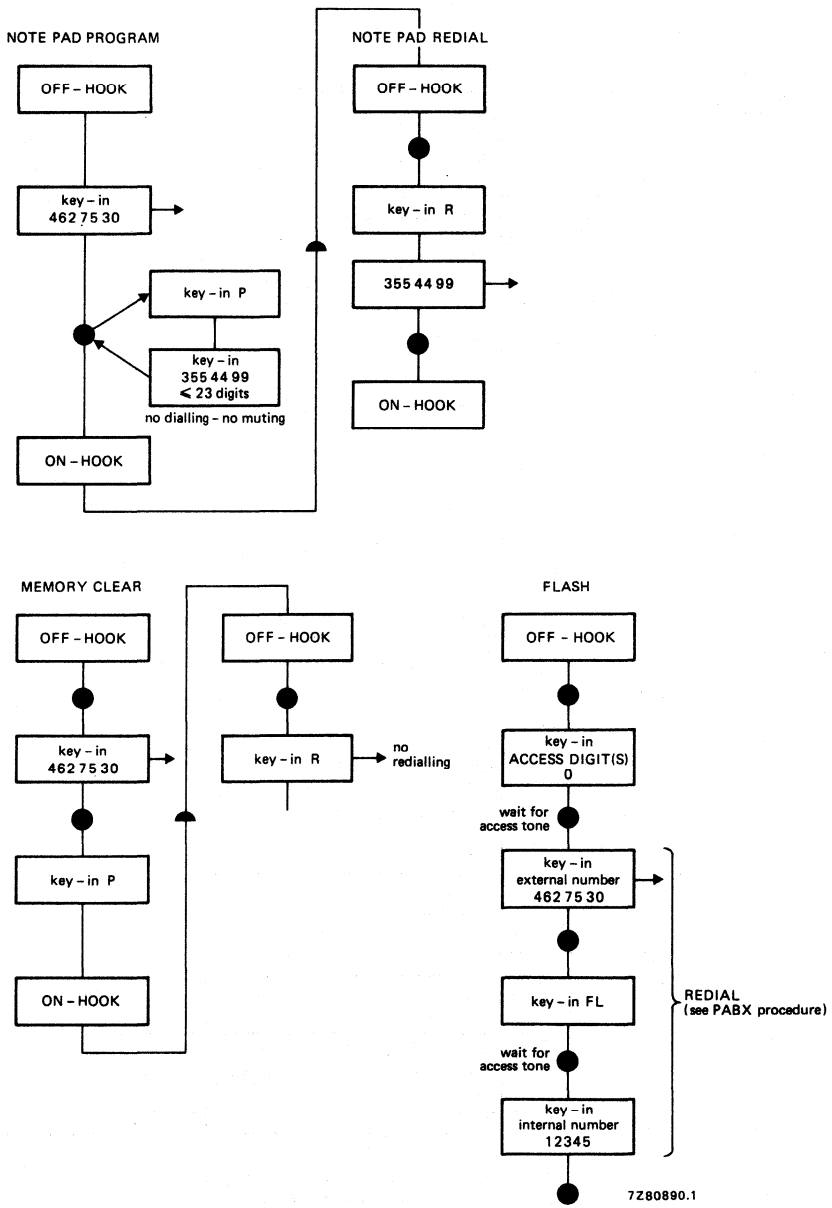


Fig.9 Notepad, memory clear, flash; independent of dialling mode

TIMING

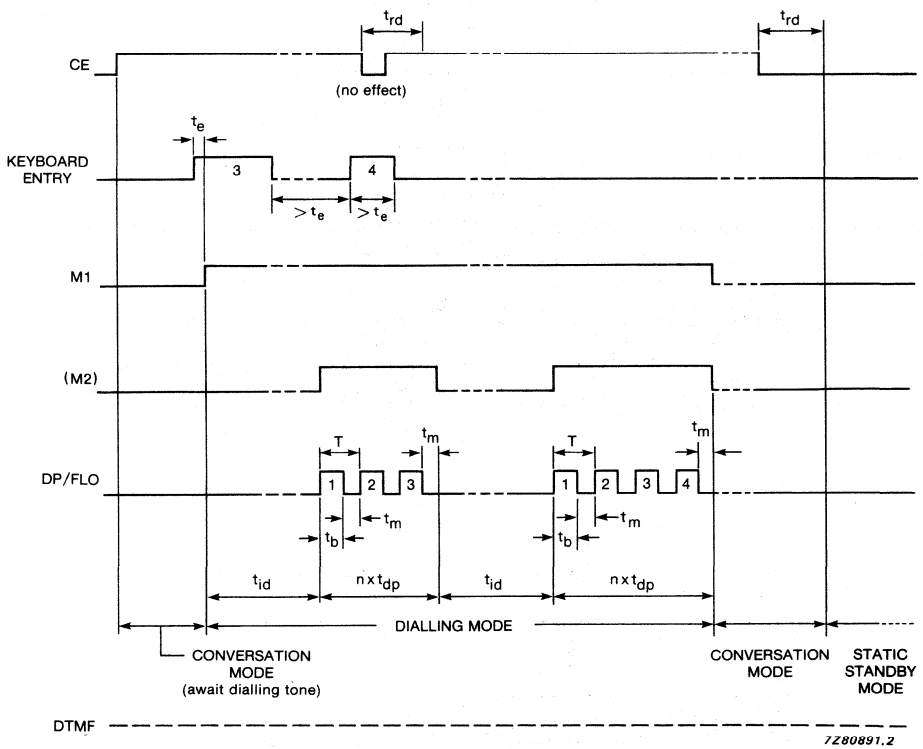


Fig.10a Timing diagram for pulse dialling ($\overline{PD}$/DTMF = V_{SS})

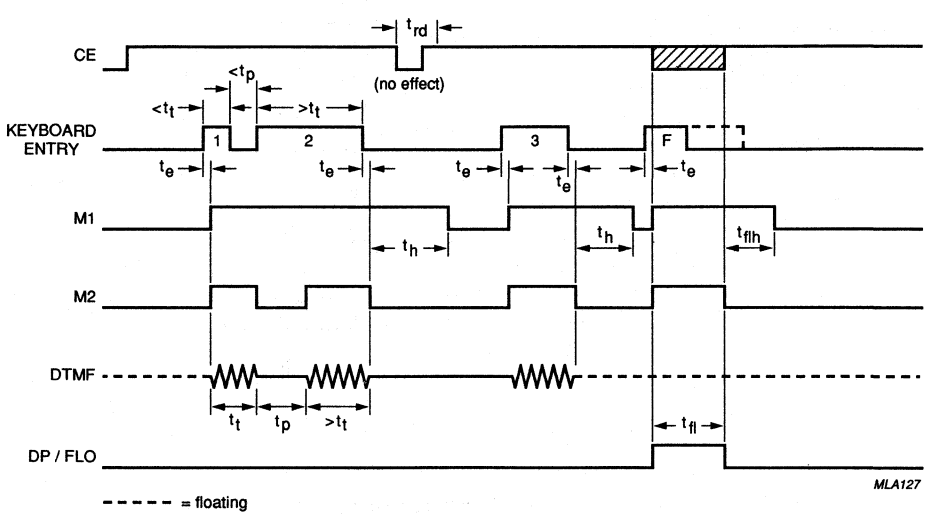


Fig.10b Timing diagram for DTMF dialling ($\overline{PD}$/DTMF = V_{DD})

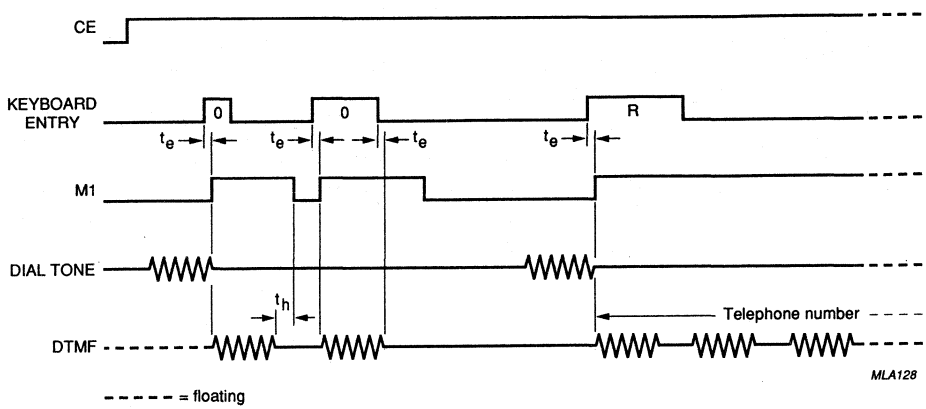


Fig.11 Timing diagram showing REDIAL where PABX access digits are the first keyboard entries in DTMF dialling mode.

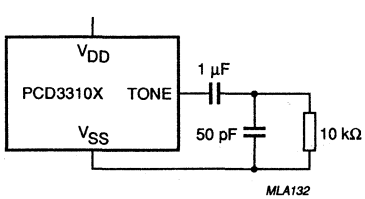


Fig.12 Tone output test circuit.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage range	−0.8	8	V
I_{DD}	supply current		50	mA
$\pm I_I, \pm I_O$	DC current into any input or output		10	mA
V_I	all input voltages	−0.8	V_{DD} + 0.8	V
P_{tot}	total power dissipation	-	300	mW
P_o	power dissipation per output	-	50	mW
T_{stg}	storage temperature range	−65	+ 150	°C
T_{amb}	operating ambient temperature range	−25	+ 70	°C

DC CHARACTERISTICS

V_{DD} = 3 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3.579545 MHz; T_{amb} = −25 to + 70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	operating supply voltage		2.5	-	6.0	V
V_{DDO}	standby supply voltage		1.8	-	6.0	V
	Operating supply current					
I_{DDC}	conversation mode	oscillator ON	-	-	150	µA
I_{DDP}	pulse dialling or flash		-	-	200	µA
I_{DDF}	DTMF dialling	tone ON	-	0.6	0.9	mt
I_{DDF}	DTMF dialling	tone OFF	-	-	200	µA
I_{DDO}	standby supply current	V_{DD} = 1.8 V oscillator OFF; note 1	-	-	2	µA
Inputs						
V_{IL}	input voltage LOW (any pin)		0	-	0.3 V_{DD}	V
V_{IH}	input voltage HIGH (any pin)		0.7 V_{DD}	-	V_{DD}	V
$\lvert I_{IL} \rvert$	input leakage current; CE		-	-	1	µA
Keyboard inputs						
R_{KON}	keyboard ON resistance		-	-	2	kΩ
R_{KOFF}	keyboard OFF resistance		1	-	-	MΩ
Outputs						
	output sink current	V_{OL} = V_{SS} + 0.5 V				
I_{OL}	M1, $\overline{M1}$, DP/FLO, CF, FLD		0.7	-	-	mA
I_{OL}	$\overline{PD}$/DTMF	note 2	-	-	1	mA
	output source current	V_{OH} = V_{DD} − 0.5 V				
$-I_{OH}$	M1, $\overline{M1}$, DP/FLO, CF, M2		0.6	-	-	mA
$-I_{OH}$	$\overline{PD}$/DTMF	note 2	-	-	1	mA
$-I_{OH}$	FLD	note 3	-	60	-	nA
Timing and frequency						
t_{on}	clock start-up time		-	4	-	ms
t_e	debounce time		-	12	-	ms
t_{rd}	reset delay time		-	160	-	ms
Tone output (see Fig.12)						
	DTMF output voltage levels	V_{DD} = 2.5 to 6 V				
$V_{HG(rms)}$	HIGH group		158	192	205	mV
$V_{LG(rms)}$	LOW group		125	150	160	mV
Δf/f	frequency deviation		−0.6	-	+ 0.6	%
V_{DC}	DC voltage level		-	1/2 V_{DD}	-	V
$\lvert Z_O \rvert$	output impedance		-	0.1	0.5	kΩ
ΔV_G	pre-emphasis of group		1.85	2.1	2.35	dB
THD	total harmonic distortion	T_{amb} = 25 °C, note 4	-	−25	-	dB

Notes to the DC characteristics

1. Crystal connected between OSCI and OSCO; CE at V_{SS} and all other pins open-circuit.
2. < |10 mA| dynamic current to set/reset $\overline{PD}$/DTMF pin (mixed mode).
3. Flash inactive; V_{OH} = V_{SS}.
4. Related to the level of the LOW group frequency component (CEPT CS 203).

TYPE NUMBER DEPENDENT CHARACTERISTICS

PCD3310

Confidence tone output (CF)

The confidence tone output pin is pin 15 for the SOT146 package and pin 20 for the SO28; SOT136A package.

When any key is activated a square-wave (330 Hz) is generated and appears at the CF output to serve as an acoustic feed-back for the user.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Transmission and pause time					
t_t, t_p	manual dialling	68	-	-	ms
t_t, t_p	redialling	68	70	72	ms
t_{FL}	flash pulse duration	98	100	102	ms
t_{flh}	flash hold-over time	31	33	34	ms
t_h	hold-over time (muting on M1)	78	80	81	ms
Pulse dialling					
f_{dp}	dialling pulse frequency	9.8	10	10.4	Hz
t_{id}	inter-digit pause	828	840	844	ms
t_b	break time	66	67	68	ms
t_m	make time	32	33	34	ms

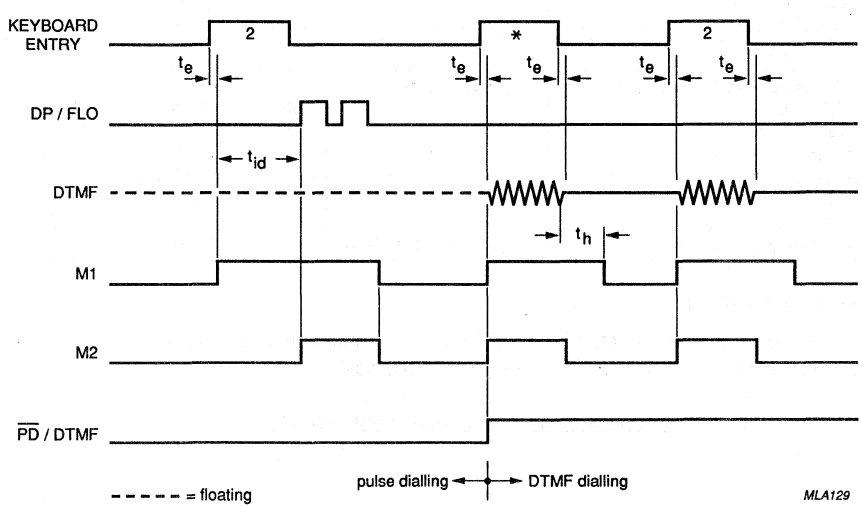


Fig.13 Timing diagram for mixed mode dialling ($\overline{PD}$/DTMF open-circuit).

PCD3310A

Confidence tone output (CF)

The confidence tone output pin is pin 15 for the SOT146 package and pin 20 for the SO28; SOT136A package.

When any key is activated a square-wave (330 Hz) is generated and appears at the CF output to serve as an acoustic feed-back for the user.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Transmission and pause time					
t_t, t_p	manual dialling	68	-	-	ms
t_t, t_p	redialling	68	70	72	ms
t_{FL}	flash pulse duration	98	100	102	ms
t_{flh}	flash hold-over time	31	33	34	ms
t_h	hold-over time (muting on M1)	78	80	81	ms
Pulse dialling					
f_{dp}	dialling pulse frequency	9.8	10	10.4	Hz
t_{id}	inter-digit pause	828	840	844	ms
t_b	break time	59	60	61	ms
t_m	make time	39	40	41	ms

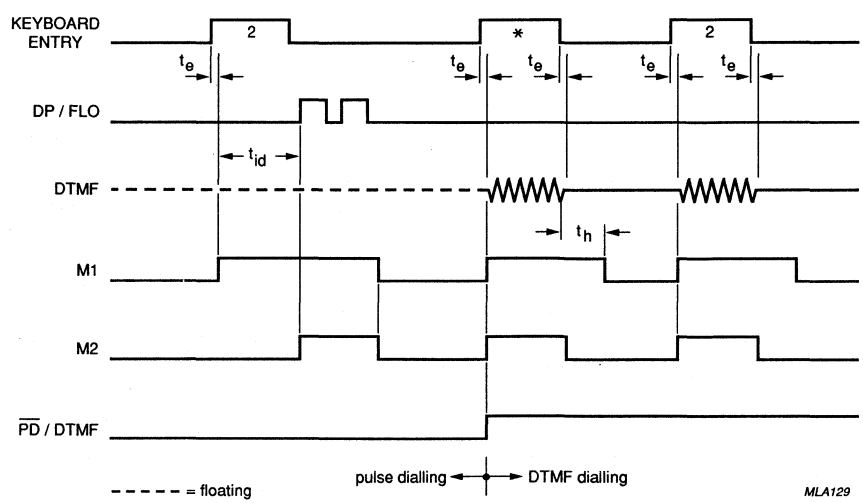


Fig.14 Timing diagram for mixed mode dialling ($\overline{PD}$/DTMF open-circuit).

PCD3310C

Dialling mode output (DMODE)

The dialling mode output is pin 15 for the SOT146 package and pin 20 for the SO28; SOT136A package.

The DMODE output represents the actual dialling status of the dialler. In pulse mode the output is LOW and in DTMF mode the output is HIGH.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Transmission and pause time					
t_t, t_p	manual dialling	68	-	-	ms
t_t, t_p	redialling	68	70	72	ms
t_{FL}	flash pulse duration	98	100	102	ms
t_{flh}	flash hold-over time	31	33	34	ms
t_h	hold-over time (muting on M1)	78	80	81	ms
Pulse dialling					
f_{dp}	dialling pulse frequency	9.8	10	10.4	Hz
t_{id}	inter-digit pause	828	840	844	ms
t_b	break time	66	67	68	ms
t_m	make time	32	33	34	ms

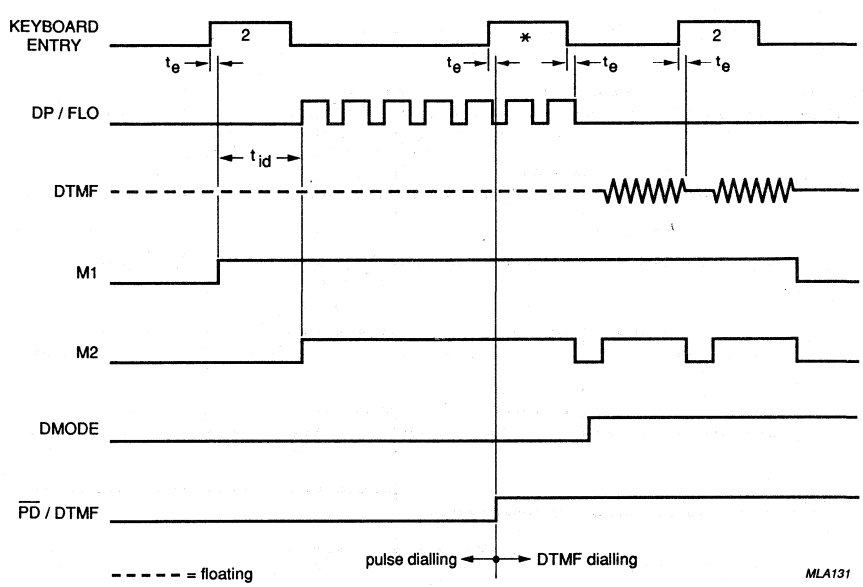


Fig.15 Timing diagram for mixed mode dialling ($\overline{PD}$/DTMF open-circuit).

PCD3310E

Pulse dialling frequency select (FS)

The frequency select pin is pin 15 for the SOT146 package and pin 20 for the SO28; SOT146 package.

If FS = V_{SS}; 10 Hz dialling selected. If FS = V_{DD}; 30 HZ dialling selected.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Transmission and pause time					
t_t, t_p	manual dialling	68	-	-	ms
t_t, t_p	retailing	68	70	72	ms
t_{FL}	flash pulse duration	98	100	102	ms
t_{flh}	flash hold-over time	31	33	34	ms
t_h	hold-over time (muting on M1)	78	80	81	ms
Pulse dialling @ 10 Hz					
f_{dp}	dialling pulse frequency	9.8	10	10.4	Hz
t_{id}	inter-digit pause	828	840	844	ms
t_b	break time	66	67	68	ms
t_m	make time	32	33	34	ms
Pulse dialling @ 20 Hz					
f_{dp}	dialling pulse frequency	19.6	20	20.8	Hz
t_{id}	inter-digit pause	496	504	512	ms
t_b	break time	33	34	35	ms
t_m	make time	16	17	18	ms

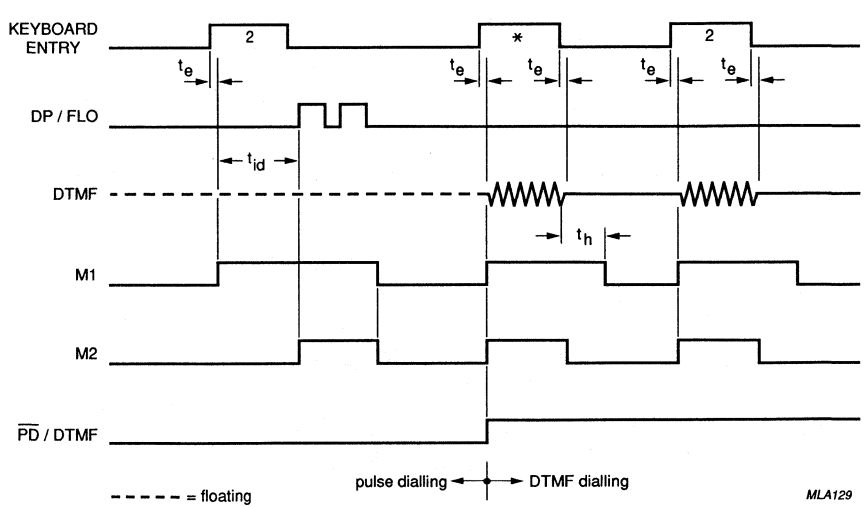


Fig.16 Timing diagram for mixed mode dialling ($\overline{PD}$/DTMF open-circuit).

PCD3310F

Confidence tone output (CF)

The confidence tone output pin is pin 15 for the SOT146 package and pin 20 for the SO28; SOT136A package.

When any key is activated a square-wave (330 Hz) is generated and appears at the CF output to serve as an acoustic feed-back for the user.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Transmission and pause time					
t_t	manual dialling	59	-	-	ms
t_p		89	-	-	ms
t_t	retailing	59	60	61	ms
t_p		89	90	91	ms
t_{FL}	flash pulse duration	98	100	102	ms
t_{flh}	flash hold-over time	31	33	34	ms
t_h	hold-over time (muting on M1)	99	100	101	ms
Pulse dialling					
f_{dp}	dialling pulse frequency	9.8	10	10.4	Hz
t_{id}	inter-digit pause	828	840	844	ms
t_b	break time	66	67	68	ms
t_m	make time	32	33	34	ms

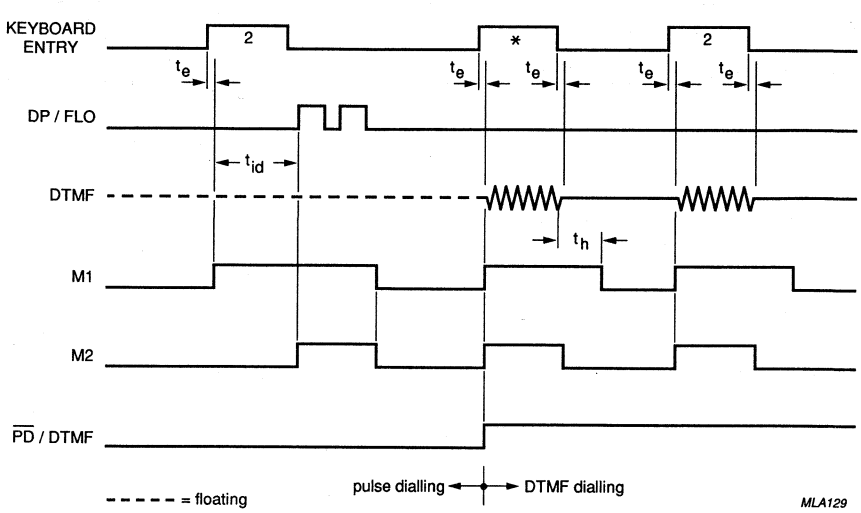


Fig.17 Timing diagram for mixed mode dialling ($\overline{PD}$/DTMF open-circuit).

PCD3310G

Confidence tone output (CF)

The confidence tone output pin is pin 15 for the SOT146 package and pin 20 for the SO28; SOT136A package.

When any key is activated a square-wave (330 Hz) is generated and appears at the CF output to serve as an acoustic feed-back for the user.

In mixed mode dialling the switch-over from pulse to DTMF mode can be activated by the * and # keys without sending out its corresponding frequencies when activated for the first time.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Transmission and pause time					
t_t, t_p	manual dialling	68	-	-	ms
t_t, t_p	retailing	68	70	72	ms
t_{FL}	flash pulse duration	98	100	102	ms
t_{flh}	flash hold-over time	31	33	34	ms
t_h	hold-over time (muting on M1)	78	80	81	ms
Pulse dialling					
f_{dp}	dialling pulse frequency	9.8	10	10.4	Hz
t_{id}	inter-digit pause	828	840	844	ms
t_b	break time	66	67	68	ms
t_m	make time	32	33	34	ms

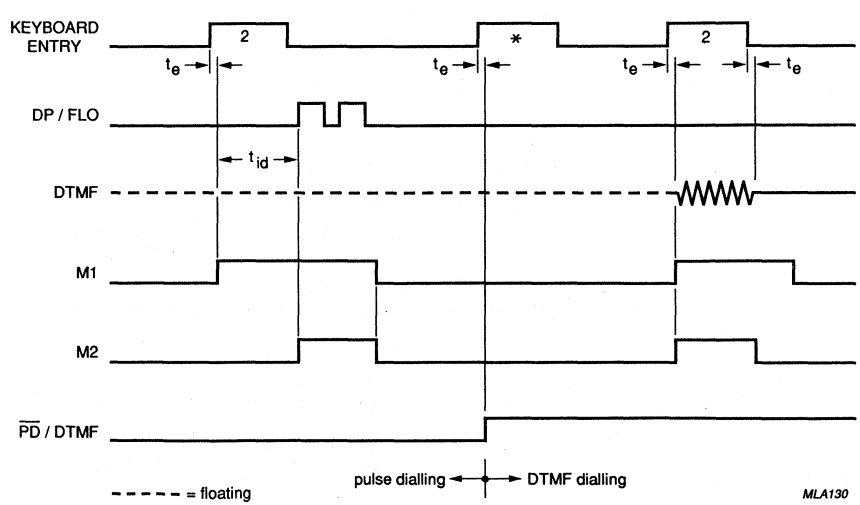


Fig.18 Timing diagram for mixed mode dialling ($\overline{PD}$/DTMF open-circuit).

APPLICATION INFORMATION

1. Automatic line compensation obtained by connecting R6 to V_{SS}.
2. The value of resistor R14 is determined by the required level at LN and the DTMF gain of the TEA 1060/61.

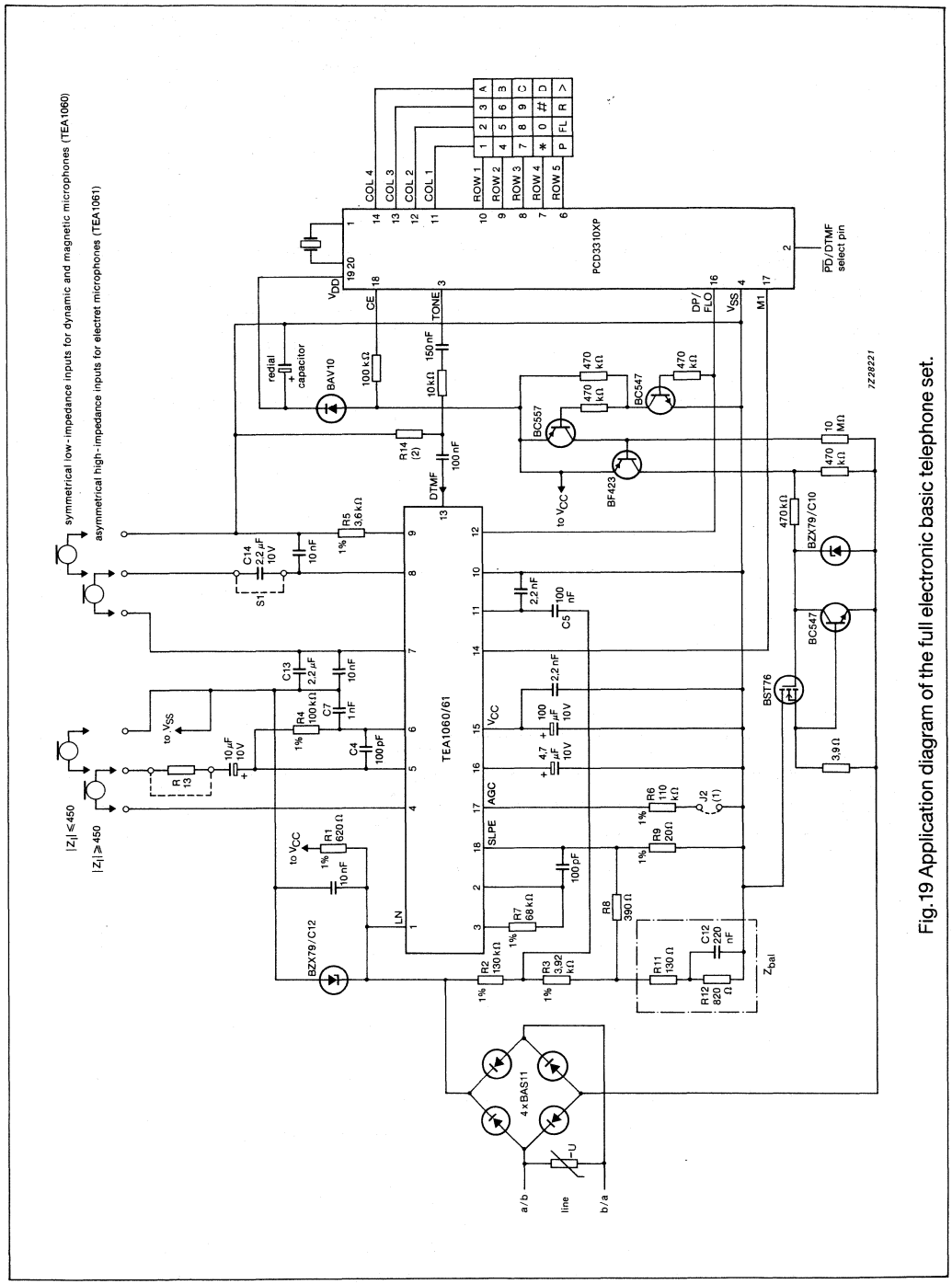


Fig. 19 Application diagram of the full electronic basic telephone set.

Repertory pulse dialler with redial PCD3315/512; PCD3315/513

FEATURES

- Redial
- Extended redial
- Number of digits per call is infinite (FIFO register)
- 10 repertory numbers (18 digits)
- Electronic note pad
- 4 x 4 keyboard (function keys: program/autodial, flash, redial and access pause)
- 2 x 5 keyboard extension for repertory dial
- Four diode or strap functions:
  - mark/space ratio
  - flash time
  - access pause time
  - tone burst time
- Special inputs: CE, $\overline{\text{HOLD}}$ and RESET
- Special outputs: $\overline{\text{AP}}$ and M1
- Mark/space ratio 2:1 or 3:2 (only for 10 Hz)
- Pulse dialling for 10, 16 and 20 Hz (PCD3315/512)
- Pulse dialling 10 Hz for Sweden and Norway (PCD3315/513)
- DTMF dial control of PCD3312A
- DTMF tone/pause 70/70 or 100/100 ms (PCD3315/512)
- DTMF tone/pause 70/70 or 170/170 ms (PCD3315/513)
- Flash 95 or 650 ms
- Manual insertion of access pause
- Automatic insertion of access pause
- Access pause time for pulse dialling 3 or 5 s
- Access pause time for DTMF 1.5 or 2.5 s
- On-chip power-on reset
- 2.5 to 6.0 V operating supply voltage
- 3.58 MHz crystal oscillator.

GENERAL DESCRIPTION

The PCD3315/512 and PCD3315/513 are single-chip CMOS dialler ICs for telephone sets. They have two dialling modes; pulse dialling (PD) and dual tone multi-frequency (DTMF) when used in conjunction with tone generator PCD3312A. In addition to manual dialling they also feature several automatic functions e.g. Redial, Extended redial, note pad and repertory dial.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCD3315P	28	DIL	plastic	SOT117
PCD3315T	28	SO28	plastic	SOT136A

Single-chip 8-bit Telecom Microcontroller

PCD3315A

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC14 OR DATA SHEET

FEATURES

- 8-bit CPU, ROM, RAM, I/O in a single 28-lead package
- 1536 bytes ROM
- 160 bytes RAM
- Over 100 instructions (based on MAB8048) all of 1 or 2 cycles
- 20 quasi-bidirectional I/O port lines
- 8-bit programmable timer/event counter 1
- Two single-level vectored interrupts: external, 8-bit programmable timer/event counter 1
- Two test inputs, one of which also serves as the external interrupt input
- Power-on reset
- Stop and idle modes
- Logic supply V_{DD}: 1.8 V to 6 V
- Low standby voltage V_{DD}: 1 V
- Low standby current I_{DD}: 1.2 µA (typ.) at 1.8 V; T_{amb} = 25 °C
- Clock frequency: 1 MHz to 16 MHz
- Operating temperature range: –25 °C to +70 °C
- Manufactured in silicon gate CMOS process

GENERAL DESCRIPTION

This data sheet details the specific properties of the PCD3315A. The shared characteristics of the PCD33XXA family of microcontrollers are described in the PCD33XXA family data sheet, which should be read in conjunction with this publication.

The PCD3315A is a microcontroller which has been designed primarily for Telecom applications. It provides 1.5k bytes of program memory, 160 bytes of RAM and 20 I/O lines. The instruction set is based on that of the MAB8048 and is software compatible with the PCD33XXA family.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	positive supply voltage	–0.5	+7.0	V
V_I	all input voltages	–0.5	V_{DD}+0.5	V
I_{DD}	positive supply current	–50	+50	mA
I_{SS}	ground supply current	–50	+50	mA
I_I, I_O	DC input or output current	–10	+10	mA
P_{tot}	total power dissipation	–	125	mW
P_O	power dissipation per output	–	30	mW
T_{stg}	storage temperature range	–55	+150	°C
T_j	operating junction temperature	–	90	°C

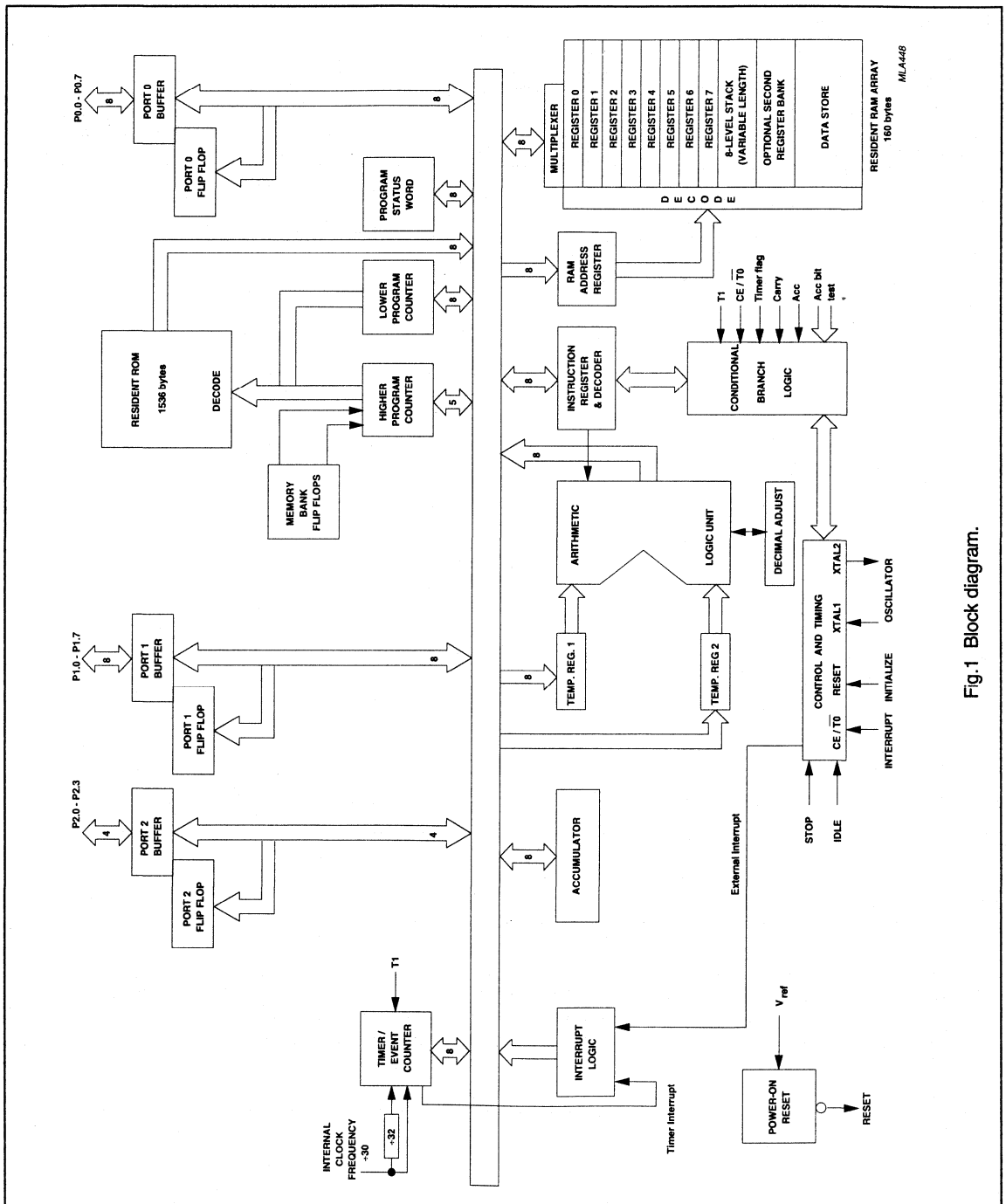


Fig.1 Block diagram.

Single-chip 8-bit Telecom Microcontroller

PCD3315A

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCD3315AP	28	DIL	plastic	SOT117
PCD3315AT	28	mini	plastic	SOT136A

Note to the Ordering Information

Full and up-to-date data for this device is available upon request via your Philips local sales office.

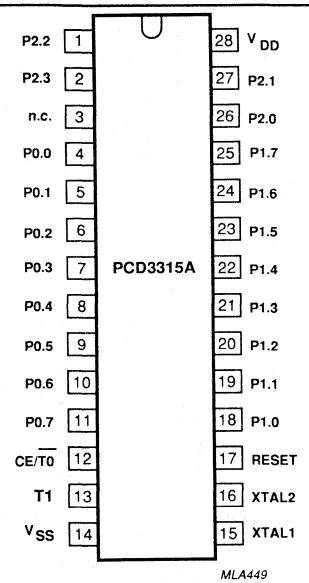


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	I/O	DESCRIPTION
P2.2–P2.3	1–2	I/O	Port 2: quasi-bidirectional I/O line
n.c.	3	–	not connected
P0.0–P0.7	4–11	I/O	Port 0: quasi-bidirectional I/O lines
CE/$\overline{T0}$	12	I	chip enable/test 0
T1	13	I	test 1/count input of 8-bit timer/event counter 1
V_{SS}	14	P	ground (0 V)
XTAL1	15	I	crystal oscillator/external clock input
XTAL2	16	O	crystal oscillator output
RESET	17	I	reset input
P1.0–P1.7	18–25	I/O	Port 1: quasi-bidirectional I/O line
P2.0–P2.1	26–27	I/O	Port 2: quasi-bidirectional I/O lines
V_{DD}	28	P	positive supply voltage

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

This Data sheet has been changed, see footnote !

PULSE DIALLER CIRCUITS WITH REDIAL

GENERAL DESCRIPTION

The PCD332XC family comprises seven CMOS pulse dialler circuits with redial. Each circuit converts 3 x 4 matrix keyboard entries into correctly-timed line current interruptions. For redial, the last-dialled number (up to 23 digits) is stored in an on-chip RAM. A RAM overflow is handled by inhibiting the redial but manual dialling of more than 23 digits still can be made. The circuits include a delayed reset for line power breaks to ensure correct operation.

Most ICs of the family regenerate an access pause during redial. Insertion of the access pause during the original entry is either automatic or via the '*' key. Termination of the regenerated access pause during redial is via the '#' key, after a built-in delay or controlled by an external tone recognizer. Other differences between the circuits are selections of pulse dialling frequency, mark/space ratio, regenerated access pause duration, mute, hold/access pause output control and oscillator frequency.

Features

- Operating supply voltage range: 2.0 to 6.0 V
- Static supply voltage (with redial memory data retention): down to 1.5 V
- Low operating supply current: typ. 60 μA
- Low static standby supply current: typ. 0.65 μA
- On-chip RAM capacity: 23 keyboard entries (digits and access pauses)
- Redial inhibited after memory overflow
- Manual dialling can continue beyond 23 keyboard entries (excess entries are stored at lower RAM addresses)
- (Re)dialling procedure is not affected by line interruptions shorter than the reset delay time (if the supply voltage does not fall below the static standby voltage)
- Line interruptions longer than the reset delay time are regarded as on-hook situations
- Hold facility for lengthening the inter-digit period
- On-chip oscillator for 3.58 MHz crystal (type for ceramic resonator is also available)
- Fully decoded and debounced inputs for 3 x 4 matrix keyboard
- Pull-up or pull-down circuits at all inputs except CE
- Electrostatic discharge protection at all inputs
- High input noise immunity
- Test mode in which the dialling frequency is increased.

Note:

the PCD3320C, PCD3322C, PCD3324C and PCD3325C are not to be used for new design-ins

The PCD332XC family of ICs comprises the following types:

PCD3320C dialler with several mute signals
PCD3321C dialler with two automatic access pauses
PCD3322C variant of PCD3320C
PCD3324C dialler with one automatic access pause
PCD3325C dialler with manual access pause control
PCD3326C variant of PCD3321C
PCD3327C variant of PCD3325C for ceramic resonator with automatic reset of access pause

functional survey		PCD . . .						
		3320C	3321C	3322C	3324C	3325C	3326C	3327C
Number of pins		18	18	18	18	18	18	18
Dialling frequency	10 Hz	●	●	●	●	●	●	●
selectable with F01, F02	16, 20 Hz		●		●	●	●	●
Mark/space ratio	3 : 2	●	●	●	●	●	●	●
selectable with M/S	2 : 1		●		●	●		●
Access pauses repeated during redial			●		●	●	●	●
Manual insertion of access pauses			●		●	●	●	●
Automatic access pause insertion								
	1 max				●			
	2 max		●				●	
Access pause duration	32 x T_{DP}		●		●		●	●
selectable with APD	64 x T_{DP}						●	
not automatically terminated						●		
$\overline{M1}$, inverted mute output		●		●				
M2, strobe output				●				
M3, AND function of mute (M1) and inverted dialling pulse (DP) outputs		●						
HOLD, dialling-interrupt input		●		●				
APO + HOLD, internally connected			●		●	●	●	●

T_{DP} = dialling pulse period

* PCD3327C for ceramic resonator

Features common to all PCD332XC family

OSC IN, OSC OUT: on-chip oscillator input and output
C1 to C3: column keyboard inputs with on-chip pull-up
R1 to R4: row keyboard outputs with on-chip pull-down
CE: chip enable input
DP: dialling pulse output to external line-switching transistor or relay
M1: mute output

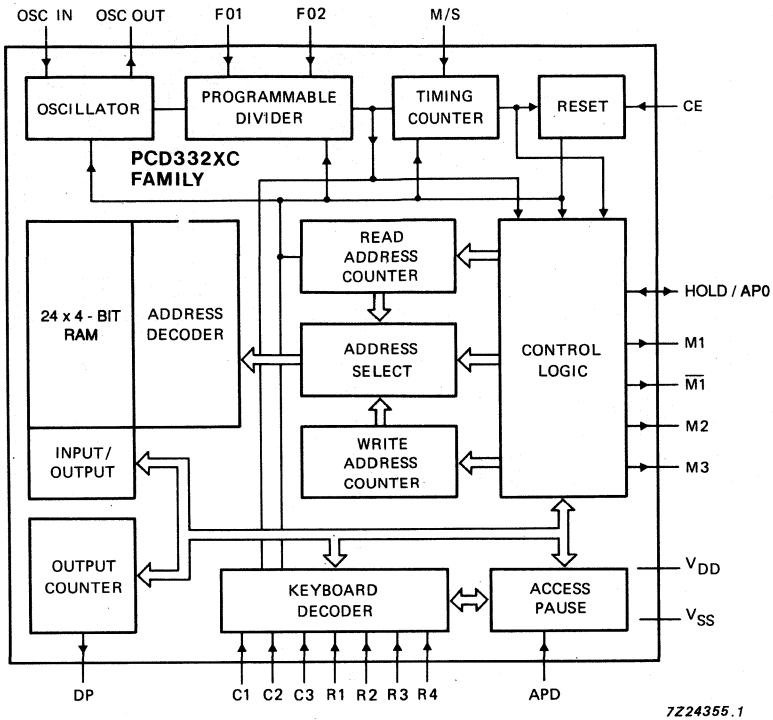


Fig.1 Block diagram.

DEVELOPMENT DATA

PACKAGE OUTLINES

PCD3320CP
PCD3321CP
PCD3322CP
PCD3324CP
PCD3325CP
PCD3326CP
PCD3327CP
: 18-lead DIL; plastic (SOT102G).

PCD3320CD
PCD3321CD
: 18-lead DIL; ceramic (SOT133B).

PCD3321CT
PCD3322CT
PCD3327CT
: 20-lead mini-pack; plastic (SOT163A).

PCD3327U: uncased chip in tray.

PINNING

pin	purpose	PCD . . .						
		3320C	3321C	3322C	3324C	3325C	3326C	3327C
Supplies								
V_{DD}	positive supply	●	●	●	●	●	●	●
V_{SS}	negative supply	●	●	●	●	●	●	●
Inputs								
M/S	controls mark/space ratio of the line pulses		●		●	●		●
F01	define the dialling pulse frequency	●	●	●	●	●	●	●
F02			●		●	●	●	●
CE	Chip enable: used to initialize the system, to select between operating and static standby mode and to handle line power breaks	●	●	●	●	●	●	●
C1	keyboard column inputs with on-chip pull-up	●	●	●	●	●	●	●
C2								
C3								
ADP	Access Pause Duration: selects the maximum duration of an access pause if no external APR appears						●	
R1	keyboard row outputs with on-chip pull-down	●	●	●	●	●	●	●
R2								
R3								
R4								
HOLD	interrupts dialling after completion of the current digit or immediately during an inter-digit pause	●		●				
Outputs								
DP	Dialling Pulse: drive of the external switching transistor or relay	●	●	●	●	●	●	●
M1	Muting: normally used for muting during the dialling sequence	●	●	●	●	●	●	●
$\overline{M1}$	inverted output of M1	●		●				

pin	purpose	PCD . . .						
		3320C	3321C	3322C	3324C	3325C	3326C	3327C
M2	strobe; HIGH during pulsing of each digit, LOW during an inter-digit pause			●				
M3	AND-function with $\overline{DP}$ and M1 as inputs; for direct drive of a switching transistor for dialling pulses and muting	●						
Oscillator								
OSC IN OSC OUT	input and output of the on-chip oscillator	● ●	● ●	● ●	● ●	● ●	● ●	● ●
Input/outputs								
HOLD/APO	The HOLD and APO features are connected together at this pin, normally an output pin but can be forced as an input		●		●	●	●	●

DEVELOPMENT DATA

PINNING (continued)

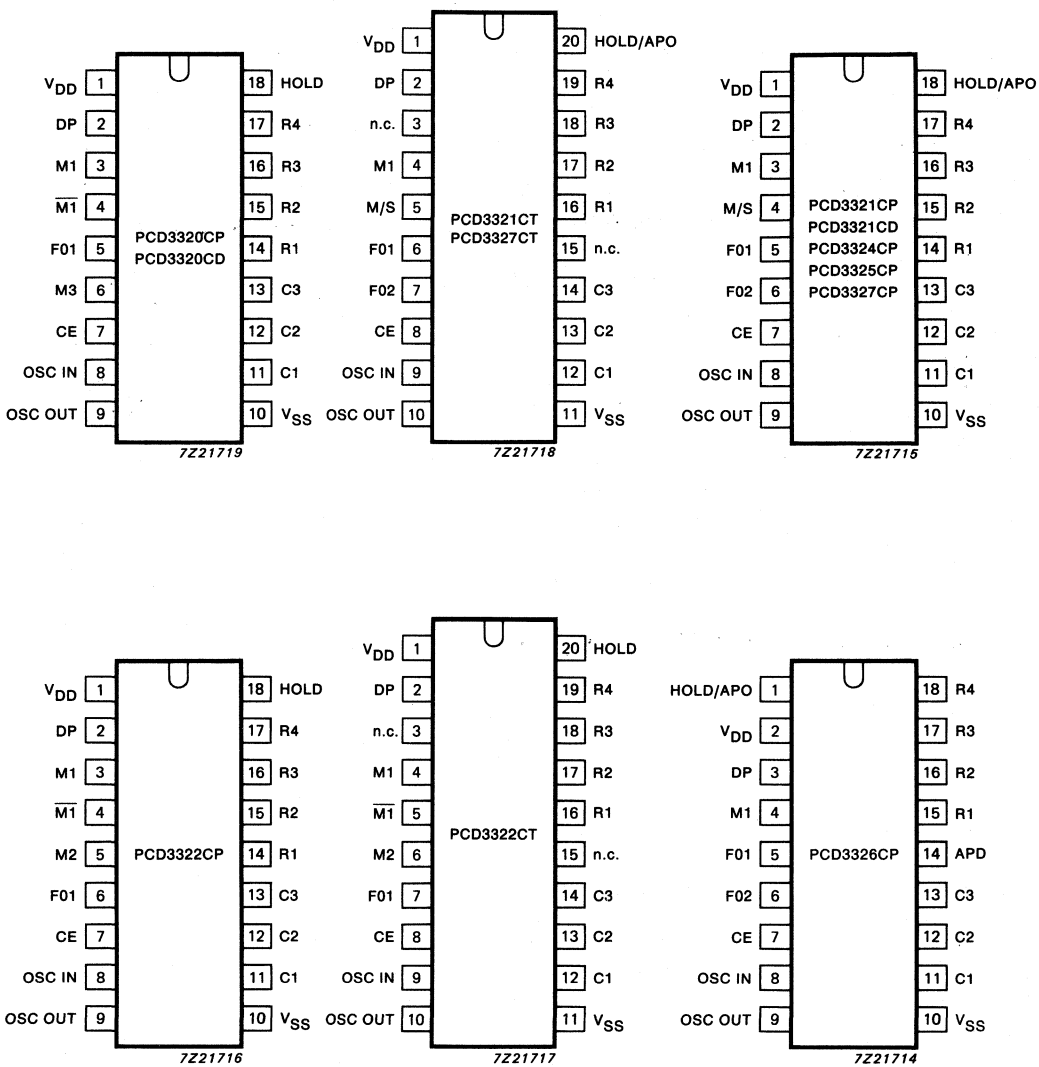


Fig.2 Pinning diagrams.

FUNCTIONAL DESCRIPTION

Clock oscillator (OSC IN, OSC OUT)

The time base for the circuit is a crystal-controlled on-chip oscillator which is completed by the connection of a crystal between the OSC IN and OSC OUT pins (a ceramic resonator may be used with the PCD3327C). Alternatively, the OSC IN pin can be driven by an external clock signal.

Clock divider (F01, F02)

The oscillator is followed by a frequency divider, the division ratio of which can be set externally (F01, F02) to provide one of four chip system clocks, i.e. three 'normal' clock frequencies and one higher frequency for testing.

Other frequencies can also be obtained by driving OSC IN, as previously stated.

Chip enable (CE)

The CE input is used to initialize the chip system.

CE = LOW provides the static standby condition. In this mode the clock oscillator is off and internal registers are clamped at reset, excepting the WRITE ADDRESS COUNTER (WAC). The keyboard input is prohibited, but data previously entered is saved in the RAM.

When CE = HIGH the clock oscillator is operating, the internal registers are enabled and data can be entered from the keyboard.

If the CE input is taken to a LOW level for more than the time t_{rd} (see Figs 5 and 6 and timing data) an internal reset pulse will be generated at the end of the t_{rd} period. The system is then in the static standby mode. Short CE pulses of $< t_{rd}$ will not affect the operation of the circuit and reset pulses are not produced.

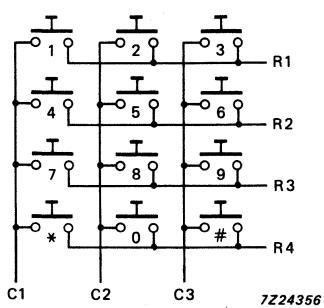
Debouncing keyboard entries (C1 to C3; R1 to R4)

The column keyboard inputs to the integrated circuits(Cn) and the row keyboard outputs (Rn) are for direct connection to a 3 x 4 single contact keyboard matrix (with or without common contact) as shown in Fig.3, or to a double contact keyboard with a common left open contact (see Fig.4). An entry is decoded into a 4-bit binary keycode by the keyboard decoder when one column input is connected to one row input. Any other input combinations are not valid and will not be accepted. Valid inputs are debounced on the leading and trailing edges as shown in Fig.5. Keyboard entries are only decoded into 4-bit binary keycodes and written into the RAM if the keyboard contact remains closed for five or six clock pulse periods (entry period t_e). The next keyboard entry will not be accepted until the previously closed contact has been left open for four or five clock pulse periods. The one clock pulse period of uncertainty in the debouncing process arises because keyboard entries are not detected until the leading edge of the first clock pulse after the entry.

Data entry

After each keyboard entry has been debounced and decoded, the keycode is written into the RAM, and the WAC is incremented by one to select the next RAM location where the next keycode will be stored. As each keycode is recalled from the RAM for line pulsing, the READ ADDRESS COUNTER (RAC) is incremented by one to select the RAM location of the next keycode to be recalled. Consequently, the difference between the contents of the WAC and of the RAC represents the number of keycodes that have been written into the RAM but not yet converted into line pulses. If more than 23 codes are written into the RAM, memory overflow results and the access keycodes replace the data in the lower-numbered locations. In this event, since an erroneous number is stored, automatic redialling is inhibited until the WAC has been reset by the first digit entry of the next telephone call.

If the first pushbutton to be pressed is not redial (#), the WAC is reset during entry time t_e, the corresponding keycode is written into the first RAM location and the WAC is then incremented by one. If the first pushbutton to be pressed is redial (#), the WAC is not reset and the keycodes stored in the RAM are sequentially recalled and converted into correctly-timed dialling pulses at output DP. If the redial pushbutton (#) is operated again during the redialling sequence it will be decoded as an Access Pause Reset (see 'Access Pause System'). During redial, no keyboard entry will be accepted and stored in the RAM. But, when all numbers stored in the RAM have been pulsed out, new keyboard entries will be accepted and stored in the RAM position after the last digit code of the original entry and converted into correctly-timed dialling pulses.



* Access pause set.
\# Redial or access pause reset.

Fig.3 Single contact keyboard.

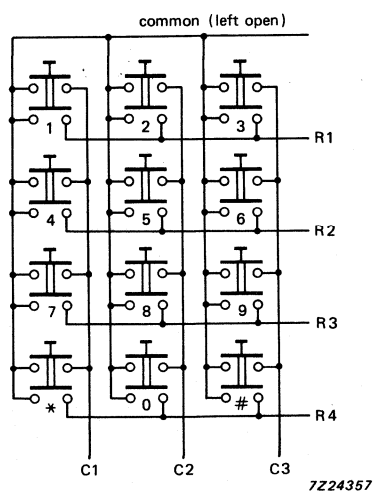


Fig.4 Double contact keyboard.

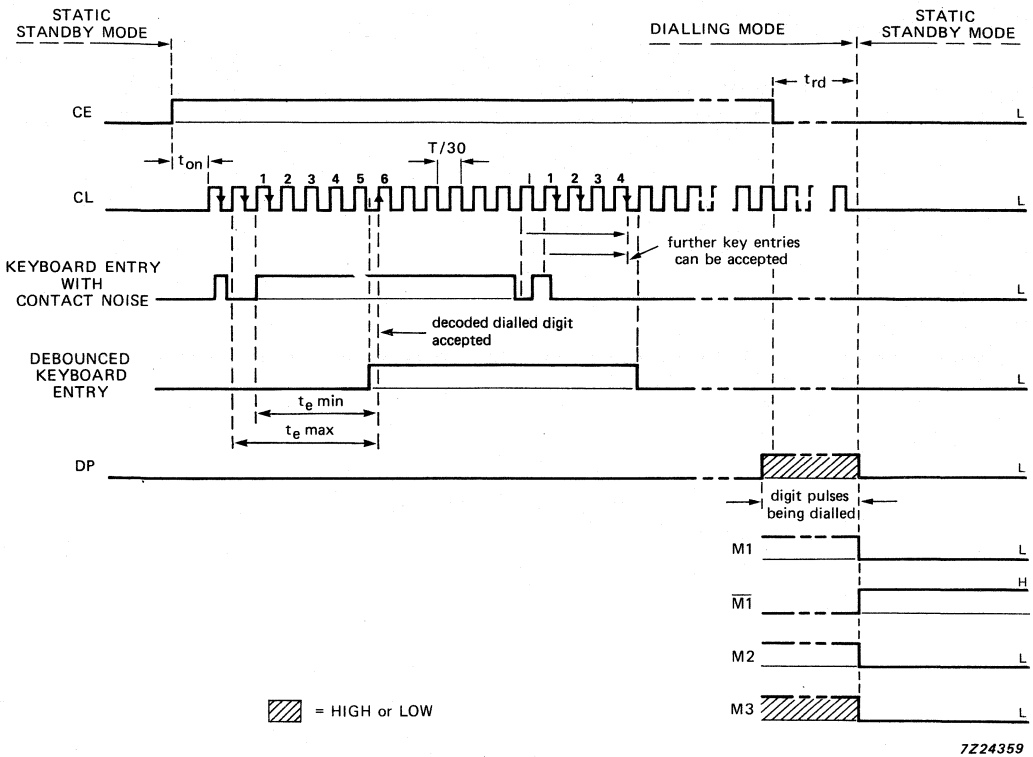


Fig.5 Timing diagram showing clock start-up, keyboard entry debouncing and the effect of interrupting the supply to CE during the transmission of dialling pulses.

DEVELOPMENT DATA

Dialling sequence

The dialling sequence can be initiated under either of the following two conditions:

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts (power supply before keyboard entry); see Fig.6.

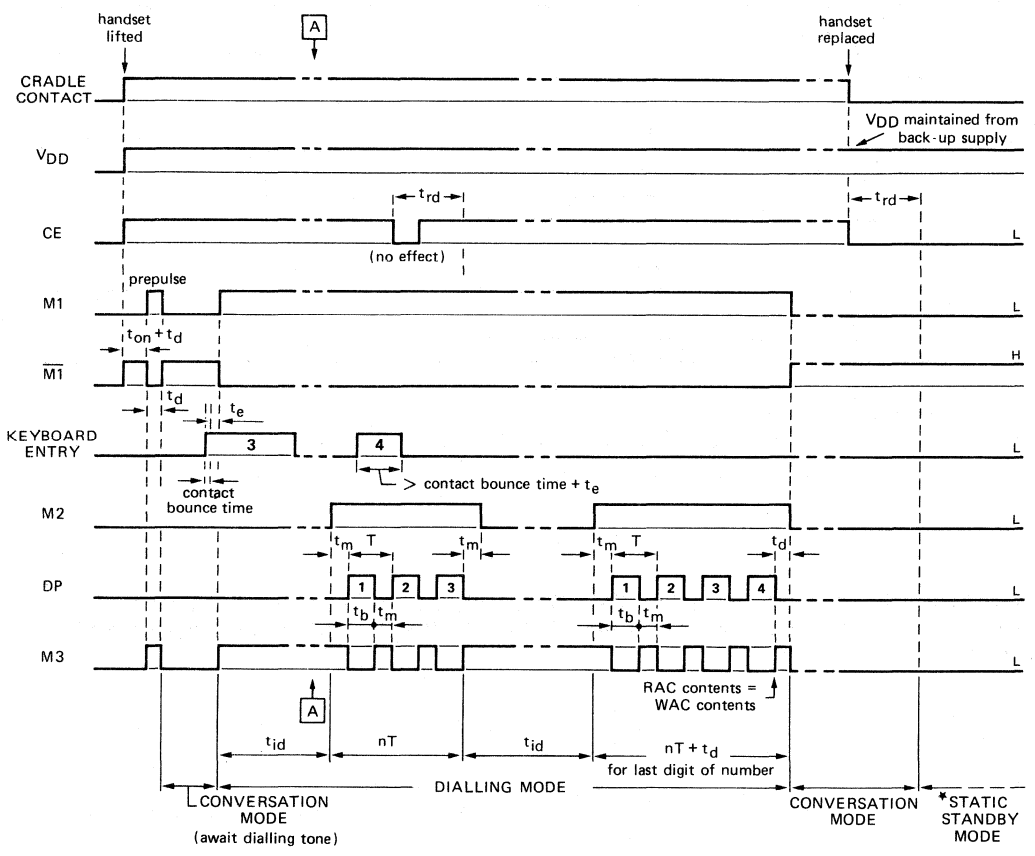
Then, approximately 4 ms (t_{on}) after CE goes HIGH, the clock pulse generator starts and ten clock pulse periods later a prepulse with a duration of ten clock pulse periods (t_d) appears at outputs M1 and M3. This prepulse ensures that if a polarized muting relay with two stable positions is used it switches to the de-muted position so that the circuit is then in the conversation mode whilst the subscriber awaits the dialling tone. When the first digit of the required number is entered at the keyboard, data entry period t_e commences.

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts in series with a common keyboard contact (see Fig.7).

When the first digit of the required number is entered at the keyboard, the common keyboard contact connects the line voltage to V_{DD} and CE becomes HIGH. Approximately 4 ms (t_{on}) after CE goes high, the clock pulse generator starts and data entry period t_e commences. After period t_e, M1 goes HIGH and the pushbutton can be released. The supply to V_{DD} and CE is then maintained via the muting circuit controlled by M1.

Dialling sequence (continued)

Referring to Fig.6, when the keyboard entry has been decoded and written into the RAM, M1 goes HIGH to mute the telephone and an inter-digit pause (t_{id}) ensues. M2 then goes HIGH, the RAC addresses the RAM and the first keycode is loaded into the register of the output counter which generates the appropriate number of correctly-timed dialling pulses at outputs DP and M3. When the digit has been pulsed out, M2 goes LOW, the RAC is incremented by one and the procedure repeats until the WAC and RAC contents are equal (all digits pulsed out). Output M1 then goes LOW, the circuit assumes the conversation mode. The circuit reverts to the static standby mode if CE goes LOW for more than the reset delay time (t_{rd} = 1.6 dialling pulse periods) at any time during the conversation or dialling mode (e.g. because the handset is replaced). CE remains LOW although V_{DD} is maintained by a back-up supply (e.g. because an external diode isolates CE from the back-up supply connected to V_{DD}). The RAM retains its contents for subsequent automatic redialling as long as the back-up supply maintains V_{DD} above the level V_{DD0} = 1.5 V, which is detected by the power-on reset circuit.



* Oscillator off; all registers reset; keyboard input inhibited; number stored in RAM until $V_{DD} < 1.5$ V.

Fig.6 Timing diagram of dialling sequence with V_{DD} and CE HIGH before keyboard entry (e.g. supply via the cradle contacts).

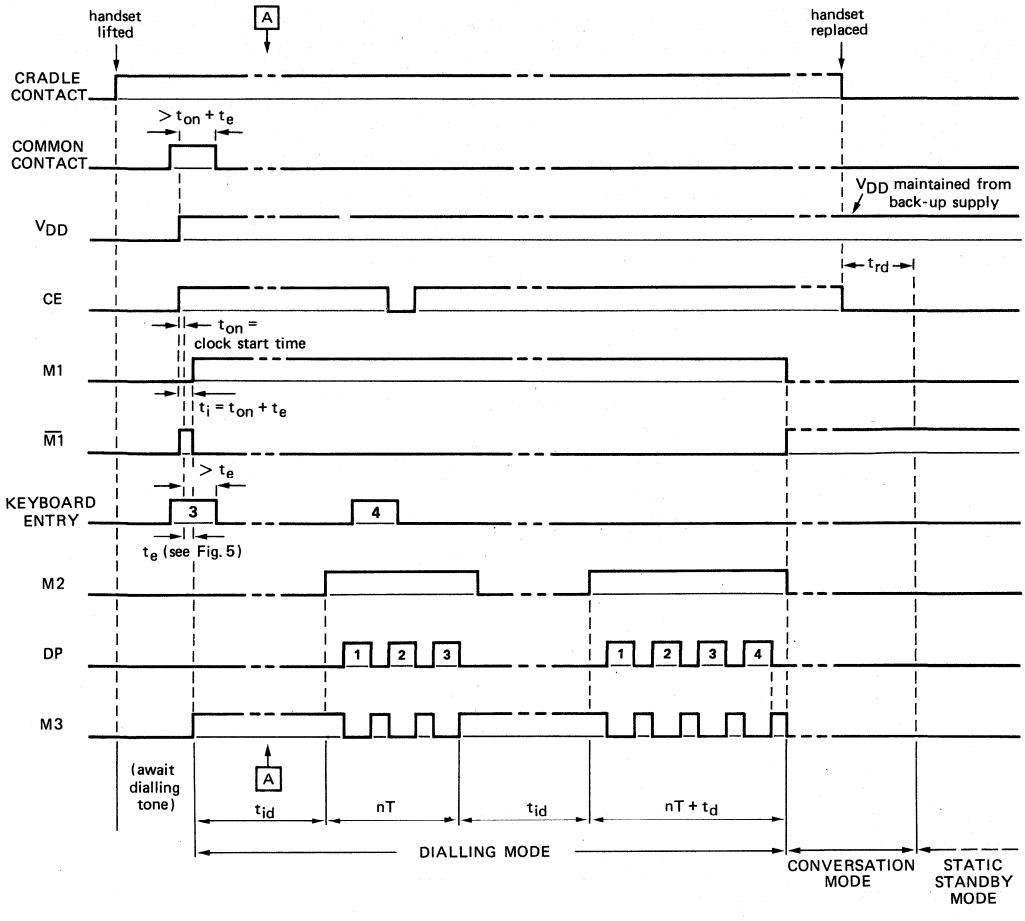


Fig.7 Timing diagram for initiating the dialling mode with V_{DD} and CE initially supplied via the cradle contacts in series with a common contact on the keyboard. See Fig.6 for pulse timings after point A.

Hold function (HOLD)

As shown in Fig.8, the hold function allows the interval between consecutive pulsed digits to be prolonged under the control of external equipment. When the HOLD input is set HIGH, the dialling pulse-train is interrupted as soon as M2 goes LOW to signal that the current digit has been pulsed out. In the hold condition, further keyboard entries will be accepted, debounced, decoded and stored in that RAM. No further keycodes will be read from the RAM to be converted into dialling pulses on M3 and DP until the HOLD input is set LOW again and an inter-digit pause has elapsed.

HOLD can be controlled by the Access Pause Output (see section "Access pause system).

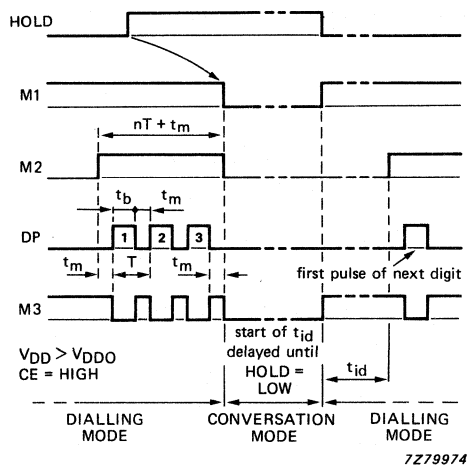


Fig.8 Timing diagram showing the effect of activating the HOLD input during the transmission of dialling pulses.

Access pause system (HOLD/APO)

The PCD3320C and PCD3322C only have the HOLD input and therefore these devices cannot reproduce the access pauses during redial (the access pause system is disabled). In all the other devices the HOLD input is internally connected to the APO output. This pin (HOLD/APO) can be used as an output, or forced as an input (e.g. by an external tone recognizer). Access pauses can be stored at appropriate positions in the RAM during the original entry of a number. As soon as the access pause code is read from the RAM, the access pause output (HOLD/APO) goes HIGH and dialling is interrupted.

Storing access pauses during dialling

Access pauses can be stored by one or both of the following ways:

- Manually by pressing the access pause key (*). The number of access pauses that can be stored in this way is limited only by the capacity of the RAM (digits + access pauses $\leqslant 23$).
- In some ICs of the family an access pause is stored automatically in the RAM (see Fig.9) during the original entry after all the digits so far entered have been transmitted (when M1 goes LOW, see Fig.6). The maximum number of access pause codes that can be entered in this manner is either one or two, depending on the type of IC.

Note: that when access pauses are manually inserted into ICs with automatic insertion of access pauses, the circuit automatically adds an access pause code after the number. This increases the RAM digit-count by one and reduces the maximum number of digits to 22 (including actual access pauses). The same would happen if the maximum number of access pauses for automatic entry is not reached before the end of the number.

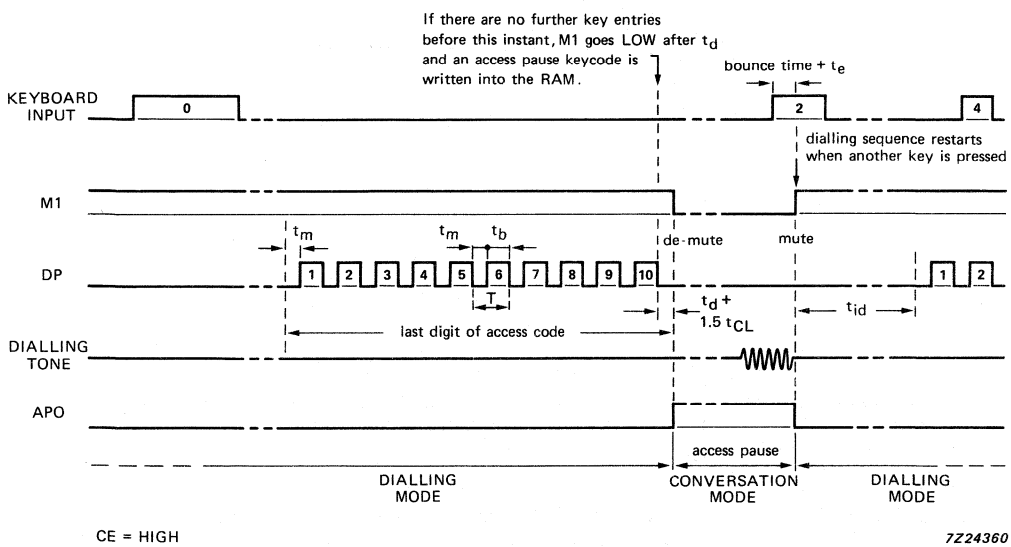


Fig.9 Dialling sequence showing how an access pause code is automatically stored in the RAM for possible redialling if no further key entries are made until all of the previously entered digits have been transmitted. The dialling sequence continues when another key is pressed.

Terminating access pauses during redial (APD)

If APO is connected to HOLD, there are three ways of terminating access pauses during redial (see Fig.10):

- Manually by pressing the redial key before t_{ap} expires.
- Automatically if the built-in time t_{ap} expires; APO, and also HOLD, then go LOW so that the next digit will be dialled. With the Access Pause Delay (APD) select input, t_{ap} can be set to one of two values. With ICs that do not terminate access pauses in this way, t_{ap} is virtually infinity.
- By forcing HOLD/APO LOW (e.g. with an external tone recognizer).

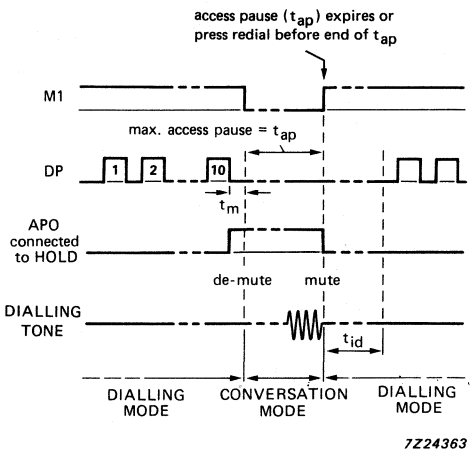
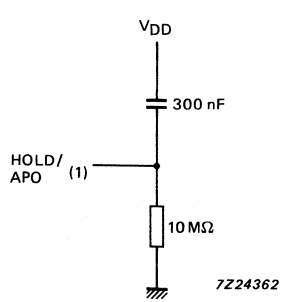


Fig.10 Timing diagram showing access pause reset.

For types with automatic reset of the access pause it is possible to lengthen the access pulse duration with external components (see Fig.11).



(1) $\Delta t_{ap} \approx 2$ s.

Fig.11 External circuit required to lengthen the access pause for ICs with automatic reset of the access pause.

FAMILY RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage		V_{DD}	−0.5	8.0	V
Voltage on any pin		V_I	V_{SS}−0.3	V_{DD} + 0.3	V
Operating ambient temperature range		T_{amb}	−25	+ 70	°C
Storage temperature ramge		T_{stg}	−55	+ 125	°C

FAMILY CHARACTERISTICS

V_{DD} = 3 V; V_{SS} = 0 V; crystal parameters f_{osc} = 3.58 MHz and R_{Smax} = 100 Ω (note 3); T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Operating supply voltage	T_{amb} = −25 to + 70 °C	V_{DD}	2.0	3.0	6.0	V
Standby supply voltage (note 1)	T_{amb} = −25 to + 70 °C	V_{DDO}	1.5	–	6.0	V
Operating supply current	CE = V_{DD}; notes 2 and 3	I_{DD}	–	60	120	μA
	V_{DD} = 6 V; CE = V_{DD}; notes 2 and 3	I_{DD}	–	200	400	μA
Standby supply current	CE = V_{SS}; note 2	I_{DDO}	–	0.65	2.0	μA
	V_{DD} = 1.8 V; T_{amb} = −25 to + 70 °C	I_{DDO}	–	–	2	μA
Input voltage LOW	1.8 V ≤ V_{DD} ≤ 6 V	V_{IL}	–	–	0.3 x V_{DD}	V
Input voltage HIGH	1.8 V ≤ V_{DD} ≤ 6 V	V_{IH}	0.7 x V_{DD}	–	–	V
CE input leakage current LOW	CE = V_{SS}	$-I_{IL}$	–	–	50	nA
HIGH	CE = V_{DD}	I_{IH}	–	–	50	nA
M/S pull-up input current	V_I = V_{SS}	$-I_{IL}$	30	100	300	nA
F01, F02, HOLD/APO APD pull-down input current	V_I = V_{DD}	I_{IH}	30	100	300	nA
Matrix keyboard operation						
Keyboard current	Cn connected to Rn; CE = HIGH	I_K	–	30	–	μA
Keyboard 'ON' resistance	contact 'ON'; note 4	R_{KON}	–	–	2	kΩ
Keyboard 'OFF' resistance	contact 'OFF'; note 4	R_{KOFF}	1	–	–	MΩ

DEVELOPMENT DATA

FAMILY CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Matrix keyboard operation (continued)						
Outputs R_1 to R_4						
sink current		I_O	–	3	–	mA
source current		$-I_O$	–	40	–	μA
Outputs M1, $\overline{M1}$, M2, M3, DP						
sink current	V_{OL} = 0.5 V	I_{OL}	0.7	2.0	4.0	mA
source current	V_{OH} = 2.5 V	$-I_{OH}$	0.65	1.8	3.6	mA
Outputs HOLD/APO						
source current	V_{OH} = 2.5 V	$-I_{OH}$	0.7	2.0	4.0	mA

Notes to family characteristics

1. V_{DDO} = 1.5 V only for redial.
2. All other inputs and outputs open.
3. Stray capacitance between OSC IN and OSC OUT pins < 3 pF.
4. Guarantees correct keyboard operation.

FAMILY TIMING DATA

V_{DD} = 3 V; V_{SS} = 0 V; f_{osc} = 3.58 MHz

parameter	conditions	symbol	min.	typ.	max.	unit
Clock start-up time	CE: from V_{SS} to V_{DD} note 1	t_{on}	–	4	–	ms

Note to family timing data

1. Stray capacitance between OSC IN and OSC OUT < 3 pF.

FAMILY CURVES

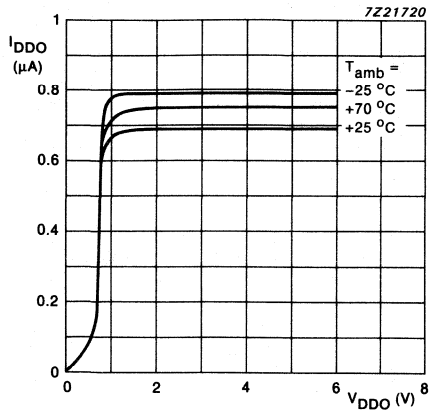


Fig.12 Standby supply current as a function of standby supply voltage.

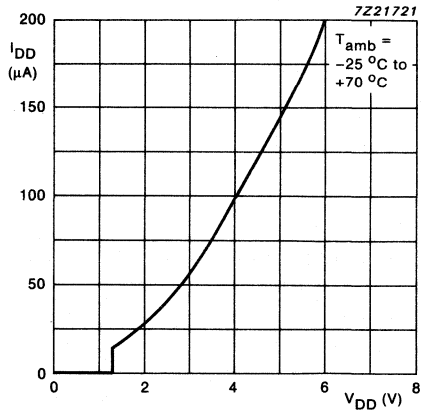


Fig.13 Operating supply as a function of operating supply voltage.

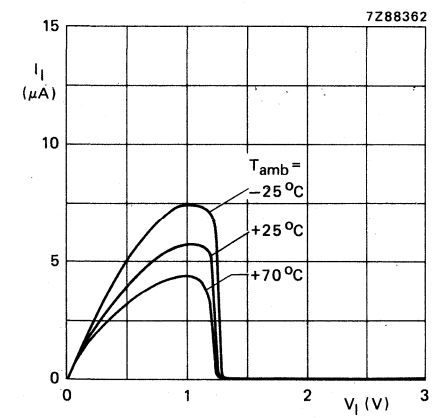


Fig.14 Pull-down input current as a function of input voltage; V_{DD} = 3 V.

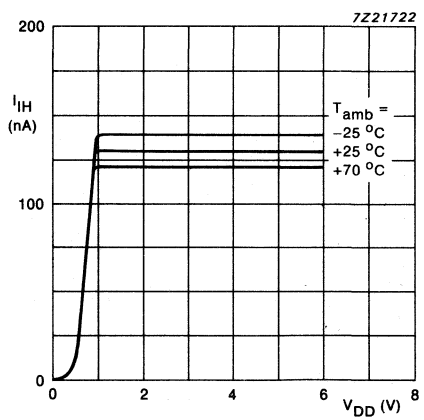


Fig.15 Pull-down input current as a function of supply voltage, $V_I = V_{DD}$.

DEVELOPMENT DATA

FAMILY CURVES (continued)

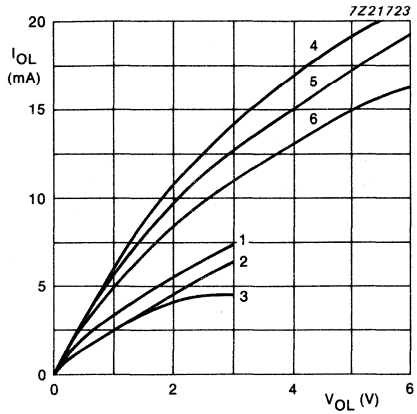


Fig.16 Output (N-channel) sink characteristics for M1, $\overline{M1}$, M2, M3 and DP.

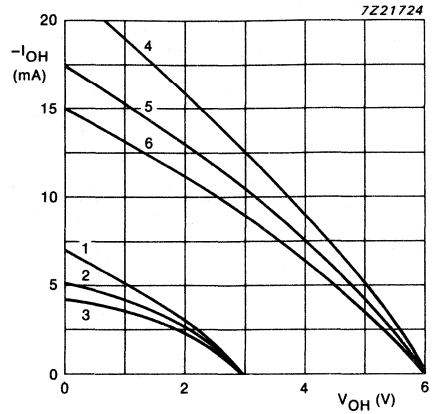


Fig.17 Output (P-channel) source characteristics for M1, $\overline{M1}$, M2, M3 and DP.

Key to Figs 16 and 17

T_{amb}	V_{DD} = 3 V	V_{DD} = 6 V
−25 °C	curve 1	curve 4
+25 °C	curve 2	curve 5
+70 °C	curve 3	curve 6

CHARACTERISTICS PER TYPE

PCD3320C specification

Inputs that are not available are defined internally as follows:
F02 = APD = LOW and M/S = HIGH

Outputs not available are M2 and APO.

Features additional to the common family specification are:

$\overline{M1}$	inverted mute output
M3	AND-function of mute (M1) and inverted dialling pulse (DP) outputs
HOLD	input that interrupts dialling

Redial of the last entered number is possible up to 23 digits; access pauses are not generated. Mark/space ratio is 3:2.

Using the F01 input it is possible to select either normal mode (F01 = LOW) or test mode (F01 = HIGH). In the test mode the oscillator input (OSC IN) must be driven by an external clock signal. The clock frequency of the circuit will be half the external clock frequency.

PCD3320C timing data

V_{DD} = 2.0 to 6 V; V_{SS} = 0 V; f_{osc} = 3.58 MHz

parameter	conditions	symbol	F01 = LOW (dialling)	unit
Dialling pulse frequency	note 1	f_{DP}	10.13	Hz
Dialling pulse period; $1/f_{DP}$	see Fig. 6 and 7	T_{DP}	98.7	ms
Clock pulse frequency; $30 \times f_{DP}$		f_{CLK}	303.9	Hz
Break time; $3/5 \times T_{DP}$	see Fig. 6	t_b	59.2	ms
Make time; $2/5 \times T_{DP}$	see Fig. 6	t_m	39.5	ms
Inter-digit pause; $8 \times T_{DP}$	see Figs 6 and 7	t_{id}	790	ms
Reset delay time; $1.6 \times T_{DP}$	see Figs 5, 6 and 7	t_{rd}	158	ms
Prepulse duration; $1/3 \times T_{DP}$	see Figs 6 and 7	t_d	33	ms
Debounce time;				
min. $5/30 \times T_{DP}$	see Fig. 5	$t_{e\,min}$	16.45	ms
max. $6/30 \times T_{DP}$	see Fig. 5	$t_{e\,max}$	19.74	ms
Initial data entry time (typ.); $t_{on} + t_e$		t_i	22	ms

Note to the PCD3320C timing data

1. f_{DP} is 10 Hz when a 3.5328 MHz crystal is used.

DEVELOPMENT DATA

CHARACTERISTICS PER TYPE (continued)

PCD3321C specification

The PCD3321C is pin-compatible with the DF320 and MT4320 types. It includes additional features that make it ideal for Private Automatic Branch Exchange (PABX) systems. Two access pauses can be stored automatically during the original entry of a number, or several made via the keyboard. The circuit regenerates access pauses during redial. A regenerated access pause can be terminated during redial either automatically after a built-in delay, via the keyboard or with an external dial tone recognizer.

Inputs that are not available are defined internally as follows:

APD = LOW

Outputs not available are $\overline{M1}$, M2 and M3.

Features additional to the common family specification are:

F01 + F02 — inputs giving selection between one of the three dialling speeds or the test speed. In the test mode the oscillator input (OSC IN) must be driven by an external clock signal. The clock frequency of the circuit will be half the external clock frequency.

HOLD/APO — input/output: input interrupts dialling; output is HIGH during access pauses (HOLD and APO are internally connected)

M/S — input for M/S ratio selection to 3:2 or 2:1

PCD3321C timing data

V_{DD} = 2.0 to 6 V; V_{SS} = 0 V; f_{osc} = 3.579545 MHz

parameter	conditions	symbol	FO1: LOW FO2: LOW	HIGH HIGH	LOW HIGH	unit
Dialling pulse frequency; $1/T_{DP}$	note 1	f_{DP}	10.13	15.54	19.42	Hz
Dialling pulse period; $1/f_{DP}$		T_{DP}	98.7	64.4	51.5	ms
Clock pulse frequency; 30 x f_{DP}		f_{CL}	303.9	466.1	582.6	Hz
Break time; 3/5 x T_{DP}	M/S = HIGH or n.c.; notes 2 and 3	t_b	59.2	38.6	30.9	ms
Make time; 2/5 x T_{DP}	M/S = HIGH or n.c.; notes 2 and 3	t_m	39.5	25.8	20.6	ms
Break time; 2/3 x T_{DP}	M/S = LOW note 4	t_b	65.8	42.9	34.3	ms
Make time; 1/3 x T_{DP}	M/S = LOW note 4	t_m	32.9	21.5	17.2	ms
Inter-digit pause; 8 x T_{DP}		t_{id}	790	515	412	ms
Reset delay time; 1.6 x T_{DP}		t_{rd}	158	103	82.4	ms
Access pause time; 32 x T_{DP}-t_m-$1/f_{CL}$		t_{ap}	3.12	2.03	1.63	s

parameter	conditions	symbol	FO1: LOW FO2: LOW	HIGH HIGH	LOW HIGH	unit
Prepulse duration; 1/3 x T_{DP}		t_d	33.0	21.5	17.2	ms
Debounce time; min. 5/30 x T_{DP}		$t_{e\ min}$	16.45	10.70	8.58	ms
max. 6/30 x T_{DP}		$t_{e\ max}$	19.74	12.88	10.30	ms
Initial data time (typ.); $t_{on} + t_e$		t_i	22.0	16.0	13.5	ms

Notes to the PCD3321C timing data

1. f_{DP} is 10 Hz when a 3.5328 MHz crystal is used.
2. In the n.c. (not connected) condition, the input is drawn to the HIGH state by internal pull-up current.
3. Mark/space ratio = 3:2.
4. Mark/space ratio = 2:1.

DEVELOPMENT DATA

CHARACTERISTICS PER TYPE (continued)

PCD3322C specification

Inputs that are not available are defined internally as follows:

F02 = APD = LOW and M/S = HIGH

Outputs not available are M3 and APO.

Features additional to the common family specification are:

$\overline{M1}$	inverted mute output
M2	strobe; HIGH during pulsing of a digit, LOW during an inter-digit pause
HOLD	input that interrupts dialling

Redial of the last entered number is possible up to 23 digits; access pauses are not generated. Mark/space ratio is 3:2.

Using the F01 input it is possible to select either normal mode (F01 = LOW) or test mode (F01 = HIGH). In the test mode the oscillator input (OSC IN) must be driven by an external clock signal. The clock frequency of the circuit will be half the external clock frequency.

PCD3322C timing data

V_{DD} = 2.0 to 6 V; V_{SS} = 0 V; f_{osc} = 3.58 MHz

parameter	conditions	symbol	FO1 = LOW (dialling)	unit
Dialling pulse frequency	note 1	f_{DP}	10.13	Hz
Dialling pulse period; $1/f_{DP}$	see Figs 6 and 7	T_{DP}	98.7	ms
Clock pulse frequency; 30 x f_{DP}		f_{CLK}	303.9	Hz
Break time; 3/5 x T_{DP}	see Fig.6	t_b	59.2	ms
Make time; 2/5 x T_{DP}	see Fig. 6	t_m	39.5	ms
Inter-digit pause; 8 x T_{DP}	see Figs 6 and 7	t_{id}	790	ms
Reset delay time; 1.6 x T_{DP}	see Figs 5,6 and 7	t_{rd}	158	ms
Prepulse duration; 1/3 x T_{DP}	see Figs 6 and 7	t_d	33	ms
Debounce time;				
min. 5/30 x T_{DP}	see Fig. 5	$t_{e\ min}$	16.45	ms
max. 6/30 x T_{DP}	see Fig. 5	$t_{e\ max}$	19.74	ms
Initial data entry time (typ.); $t_{on} + t_e$		t_i	22	ms

Note to the PCD3322C timing data

1. f_{DP} is 10 Hz when a 3.5328 MHz crystal is used.

PCD3324C specification

The PCD3324C is pin-compatible with the DF320 and MT4320 types. It includes additional features that make it ideal for PABX systems. One access pause can be stored automatically during the original entry of a number, or several made via the keyboard. The circuit regenerates access pauses during redial. A regenerated access pause can be terminated during redial either automatically after a built-in delay, via the keyboard or with an external dial tone recognizer.

Inputs that are not available are internally defined as follows:

APD = LOW

Outputs not available are $\overline{M1}$, M2 and M3.

Features additional to the common family specification are:

F01 + F02	inputs giving selection between one of the three dialling speeds or the test speed. In the test mode the oscillator input (OSC IN) must be driven by an external clock signal. The clock frequency of the circuit will be half the external clock frequency.
HOLD/APO	input/output: input interrupts dialling; output is HIGH during access pauses (HOLD and APO are internally connected)
M/S	input for M/S ratio selection to 3:2 or 2:1.

CHARACTERISTICS PER TYPE (continued)

PCD3324C timing data

V_{DD} = 2.0 to 6 V; V_{SS} = 0 V; f_{osc} = 3.579545 MHz

parameter	conditions	symbol	FO1: LOW FO2: LOW	HIGH HIGH	LOW HIGH	unit
Dialling pulse frequency $1/T_{DP}$	note 1	f_{DP}	10.13	15.54	19.42	Hz
Dialling pulse period: $1/f_{DP}$		T_{DP}	98.7	64.4	51.5	ms
Clock pulse frequency; 30 x f_{DP}		f_{CLK}	303.9	466.1	582.6	Hz
Break time; 3/5 x T_{DP}	M/S = HIGH or n.c.; notes 2 and 3	t_b	59.2	38.6	30.9	ms
Make time; 2/5 x T_{DP}	M/S = HIGH or n.c.; notes 2 and 3	t_m	39.5	25.8	20.6	ms
Break time; 2/3 x T_{DP}	M/S = LOW note 4	t_b	65.8	42.9	34.3	ms
Make time; 1/3 x T_{DP}	M/S = LOW note 4	t_m	32.9	21.5	17.2	ms
Inter-digit pause; 8 x T_{DP}		t_{id}	790	515	412	ms
Reset delay time ; 1.6 x T_{DP}		t_{rd}	158	103	82.4	ms
Access pause time; 32 T_{DP}-t_m-$1/f_{CL}$		t_{ap}	3.12	2.03	1.63	s
Prepulse duration; 1/3 x T_{DP}		t_d	33.0	21.5	17.2	ms
Debounce time; min. 5/30 x T_{DP}		$t_{e\,min}$	16.45	10.70	8.58	ms
max. 6/30 x T_{DP}		$t_{e\,max}$	19.74	12.88	10.30	ms
Initial data entry time (typ.) t_{on} + t_e		t_i	22.0	16.0	13.5	ms

Notes to the PCD3324C timing data

1. f_{DP} is 10 Hz when a 3.5328 MHz crystal is used.
2. In the n.c. (not connected) condition, the input is drawn to the HIGH state by the internal pull-up current.
3. Mark/space ratio = 3:2.
4. Mark/space ratio = 2:1.

PCD3325C specification

The PCD3325C is pin-compatible with the DF320 and MT4320 types. It includes additional features that make it ideal for PABX systems. Access pauses can be stored via the keyboard during the original entry of a number (there is no automatic storage of access pauses). The circuit regenerates access pauses during redial. A regenerated access pause can be terminated during redial either via the keyboard or with an external dial tone recognizer.

Inputs that are not available are defined internally as follows:

APD = LOW

Outputs not available are $\overline{M1}$, M2 and M3.

Features additional to the common family specification are:

F01 + F02	inputs giving selection between one of the three dialling speeds or the test speed. In the test mode the oscillator input (OSC IN) must be driven by an external clock signal. The clock frequency of the circuit will be half the external clock frequency.
HOLD/APO	input/output: input interrupts dialling; output is HIGH during access pauses (HOLD and APO are internally connected).
M/S	input for M/S ratio selection to 3:2 or 2:1.

CHARACTERISTICS PER TYPE (continued)

PCD3325C timing data

V_{DD} = 2.0 to 6 V; V_{SS} = 0 V; f_{osc} = 3.579545 MHz

parameter	conditions	symbol	FO1: LOW FO2: LOW	HIGH HIGH	LOW HIGH	unit
Dialling pulse frequency; $1/T_{DP}$	note 1	f_{DP}	10.13	15.54	19.42	Hz
Dialling pulse perid; $1/f_{DP}$		T_{DP}	98.7	64.4	51.5	ms
Clock pulse frequency; 30 x f_{DP}		f_{CLK}	303.9	466.1	582.6	Hz
Break time; 3/5 x T_{DP}	M/S = HIGH or n.c.; notes 2 and 3	t_b	59.2	38.6	30.9	ms
Make time; 2/5 x T_{DP}	M/S = HIGH or n.c.; notes 2 and 3	t_m	39.5	25.8	20.6	ms
Break time; 2/3 x T_{DP}	M/S = LOW note 4	t_b	65.8	42.9	34.3	ms
Make time; 1/3 x T_{DP}	M/S = LOW note 4	t_m	32.9	21.5	17.2	ms
Inter-digit pause; 8 x T_{DP}		t_{id}	790	515	412	ms
Reset delay time; 1.6 x T_{DP}		t_{rd}	158	103	82.4	ms
Prepulse duration; 1/3 x T_{DP}		t_d	33.0	21.5	17.2	ms
Debounce time min. 5/30 x T_{DP}		t_e min	16.45	10.70	8.58	ms
max. 6/30 x T_{DP}		t_e max	19.74	12.88	10.30	ms
Initial data entry time (typ.); $t_{on} + t_e$		t_i	22.0	16.0	13.5	ms

Notes to the PCD3325C timing data

1. f_{DP} is 10 Hz when a 3.5328 MHz crystal is used.
2. In the n.c. (not connected) condition, the input is drawn to the HIGH state by the internal pull-up current.
3. Mark/space ratio = 3:2.
4. Mark/space ratio = 2:1.

PCD3326C specification

The PCD3326C includes many additional features that make it ideal for PABX systems. Two access pauses can be stored automatically during the original entry of a number, or several stored via the keyboard. The circuit regenerates access pauses during redial. A regenerated access pause can be terminated during redial either automatically after a built-in delay, via the keyboard or with an external dial tone recognizer.

Inputs that are not available are internally defined as follows:

M/S = HIGH

Outputs not available are $\overline{M1}$, M2 and M3.

Features additional to the common family specification are:

F01 + F02	inputs giving selection between one of the three dialling speeds or the test speed. In the test mode the oscillator input (OSC IN) must be driven by an external clock signal. The clock frequency of the circuit will be half the external clock frequency.
HOLD/APO	input/output: input interrupts dialling; output is HIGH during access pauses (HOLD and APO are internally connected)
APD	input for selecting access pause duration.

CHARACTERISTICS PER TYPE (continued)

PCD3326C timing data

V_{DD} = 2.0 to 6 V; V_{SS} = 0 V; f_{osc} = 3.579545 MHz

parameter	conditions	symbol	FO1: LOW FO2: LOW	HIGH HIGH	LOW HIGH	unit
Dialling pulse frequency; $1/T_{DP}$	note 1	f_{DP}	10.13	15.54	19.42	Hz
Dialling pulse period; $1/f_{DP}$		T_{DP}	98.7	64.4	51.5	ms
Clock pulse frequency; 30 x f_{DP}		f_{CLK}	303.9	466.1	582.6	Hz
Break time; 3/5 x T_{DP}	note 2	t_b	59.2	38.6	30.9	ms
Make time; 2/5 x T_{DP}	note 2	t_m	39.5	25.8	20.6	ms
Inter-digit pause; 8 x T_{DP}		t_{id}	790	515	412	ms
Reset delay time; 1.6 x T_{DP}		t_{rd}	158	103	82.4	ms
Access pause time	APD = LOW;					
32 x T_{DP}-t_m-$1/f_{CL}$	or n.c.; note 3	t_{ap}	3.12	2.03	1.63	s
64 x T_{DP}-t_m-$1/f_{CL}$	APD = HIGH	t_{ap}	6.28	4.09	3.28	s
Prepulse duration; 1/3 x T_{DP}		t_d	33.0	21.5	17.2	ms
Debounce time;						
min. 5/30 x T_{DP}		$t_{e\ min}$	16.45	10.70	8.58	ms
max. 6/30 x T_{DP}		$t_{e\ max}$	19.74	12.88	10.33	ms
Initial data entry time (typ.); $t_{on} + t_e$		t_i	22.0	16.0	13.5	ms

Notes to the PCD3326C timing data

1. f_{DP} is 10 Hz when a 3.5328 MHz crystal is used.
2. Mark/space ratio = 3:2.
3. In the n.c. (not connected) condition, the input is drawn to the LOW state by the internal pull-down current.

PCD3327C specification

The PCD3327C contains an oscillator with sufficient gain to provide oscillation when using an inexpensive 455 kHz ceramic resonator. Two additional capacitors are required as shown in Fig.18. Alternatively, the OSC IN pin may be driven from an external 455 kHz clock signal.

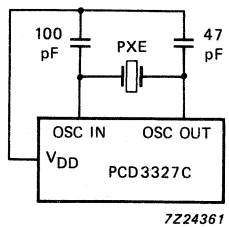


Fig.18 PCF3327 oscillator circuit.

This IC is pin-compatible with the DF320 and MT4320 types and includes additional features that make it ideal for PABX systems. The circuit allows several access pauses to be stored via the keyboard and regenerates the access pauses during redial. A regenerated access pause can be terminated during redial either automatically after a built-in delay, via the keyboard or with an external dial tone recognizer.

Inputs that are not available are internally defined as follows:

APD = LOW

Outputs not available are $\overline{M1}$, M2 and M3.

Features additional to the common family specification are:

F01 + F02	inputs giving selection between one of the three dialling speeds or the test speed. In the test mode the oscillator input (OSC IN) must be driven by an external clock signal. The clock frequency of the circuit will be half the external clock frequency.
HOLD/APO	input/output: input interrupts dialling; output is HIGH during access pauses (HOLD and APO are internally connected).
M/S	input for M/S ratio selection to 3:2 or 2:1.

DEVELOPMENT DATA

CHARACTERISTICS PER TYPE (continued)

PCD3327C timing data

V_{DD} = 2.0 to 6 V; V_{SS} = 0 V; f_{osc} = 455 kHz

parameter	conditions	symbol	FO1: LOW FO2: LOW	HIGH HIGH	LOW HIGH	unit
Dialling pulse frequency; $1/T_{DP}$	note 1	f_{DP}	10.3	15.8	19.7	Hz
Dialling pulse period; $1/f_{DP}$		T_{DP}	97	63	51	ms
Clock pulse frequency; 30 x f_{DP}		f_{CLK}	309	474	592	Hz
Break time; 3/5 x T_{DP}	M/S = HIGH or n.c.; notes 2 and 3	t_b	58	38	30	ms
Make time; 2/5 x T_{DP}	M/S = HIGH or n.c.; notes 2 and 3	t_m	39	25	20	ms
Break time; 2/3 x T_{DP}	M/S = LOW note 4	t_b	65	42	34	ms
Make time; 1/3 x T_{DP}	M/S = LOW note 4	t_m	32	21	17	ms
Inter-digit pause; 8 x T_{DP}		t_{id}	776	506	405	ms
Reset delay time; 1.6 x T_{DP}		t_{rd}	155	101	81	ms
Access pause time; 32 x T_{DP}-t_m-$1/f_{CL}$		t_{ap}	3.12	2.03	1.63	s
Prepulse duration; 1/3 x T_{DP}		t_d	32	21	17	ms
Debounce time; min. 5/30 x T_{DP}		$t_{e\ min}$	16.18	10.54	8.45	ms
max. 6/30 x T_{DP}		$t_{e\ max}$	19.41	12.66	10.13	ms
Initial data entry time (typ.); $t_{on} + t_e$		t_i	22.0	16.0	13.5	ms

Notes to the PCD3327C timing data

1. f_{DP} is 10 Hz when a 441.6 PXE ceramic resonator is used.
2. In the n.c. (not connected) condition, the input is drawn to the HIGH state by the internal pull-up current.
3. Mark/space ratio = 3:2.
4. Mark/space ratio = 2:1.

Multistandard repertory dialler/ringer with EEPROM

PCD3330-1

FEATURES

Pulse/DTMF dialling

- Pulse dialling
- DTMF dialling
- Mixed mode dialling
- Number of digits per call is infinite (FIFO register)
- Flash or register recall
- Connect a/b to Earth function
- Mute functions
- Disconnect function
- Standard 4 x 4 keyboard for: 0 to 9 and *, #, A, B, C and D
- Function keys for: Flash, Hook, Mute, Tone and Disconnect
- On-hook dialling control
- Country specifications which can be stored in EEPROM are:
  Will * and/or # be transmitted when switching over to DTMF dialling mode
  Mark-to-space ratio (3 : 2 or 2 : 1)
  6 Tone time selections (60/90, 70/70, 80/80, 100/100, 100/140 or 140/140 ms)
  4 Flash time selections (100, 115, 270 or 600 ms)
  Mute output type selection (M1, $\overline{M1}$, M2 or $\overline{M2}$)
  DTMF keys or Function keys selection
- On-chip voltage reference for stabilized supply and temperature independent tone output
- On-chip filtering for low output distortion (CEPT CS 203 compatible)

Number storage

- Redial Cursor method (maximum 24 digits) stored in internal EEPROM
- Storage for 13 repertory dial numbers (16 digits each) or 10 repertory dial numbers (20 digits each) in internal EEPROM
- Access pause generation and termination: manually or by Atlanta procedure
- Function keys for: LNR, Memory recall, Store, Access Pause and 1 key repertory
- Country specifications which can be stored in EEPROM are:
  Access pause time selection (1.5/1.0, 2.5/1.5, 3.0/3.5 or 6.0/6.0 s)
  10 Number repertory dialler selection (1 or 2 key)
  Two repertory number programming procedures (General or Germany)
  Repertory length (16 or 20 digits)

Ringer

- Ringer input frequency detection
- Function key for: Program Ringer
- Three-tone ringer with 4 different ringer frequencies
- Ringer melody generation with four signal speeds and four output volume steps, keypad controlled
- Country specifications which can be stored in EEPROM are:
  Ringer input frequency detection selection
  Ringer output selection (via DTMF or special RTO output)
  4 possible ringer melodies
  4 possible ringer repetition rates
  4 possible ringer volumes

General

- On-chip oscillator uses low-cost 3.58 MHz (TV colour burst) crystal or PXE resonator
- On-chip power-on reset (typically 2.0 V)
- Supply voltage range 1.8 to 6.0 V (2.5 to 6.0 V in EEPROM erase/write and DTMF and ringer mode)

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCD3330-1P	28	DIL	plastic	SOT117
PCD3330-1T	28	mini-pack	plastic	SO28; SOT136A

Multistandard repertory dialler/ringer with EEPROM

PCD3330-1

GENERAL DESCRIPTION

The PCD3330-1 is a mixed-mode multistandard repertory dialler/ringer IC frabricated in a low threshold voltage CMOS technology and is a member of the Philips family of telecommunication ICs.

The (maximum 13) repertory numbers, redial and various country specifications are stored in EEPROM so that memory retention is guaranteed for 10 years without using a battery back-up.
Therefore, different models can be created by changing the contents of some EEPROM bytes.

The various country specifications can be fulfilled by changing a few bytes in EEPROM which contain the different telephone timing and dialling procedures.

The two on-chip tone generators are used for Dual Tone Multi-Frequency (DTMF) dialling, and for generating a melody during ringing, which is activated when a correct incoming ringer frequency is detected.

As an output transducer for the ringer, a loudspeaker (ringer out via tone output) or a PXE (ringer out via the special ringer output which generates square wave ringer tones with a peak-to-peak voltage of V_{DD} to V_{SS}) can be used.

The operating supply voltage is 1.8 V (2.5 V in EEPROM erase/write and DTMF and ringer mode) to 6.0 V with a low current consumption in all operating modes: standby, conversation, dialling, programming and ringer.

Multistandard repertory dialler/ringer with EEPROM

PCD3330-1

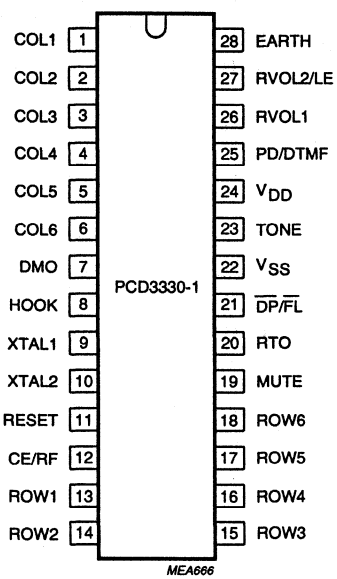


Fig.1 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
COL1	1	sense column keyboard input/programming EEPROM
COL2	2	sense column keyboard input/programming EEPROM
COL3	3	sense column keyboard input/programming EEPROM
COL4	4	sense column keyboard input/programming EEPROM
COL5	5	sense column keyboard input
COL6	6	sense column keyboard input
DMO	7	dial mode output
HOOK	8	cradle contact input
XTAL1	9	crystal/PXE oscillator input
XTAL2	10	crystal/PXE oscillator output
RESET	11	reset input
CE/RF	12	chip enable and zero crossing for ringer input
ROW1	13	scanning row keyboard output
ROW2	14	scanning row keyboard output
ROW3	15	scanning row keyboard output
ROW4	16	scanning row keyboard output
ROW5	17	scanning row keyboard output
ROW6	18	scanning row keyboard output
MUTE	19	mute output
RTO	20	ringer melody output
$\overline{DP}/\overline{FL}$	21	dial pulse/flash inverted output
V_{SS}	22	negative supply
TONE	23	DTMF tones or ringer melody output
V_{DD}	24	positive supply
PD/DTMF	25	pulse/DTMF dial selection
RVOL1	26	ringer volume output 1
RVOL2/LSE	27	ringer volume output 2/loudspeaker enable output
EARTH	28	earth output

Multistandard pulse/tone dialler/ringer

PCD3331-1

FEATURES

- Pulse and DTMF mixed mode dialling
- Last number redial up to 24 digits
- Flash and Earth register recall
- Access pause generation and termination
- Function keys for: Recall, LNR/access pause and Tone
- Strap functions:
  Mark-to-space ratio (3 : 2 or 2 : 1)
  Tone burst times
  Access pause time
  Pulse or DTMF (fixed setting)
  Register recall Flash or Earth
- Ringer tone generation
- Ringer input frequency discriminator (23 to 54 Hz)
- Ringer sound selection via keypad

GENERAL DESCRIPTION

The PCD3331-1 is a mixed-mode multistandard dialler/ringer IC fabricated in a low threshold voltage CMOS technology and is a member of the Philips family of telecommunication ICs.

Dial parameters of this IC can be set by diode options to specific country requirements.

The on-chip tone generators are used for DTMF dialling and ringer melody generation.

A discriminator input enables the tone output only if a correct ringer frequency is applied.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCD3331-1P	20	DIL	plastic	SOT146
PCD3331-1T	20	mini-pack	plastic	SO20; SOT163A

Multistandard pulse/tone dialler/ringer

PCD3331-1

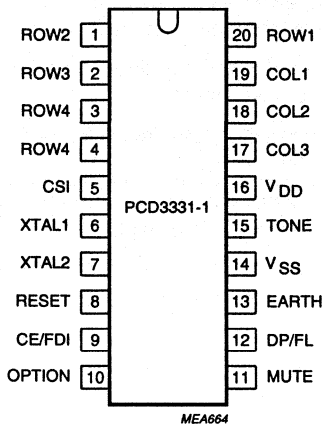


Fig.1 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
ROW2	1	row keyboard output
ROW3	2	row keyboard output
ROW4	3	row keyboard output
ROW5	4	row keyboard output
CSI	5	cradle detection input
XTAL1	6	oscillator input
XTAL2	7	oscillator output
RESET	8	reset input
CE/FDI	9	chip enable
OPTION	10	options selection
MUTE	11	mute output
DP/FL	12	pulse/recall output
EARTH	13	earth recall output
V_{SS}	14	negative supply
TONE	15	DTMF tones output
V_{DD}	16	positive supply
COL3	17	column keyboard input
COL2	18	column keyboard input
COL1	19	column keyboard input
ROW1	20	row keyboard output

Multistandard pulse/tone repertory dialler/ringer

PCD3332-1

FEATURES

- Pulse and DTMF mixed mode dialling
- 10 number repertory dial up to 32 digits
- Last number redial up to 32 digits
- Flash and Earth register recall
- Access pause generation and termination
- Function keys for: Program, Memory recall, Flash, LNR, pause and Tone
- Strap functions:
  Mark-to-space ratio (3 : 2 or 2 : 1)
  Tone burst times
  Access pause time
  Pulse or DTMF switch
  Register recall Flash or Earth
  Parcifier tones select
  Ringer frequency select
- Ringer tone generation
- Ringer input frequency discriminator (20 to 54 Hz)
- Ringer sound selection via keypad
- Memory monitor
- Parcifier tones

GENERAL DESCRIPTION

The PCD3332-1 is a mixed-mode multistandard repertory dialler/ringer IC fabricated in a low threshold voltage CMOS technology and is a member of the Philips family of telecommunication ICs.

Dial parameters of this IC can be set by diode options to specific country requirements.

The on-chip tone generators are used for DTMF dialling and ringer melody generation.

A discriminator input enables the tone output only if a correct ringer frequency is applied.

The memory contents of a repertory dial location can be up to 32 digits with a maximum total of 254 digits.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCD3332-1P	28	DIL	plastic	SOT117
PCD3332-1T	28	mini-pack	plastic	SO28; SOT136A

Multistandard pulse/tone repertory dialler/ringer

PCD3332-1

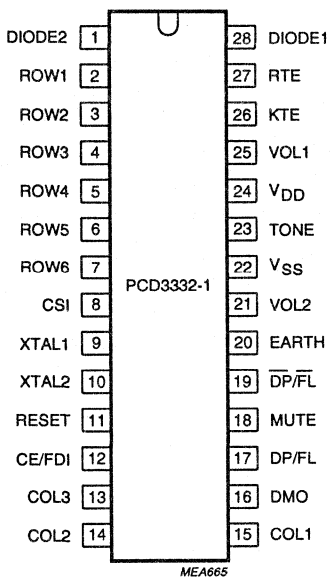


Fig.1 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
DIODE2	1	diode 2 option row
ROW1	2	row keyboard output
ROW2	3	row keyboard output
ROW3	4	row keyboard output
ROW4	5	row keyboard output
ROW5	6	row keyboard output
ROW6	7	row keyboard output
CSI	8	cradle switch input
XTAL1	9	oscillator input
XTAL2	10	oscillator output
RESET	11	reset input
CE/FDI	12	chip enable/frequency discriminator
COL3	13	column keyboard input
COL2	14	column keyboard input
COL1	15	column keyboard input
DMO	16	dial mode output
DP/FL	17	dial pulse/flash output
MUTE	18	mute output
$\overline{DP/FL}$	19	dial pulse/flash inverted
EARTH	20	earth recall output
VOL2	21	volume 2 output
V_{SS}	22	negative supply
TONE	23	tone generator output
V_{DD}	24	positive supply
VOL1	25	volume 1 output
KTE	26	key tone enable
RTE	27	ringer tone enable
DIODE1	28	diode 1 option row

Single-chip 8-bit Telecom Microcontroller

PCD3343A PCD3348A

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC14 OR DATA SHEET

FEATURES

- 8-bit CPU, ROM, RAM, I/O in a single 28-lead package
- 3 k ROM bytes, 224 RAM bytes (PCD3343A)
- 8 k ROM bytes, 256 RAM bytes (PCD3348A)
- Serial I/O interface with multi-master capability
- Over 100 instructions (based on MAB8048) all of 1 or 2 cycles
- 20 quasi-bidirectional I/O port lines
- 8-bit programmable timer/event counter 1 - 3 single-level vectored interrupts; external, 8-bit programmable timer/event counter 1, SIO/derivative
- Two test inputs, one of which also serves as the external interrupt input
- Power-on reset
- Stop and idle modes
- Logic supply from 1.8 V to 6 V
- Low standby voltage of 1 V
- Low standby current of 2 µA (typ.)
- Clock frequency from 1 MHz to 16 MHz
- Oscillator with output drive for peripherals (e.g. PCD3312 DTMF generator)
- Manufactured in silicon gate CMOS process

GENERAL DESCRIPTION

This data sheet details the specific properties of the PCD3343A and PCD3348A. The shared characteristics of the PCD33XXA family of microcontrollers are described in the PCD33XXA family data sheet, which should be read in conjunction with this publication.

The PCD3343A and PCD3348A are microcontrollers which have been designed primarily for Telecom applications. They provide 3 k and 8 k bytes of program memory and 224 and 256 bytes of RAM respectively. In addition to 20 I/O port lines, the microcontrollers provide an on-chip serial I/O interface. This two-line serial bus extends the microcontroller capabilities when implemented with the powerful I²C-bus devices of the PCF85xx, PCD33xx and "Clips" peripheral families. These include liquid crystal display drivers, pulse and/or DTMF diallers, ringers, AD/DA converters, clock/calendar circuits, EEPROM and RAM. The instruction set is based on that of the MAB8048 and is software compatible with the PCD33XXA family.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	positive supply voltage	–0.5	+7.0	V
V_I	all input voltages	–0.5	V_{DD} +0.5	V
I_I, I_O	DC input or output current	–10	+10	mA
I_{SS}	ground supply current	–50	+50	mA
P_{tot}	total power dissipation	–	125	mW
P_O	power dissipation per output	–	30	mW
T_{stg}	storage temperature range	–55	150	°C
T_j	operating junction temperature	–	90	°C

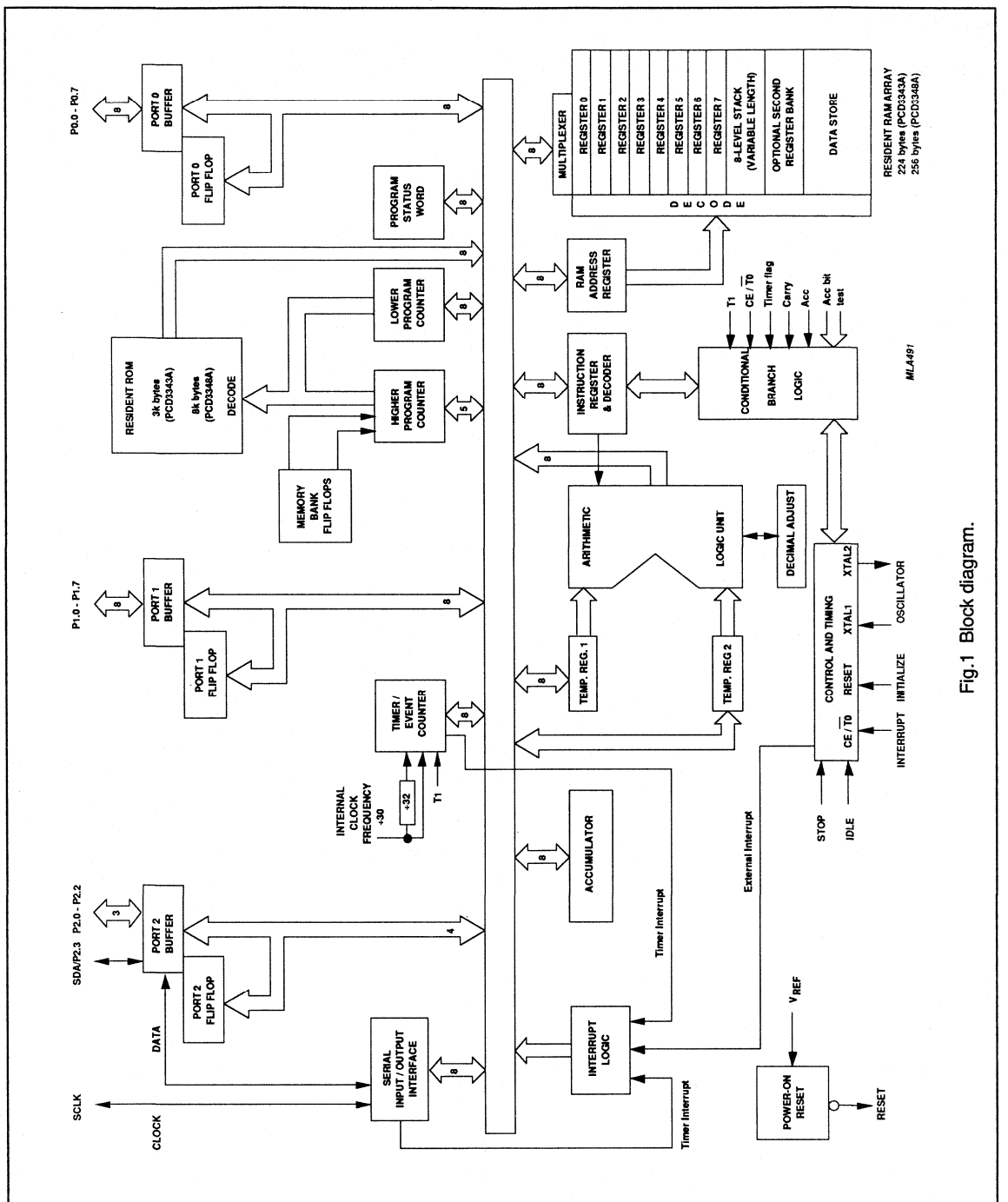


Fig.1 Block diagram.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCD3343AP/48AP	28	DIL	plastic	SOT117
PCD3343AT/48AT	28	mini-pack	plastic	SOT136A

Note to the Ordering Information

Full and up-to-date data for this device is available upon request via your Philips local sales office.

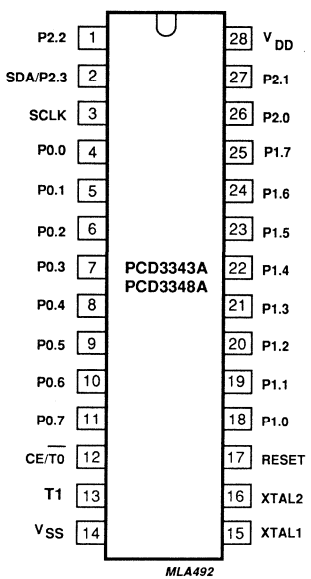


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	I/O	DESCRIPTION
P2.2	1	I/O	Port 2: quasi-bidirectional I/O lines
SDA/P2.3	2	I/O	bidirectional data line of the serial I/O interface / Port 2: quasi bidirectional I/O line
SCLK	3	I/O	bidirectional clock line of the serial I/O interface
P0.0-P0.7	4-11	I/O	Port 0: quasi-bidirectional I/O lines
CE/$\overline{T0}$	12	I	chip enable/test 0
T1	13	I	test 1/count input of 8-bit timer/event counter 1
V_{SS}	14	P	ground
XTAL1	15	I	crystal oscillator /external clock
XTAL2	16	O	crystal oscillator output
RESET	17	I	reset input
P1.0-P1.7	18-25	I/O	Port 1: quasi-bidirectional I/O lines
P2.0-P2.1	26-27	I/O	Port 2: quasi-bidirectional I/O lines
V_{DD}	28	P	positive supply voltage

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

Repertory pulse/DTMF dialler with redial PCD3344/004

FEATURES

- Display control via I²C-bus
- Redial
- Extended redial
- Number of digits per call is infinite (FIFO register)
- 20 repertory numbers (218 digits)
- 4 x 5 keyboard (function keys: program/autodial, flash, redial, tone, hold, access pause and shift)
- Keyboard extension for maximum 20 repertory numbers
- Special inputs: CE, RESET and access pause
- Special outputs: music-on-hold, MUTE and DP/FL
- Mark/space ratio 2:1 or 3:2
- Pulse dialling for 10 or 20 Hz
- DTMF tone/pause 70/70 or 100/100 ms
- Flash 100 or 650 ms
- Manual insertion of access pause
- Automatic insertion of access pause
- Access pause time for pulse dialling 3 or 5 s
- Access pause time for DTMF 1.5 or 2.5 s
- On-chip power-on reset
- 2.5 to 6.0 V operating supply voltage
- 3.58 MHz crystal oscillator.

GENERAL DESCRIPTION

The PCD3344/004 is a single-chip CMOS dialler IC for telephone sets. It has two dialling modes; pulse dialling (PD) and dual tone multi-frequency (DTMF). In addition to manual dialling it also features several automatic functions e.g. Redial, Extended redial, note pad and repertory dial.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCD3344P/004	28	DIL	plastic	SOT117
PCD3344T/004	28	SO28	plastic	SOT136A

Repertory pulse/DTMF dialler with redial and on-hook dialling

PCD3344/011

FEATURES

- On-hook dialling
- Redial
- Extended redial
- Number of digits per call is infinite (FIFO register)
- 10 or 20 repertory numbers of maximum 36 digits (total 240 digits)
- Electronic note pad
- 4 x 5 keyboard (function keys: store, flash, Last Number Redial (LNR), tone, hold, hook, access pause and shift)
- Keyboard extension for maximum 20 repertory numbers
- Eleven diode or strap functions:
  - mark-to-space ratio: 2:1 or 3:2 (only for 10 Hz)
  - flash time (100, 270, 540 or 650 ms)
  - dial frequency (10 or 20 Hz)
  - normal or direct dialling (emergency)
  - tone burst time (70/80 or 100/140 ms)
  - pulse dialling for Sweden
  - pulse dialling for Norway and New Zealand
  - dial mode: pulse or DTMF
  - flash entry store
  - key depressing/tone burst (instead of continuous tone)
  - access pause time (1.5/3 or 3/6 s)
- Special inputs: CE and RESET
- Special outputs: music-on-hold and MUTE
- Manual insertion of access pause
- Automatic insertion of access pause
- Access pause time for pulse dialling 3 or 6 s
- Access pause time for DTMF 1.5 or 2.5 s
- On-chip power-on reset
- 2.5 to 6.0 V operating supply voltage
- 3.58 MHz crystal oscillator.

GENERAL DESCRIPTION

The PCD3344/011 is a single-chip CMOS dialler IC for telephone sets with on-hook dialling and up to 20 number repertory dial facilities. It has an on-chip DTMF/melody generator including switch capacitor filters to provide low harmonic distortion, fulfilling the CEPT requirements. In addition to manual dialling it also features several automatic functions.
Described in PCALE Application Report "PCD3344/006".

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCD3344P/011	28	DIL	plastic	SOT117
PCD3344T/011	28	SO28	plastic	SOT136A

Repertory pulse/DTMF dialler with redial PCD3344/047

FEATURES

- Pulse and DTMF dialling
- Redial
- Automatic redial
- Number of digits per call is infinite (FIFO register)
- 13 repertory numbers of maximum 36 digits (total 282 digits)
- 4 x 5 keyboard (function keys: store, recall, Last Number Redial (LNR), data, access pause and, memory recall and reset)
- 3 direct accessible repertory numbers
- 10 two-touch accessible repertory numbers
- Recall/register recall
- Special inputs: CE and RESET
- Special outputs: MUTE, $\overline{\text{MUTE}}$, DIALMODE, $\overline{\text{DIALMODE}}$, DP/FL and MUTE2
- Access pause generation and termination
- Automatic recognition of PABX-digits (automatic pause insertion)
- Memory overflow indication
- Cursor method for Last Number Redial (LNR)
- Eight strap functions:
  - mark-to-space ratio: 2:1 or 3:2
  - 4 recall time selections (100, 270, 540 or 650 ms)
  - dial frequency (10 Hz, 20 Hz, Sweden or Norway/New Zealand)
  - 4 tone burst times (70/70, 70/100, 80/80 or 100/100)
  - interdigit pause (840 or 540 ms)
  - recall entry store (stored/not stored)
  - tone transmit length (key press time or burst)
  - access pause time (1/1.5, 1.5/2.5, 2/3.5 or 3.5/3 s)
- On-chip power-on reset
- Programmed for improved noise immunity
- 2.5 to 6.0 V operating supply voltage
- 3.58 MHz crystal oscillator.

GENERAL DESCRIPTION

The PCD3344/047 is a single-chip CMOS dialler IC for telephone sets. It has two dialling modes; pulse dialling (PD) and dual tone multi-frequency (DTMF). In addition to manual dialling it also features several automatic functions e.g. Redial, Extended redial, note pad and repertory dial. The dialler can be used in many countries (including the Swedish, Norwegian and New Zealand pulse dialling modes).

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCD3344P/047	28	DIL	plastic	SOT117
PCD3344T/047	28	SO28	plastic	SOT136A

Single-chip 8-bit Telecom Microcontroller

PCD3344A PCD3349A

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC14 OR DATA SHEET

FEATURES

- 8-bit CPU, ROM, RAM, I/O in a single 28-lead package
- 2 k ROM bytes (PCD3344A)
- 4 k ROM bytes (PCD3349A)
- 224 bytes RAM
- Over 100 instructions (based on MAB8048) all of 1 or 2 cycles
- 20 quasi-bidirectional I/O port lines
- 8-bit programmable timer/event counter 1
- Two single-level vectored interrupts: external, 8-bit programmable timer/event counter 1
- Two test inputs, one of which also serves as the external interrupt input
- DTMF tone generator
- Reference for supply and temperature-independent tone output
- Filtering for low output distortion (CEPT CS203 compatible)
- Power-on reset
- Stop and idle modes
- Logic supply from 1.8 V to 6 V (DTMF tone output from 2.5 V)
- Low standby voltage of 1 V
- Low standby current of 2 μA (typ.)
- Clock frequency from 1 MHz to 16 MHz (3.58 MHz for DTMF suggested)
- Manufactured in silicon gate CMOS process.

GENERAL DESCRIPTION

This data sheet details the specific properties of the PCD3344A and PCD3349A. The shared characteristics of the PCD33XXA family of microcontrollers are described in the PCD33XXA family data sheet, which should be read in conjunction with this publication.
The PCD3344A and PCD3349A are microcontrollers which have been designed primarily for Telecom applications. They include an on-chip dual tone multi-frequency (DTMF) generator. The PCD3344A and the PCD3349A provide 2 k and 4 k bytes respectively of program memory, 224 bytes of RAM and 20 I/O lines. The instruction set is based on that of the MAB8048 and is software compatible with the PCD33XXA family.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	positive supply voltage	−0.5	+7.0	V
V_I	all input voltages	−0.5	V_{DD}+0.5	V
I_I,I_O	DC input or output current	−10	+10	mA
I_{SS}	ground supply current	−50	+50	mA
P_{tot}	total power dissipation	−	125	mW
P_O	power dissipation per output	−	30	mW
T_{stg}	storage temperature range	−55	+150	°C
T_j	operating junction temperature	−	90	°C

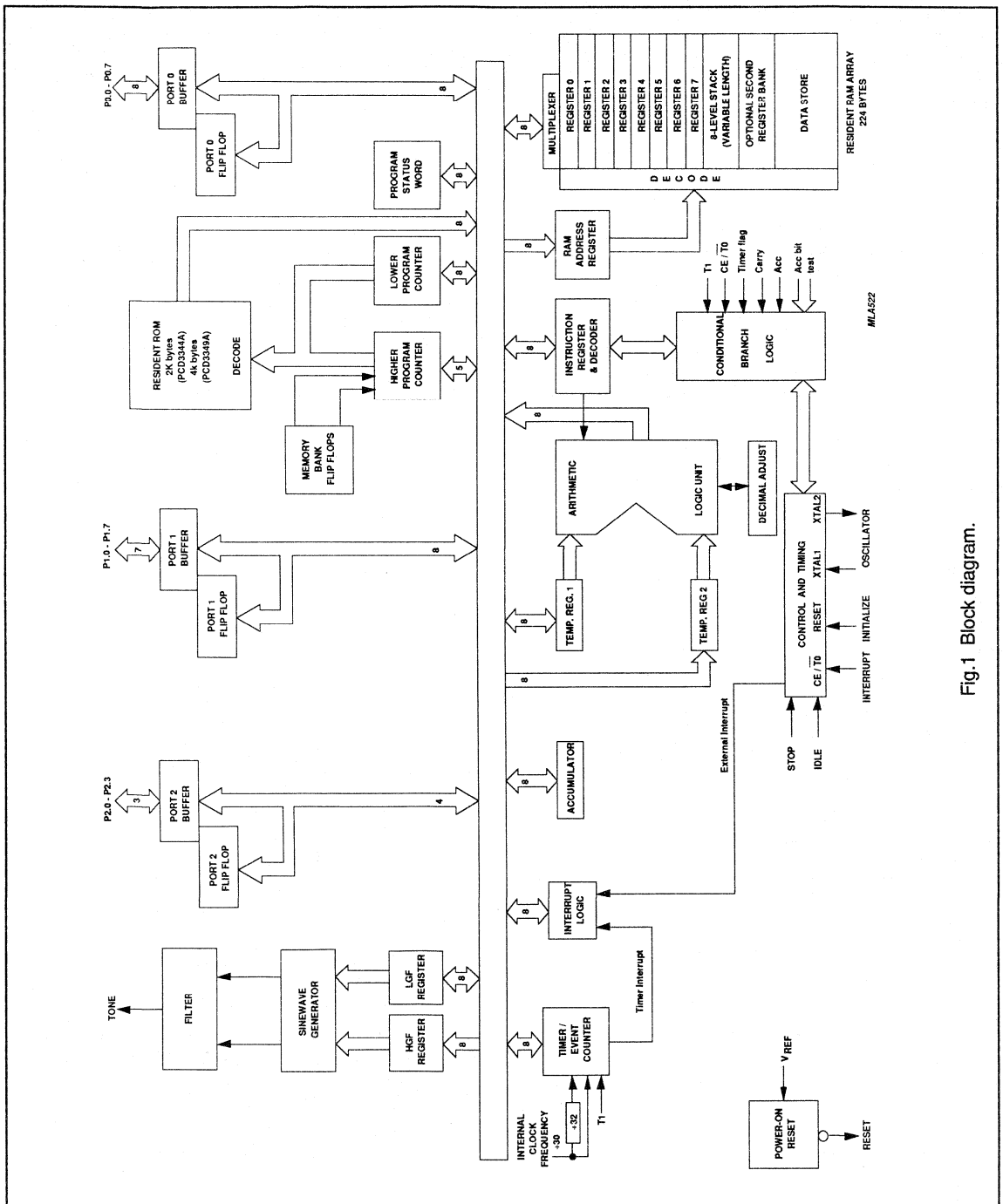


Fig.1 Block diagram.

Single-chip 8-bit Telecom Microcontroller

PCD3344A PCD3349A

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCD3344AP/49AP	28	DIL	plastic	SOT117
PCD3344AT/49AT	28	mini-pack	plastic	SOT136A

Note to the Ordering Information

Full and up-to-date data for this device is available upon request via your Philips local sales office.

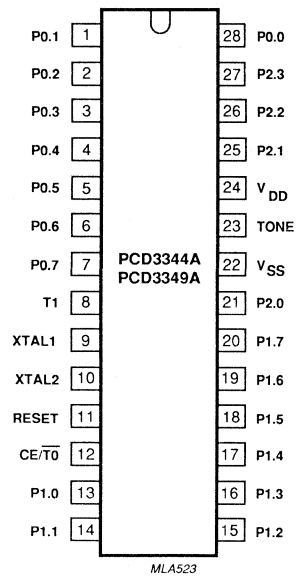


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	I/O	DESCRIPTION
P0.1-P0.7	1-7	I/O	Port 0: quasi-bidirectional I/O lines
T1	8	I	test 1/count input of 8-bit timer/event counter 1
XTAL1	9	I	crystal oscillator/ external clock input
XTAL2	10	O	crystal oscillator output
RESET	11	I	reset input
CE/$\overline{T0}$	12	I	chip enable / test 0
P1.0-P1.7	13-20	I/O	Port 1: quasi-bidirectional I/O line
P2.0	21	I/O	Port 2: quasi-bidirectional I/O line
V_{SS}	22	P	ground
TONE	23	O	DTMF output
V_{DD}	24	P	positive supply voltage
P2.1-P2.3	25-27	I/O	Port 2: quasi-bidirectional I/O lines
P0.0	28	I/O	Port 0: quasi-bidirectional I/O line

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC14 OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER

DESCRIPTION

The PCD3346 is a single-chip 8-bit microcontroller manufactured in CMOS technology. The PCD3346 is a member of the PCD33XX family and as such has special on-chip features for telephony applications.

The PCD3346 has 20 quasi-bidirectional I/O port lines, a serial I/O interface, a single-level vectored interrupt circuit, two 8-bit timer event counters and on-board clock oscillator and clock circuits. The PCD3346 also incorporates 256 bytes of EEPROM permitting intermediate data storage without the need for battery back-up.

The instruction set is based on that of the MAB8048 and is instruction set compatible with the MAB8400 family. The PCD3346 has bit handling abilities for both binary and BCD arithmetic.

Features

- 8-bit CPU, ROM, EEPROM, RAM, I/O in a single 28-lead DIL or SO package
- 4 K ROM bytes
- 128 RAM bytes
- 256 bytes EEPROM
- 20 quasi-bidirectional I/O port lines
- 2 x 8-bit programmable timers
- Two test inputs: one of which is also the external interrupt input (CE/$\overline{T0}$)
- Single-level vectored interrupts: external, timer/event counter, serial I/O and derivative port
- I^2C hardware interface for serial data transfer on two lines (serial I/O data via an existing port line and clock via a dedicated line)
- Clock frequency 450 kHz to 10 MHz
- Over 80 instructions (based on MAB8048) all of 1 or 2 cycles
- Single supply voltage from 2.5 V to 6.0 V
- STOP and IDLE mode
- On-chip oscillator with output drive capability for peripherals (e.g. PCD3312 DTMF generator)
- Individual mask configuration of all port lines for: pull-up, push-pull or open drain
- Power-on-reset circuit and low supply voltage detection
- Individual mask selection of reset state for all ports
- Operating temperature range: −25 to + 70 °C

PACKAGE OUTLINES

PCD3346P: 28-lead DIL; plastic (SOT117).
PCD3346T: 28-lead mini-pack; plastic (SO28; SOT136A).

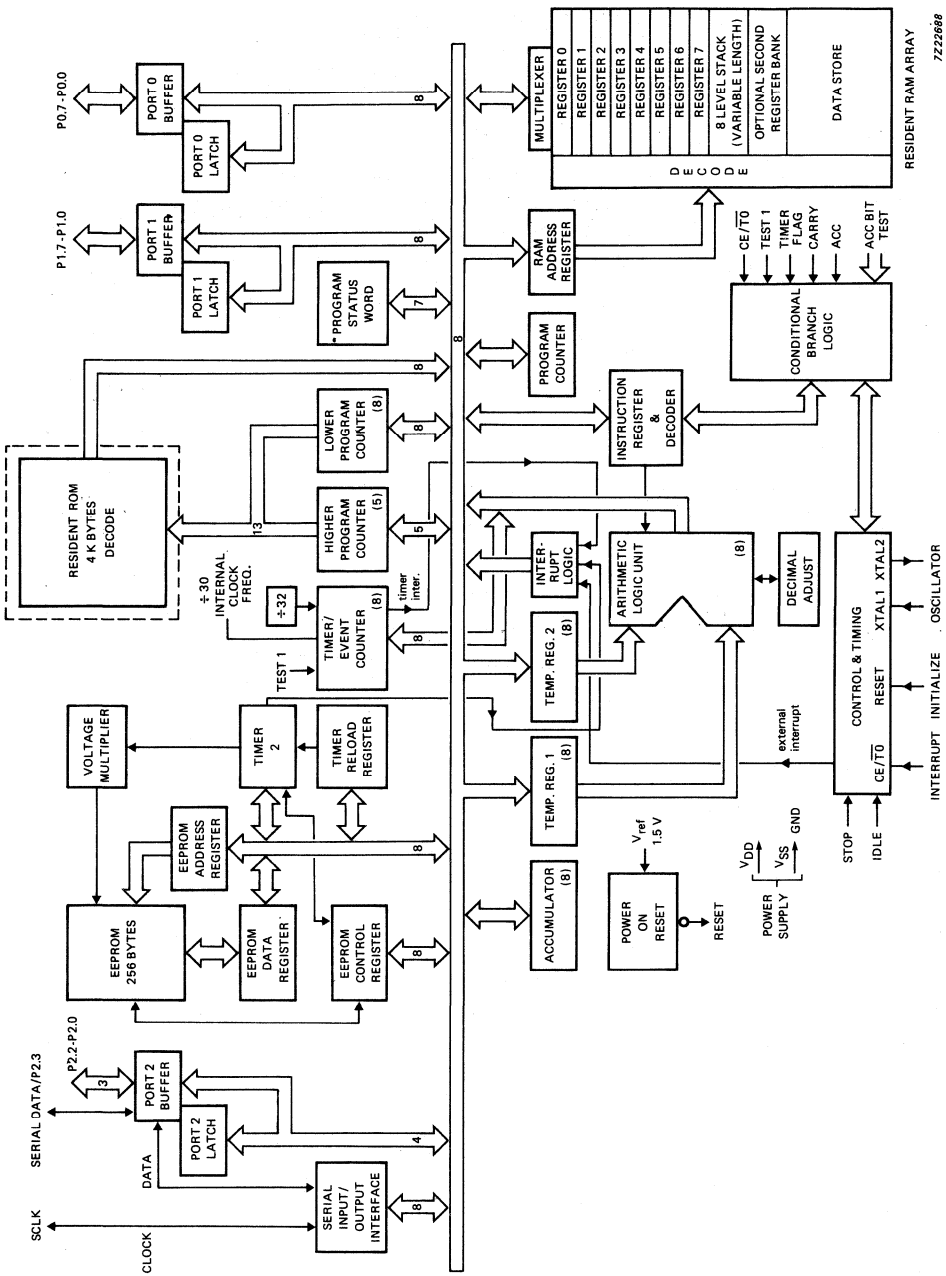


Fig. 1 Block diagram.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC14 OR DATA SHEET

CMOS MICROCONTROLLER WITH ON-CHIP DTMF GENERATOR

GENERAL DESCRIPTION

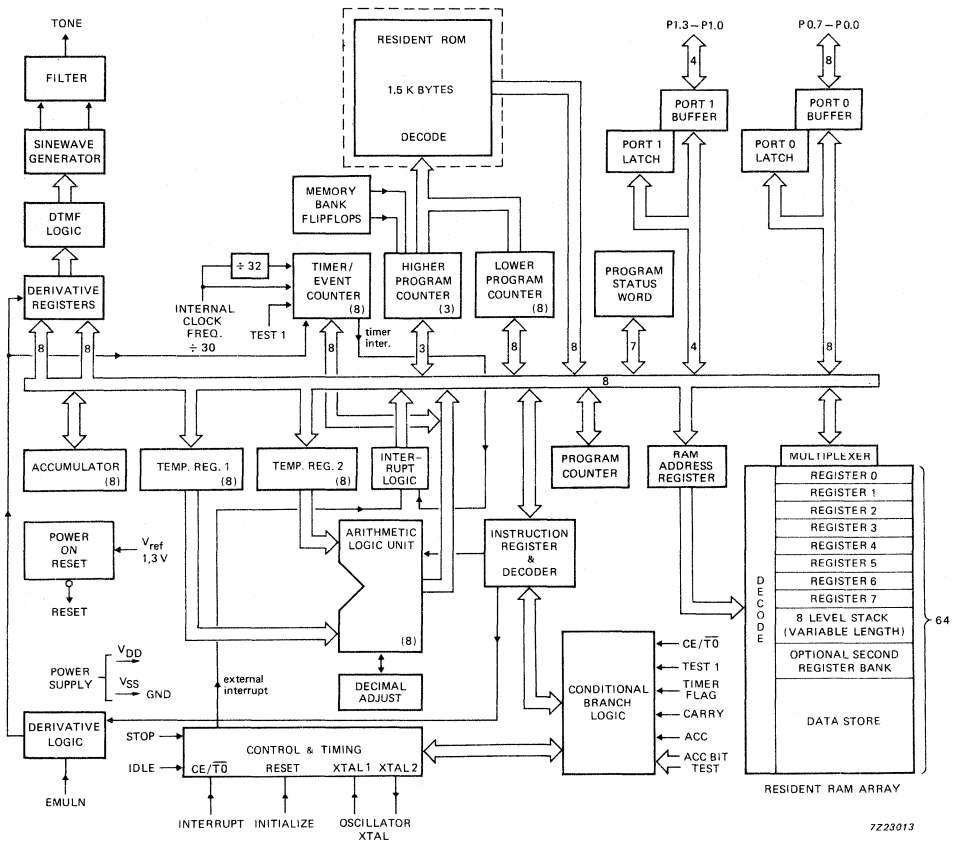
The PCD3347 is a single-chip 8-bit microcontroller fabricated in CMOS and is a member of the PCD33XX family. It has an on-chip dual tone multi-frequency (DTMF) generator and other features for application in telephone sets. For further detailed information, see PCD33XX family specification.

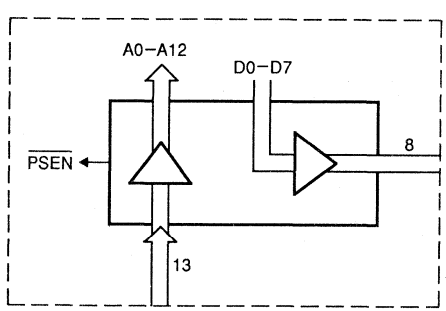
Features

- 8-bit CPU, ROM, RAM, I/O in a single 20-lead DIL or SO package
- 1536 ROM bytes
- 64 RAM bytes
- On-chip DTMF tone generator
- On-chip voltage reference for supply and temperature-independent tone output
- On-chip filtering for low output distortion (CEPT CS203 compatible)
- 12 quasi-bidirectional I/O port lines
- Two test inputs: one of which is also the external interrupt input (CE/$\overline{T0}$)
- Single-level vectored interrupts: external, timer/event counter
- 8-bit programmable timer/event counter
- Over 80 instructions (based on MAB8048)
- All instructions 1 or 2 cycles
- Clock frequency 3,58 MHz
- Single supply voltage from 2,5 V to 6 V
- Low standby voltage and current
- STOP and IDLE mode
- On-chip oscillator
- Configuration of all I/O port lines individually selected by mask: pull-up, open drain or push-pull
- Power-on-reset circuit and low supply voltage detection
- Reset state of all ports individually selected by mask
- Operating temperature range: −25 to + 70 °C

PACKAGE OUTLINES

PCD3347P: 20-lead DIL; plastic (SOT146).
PCD3347T: 20-lead mini-pack; plastic (SO20; SOT163A).





(a)

Fig. 1 PCD3347 block diagram: the function in the dotted outline is replaced as shown in (a) for the PCD3344B 'piggy-back' version.

Pulse/DTMF dialler for France PCD3347/001

FEATURES

- Redial (maximum 23 digits)
- Number of digits per call is infinite (FIFO register)
- 4 x 4 keyboard (function keys: flash, redial, access pause and dial mode)
- Special input: CE
- Special outputs: DP/FL and M1
- Mark/space ratio 2:1 or 3:2
- Pulse dialling for 10 Hz
- DTMF tone/pause 80/80 ms
- Flash 100, 270 or 450 ms
- Manual insertion of access pause
- Access pause time for pulse dialling 3 s
- Access pause time for DTMF 3 s
- On-chip power-on reset
- 2.5 to 6.0 V operating supply voltage
- 3.58 MHz crystal oscillator.

GENERAL DESCRIPTION

The PCD3347/001 is a single-chip CMOS dialler IC for telephone sets. It has two dialling modes; pulse dialling (PD) and dual tone multi-frequency (DTMF). This dialler is specially designed for the French market.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCD3347P/001	20	DIL	plastic	SOT146
PCD3347T/001	20	SO20	plastic	SOT163A

Pulse/DTMF dialler with redial PCD3347/020

FEATURES

- Redial (maximum 23 digits)
- Prepulse option
- Number of digits per call is infinite (FIFO register)
- 4 x 4 keyboard (function keys: flash/earth, redial, mute and program)
- Four diode or strap functions:
  - flash or earth
  - access pause mode
  - prepulse mode selection
  - dial mode selection
- Special inputs: CE and RESET
- Special outputs: DP/FL, M1 and EARTH
- Mark/space ratio 3:2
- Pulse dialling for 10 Hz
- DTMF tone/pause 80/80 ms
- Flash 80 ms
- Earth 425 or 1020 ms
- Automatic insertion of access pause
- Access pause time for pulse dialling 3 s
- Access pause time for DTMF 3 s
- On-chip power-on reset
- 2.5 to 6.0 V operating supply voltage
- 3.58 MHz crystal oscillator.

GENERAL DESCRIPTION

The PCD3347/020 is a single-chip CMOS dialler IC for telephone sets. It has two dialling modes; pulse dialling (PD) and dual tone multi-frequency (DTMF). An Applicaton report "PCD3347/002 for FeAp 01" is available.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCD3347P/020	20	DIL	plastic	SOT146
PCD3347T/020	20	SO20	plastic	SOT163A

Pulse/DTMF dialler with redial PCD3349/018

FEATURES

- Pulse and DTMF dialling plus data transmission
- Redial (maximum 30 digits)
- Number of digits per call is infinite (FIFO register)
- Up to 80 repertory dial numbers of 20 digits (external RAM)
- Keyboard possibility for 8, 16 or 32 direct-accessible repertory numbers (16 one-touch or 32 two-touch)
- Function keys: store, recall, flash, Last Number Redial (LNR), access pause, tone, display, shift, hold, hook and monitor
- Flash or register recall
- Access pause generation and termination
- Automatic recognition of PABX digits (automatic pause insertion)
- Eight diode or strap functions:
  - mark-to-space ratio: 2:1 or 3:2
  - 4 flash time selections (100, 270, 540 or 650 ms)
  - access pause time (1.5/3 or 2.5/5 s for DTMF/pulse)
  - DTMF tone burst times (70 or 100 ms)
  - emergency call (yes or no)
  - pulse or DTMF dialling
  - number blocking for fixed predigits (yes or no)
- Music-on-hold using the on-board tone generator
- On-hook dialling
- Listening-in control
- Memory-card access (smart card)
- LCD control, 16 digits of 7 segments plus 9 labels
- Monitor function to display memory locations
- Clock, calendar and timer/counter function
- Number blocking
- Emergency call (hot line)
- On-chip power-on reset
- 2.5 to 6.0 V operating supply voltage
- 3.58 MHz crystal oscillator.

GENERAL DESCRIPTION

The PCD3349/018 is a single-chip CMOS dialler IC for telephone sets. It has two dialling modes; pulse dialling (PD) and dual tone multi-frequency (DTMF). Up to 80 number repertory pulse/DTMF dialling of 20 digits (by 4 x PCF8570 or 3 x PCF8570 + 1 x PCF8583, each for 20 numbers), part directly accessible and part two-touch via the numerical keyboard.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCD3349P/018	28	DIL	plastic	SOT117
PCD3349T/018	28	SO28	plastic	SOT136A

Single-chip 8-bit Telecom Microcontroller

PCD3350A

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC14 OR DATA SHEET

FEATURES

- 8-bit CPU, ROM, EEPROM, RAM, I/O in a 44-lead quad flat pack
- 8k ROM bytes; 256 RAM bytes
- 256 EEPROM bytes
- 32 kHz crystal oscillator for real-time clock
- EEPROM programmable real-time clock
- Over 100 instructions (based on MAB8048) all of 1 or 2 cycles
- 34 quasi-bidirectional I/O port lines
- 8-bit programmable timer/event counter 1
- 8-bit reloadable timer 2
- 3 single-level vectored interrupts: external, 8-bit programmable timer/event counter 1, derivative (triggered by reloadable timer 2)
- Two test inputs, one of which also serves as the external interrupt input
- DTMF tone generator
- Reference for supply and temperature-independent tone output
- Filtering for low output distortion (CEPT CS203 compatible)
- Melody output for ringer application
- Programmable DTMF clock divider
- Power-on reset
- Stop and idle modes
- Logic supply V_{DD}: 1.8 V to 6 V (DTMF tone output and EEPROM erase/write from 2.5 V)
- CPU Clock frequency: 1 MHz to 16 MHz (3.58 MHz or 10.74 MHz for DTMF)
- Operating temperature range: –25 °C to 70 °C
- Manufactured in silicon gate CMOS process

GENERAL DESCRIPTION

This data sheet details the specific properties of the PCD3350A. The shared characteristics of the PCD33xxA family of microcontrollers are described in the PCD33xxA family data sheet, which should be read in conjunction with this publication.

The PCD3350A is a microcontroller oriented towards telephony applications. It includes 8k ROM bytes, 256 RAM bytes, 34 I/O lines, and an on-chip dual tone multi-frequency (DTMF) generator. In addition to dialling, the generated frequencies can be made available as square waves on port line P1.7/MDY for melody generation, providing ringer operation. The PCD3350A also incorporates 256 bytes of electrically erasable programmable read-only memory (EEPROM), permitting data storage without battery back-up. The EEPROM can be used for storing telephone numbers. Finally, the PCD3350A includes a low power 32 kHz crystal oscillator with an EEPROM programable real time clock (RTC) working in standby mode. The instruction set is based on that of the MAB8048 and is software compatible with the PCD33xxA family.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCD3350AH	44	QFP	plastic	SOT205AG

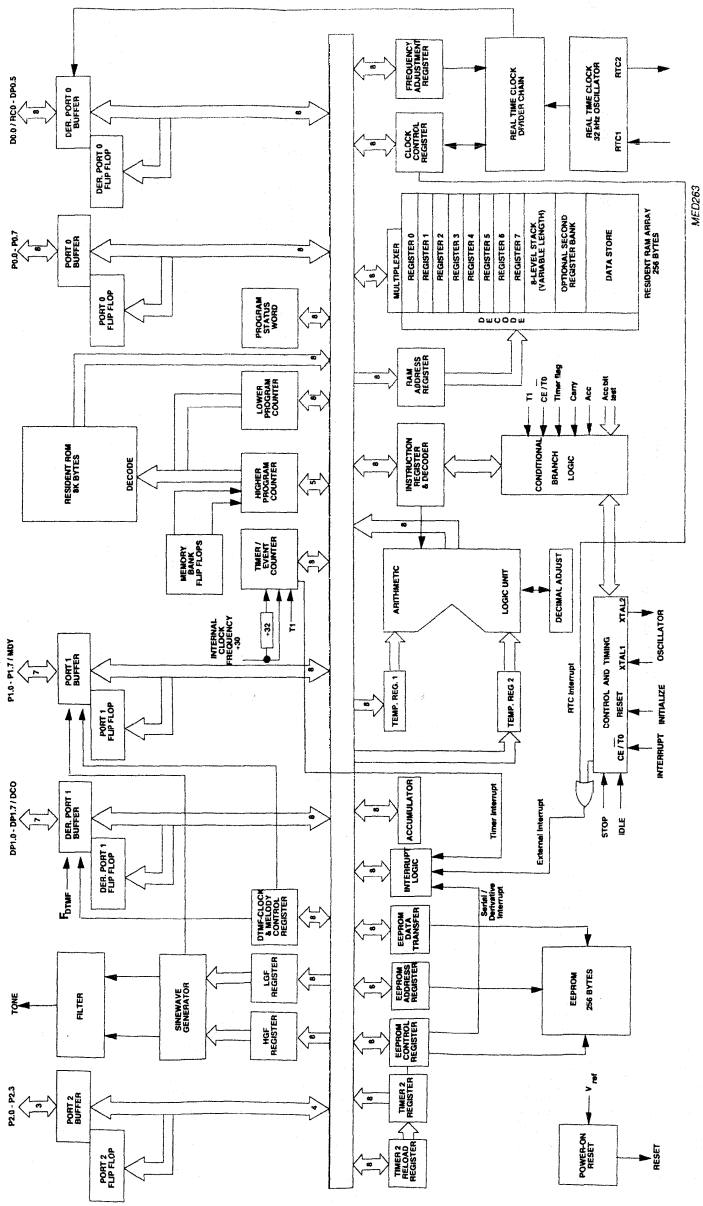


Fig.1 Block diagram.

Single-chip 8-bit Telecom Microcontroller

PCD3351A/52A/53A

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC14 OR DATA SHEET

FEATURES

- 8-bit CPU, ROM, RAM, I/O in a single 28-lead package
- 2 k ROM bytes; 64 RAM bytes (PCD3351A)
- 4 k ROM bytes; 128 RAM bytes (PCD3352A)
- 6 k ROM bytes; 128 RAM bytes (PCD3353A)
- 128 EEPROM bytes
- Over 100 instructions (based on MAB8048) all of 1 or 2 cycles
- 20 quasi-bidirectional I/O port lines
- One 8-bit programmable timer/event counter
- Two 8-bit reloadable timers
- 3 single-level vectored interrupts: external, 8-bit programmable timer/event counter 1, derivative (triggered by reloadable timer 2)
- Two test inputs, one of which also serves as the external interrupt input
- DTMF tone generator
- Reference for supply and temperature-independent tone output
- Filtering for low output distortion (CEPT CS203 compatible)
- Melody output for ringer application
- Power-on reset
- Stop and idle modes
- Logic supply from 1.8 V to 6 V (DTMF tone output and EEPROM erase/write from 2.5 V)
- Clock frequency from 1 MHz to 16 MHz (3.58 MHz for DTMF suggested)
- Manufactured in silicon gate CMOS process

GENERAL DESCRIPTION

This data sheet details the specific properties of the PCD3351A , PCD3352A and PCD3353A. The shared characteristics of the PCD33XXA family of microcontrollers are described in the PCD33XXA family data sheet, which should be read in conjunction with this publication.

The PCD3351A, PCD3352A and PCD3353A are microcontrollers orientated towards telephony applications which contain an on-chip dual tone multi-frequency (DTMF) generator. In addition to dialling, the generated frequencies can be made available as square waves on port line P1.7/MDY for melody generation thus providing ringer operation. The PCD3351A/52A/53A also incorporate 128 bytes of electrically erasable programmable read-only memory (EEPROM), permitting data storage without battery back-up. The EEPROM can be used for storing telephone numbers, particularly for implementing redial functions. The instruction set is based on that of the MAB8048 and is software compatible with the PCD33XXA family.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	positive supply voltage	−0.8	+7.0	V
V_I	all input voltages	−0.5	V_{DD}+0.5	V
I_I,I_O	DC input or output current	−10	+10	mA
I_{SS}	ground supply current	−50	+50	mA
P_{tot}	total power dissipation	−	125	mW
P_O	power dissipation per output	−	30	mW
T_{stg}	storage temperature range	−55	+150	°C
T_j	operating junction temperature	−	90	°C

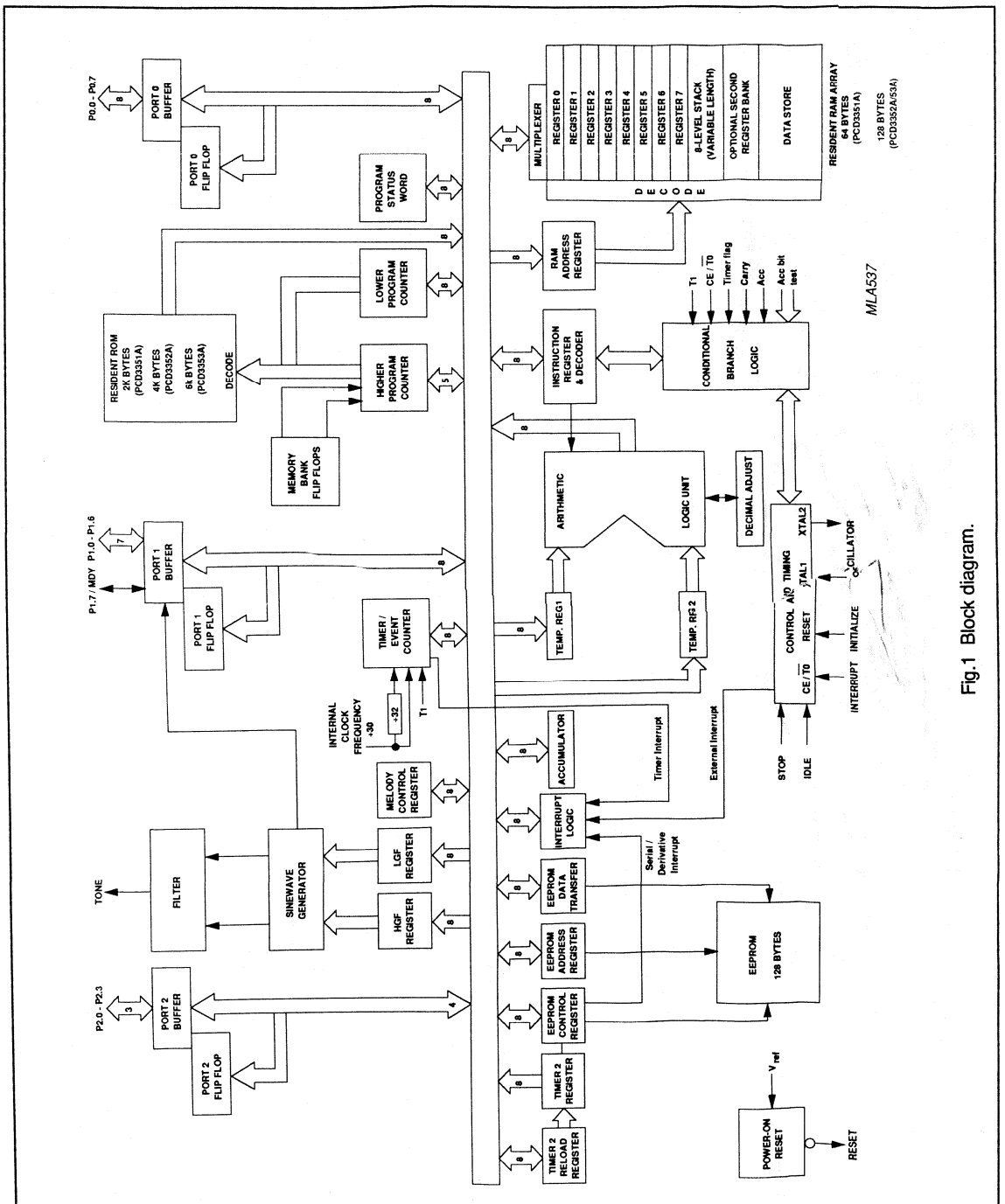


Fig.1 Block diagram.

Single-chip 8-bit Telecom Microcontroller with on-chip DTMF

PCD3354A

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC14 OR DATA SHEET

FEATURES

- 8-bit CPU, ROM, RAM, EEPROM, I/O in a 44-lead quad flat pack
- 8k ROM bytes; 256 RAM bytes
- 256 EEPROM bytes
- Over 100 instructions (based on MAB8048) all of 1 or 2 cycles
- 36 quasi-bidirectional I/O port lines
- 8-bit programmable timer/event counter 1
- 8-bit reloadable timer 2
- 3 single-level vectored interrupts: external, 8-bit programmable timer/event counter 1, derivative (triggered by reloadable timer 2)
- Two test inputs, one of which also serves as the external interrupt input
- DTMF tone generator
- Reference for supply and temperature-independent tone output
- Filtering for low output distortion (CEPT CS203 compatible)
- Melody output for ringer application
- Programmable DTMF clock divider
- Power-on reset
- Stop and idle modes
- Logic supply V_{DD}: 1.8 V to 6 V (DTMF tone output and EEPROM erase/write from 2.5 V)
- CPU Clock frequency: 1 MHz to 16 MHz (3.58 MHz, 10.74 MHz for DTMF)
- Operating temperature range: –25 °C to 70 °C
- Manufactured in silicon gate CMOS process

GENERAL DESCRIPTION

This data sheet details the specific properties of the PCD3354A. The shared characteristics of the PCD33xxA family of microcontrollers are described in the PCD33xxA family data sheet, which should be read in conjunction with this publication.

The PCD3354A is a microcontroller oriented towards telephony applications. It includes 8k ROM bytes, 256 RAM bytes, 36 I/O lines, and an on-chip dual tone multi-frequency (DTMF) generator. In addition to dialling, the generated frequencies can be made available as square waves on port line P1.7/MDY for melody generation, providing ringer operation. The PCD3354A also incorporates 256 bytes of electrically erasable programmable read-only memory (EEPROM), permitting data storage without battery back-up. The EEPROM can be used for storing telephone numbers. The instruction set is based on that of the MAB8048 and is software compatible with the PCD33xxA family.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCD3354AH	44	QFP	plastic	SOT205AG

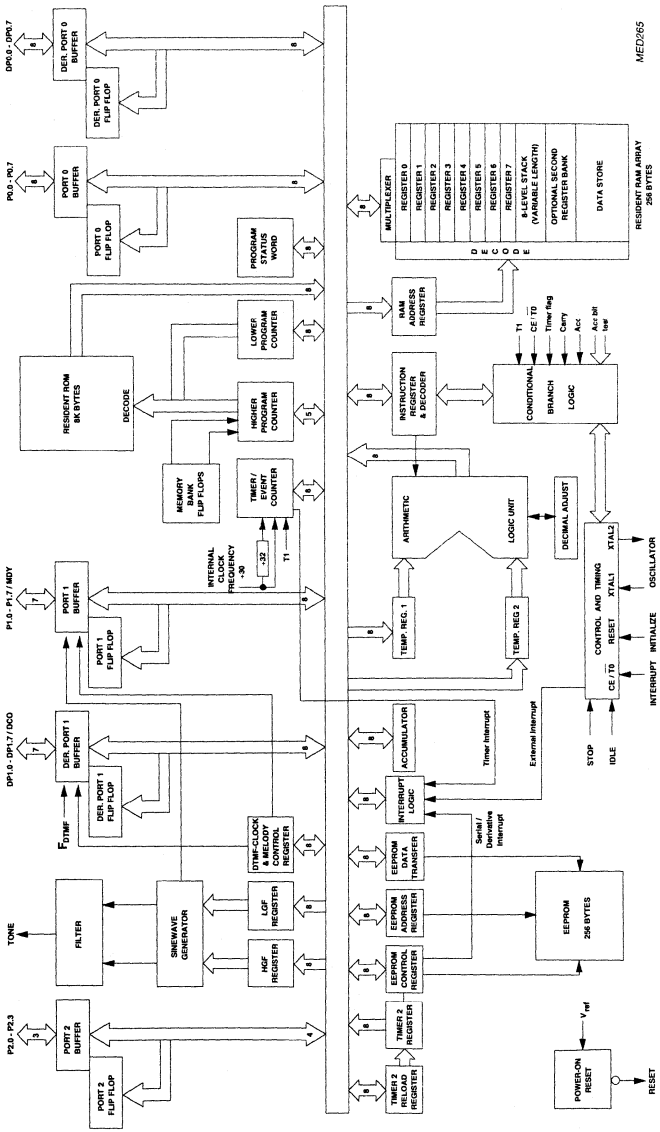


Fig.1 Block diagram.

PROGRAMMABLE MULTI-TONE TELEPHONE RINGER

GENERAL DESCRIPTION

The PCD3360 is a CMOS integrated circuit, designed to replace the electro-mechanical bell in telephone sets. It meets most postal requirements, particularly with tone sequence possibilities and input frequency selectivity. Output signals for a loudspeaker or for a piezo-electric (PXE) transducer are provided. No audio transformer is required since the loudspeaker is driven in class D.

Features

- Output signals for electro-dynamic transducer (loudspeaker) or for piezo-electric transducer (PXE)
- 7 basic frequencies (tones) and a pause
- 4 selectable tone sequences
- 4 selectable repetition rates
- 3 selectable impedance settings
- 3-step automatic swell
- Delta-modulated output signal that approximates a sinewave
- Input frequency discriminator with selectable upper and lower frequency limits
- Output for optical signal

Note

Tone sequences (up to 16 tones long), impedance settings and automatic swell levels are mask programmable for customized versions.

QUICK REFERENCE DATA

Available frequencies (tones)		533/600/667/800/ 1000/1067 and 1333	Hz
Number of intervals per tone sequence		15 or 16	
Lower limits of frequency discriminator		13,33 or 20	Hz
Upper limits of frequency discriminator		30 or 60	Hz
Impedance settings (with 50 Ω loudspeaker)	approx.	7 or 10,5 or 17,5	kΩ
Switch-on delay at 25 Hz	max.	60	ms

PACKAGE OUTLINES

PCD3360P: 16-lead DIL; plastic (SOT38).
PCD3360T: 16-lead mini-pack; plastic (SO16L; SOT162A).

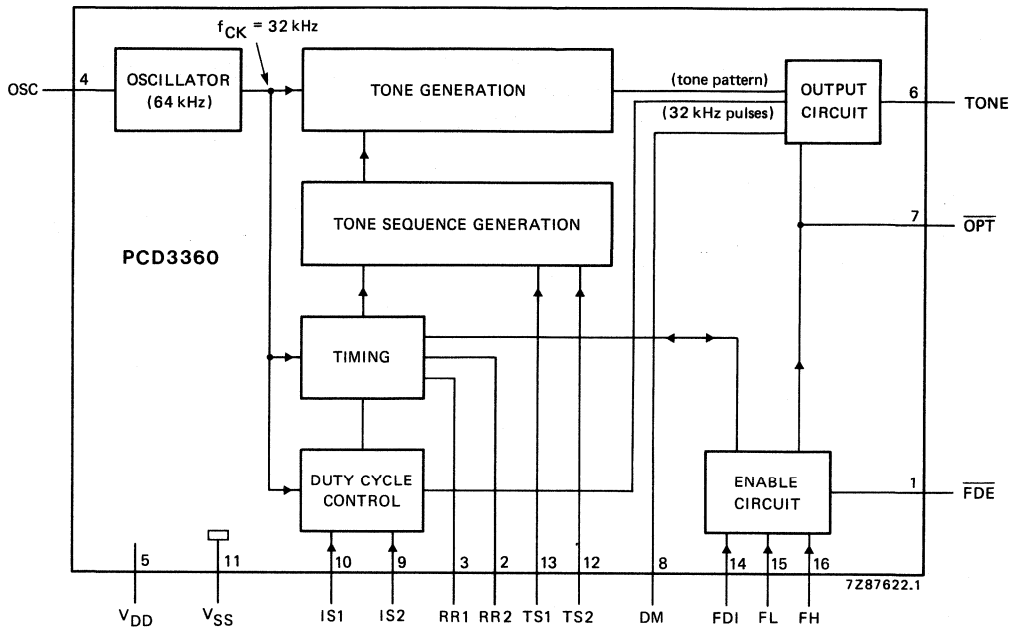


Fig. 1 Block diagram.

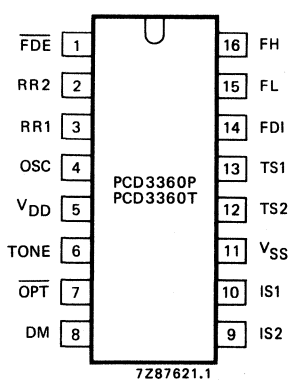


Fig. 2 Pinning diagram for PCD3360P and PCD3360T.

PINNING

1	$\overline{FDE}$	frequency discriminator enable
2	RR2	repetition rate selection
3	RR1	repetition rate selection
4	OSC	oscillator
5	V_{DD}	positive supply
6	TONE	tone output
7	$\overline{OPT}$	optical signal output
8	DM	drive mode selection
9	IS2	impedance setting and automatic swell
10	IS1	impedance setting and automatic swell
11	V_{SS}	negativ supply
12	TS2	tone sequence selection
13	TS1	tone sequence selection
14	FDI	frequency discriminator input
15	FL	lower frequency limit selection
16	FH	upper frequency limit selection

FUNCTIONAL DESCRIPTION (see Fig. 1)

Supply pins (V_{DD} and V_{SS})

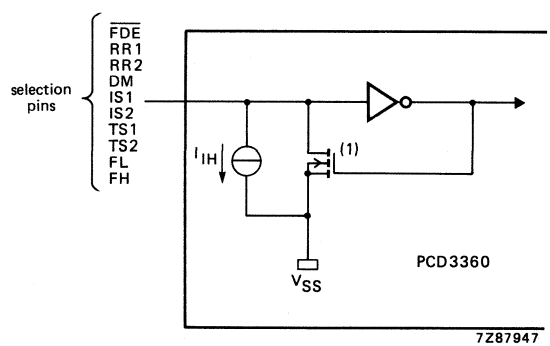
If the supply voltage (V_{DD}) drops below the standby voltage (V_{SB}), the oscillator and most other functions are switched off and the supply current is reduced to the standby current (I_{SB}). The automatic swell register retains its information until V_{DD} drops further to a value V_{AS} at which reset occurs.

Oscillator (OSC)

The 64 kHz oscillator is operated via an external resistor and capacitor connected to pin OSC. The oscillator signal is divided by two to provide the 32 kHz internal system clock.

Selection pins ($\overline{FDE}$, RR2, RR1, DM, IS2, IS1, TS2, TS1, FL and FH)

These pins are pulled down internally by a pull-down current I_{IH} when they are connected to V_{DD}, and by a pull-down resistance R_{IL} when they are connected to V_{SS} (see Fig. 3). Thus when the pins are open-circuit they are defined LOW. Therefore only a single-contact switch is required to connect the pins to V_{DD}; yet the supply current is only marginally increased as I_{IH} is very small.



(1) Transistor resistance = R_{IL} when switched on.

Fig. 3 Input circuit of selection pins.

Frequency discriminator circuit (pins $\overline{FDE}$ and FDI)

The frequency discriminator circuit prevents the ringer being activated by dial pulses, speech or other unqualified signals.

The circuit is enabled or disabled by input $\overline{FDE}$.

When $\overline{FDE}$ is HIGH, FDI acts as a logic enable input.
The circuit will produce tone sequences provided FDI is HIGH and V_{DD} exceeds V_{SB}.
When $\overline{FDE}$ is LOW, FDI acts as the frequency discriminator input.
The circuit will produce tone sequences provided V_{DD} exceeds V_{SB} and the signal at FDI fulfils the conditions set by FL and FH.

When the frequency discriminator is enabled ($V_{DD} > V_{SB}$ and $\overline{FDE}$ = LOW) the circuit will start to produce tone sequences after two rising or two falling edges have occurred at FDI. The time between these edges must be within the limits set by FL and FH.

FUNCTIONAL DESCRIPTION (continued)

The circuit will continue to produce tone sequences provided the time between subsequent falling edges or between subsequent rising edges remains within the limits set by FL and FH, otherwise it will stop. Because two edges are required for detection, either positive or negative, the switch-on delay will vary between 1 and 1,5 cycles of the incoming ringing frequency.

FDI has a Schmitt-trigger action; the levels are set by an external resistor R2 (see Fig. 8) and an internal sink current that is switched from 20 μA (typ.) for FDI = LOW to $< 0{,}1$ μA for FDI = HIGH. Excess current entering FDI via R2 is absorbed by internal diodes clamped to V_{DD} and V_{SS}.

Selection of frequency discriminator limits (FL and FH)

With the frequency discriminator enabled ($V_{DD} > V_{SB}$ and $\overline{FDE}$ = LOW) the lower and upper limits of the input frequency are set by inputs FL and FH as shown by Table 1 and Table 2 respectively.

Table 1 Selection of lower frequency discriminator limits (f_{osc} = 64 kHz)

FL input state	lower discriminator limit (Hz)
LOW	20
HIGH	13,33

Table 2 Selection of upper frequency discriminator limits (f_{osc} = 64 kHz)

FH input state	upper discriminator limit (Hz)
LOW	60
HIGH	30

Selection of tone sequences (TS1 and TS2)

A tone sequence is composed of 15 or 16 equal time intervals. Each time interval may be filled with one of seven available tones or with a pause; these are shown together with their corresponding internal ROM tone code in Fig. 4.

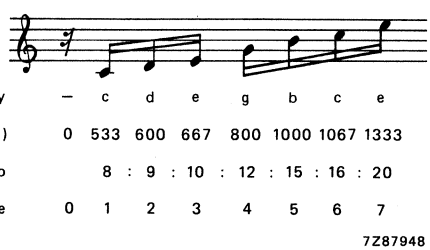


Fig. 4 Available tones and their corresponding internal ROM tone code.

Four tone sequences are programmed in the internal ROM (see Fig. 5). Inputs TS1 and TS2 determine which tone sequence is selected and output at pin TONE. The sequences are mask programmable with any length up to 16 time intervals.

The tone sequences are repeated continuously provided the enable conditions at inputs $\overline{FDE}$ and FDI are valid and $V_{DD} > V_{SB}$; the first sequence always starts with the first tone shown in Fig. 5.

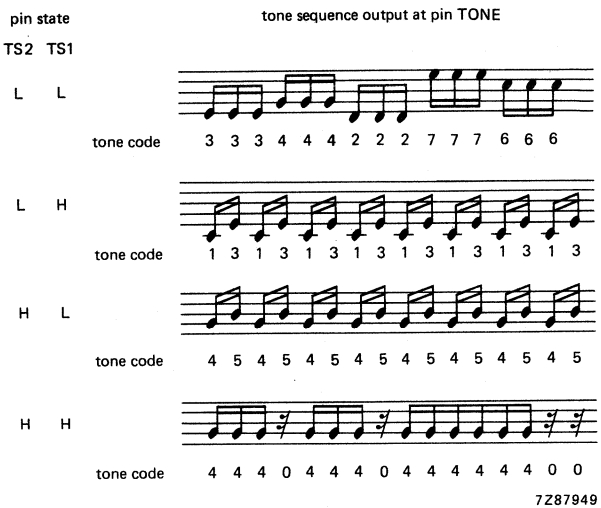


Fig. 5 Tone sequences mask-programmed in the PCD3360.

Selection of repetition rates (RR1 and RR2)

The duration of a time interval within a tone sequence is determined by the state of inputs RR1 and RR2 as shown in Table 3. The resultant variation of repetition rate acts as a distinguishing feature between adjacent telephones.

Table 3 Duration of time intervals (f_{osc} = 64 kHz)

input state		time interval ms
RR1	RR2	
L	L	15
L	H	30
H	L	45
H	H	60

The repetition rate variation can be extended by mask programming (for customer defined versions) the same tone combination for all 4 tone sequences, but with a different number of time intervals per tone. Thus the repetition rate can be selected from 16 values by inputs RR1, RR2, TS1 and TS2.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

Drive mode selection (DM)

The output signal at pin TONE can be selected for application with electro-dynamic or piezo-electric transducers. An example of both signals, for a tone frequency of 667 Hz, is shown in Fig. 6.

Loudspeaker mode

In the loudspeaker mode (DM = LOW), pin TONE outputs a delta-modulated signal that approximates a sinewave sampled at a rate of 32 kHz. The output pulse duration is determined by pins IS1 and IS2. The resultant acoustic spectrum is aurally more acceptable and has greater penetration than a square wave spectrum because more power is concentrated at the fundamental frequency.

PXE mode

In the PXE mode (DM = HIGH), pin TONE outputs a square wave. In this mode the ringer impedance and sound pressure level are determined by the characteristics (e.g. the size) of the PXE transducer; inputs IS1 and IS2 are inactive.

Setting of impedance, sound pressure level and automatic swell (IS1 and IS2)

With DM = LOW (loudspeaker mode), inputs IS1 and IS2 determine the pulse duration of the output signal and thereby the d.c. resistance R_{xy} (seen at points x and y in Fig. 8), the input impedance Z_I and and also the Sound Pressure Level (SPL). The selection of 3 impedance settings and automatic swell is shown in Table 4.

Table 4 Setting of pulse duration and automatic swell (DM = LOW)

input state		function	ringing burst number (N)	pulse duration (μs)		R_{xy} (kΩ)	Z_I (kΩ)	SPL (dBr)
IS1	IS2			fund.	harm.			
L	L	automatic swell	1	1,9	–	40	tbf	tbf
			2	2,9	–	20	17,5	–4
			> 2	4,1	1,8	5	7	0
L	H	constant level	–	2,9	–	20	17,5	–4
H	L		–	3,8	–	10	10,5	tbf
H	H		–	5,4	–	5	7	0

Where:

1. Typical pulse duration values of the fundamental and harmonic frequencies are for f_{osc} = 64 kHz and f_{CK} = 32 kHz.
2. SPL is the relative Sound Pressure Level, and 0 dBr is defined as the SPL for IS1 = IS2 = HIGH.
3. Values of the d.c. resistance R_{xy}, bell impedance (Z_I) and SPL are valid for a value of input voltage V_I = 40 V_{rms} at 25 Hz in Fig. 8.

Setting of impedance, sound pressure level and automatic swell

When pins IS1 and IS2 are both LOW, the circuit operates in the automatic swell mode. The SPL then increases in three steps so that the maximum level is reached for the third ringing burst.
Each time V_{DD} drops below V_{AS} the automatic swell register is reset and the next ringing burst is considered as N = 1 (see Table 4).
A buffer capacitor C3 (see Fig. 8) must hold $V_{DD} > V_{AS}$ during the time between two consecutive ringing bursts of a series.

For each of the other three combinations of pins IS1 and IS2 the pulse duration has a constant value. Thus the ringer can be designed so that the impedance represented at the telephone line will comply with postal requirements that vary in relation to parallel or series connections of more than one ringer.

To satisfy some applications, a harmonic signal is added to the fundamental frequency in the last step of the automatic swell mode. The pulses representing this harmonic signal are interleaved with the pulses of the fundamental signal (see Fig. 7). The difference in pulse duration shown in Table 4, is chosen so that the harmonic level is 10 dB below the fundamental level.
The harmonic frequency range is from 2 kHz to 3,2 kHz. The individual harmonic frequencies for the seven tone codes and the relative fundamental frequencies are shown in Table 5.

Table 5 Harmonic frequency in relation to tone code and fundamental frequency

tone code	frequency (Hz)	
	fundamental	harmonic
1	533	3200
2	600	2400
3	667	2667
4	800	3200
5	1000	2000
6	1067	2133
7	1333	2667

Using a single mask it is possible to program the following:

- Addition of harmonics in all the other input states of IS1 and IS2
- All pulse duration values
- Other even harmonic frequencies.

Optical output ($\overline{OPT}$)

The $\overline{OPT}$ output is designed to drive an optical signal transducer or lamp. It is LOW when the ringer circuit is enabled and HIGH when the ringer circuit is disabled. This output can also be used to switch the transmitter ON and OFF in the base of a cordless telephone set.

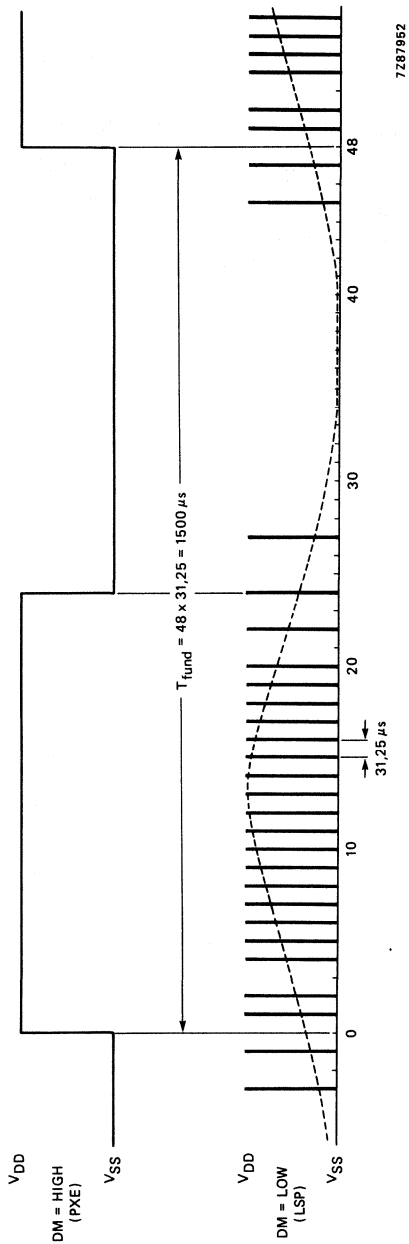


Fig. 6 Fundamental signal (667 Hz) at pin TONE (for f_{osc} = 64 kHz, to provide f_{CK} = 32 kHz).

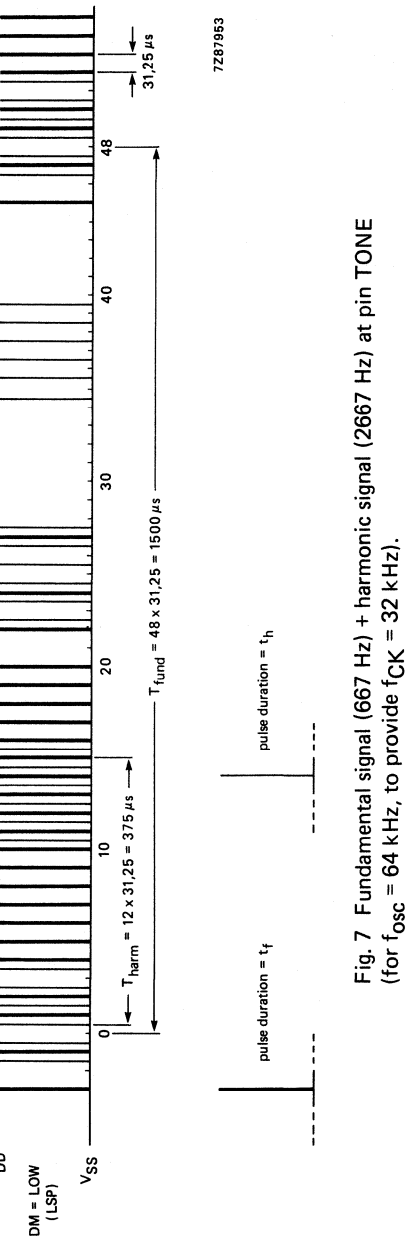


Fig. 7 Fundamental signal (667 Hz) + harmonic signal (2667 Hz) at pin TONE (for f_{osc} = 64 kHz, to provide f_{CK} = 32 kHz).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}		−0,8 to + 9	V
Supply current	I_{DD}	max.	50	mA
D.C. current into any input or output	$\pm I_I, \pm I_O$	max.	10	mA
All input voltages	V_I		−0,8 V to V_{DD} + 0,8	V
Total power dissipation	P_{tot}	max.	300	mW
Total dissipation per output	P_O	max.	50	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Operating ambient temperature range	T_{amb}		−25 to + 70	°C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

DEVELOPMENT DATA

D.C. CHARACTERISTICS

V_{DD} = 6 V; V_{SS} = 0; f_{osc} = 64 kHz; T_{amb} = −25 to + 70 °C; valid enable conditions at FDI and $\overline{FDE}$; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Operating supply voltage	V_{DD}	V_{SB}+0,1	–	8,0	V
Standby supply voltage (note 1)	V_{SB}	3,9	4,8	5,7	V
Supply voltage for automatic swell reset (note 2)	V_{AS}	–	0,5V_{SB}	–	V
Operating supply current (note 3)	I_{DD}	–	110	140	μA
Standby supply current at $V_{DD} < V_{SB}$ (note 4)	I_{SB}	–	3	8	μA
Inputs					
Input voltage LOW (any pin)	V_{IL}	0	–	0,3V_{DD}	V
Input voltage HIGH (any pin)	V_{IH}	0,7V_{DD}	–	V_{DD}	V
Pull-down circuits of inputs					
FDE, RR1, RR2, DM, IS1, IS2, TS1, TS2, FL, FH					
pull-down resistance with input at V_{SS}	R_{IL}	–	20	–	kΩ
pull-down current with input at V_{DD}	I_{IH}	–	0,1	–	μA
Pull-down circuit of FDI					
pull-down current with V_{FDI} = 0,3V_{DD}; T_{amb} = 25 °C	I_{SL}	14	23	32	μA
temperature coefficient of I_{SL}	$-\Delta I_{SL}$	–	0,5	–	%/°C
pull-down current with V_{FDI} = 0,8V_{DD}	I_{SH}	–	0,1	–	μA
pull-down current with $V_{DD} < V_{SB}$	I_{SX}	–	0,1	–	μA
Current into input FDI (note 5)	$\pm I_{IS}$	–	–	0,2	mA
Outputs					
TONE, $\overline{OPT}$					
Output sink current at V_{OL} = 0,5 V	I_{OL}	1	2	–	mA
Output source current at V_{OH} = V_{DD}−0,5 V	$-I_{OH}$	1	2	–	mA

A.C. CHARACTERISTICS

V_{DD} = 6 V; V_{SS} = 0; f_{osc} = 64 kHz; T_{amb} = −25 to + 70 °C; valid enable conditions at FDI and $\overline{FDE}$; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Switch-on delay (with $\overline{FDE}$ = LOW and ringing frequency within limits set by FL and FH)	$t_{d(on)}$	1	–	1,5	note 6
Switch-off delay (with $\overline{FDE}$ = LOW)					
at FL = LOW	$t_{d(off)}$	–	–	50	ms
at FL = HIGH	$t_{d(off)}$	–	–	75	ms
Oscillator frequency					
at R_{osc} = 365 kΩ; C_{osc} = 56 pF; T_{amb} = 25 °C (note 7)	f_{osc}	60	64	68	kHz
Frequency variation					
as a function of V_{DD}	$-\Delta f_{osc}$	–	1	–	%/V
as a function of T_{amb}	$-\Delta f_{osc}$	–	0,05	–	%/K

DEVELOPMENT DATA

Notes to the characteristics

1. For $V_{DD} < V_{SB}$ the circuit is in standby.
2. At $V_{DD} = V_{AS}$ the automatic swell register is reset.
3. R_{osc} = 365 kΩ; C_{osc} = 56 pF; FDI = $\overline{FDE}$ = V_{DD}; all other inputs and outputs open circuit.
4. The standby supply current is measured with all inputs and outputs open-circuit with the exception of OSC.
5. The current I_{IS} is clamped to V_{DD} and to V_{SS} by two internal diodes. Correct operation is ensured with $V_{FDI} > V_{DD}$ or $V_{FDI} < V_{SS}$, provided the maximum value of I_{IS} is not exceeded. (The input FDI has an extended HIGH and LOW input voltage range.)
6. The switch-on delay is measured in cycles of incoming ringing frequency.
7. Lead lengths of R_{osc} and C_{osc} to be kept to a minimum.

APPLICATION INFORMATION

Application of the PCD3360 in a telephone ringer circuit together with a loudspeaker is shown in Fig. 8.

The threshold levels V_H and V_L of the frequency discriminator circuit are determined by:

- The logic threshold of input FDI ($0{,}5V_{DD}$ typ. 3,4 V for V_{DD} = 6,8 V)
- The pull-down current of input FDI (20 μA typ. for FDI $<$ 3,4 V)
- The value of R2 (680 kΩ in Fig. 8)

For a positive slope, the voltage at R2 must exceed the value V_H before FDI will become HIGH; V_H is the sum of the input threshold and the voltage drop across R2 thus:

$$V_H = 3{,}4 + (680 \times 10^3) \times (20 \times 10^{-6}) = 17 \text{ V}.$$

For a negative slope, the voltage at R2 must decrease below the value V_L before FDI will become LOW. Because the current into FDI is negligible with FDI = HIGH the voltage drop across R2 can be discounted, thus V_L = 3,4 V.

The minimum operating voltage across C3 is 17,8 V which is determined by:

- The minimum operating voltage of the PCD3360 (5,8 V)
- The supply current of the PCD3360 (120 μA max.)
- The value of R3 (100 kΩ in Fig. 8)

The total switch-on delay equals approximately the time required to charge the supply capacitor C3 to the minimum operating value, plus the specified switch-on delay of the PCD3360.

The high operating voltage combined with the class D output stage ensures optimal energy conversion and thereby a high sound level. The design can easily be optimized for parallel or series connection of more than one ringer. The diode bridge, zener diode (D1) and resistor R1 protect the ringer against transients up to 5 kV. During these surges the voltage on the 68 V zener diode (BZW03) can rise to 100 V; the DMOS transistor BST72A (TR1) has a maximum drain-source voltage of 100 V. Up to 220 V, 50 Hz can be applied to the a/b terminals without damaging the ringer.
The choke (L1) in series with the 50 Ω loudspeaker increases the sound pressure level by approximately 3 dB by suppression of the 32 kHz carrier frequency and its sidebands.
The flyback diode BAX18A (D2) is a fast type with low forward voltage to obtain high efficiency.

Application of the PCD3360 together with a PXE transducer is shown in Fig. 9. The only significant difference between Fig. 8 and Fig. 9 is the output stage. Two BST72A transistors provide an output voltage swing almost equal to the voltage at C3. Pins IS1 and IS2 are inoperative because DM = HIGH. Volume control is possible using resistor R_V.

DEVELOPMENT DATA

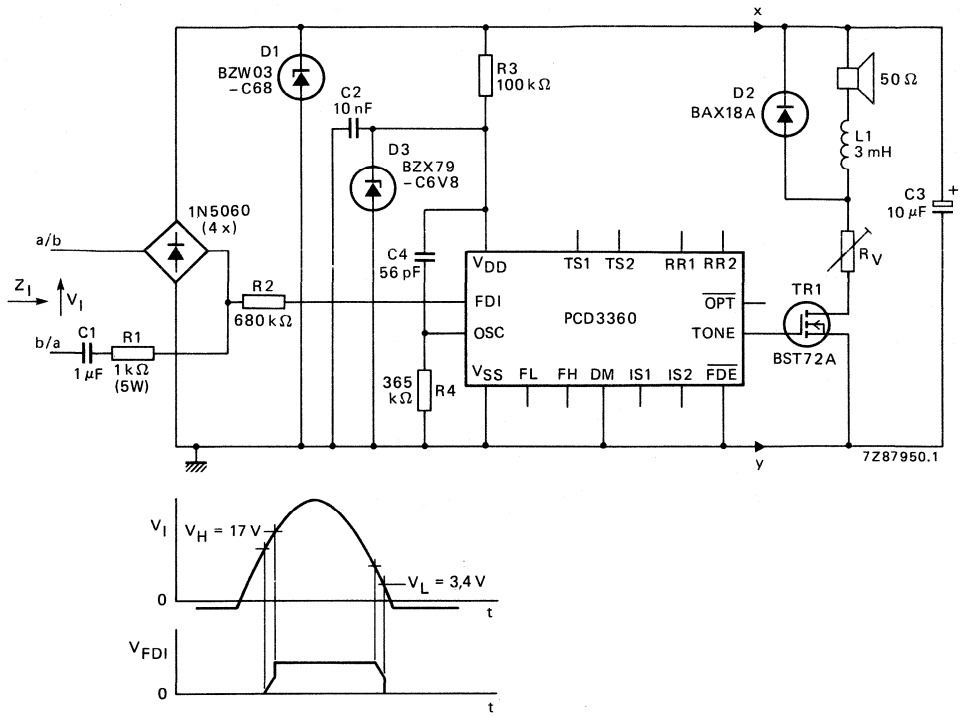


Fig. 8 Transformerless electronic ringer with PCD3360 and a loudspeaker.

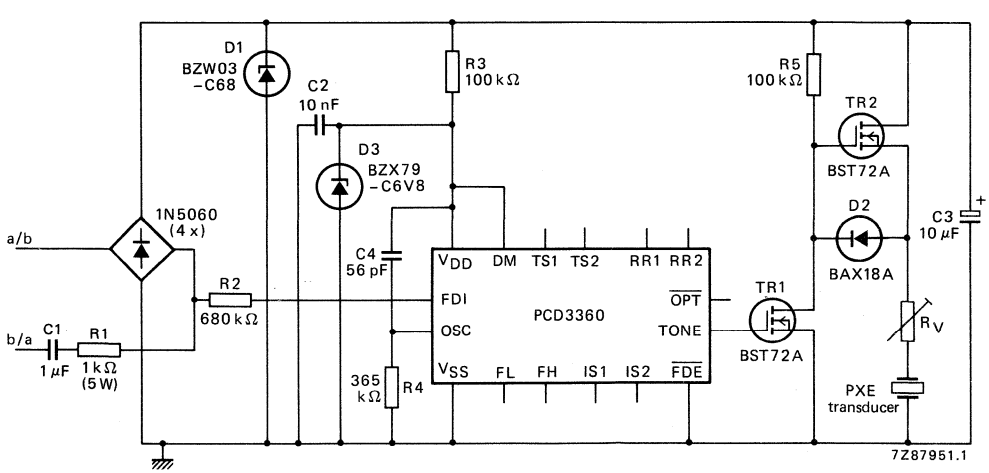
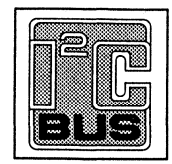


Fig. 9 PCD3360 ringer with PXE transducer.

Analog Voice Scrambler/Descrambler

PCD4440T



FEATURES

- Scrambler or descrambler function
- Scrambling in frequency domain
- Selectable split frequency (up to 10 selections per second)
- Telephony-band filtering included
- No increase in bandwidth
- No external components required
- Small signal delay
- Insensitive to distortion and group delay of transmission channel
- Control via serial (I²C) bus
- Low transfer loss of speech
- Mute option
- Transparent mode
- High signal input impedance
- Low signal output impedance
- Low power consumption

APPLICATIONS

- Cordless telephones
- Security telephones
- Portable phones
- PMR

GENERAL DESCRIPTION

The PCD4440 is a silicon gate CMOS integrated circuit intended to be used in radio, mobile- and line powered telecommunications products utilizing a microcontroller for the control functions. Analog scrambling/descrambling is based on the split frequency method realized in a sophisticated switched-capacitor technology. The PCD4440 is compatible with most microcontrollers and communicates via a two line bidirectional bus (I²C).

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCD4440T	8	mini-pack	plastic	SOT176C

Analog Voice Scrambler/Descrambler

PCD4440T

BLOCK DIAGRAM

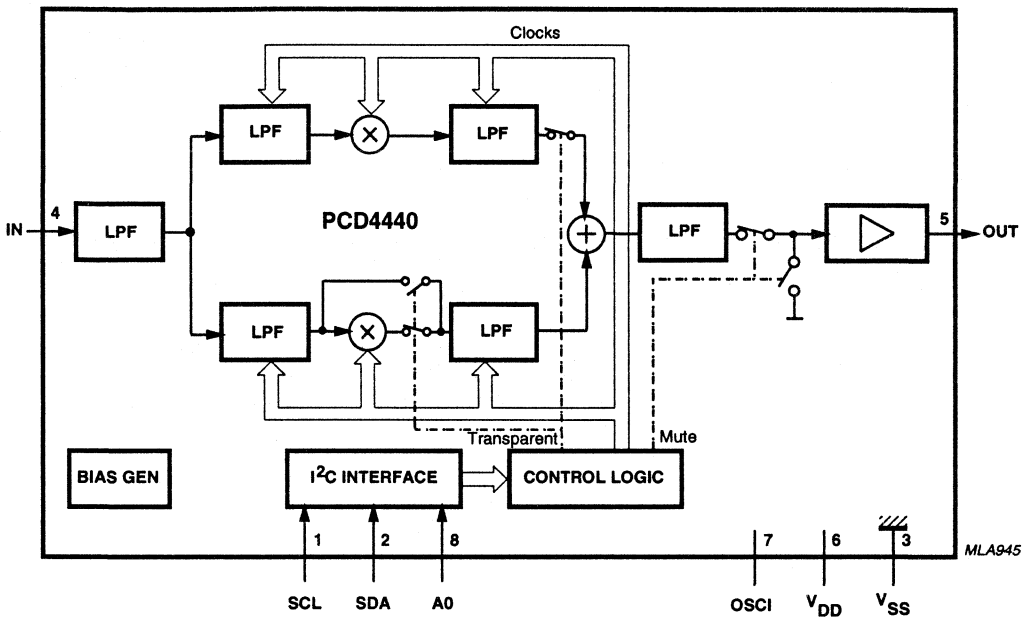


Fig.1 Block diagram.

Analog Voice Scrambler/Descrambler

PCD4440T

PINNING

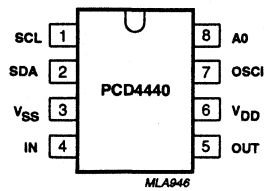


Fig.2 Pin configuration.

Pin Description

SYMBOL	PIN	FUNCTION
SCL	1	serial clock line (I²C)
SDA	2	serial data line (I²C)
V_{SS}	3	negative Supply
IN	4	signal input
OUT	5	signal output
V_{DD}	6	positive supply
OSCI	7	oscillator input
A0	8	slave address input (I²C)

FUNCTIONAL DESCRIPTION

To provide privacy for the end user of a cordless telephone set, the radio-link audio signal must be scrambled. In the microphone and the incoming telephone line audio path a scrambler circuit has to be implemented. Consequently the audio signal to the telephone line and to the earpiece must be descrambled. Both functions can be fulfilled by the PCD4440 by simply inserting it in the audio path.

The PCD4440 accomplishes this task by first filtering the incoming signal, limiting the bandwidth to 3500 Hz. Then the signal is split into a high ($> f_S$) and a low ($< f_S$) frequency band. Both frequency bands are inverted and added again to provide a single output signal.

Values for 9 split frequencies f_S can be controlled by a scramble code table in the microcontroller. Control of these split frequencies is accomplished via the serial two wire I²C-bus. In addition to the split frequencies (fs), a transparent mode and mute instruction can be selected.

In Fig.3, the signal path for both bands is drawn. The lower band path (on the left side of the diagram) operates on frequencies $f \leq f_S$ (Split Frequency), the upper band path (on the right side) on frequencies $f \geq f_S$.

The input signal contains frequencies from f_1 up to f_2. The output signal is band limited (only in scrambling mode) from f_l (300 Hz) to f_h (3500 Hz). In the left path, the input signal is first limited to f_S. The following modulator inverts the lower band. f_l is folded up to f_S, f_S down to f_l. In general, an input frequency f_{in} is folded to $f_{out} = f_S + f_l - f_{in}$. Finally the folded signal is band limited to f_S again.

In the right path, the input signal is first limited to f_h. The following modulator inverts the upper band. f_S is folded up to f_h, f_h down to f_S. In general, an input frequency f_{in} is folded to $f_{out} = f_S + f_h - f_{in}$. Finally, the folded signal is band limited to f_h again. In the last step, the bands are added and buffered.

In the transparent mode, the input signal is band limited to 3500 Hz. Frequencies form 0 - 300 Hz are not filtered out.

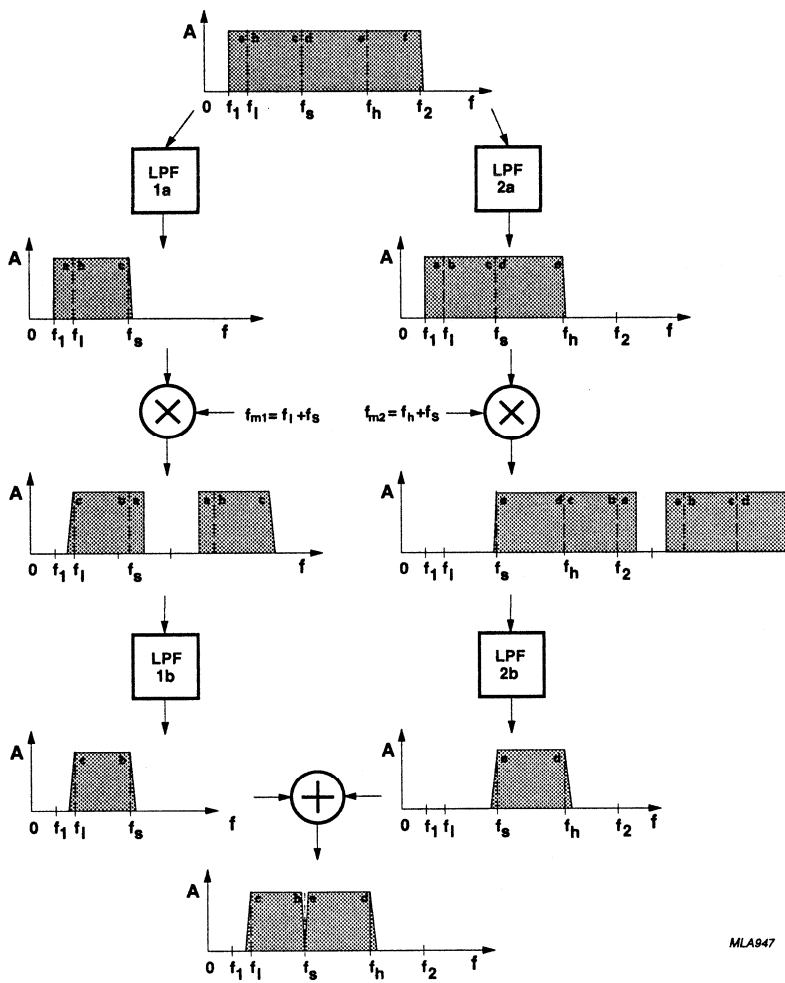


Fig.3 Scrambler signal path.

APPLICATIONS

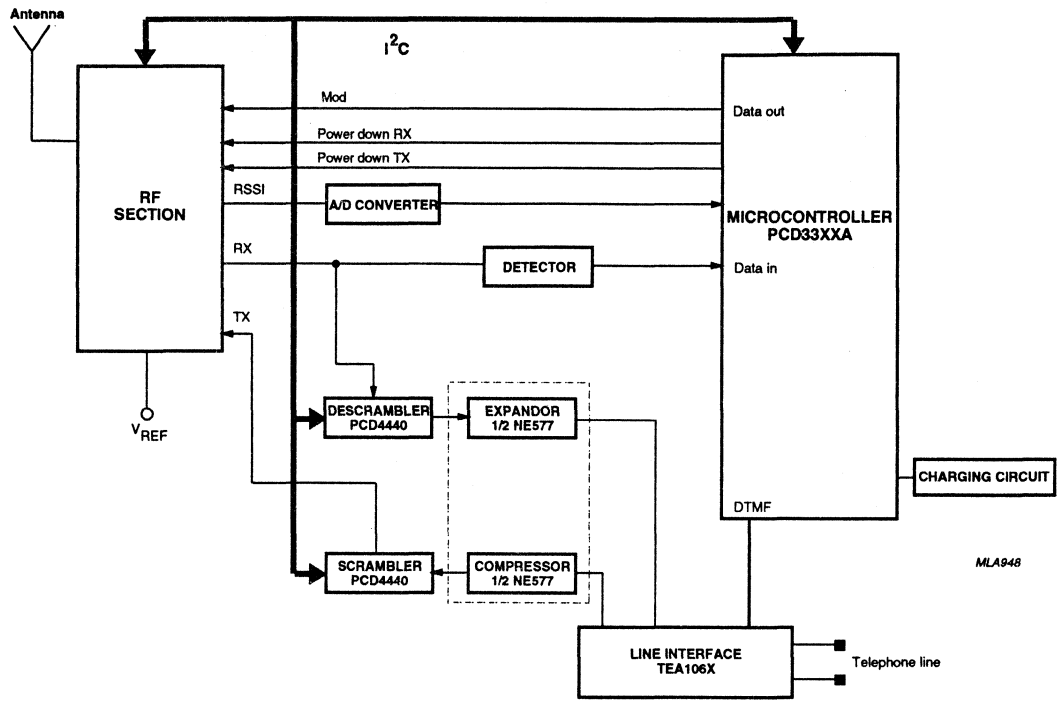


Fig.4 CT0 handset with direct (Manchester code) data system.

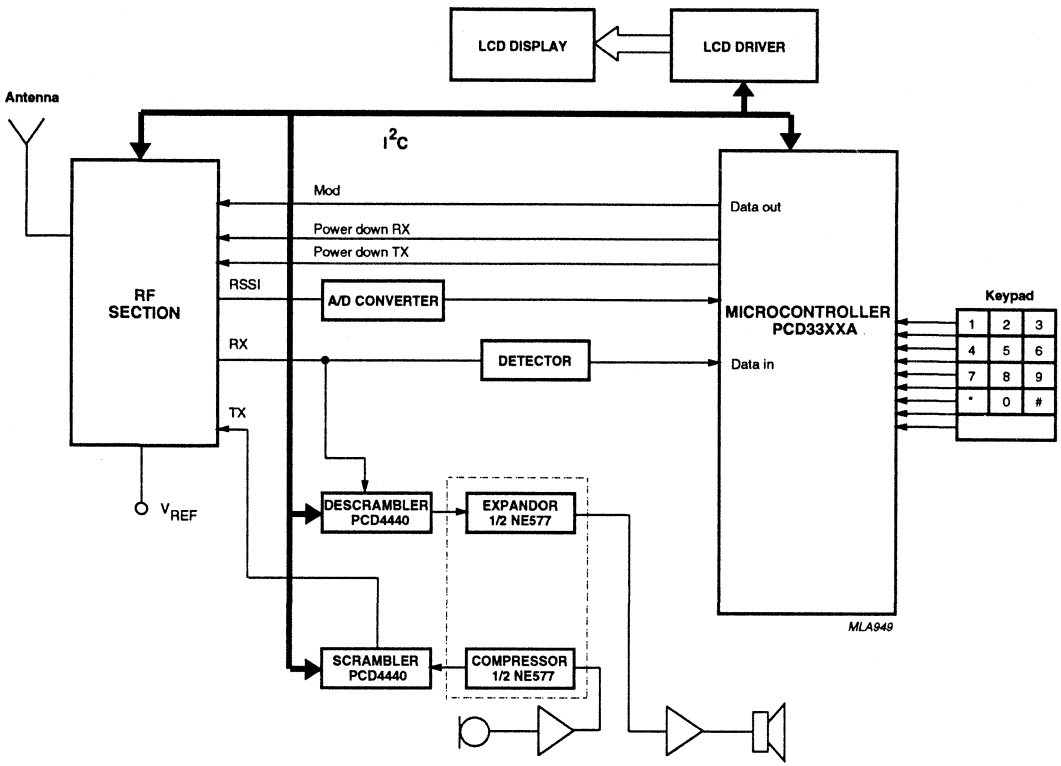


Fig.5 CT0 Base unit with direct (Manchester code) data system.

HANDLING

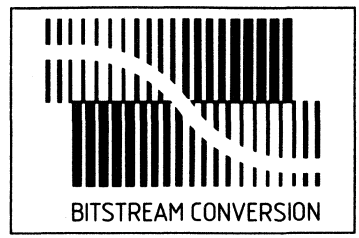
Handling MOS devices
Inputs and outputs are protected against electrostatic discharge in normal handling. However, it is good practice to take normal precautions appropriate to handling MOS devices.

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

ADPCM CODEC for digital cordless telephone

PCD5032



FEATURES

- G.721 compliant ADPCM encoding and decoding
- BITSTREAM analog-to-digital and digital-to-analog decoding
- On-chip receive and transmit filter
- On-chip ringer and tone generator
- Programmable gain of receive and transmit path
- Serial ADPCM interface with independent timing for maximum flexibility
- Linear PCM data accessible for digital echo cancelling
- Programmable via I²C-bus interface
- Fast receiver mute input via pin
- On-chip reference voltage
- On-chip symmetrical supply for electret microphone
- Few external components
- Low power consumption in standby mode
- Low supply voltage (single supply 2.7 V up to 6 V)
- CMOS technology

APPLICATIONS

- Digital European Cordless Telephony (DECT)
- CT2 cordless

GENERAL DESCRIPTION

The PCD5032 is a CMOS device designed for use in Digital European Cordless Telephone systems (DECT) but is also suitable for other cordless telephony applications (e.g. CT2). The PCD5032 performs analog-to-digital and digital-to-analog conversion, ADPCM encoding and decoding compliant to CCITT recommendation G.721 (blue book 1988). The PCD5032 contains on-chip microphone and earpiece amplifiers. The device can be used in both handset and base station designs.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCD5032	44	QFP44S14	plastic	SOT205AG

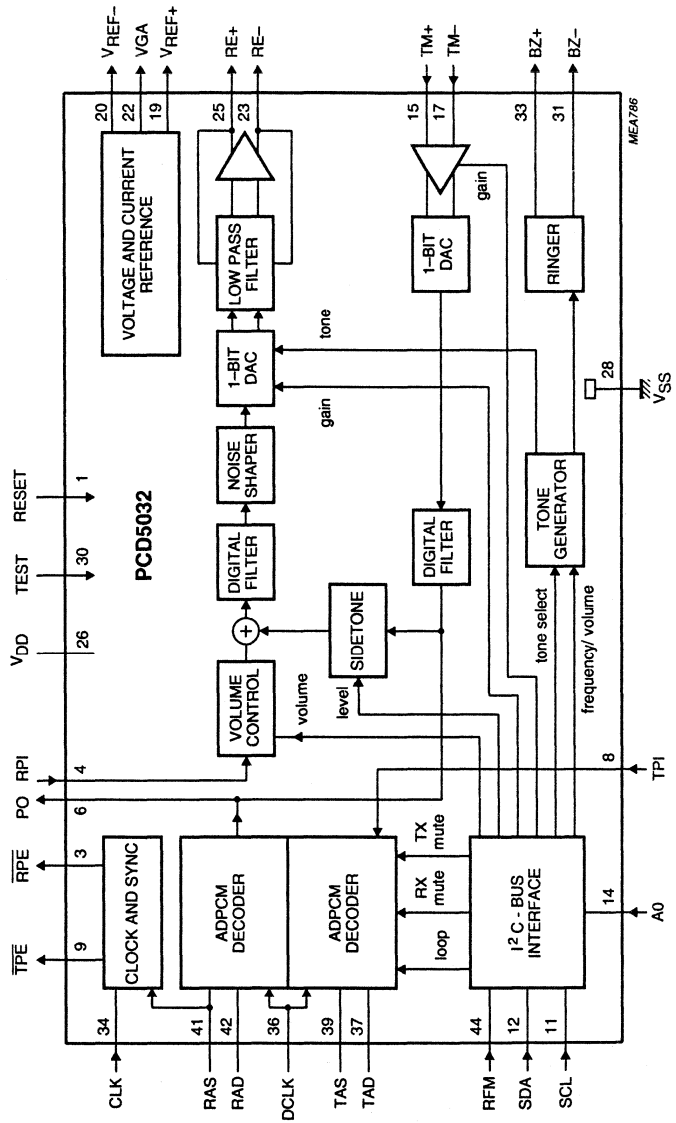


Fig.1 Block diagram.

PINNING

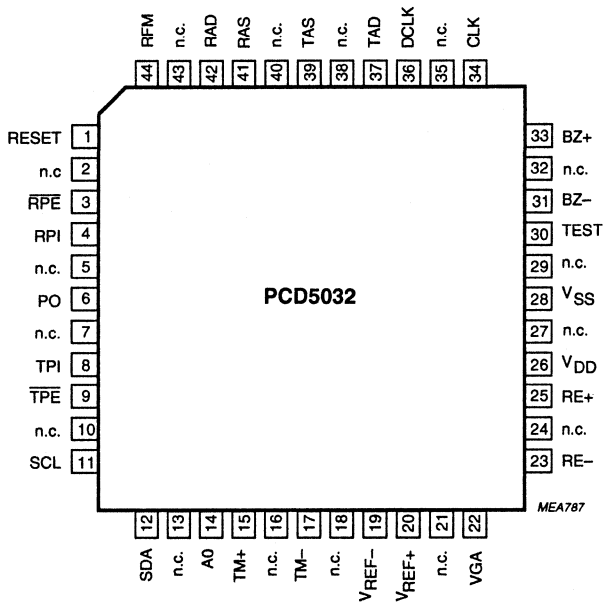


Fig.2 Pin configuration.

SYMBOL	PIN	DESCRIPTION
RESET	1	reset input; active HIGH
n.c.	2	not connected
$\overline{\text{RPE}}$	3	receiver PCM output enable (active LOW) ; direction from ADPCM interface to earpiece
RPI	4	receiver PCM input; direction from ADPCM interface to earpiece
n.c.	5	not connected
PO	6	PCM data output
n.c.	7	not connected
TPI	8	transmitter PCM input; direction from microphone to ADPCM interface
$\overline{\text{TPE}}$	9	transmitter PCM output enable (active LOW); direction from microphone to ADPCM interface
n.c.	10	not connected
SCL	11	serial clock input; I²C-bus
SDA	12	serial data input; I²C-bus
n.c.	13	not connected
A0	14	address select input; I²C-bus

SYMBOL	PIN	DESCRIPTION
TM+	15	transmitter audio positive input (microphone)
n.c.	16	not connected
TM–	17	transmitter audio negative input (microphone)
n.c.	18	not connected
V_{REF-}	19	negative reference voltage output; internally generated, intended for electret microphone supply
V_{REF+}	20	positive reference voltage output; internally generated, intended for electret microphone supply
n.c.	21	not connected
VGA	22	analog signal ground output
RE–	23	receiver audio negative output (earpiece)
n.c.	24	not connected
RE+	25	receiver audio positive output (earpiece)
V_{DD}	26	positive supply voltage (2.9 V to 6 V)
n.c.	27	not connected
V_{SS}	28	negative supply voltage (0 V)
n.c.	29	not connected
TEST	30	test mode input; to be connected to V_{SS} in normal application
BZ–	31	ringer negative output
n.c.	32	not connected
BZ+	33	ringer positive output
CLK	34	clock input
n.c.	35	not connected
DCLK	36	data clock input (ADPCM)
TAD	37	transmitter ADPCM data output; direction from microphone to ADPCM interface
n.c.	38	not connected
TAS	39	transmitter ADPCM sync input; direction from microphone to ADPCM interface
n.c.	40	not connected
RAS	41	receiver ADPCM sync input; direction from ADPCM interface to earpiece
RAD	42	receiver ADPCM data input; direction from ADPCM interface to earpiece
n.c.	43	not connected
RFM	44	receiver fast mute input; direction from ADPCM interface to earpiece

Note to the pin description

1. Pins 19, 20, 22, 26 and 28 are general pins.
   Pins 15, 17, 23, 25, 31 and 33 are analog pins.
   Pins 1, 3, 4, 6, 8, 9, 11, 12, 14, 30, 34, 36, 37, 39, 41, 42 and 44 are digital pins.

APPLICATION INFORMATION

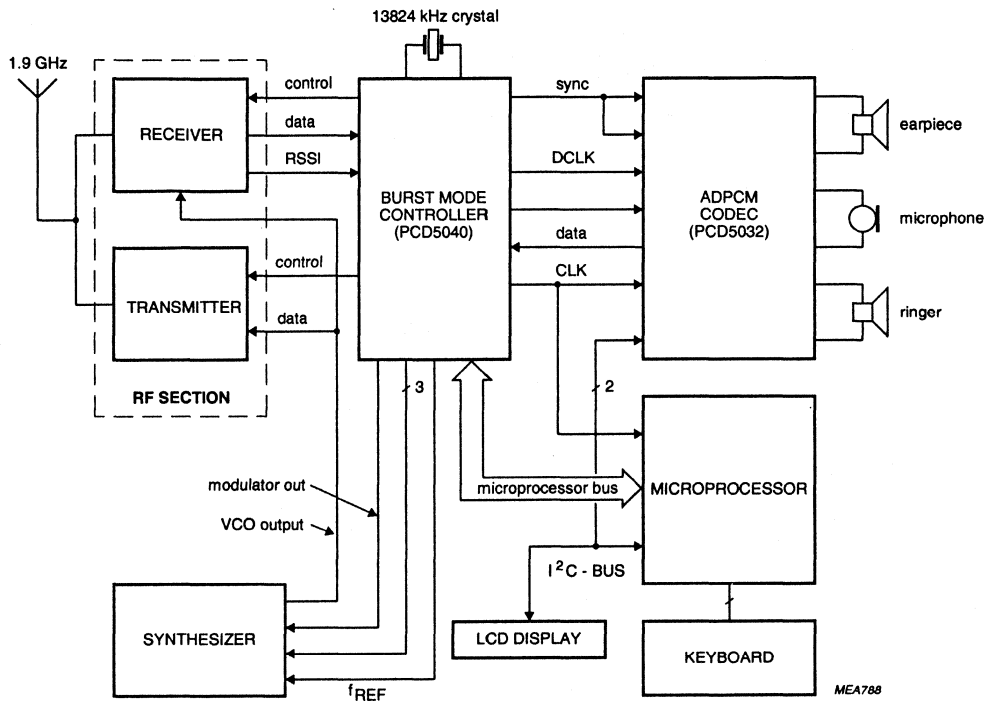


Fig.3 Typical block diagram for a DECT handset.

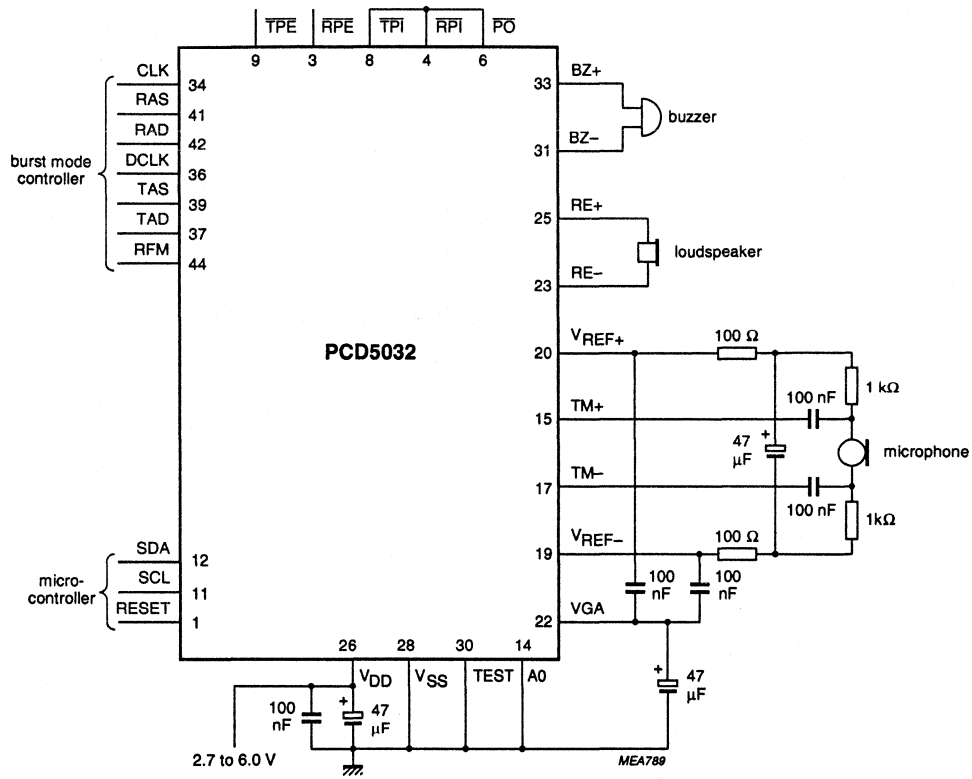


Fig.4 Typical handset application diagram for the PCD5032.

DECT burst mode controller PCD5040/PCD5041

FEATURES

- An embedded RISC controller (PCC) with 4 k byte (RAM/ROM) program memory for implementation of Traffic Bearer Control (TBC), MAC message handling, scanning and the general control of the BMC hardware
- PP and FP modes
- TDMA frame (de)multiplexing
- Encryption
- Scrambling
- CRC generation and checking
- Beacon transmission control
- Switches up to 12 simultaneous active speech channels from speech interface to 1152 kbs radio interface, and vice versa
- RSSI measurement with on-chip peak/hold detector and 4-bit ADC
- Local call switching for up to 6 internal calls
- Quality control report
- Digital Phase-Locked Loop
- Synchronization (handset to active bearer, base station to cluster of RFPs)
- Seamless handover procedure
- Fast (hardware) and slow (software) mute function
- 1.5 k byte extended RAM memory for the handset
- On-chip crystal oscillator (13.824 MHz)
- Programmable microcontroller clock frequency
- Programmable interrupts
- Low power consumption in standby mode
- Low supply voltage (2.7 V to 6 V)
- SACMOS technology

Interfaces to:

- 1 ADPCM codec in the handset mode of operation
- Up to 2 ADPCM codecs in a simple base station (with up to 2 analog lines)
- 2048 kb/s highway interface for systems requiring more than 2 connections to the network
- Radio head
- 80C51-type microcontroller, or a 68000-type microcontroller
- Programmable synthesizer interface (8, 16, 24 bits)

GENERAL DESCRIPTION

The PCD5040/PCD5041 DECT Burst Mode Controller (BMC) is a custom IC that performs the DECT physical layer and Medium Access Control layer (MAC) time critical functions for application in DECT handset and base station products which comply with the following standards (plus updates):

- DECT CI part 2; physical layer (DE/RES 3001-2)
- DECT CI part 3; medium access control layer (DE/RES 3001-3)
- DECT CI part 7; security features for DECT (DE/RES 3001-7)
- DECT CI part 9; public access profile (DE/RES 3001-9)

The BMC is designed to be connected to an ADPCM codec (PCD5032) and an 8051-type microcontroller without glue logic. Other codecs and microcontrollers (e.g. 68000-family) are also supported. Two versions of the BMC will become available. The PCD5040 will have a RAM supported memory containing the BMC firmware, while the PCD5041 has a ROM instead. Both versions have the same pinning.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCD5040/PCD5041	64	QFP64REC	plastic	SOT208A

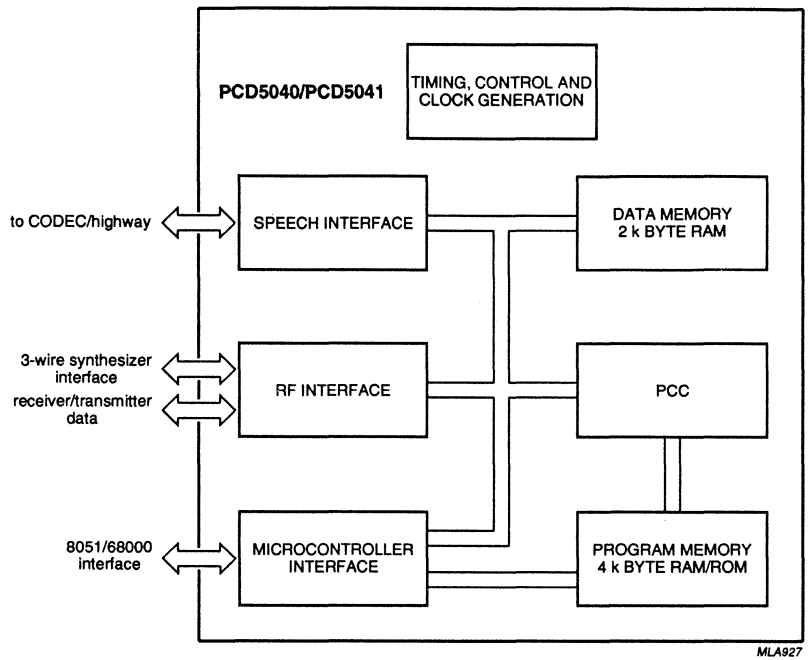


Fig.1 Block diagram.

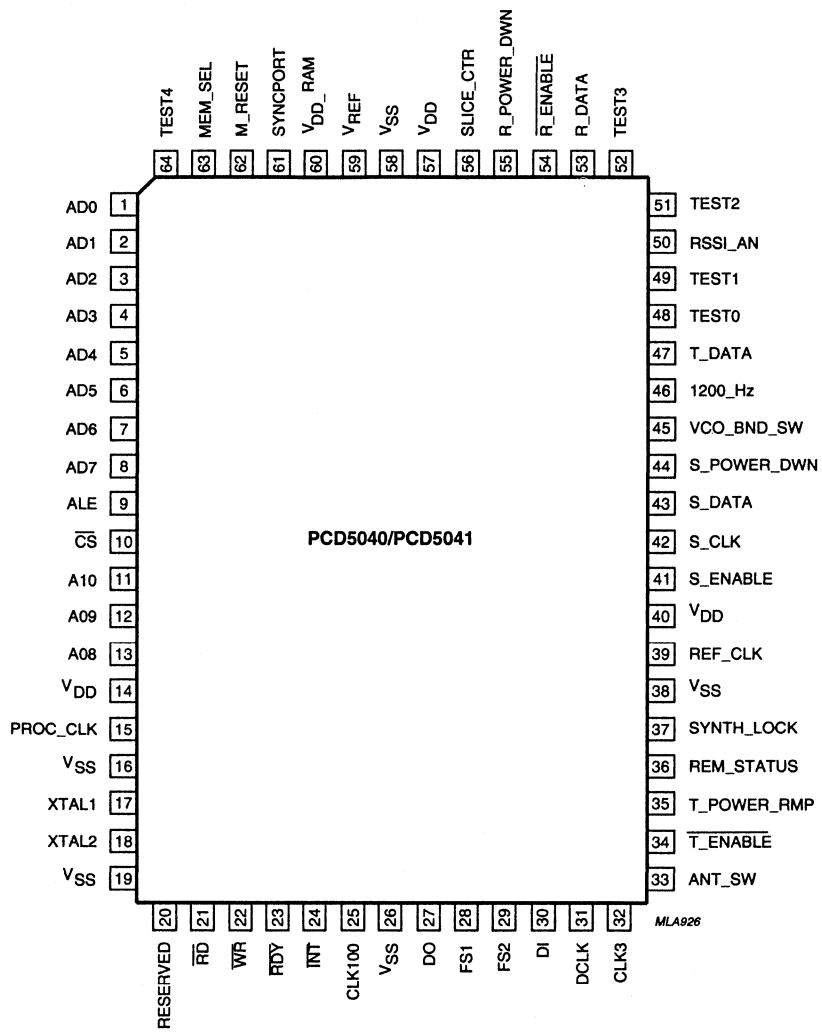


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
AD0 to AD7	1 to 8	address/data bus input/output lines
ALE	9	address latch enable input
$\overline{CS}$	10	chip select input; active LOW
A10 to A8	11 to 13	address bus input lines
V_{DD}	14	positive supply voltage
PROC_CLK	15	microcontroller clock output; programmable from $f_{CLK/96}$ to f_{CLK}, where f_{CLK} is the crystal oscillator frequency
V_{SS}	16	negative supply voltage
XTAL1	17	crystal oscillator input
XTAL2	18	crystal oscillator output
V_{SS}	19	negative supply voltage
RESERVED	20	reserved
$\overline{RD}$	21	read input; active LOW
$\overline{WR}$	22	write input; active LOW
$\overline{RDY}$	23	ready signal output; active LOW, to initiate wait states in the microcontroller
$\overline{INT}$	24	interrupt output; active LOW
CLK100	25	100 Hz frame timer output
V_{SS}	26	negative supply voltage
DO	27	3-state data output on the speech interface
FS1	28	8 kHz framing signal output to ADPCM codec 1 for simple base plus handset, otherwise 8 kHz framing input
FS2	29	8 kHz framing signal output to ADPCM codec 2 in the base station mode
DI	30	data input on the speech interface
DCLK	31	1152 kHz data clock output for simple base plus handset, otherwise 2048 kHz data clock input signal
CLK3	32	3.456 MHz clock output; nominal value, used to adjust system timing
ANT_SW	33	switch output; selects one of two antennas
$\overline{T\_ENABLE}$	34	transmitter enable input; active LOW
T_POWER_RMP	35	transmitter power ramp control output
REM_STATUS	36	8-bit serial data input; can be read in for each s-lot
SYNTH_LOCK	37	lock indication input from synthesizer
V_{SS}	38	negative supply voltage
REF_CLK	39	reference frequency output for the synthesizer; i.e. the crystal oscillator clock f_{CLK}
V_{DD}	40	positive supply voltage
S_ENABLE	41	synthesizer enable output
S_CLK	42	clock signal output; to be used with S_DATA
S_DATA	43	serial data output to the synthesizer
S_POWER_DWN	44	synthesizer power down control output

SYMBOL	PIN	DESCRIPTION
VCO_BND_SW	45	VCO bandswitch control signal output
1200_Hz	46	control signal output for dual synthesizer schemes
T_DATA	47	serial data output to transmitter
TEST0	48	input to select test mode 0; normal operation set to logic 0
TEST1	49	input to select test mode 1; normal operation set to logic 0
RSSI_AN	50	analog input signal for basic DECT systems; peak signal strength measured after a low-pass filter
TEST2	51	input to select test mode 2; normal operation set to logic 0
TEST3	52	input to select test mode 3; normal operation set to logic 0
R_DATA	53	receive data input
$\overline{\text{R\_ENABLE}}$	54	receiver enable output; active LOW
R_POWER_DWN	55	receiver power down output
SLICE_CTR	56	slice time constant control output
V_{DD}	57	positive supply voltage
V_{SS}	58	negative supply voltage
V_{REF}	59	reference input fot the ADC
V_{DD}_RAM	60	positive supply voltage for data RAM
SYNCPORT	61	this signal is the SYNCPORT input/output in the base station; it is an output in a master base station, input in a slave base station, in accordance with Annex C, DECT CI specification part 2. SYNCPORT is not active in the handset
M_RESET	62	BMC master reset input signal
MEM_SEL	63	input to select PCC program memory at the microcontroller interfcae
TEST4	64	input to select test mode 4; normal operation set to logic 0

POCSAG Paging Decoder PCF5001T

FEATURES

- Wide operating supply voltage range (1.5 V to 6.0 V)
- Extended temperature range: –40 to +85 °C (between –40 to –10 °C, minimum supply voltage restricted to 1.8 V), see section Limiting Values
- Very low supply current (60 μA typ. with 76.8 kHz crystal)
- Decodes CCIR Radio paging Code No.1 (POCSAG-Code)
- Programmable call termination conditions
- 512 and 1200 bit/s data rates (2400 bit/s with some restrictions), see section Decoding of the POCSAG data stream
- Improved ACCESS synchronization algorithm
- Supports 4 user addresses (RICs) in two independent frames
- Eight different alert cadences
- Directly drives magnetic or piezo ceramic beeper
- High level alert requires only a single external transistor
- Optional vibrator type alerting
- Silent call storage, up to eight different calls
- Repeat alarm facility
- Programmable duplicate call suppression
- Interfaces directly to UAA2033T, UAA2050T and UAA2080 digital paging receivers
- Programmable receiver power control for battery economy
- On-chip non-volatile EEPROM storage
- On-chip voltage converter with improved drive capability
- Serial microcontroller interface for display pager applications
- Optional visual indication of received call data using a modified RS232 format
- Level shifted microcontroller interface signals
- Alert on low battery
- Optional out-of-range indication.

APPLICATIONS

- Alert-only pagers, display pagers
- Telepoint
- Telemetry/data receivers.

GENERAL DESCRIPTION

The PCF5001T is a fully integrated low-power decoder and pager controller. It decodes the CCIR Radio paging Code No.1 (POCSAG-Code) at 512 and 1200 bit/s data rates. The PCF5001T is fabricated in SACMOS technology to ensure low power consumption at low supply voltages.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF5001T	28	mini-pack	plastic	SOT136A

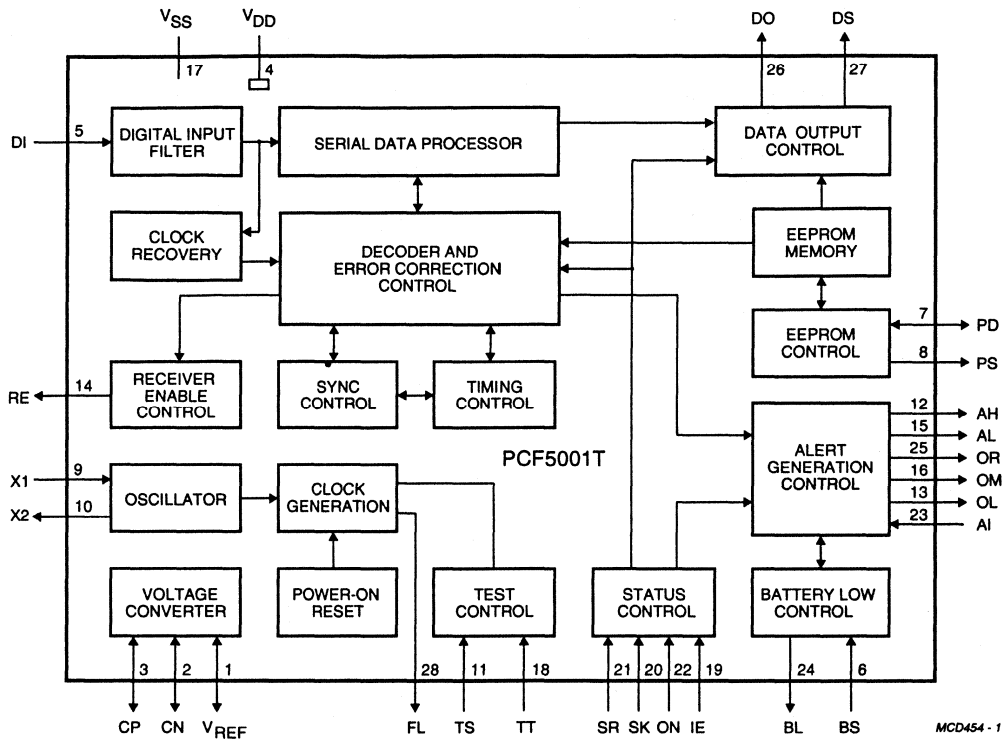


Fig.1 Block diagram.

PINNING

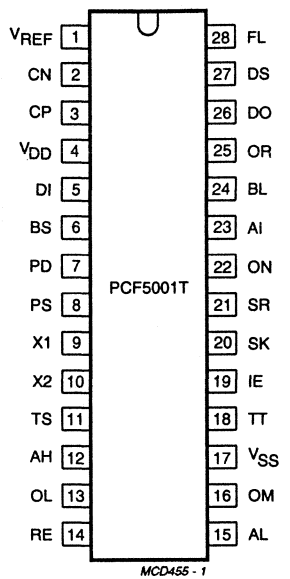


Fig.2 Pin configuration.

SYMBOL	PIN	I/O	DESCRIPTION
V_{REF}	1	O	microcontroller interface reference voltage. The LOW level of pins FL, DS, DO, OR, BL, AI, ON, SK, SR and IE is related to the voltage on V_{REF}. May be driven from an external negative voltage source or must be connected to V_{SS}, if pins CN and CP are left open-circuit. When the on-chip voltage converter is used, this pin provides a negative output voltage.
CN	2		voltage converter external shunt capacitance, negative side. Connect the negative side of the shunt capacitor to this pin, if the on-chip voltage converter function is used.
CP	3		voltage converter external shunt capacitor, positive side. Connect the positive side of the shunt capacitor to this pin, if the on-chip voltage converter function is used.
V_{DD}	4		main positive power supply. This pin is common to all supply voltages and is referred to as 0 V (common).
DI	5	I	serial data input (POCSAG code). The serial data signal train applied to this pin is processed by the decoder. Pulled LOW by an on-chip pull-down when the receiver is disabled (RE = LOW).
BS	6	I	battery low indication input. The decoder samples this input during synchronization scan, when it is in ON or SILENT status and the receiver is enabled (RE = HIGH). A battery low condition is assumed, if the decoder detects four consecutive samples HIGH. An audible battery low indication is made by the decoder, when operating in ON status. Normally LOW by the operation of an on-chip pull-down.

SYMBOL	PIN	I/O	DESCRIPTION
PD	7	I/O	EEPROM programming data input and output. Normally HIGH by the operation of an on-chip pull-up. During programming of the on-chip EEPROM, PD is a bi-directional data and control signal.
PS	8	I	EEPROM programming strobe input. Normally LOW by the operation of an on-chip pull-down. During programming of the on-chip EEPROM, PS is a uni-directional control input.
X1	9	I	crystal oscillator input. Connect a 32768 kHz or 76800 kHz crystal and a biasing resistor between this pin and X2. In addition, provide a load capacitance to V_{DD}, which may also be used for frequency tuning.
X2	10	O	crystal oscillator output. Return connection for the external crystal and resistor at X1.
TS	11	I	scan test mode enable input. Always LOW by operation of an on-chip pull-down.
AH	12	O	alert high-level output. This output can directly drive an external bipolar transistor to control high-level alerting in conjunction with AL, by means of an alerter or beeper.
OL	13	O	LED indication output. This output can directly drive an external bipolar transistor to control the visual alert function by means of a LED. It may also be used for visual indication of received call data during call reception.
RE	14	O	receiver enable output. May be used to control the paging receiver power control input, to minimize power consumption. The decoder provides a HIGH level at this pin, when receiver operation is requested. Each time the decoder does not require any input data at DI the receiver enable output is LOW.
AL	15	O	alert low-level output. Open drain alert output in anti-phase to AH, to provide low-level alerting. High-level alerting is generated in conjunction with AH.
OM	16	O	vibrator output. This output can directly drive an external bipolar transistor to control a vibrator type alerter.
V_{SS}	17		main negative supply voltage.
TT	18	I	test mode enable input. Always LOW by operation of an on-chip pull-down.
IE	19	I	interface enable input. While the interface enable input is active HIGH, operation of the ON, SK, SR, AI, BL and OR inputs and outputs is possible. When IE is LOW the inputs do not respond to applied signals and the outputs are made HIGH impedance. In alert only pager mode the interface enable input does not have any effect on the operation of inputs ON, SK and SR, but IE must be referenced to LOW or HIGH.
SK	20	I	silent state control input. The silent control input selects the decoder ON status (LOW level) or SILENT status (HIGH level), if the ON input is active HIGH. An on-chip pull-up is provided, if the decoder has been programmed for alert-only pager mode, whereby the pull-up is disabled for display pager mode. In display pager mode status change is possible provided the interface enable input (IE) is HIGH and the status is latched on the falling edge of IE.
SR	21	I	status request and reset input. A HIGH-going pulse on this input causes (a) status indication cadence to be generated, if the decoder is not alerting or (b) resetting of a call alert, repeated call alert or battery low alert, if active or (c) triggers the call store re-alert facility, if repeat mode is active. In display pager mode operation of SR is possible only, if the interface control input is active. Normally LOW by the operation of an on-chip pull-down.

SYMBOL	PIN	I/O	DESCRIPTION
ON	22	I	on/off control input. The on/off control input selects the decoder ON status (HIGH level) or OFF status (LOW-level). An on-chip pull-up resistor is provided, if the decoder has been programmed for alert-only pager mode, but the pull-up resistor is disabled for display pager mode. In display pager mode status change is possible provided the interface enable input (IE) is HIGH and the status is latched on the falling edge of IE.
AI	23	I	alarm input. A HIGH level on this input causes generation of a continuous high-level alert via AH and AL outputs, if the decoder operates in ON status or OFF status. In addition, the LED output is active independent from the decoder status, but in accordance with AI. Pulsing the input may be used to modulate the alert and LED indication. Normally LOW in alert-only pager mode by operation of an on-chip pull-down.
BL	24	O	battery low indication output. If the decoder encounters a battery low condition a battery low output latch is set HIGH. The battery low output latch may be tested for a battery low condition, whenever the interface enable input (IE) is active (HIGH), otherwise the battery low output is made HIGH impedance. The battery low output latch is reset only, by switching the decoder to OFF status.
OR	25	O	out-of-range indication output. Whenever the decoder detects an out-of-range condition a out-of-range output latch is set HIGH after expiry of the programmed out of range hold-off time selected by means of special programming (SPF06 and SPF07) of the EEPROM. The out-of-range latch may be tested for an out-of-range condition, whenever the interface enable input (IE) is active (HIGH), otherwise the out-of-range output is made HIGH impedance. The out-of-range output is reset by detection of a valid data transmission or by switching the decoder to OFF status.
DO	26	O	serial interface data output. During normal decoder operation, accepted calls and possibly subsequent message data are serially output via this pin in conjunction with the data strobe output (DS). This pin is also used to output the EEPROM contents upon special command, if the decoder is programmed for display pager.
DS	27	O	serial interface data strobe output. Provides a clock signal for the received call data and EEPROM data appearing at the data output (DO). Each time this output is LOW the data at DO is valid. Additional start and stop conditions allow easy identification of data sequence start and end.
FL	28	O	frequency reference output. When programmed for display pager mode, this output provides a clock reference with 16384 cycles or 32768 cycles per second, selected by SPF32. See section EEPROM Read Operation.

FUNCTIONAL DESCRIPTION

The PCF5001T is a very low power Decoder and Pager Controller specifically designed for use in new generation Radio pagers. The architecture of the PCF5001T allows for flexible application in a wide variety of Radio pager designs.

The PCF5001T is fully compatible with CCIR Radio paging Code Number 1 (also known as the POCSAG code) operating at the originally specified 512 bps data rate, and also at the newly specified 1200 bps data rate. 2400 bps operation is also possible. The PCF5001T also offers features which extend the basic flexibility and efficiency of this code standard.

The PCF5001T supports two basic modes of operation:

In Alert-Only-Pager mode only a minimum number of external components are required to build a complete tone-only pager. Selection of operating states ON, OFF or SILENT is acieved using a slider switch interface.

In Display-Pager mode the state input logic is switched to a bus interface structure. Received calls and messages are transferred to an external microcontroller via the serial microcontroller interface. A built-in voltage converter with increased drive capabilities can supply doubled supply voltage output, and appropriate logic level shifting on microcontroller interface signals is provided.

Upon reception of valid calls one of eight different call cadences is generated; upon status interrogation status indication tones make the current status of the decoder available to the user.

On-chip non-volatile 114-bit EEPROM storage is provided to hold up to four user addresses, two frame numbers and the programmed decoder configuration.

Synchronization to the input data stream is achieved using the improved ACCESS algorithm, which allows for data synchronization and re-synchronization without preamble detection while minimizing battery power consumption by receiver power control. One of four error correction algorithms is applied to the received data to optimize the call success rate.

The POCSAG paging code

A transmission using the CCIR Radio paging Code No.1 (POCSAG code) is constructed in accordance with the following rules, see Fig.3.

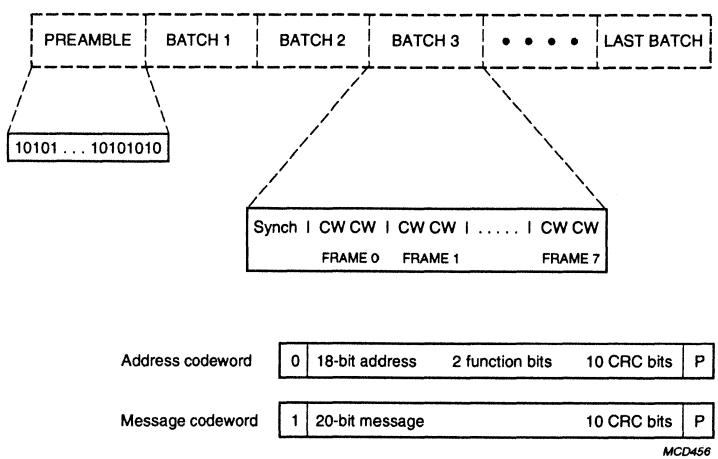


Fig.3 POCSAG code structure.

The transmission is started by sending a preamble, which is a sequence of at least 576 continually alternating bits (10101010...). The preamble precedes a number of batch blocks. The transmission is terminated after the last batch.

Each batch comprises a synchronization codeword with a fixed 32-bit pattern followed by eight frames (numbered 0 to 7). Only complete batches are transmitted.

A frame consists of two codewords, each 32-bits long. A codeword is either an address or a message or an idle codeword. Idle codewords are transmitted to fill empty batches or to separate messages.

An address codeword is coded as shown in Fig.3. The upper 18-bits of the 21-bit digital user address (or RIC = Receiver Identification Code) are coded in the codeword itself (bits 2 to 19), which is protected against transmission errors by a number of CRC checkbits (bits 22 to 31). Bit 32 is a simple overall even-parity bit. The lower three bits of the digital user address are coded in the number of the frame, in which the address codeword is transmitted. Two function bits (bits 20 and 21) allow distinguishing of four different calls to one user address.

In a message codeword 20-bits of any display information can be put into the message bits, which are protected again by additional checkbits.

Modes and states of the decoder

The PCF5001T supports two basic operating modes: Alert-only pager and Display pager mode. Two further modes, the Programming mode and the Test mode, are implemented to program and verify the EEPROM contents and to support pager production and approval tests, respectively.

In Alert-only pager mode no external microcontroller is required, see Fig.19. A three position slider switch interface is provided to select the internal state of the decoder. The decoder performs regular scanning of the switch inputs to detect a status change. A push-button interface is provided on the SR input, which is used as input for user acknowledgment actions and status interrogation. Upon reception of valid calls, tone alert cadences are generated. A call storage is provided to store calls received while operating in Silent status and to recall cadences upon repeat mode operation. The voltage doubler and the frequency reference output are disabled in this mode.

In Display pager mode the PCF5001T operates as decoder and pager controller in combination with an external microcontroller, see Fig.20. The internal states of the decoder are determined by appropriate logic levels on the status inputs. A bus type interface structure is used to interface the decoder to the microcontroller. The decoder's on-chip voltage converter provides doubled supply voltage output to provide a higher supply voltage to the microcontroller and any additional hardware. The logic levels of the interface's input and output signals are level shifted to allow for direct coupling between microcontroller and the decoder. Upon detection of a valid call, address and message information are transferred to the external microcontroller using the serial microcontroller interface. In addition, appropriate call alert cadences are generated.

If the decoder is in one of the two operating modes, it is always in one of the following three internal states:

- OFF status. This is the power saving, inactive status of the PCF5001T. The paging receiver is disabled, no decoding of input data takes place. However, the crystal oscillator is kept running to ensure that scanning of the status inputs/status switch is maintained to allow changing into one of the following two active states.
- ON status. This is the normal active status of the decoder. Incoming calls are compared with the user addresses stored in the internal EEPROM. Upon detection of valid calls, alert cadences and LED indication are generated and data is shifted out at the serial microcontroller interface.
- SILENT status. The Silent status is the same as the On status with the exception that valid calls no longer cause generation of call alert cadences. Instead, if programmed as alert-only pager, the decoder stores up to eight different calls and generates appropriate alert cadences after the decoder has been put back into the On status. However, special silent override calls will cause generation of alert cadences, if enabled.

The decoder operating status is selected as indicated in Table 1.

When programmed for alert-only pager a switch debounce period is applied to the status inputs. For status change and status interrogation in display pager mode, see Figs 4 and 5.

Table 1 Truth table for decoder operating status.

ON INPUT	SK INPUT	OPERATING STATUS
0	0	OFF
0	1	OFF (EEPROM transfer mode; note 1)
1	0	ON
1	1	SILENT

Note to Table 1

1. The EEPROM transfer mode applies to display pager mode only.

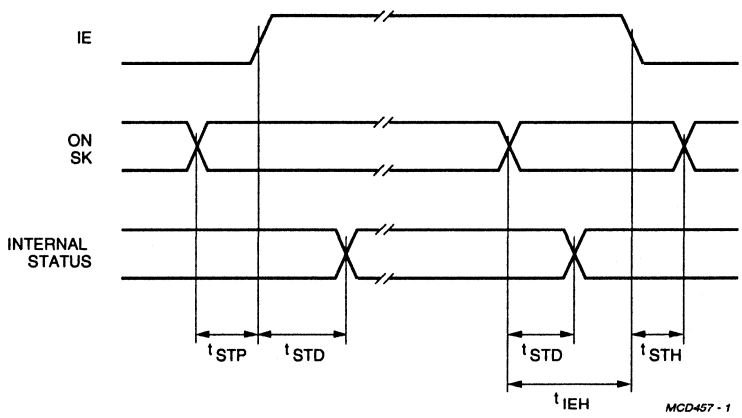


Fig.4 Status change in display pager mode.

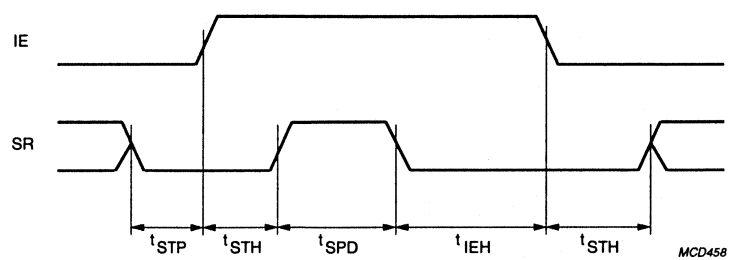


Fig.5 Status interrogation in display pager mode.

Decoding of the POCSAG data stream

The POCSAG coded input data stream is first noise filtered by a digital filter. From the filtered data a sampling clock synchronous to the data rate is derived. The PCF5001T supports 512-bit/s and 1200-bit/s data rates. This results in a 512 Hz or 1200 Hz sampling clock frequency, respectively. Synchronization on the POCSAG code structure is performed using the improved Philips ACCESS algorithm, which employs a state machine with six internal states.

A data rate of 2400-bit/s is possible if an external clock generator of 153.6 kHz is connected to X1. The minimum supply voltage is then 1.8 V.

The receiver enable output is activated a period equal to t_{RXON} before the input data is actually needed.
The decoder has first to achieve bit and word synchronization before it can receive calls. The algorithm searches first for the preamble and then for synchronization codeword patterns. This is carried out for the duration of 3 batches in Power-on mode or 1 batch (= preamble duration) in Preamble Receive mode. Error correction algorithms are applied to the data before it is compared with preamble and synchronization codeword patterns. The synchronization process is terminated and thus Data Receive mode entered as soon as synchronization codewords are seen at the beginning of each batch.
The decoder handles loss of synchronization in three steps: if the decoder fails to detect the synchronization pattern at the beginning of the current batch it continues data reception as normal. This Data Fail mode is signalled in the message output when an address codeword was received, as shown in Table 4. If also at the beginning of the next batch no synchronization codeword can be detected, the algorithm assumes a small bit shift in the Fade Recovery mode and performs more synchronization codeword checks around the expected position for the following 15 batches. Call reception is suspended. If it fails to re-synchronize in the Fade Recovery mode, the Carrier Off mode is selected, in which the decoder attempts to regain synchronization by bit-wise shifting its synchronization scan window. Using this technique re-synchronization is obtained within a continuous data stream of at least 18 batches without preamble detection.

In Data Receive mode, the input data stream is sampled at the synchronization codeword position and the programmed frame positions. The received codewords are error corrected and then, if address codewords, compared with the stored user addresses related to that frame. On detection of a valid call, the decoder performs the following three operations:

1. Set a store for call alert cadence generation according to the combination of the function bits in the accepted address codeword. The call alert cadence will not be generated before the call has been terminated.
2. Keep the receiver enable output (RE) active and receive subsequent message codewords, until any of the call termination criteria are fulfilled.
3. Trigger the serial message transfer by sending a start condition and transfer deformatted message codewords as attached to the address codeword via the serial microcontroller interface to an external microcontroller, followed by a stop condition.

Normally call termination is assumed, when a valid idle or address codeword is received. On reception of uncorrectable codewords, call termination takes place in accordance with conditions shown in Table 2.

Generation of output signals

The PCF5001T provides output indications for call alert, repeat mode alert, out of range alert, battery low alert, status indication alert and start-up alert. Some of the alert functions may be freely configured by programming of SPF bits within the EEPROM. Table 3 shows the outputs which are used for special output indications, if the decoder operates in ON status.

Note:

Reception of special silent override calls causes the decoder to generate call alert indication via AL and AH even if it operates in SILENT status.

Table 2 Call termination on error.

SPF12	SPF13	CALL TERMINATION EVENT
0	X	any two consecutive codewords or the codeword directly following the address codeword uncorrectable
1	0	any single codeword uncorrectable
1	1	any two consecutive codewords uncorrectable

Table 3 Output signals.

ALERT FUNCTION	OUTPUT ACTIVE (note 1)					
	AL	AH	OL	OM	OR	BL
start-up	(yes)	–	yes	yes	–	–
status indication	yes	–	–	–	–	–
call reception	(yes)	(yes)	yes	SPF11	–	–
repeat mode	(SPF16)	(SPF16)	SPF16	–	–	–
out of range	–	–	SPF15	–	yes	–
battery low	(yes)	(yes)	–	–	–	yes
alarm input	(yes)	(yes)	yes	–	–	–

Note to Table 3

1. Entries in parenthesis are not valid, if the decoder operates in SILENT status.

Alerter

The PCF5001T provides the AL and AH outputs for acoustical low-level and high-level signalling. Low-level alerting is provided by the AL output only. For high-level alerting both, AL and AH are active in antiphase. The square-wave output signals produce tone alert cadences by means of a magnetic or piezo ceramic beeper. The alert frequency, 2048 Hz or 2731 Hz square-wave, is selected by programming of SPF31.

When valid calls are received while operating in ON status, the PCF5001T generates call alert cadences. The first four seconds are generated at low-level, a further twelve seconds are generated at high-level. Alert tone generation and LED indication automatically terminate after sixteen seconds unless terminated by pulsing the status request and reset input (SR). Call alert generation is inhibited until completion of message codeword reception and the termination word is sent by the decoder. Call alert generation commences after an alert delay period, t_{ALD}, at the earliest, see Fig.6. Call alert deletion is possible during the alert delay period.

The call alert cadence is modulated according to the two function bits (FC) in the received address codeword, see Fig.7.

Valid calls received on RIC B or RIC D cause the alerter frequency to be warbled by means of an additional 16 Hz and 1024 Hz signal (respective 1365 Hz for SPF31 = 1) as opposed to RIC A and RIC C where no alert frequency warble takes place. Thus, eight different call cadences are distinguishable.

On status interrogation by the status request and reset input (SR) the PCF5001T generates a status cadence at low-level, in accordance with the present internal decoder status, see Fig.8.

When detecting a battery low condition the PCF5001T provides a battery low indication. Operating in ON status causes generation of a battery low alert at high-level for sixteen seconds or until terminated by pulsing SR. Operating in SILENT status or repeat mode the battery low alert is stored and inhibited until switching to ON status.

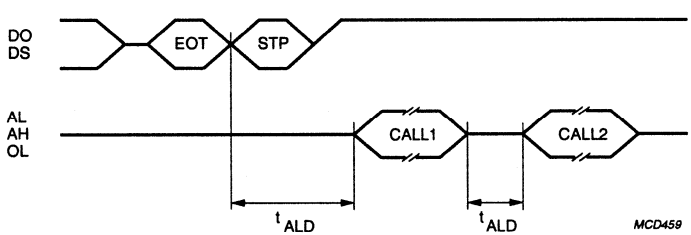


Fig.6 Call alert delay.

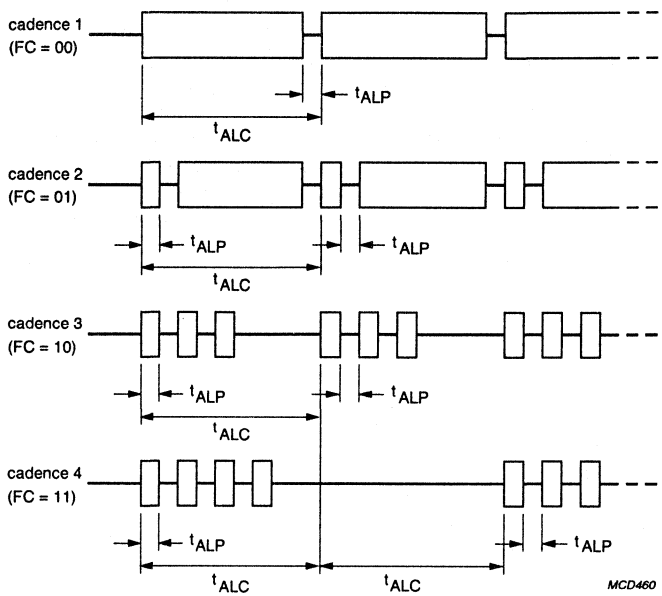


Fig.7 Call alert cadences.

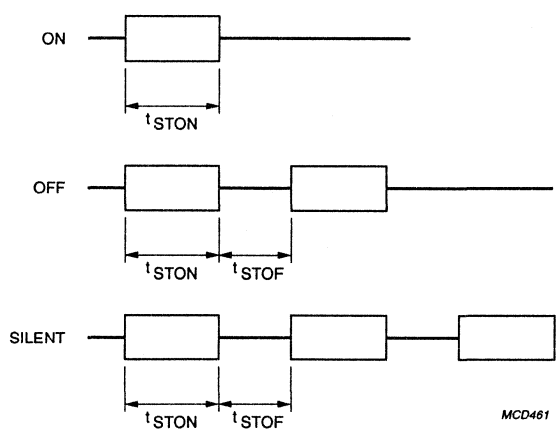


Fig.8 Status indication cadences.

Silent call storage and Repeat mode

When programmed for alert only pager the PCF5001T provides a call alert storage for storing of call alerts received during SILENT status or for call alerts which caused the decoder to enter Repeat mode. Call alert is not stored, when call indication is terminated by action of the status request and reset input (SR).

Allowing the call indication to time out by expiration of a sixteen second alert operation causes the Repeat mode to be entered, while operating in ON status or SILENT status. Such call alerts are stored for later repeated call alert on interrogation by the user. When Repeat mode has been entered and the decoder operates in ON status, the repeat call store is interrogated by pulsing the status request and reset input (SR) or on switching to ON status if the decoder operates in SILENT status. When silent override calls are received, which entered the Repeat mode, interrogation of repeat call store operates as in decoder ON status. After interrogation of repeat call store and subsequent generation of all stored call alerts the call store is cleared and the Repeat mode is terminated.

When programmed by means of SPF16, a repeat alert cadence is generated periodically, whenever Repeat mode has been entered. Operating in ON status causes the repeat alert cadence to be generated at high-level and warbled by means of an additional 16 Hz and 1024 Hz signal (respective 1365 Hz for SPF31 = 1) as shown in Fig.9. The LED output indicates the same alert cadence and alert warble. In SILENT status only the LED output is active.

No call alert storage occurs when the decoder is programmed for display pager mode.

Duplicate Call Suppression

The PCF5001T provides a Duplicate Call Suppression with time out facility, to identify duplicate call reception. When selected by programming of SPF14, the PCF5001T inhibits any duplicate call alert in alert-only pager mode. In display pager mode, duplicate call indication is achieved only via the serial microcontroller interface. A call is assumed to be duplicate if its address and function bit setting is equal to the latest received call, which initialized the call address and function bit reference. The Duplicate Call Suppression time out is selectable by programming of SPF06 and SPF07.

LED indicator

The PCF5001T provides for visual signalling using a LED via output OL.

Call alert indication is provided by the LED with the same cadence and warble modulation as for the alerter outputs AL and AH. Call alert indication occurs in ON and SILENT status and automatically terminates after sixteen seconds time out unless terminated by pulsing the status request and reset input (SR).

When detecting an out-of-range condition and enabled by programming of SPF15, the LED output provides an out-of-range indication as shown in Fig.10.

The LED output can be made to provide message data by programming SPF17. Alert signals are inhibited during message data transfer.

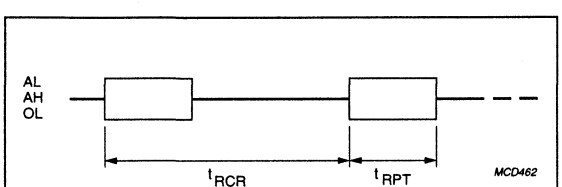


Fig.9 Repeat alert cadence.

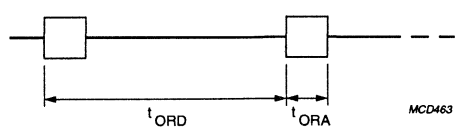


Fig.10 Out-of-range indication.

Vibrator output

The PCF5001T provides the OM output for activating a vibrator-type alerter for call alert indication. The vibrator output is enabled by programming of SPF11.

Calls received while operating in SILENT status cause activation of the vibrator output for the normal call alert cadence or until terminated by operation of the status request and reset input (SR). Silent override calls, calls received in decoder ON status and repeated call alerts are alerted normally by the AL and AH outputs.

Start-up alert

To indicate the establishment of operational condition whenever the decoder status has been changed from OFF to ON or SILENT status, the PCF5001T provides a start-up alert indication. Switching from OFF to ON status causes generation of a start-up alert cadence at low-level and on the LED output OL, see Fig.11.

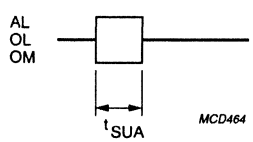


Fig.11 Start-up alert.

When changing from OFF to SILENT status, the start-up alert will be indicated on the LED output and the vibrator output OM.

Serial communication interface

To transmit any call message data received to an external microcontroller for post-processing, a serial communication interface has been provided by a serial data output signal DO and a data strobe signal DS as shown in Fig.13.

Upon interrogation the PCF5001T is also able to transfer EEPROM contents via the serial communication interface, see Section Read-Back operation via Microcontroller Interface.

Message data transfer

The transfer of message data via DO and DS is organized in 8–bit words providing additional start and stop conditions as shown in Fig.12.

On reception of a valid call address the PCF5001T generates a start condition and outputs an address word as shown in Fig.13 (a).

The address word indicates call address, function bit setting and decoder flags as shown in Table 4.

Message codewords received and concatenated to a valid call address are transferred after completion of the address word. The message bits received in the message codewords are split into blocks and are converted to obtain the message words. The message words comprise an error flag to indicate message words, which are derived from uncorrectable message codewords as shown in Table 5.

Message data is output at a rate of 2048 bps with a minimum delay of 2 bits between consecutive message words.

Termination of call reception causes a termination word to be transferred, which indicates successful or unsuccessful call termination as shown in Table 6.

Serial data transfer for a received call ends with a stop condition as shown in Fig.13 (c).

Call Data output on LED

When enabled by programming of SPF17 (= 1), message data will appear on the LED output OL. The data format and timing are equal to the signal on DO, except that the start/stop conditions are replaced with start/stop bits (respectively 1 and 0). The data format is shown in Fig.14. No alert signals will appear on OL during message data transfer.
Consecutive message words have a minimum separation of 1 start bit and 1 stop bit.

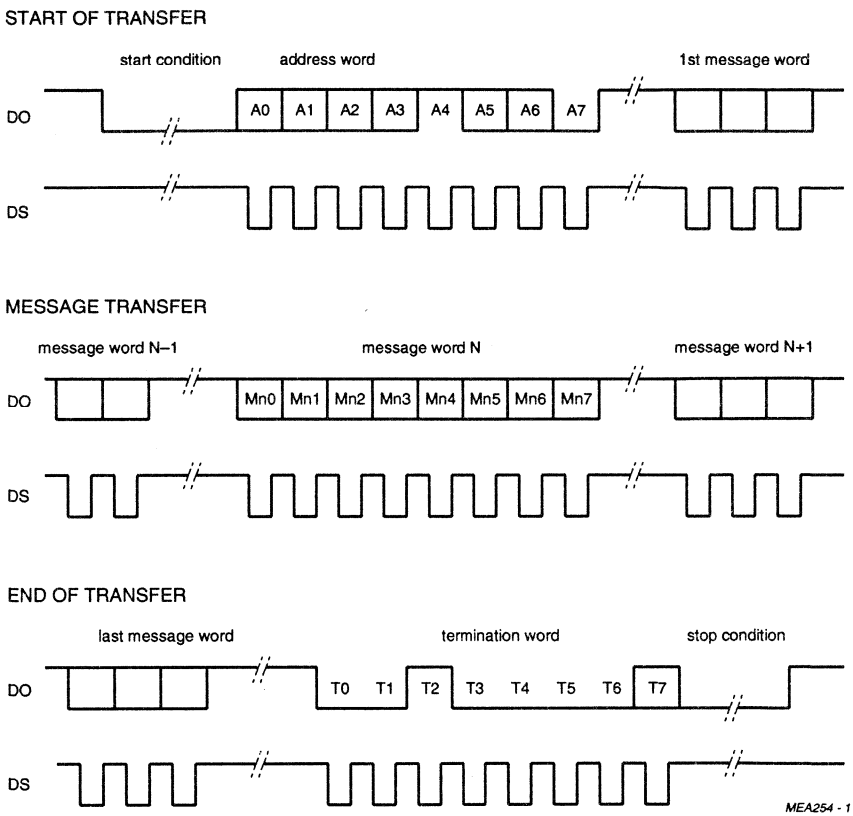
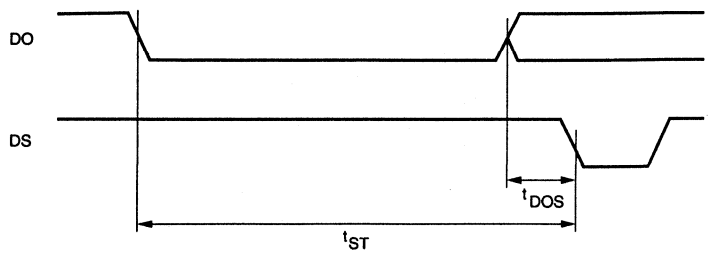
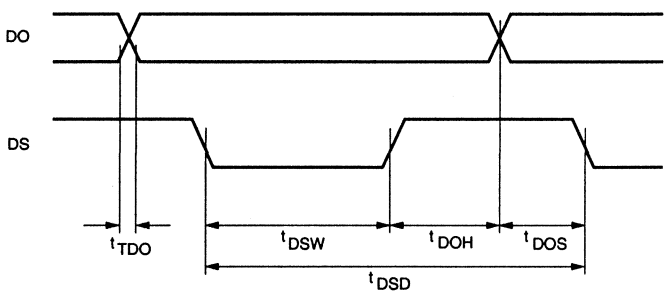


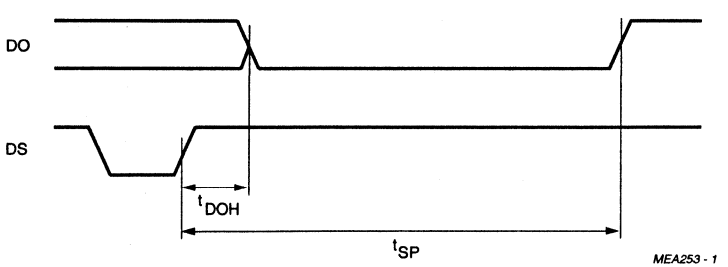
Fig.12 Call data transfer on the serial communication interface.



(a) Start condition



(b) Data bit



(c) Stop condition

Fig.13 Serial communication interface timing.

Serial communication call data format

Table 4 Address word format.

FUNCTION CODE		CALL ADDRESS				SYNC STATUS	DUPL CALL	
BIT 0 (LSB)	BIT 1 (MSB)	BIT 2	BIT 3	RIC	BIT 4	BIT 5	BIT 6	BIT 7
Bit 21 of address codeword	Bit 20 of address codeword	0	0	A	1	0 = Data Receive 1 = Data Fail	1 = Dupl Call time out active	0
		0	1	B				
		1	0	C				
		1	1	D				

Table 5 Message word format.

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7 (note 1)
LSB	MESSAGE BITS					MSB	ERROR FLAG

Note to Table 5

1. Bit 7 = 1, if message codeword could not be corrected.

Table 6 Termination word format.

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7 (note 1)
0	0	1	0	0	0	0	ERROR FLAG

Note to Table 6

1. Bit 7 = 1, if call termination on error.

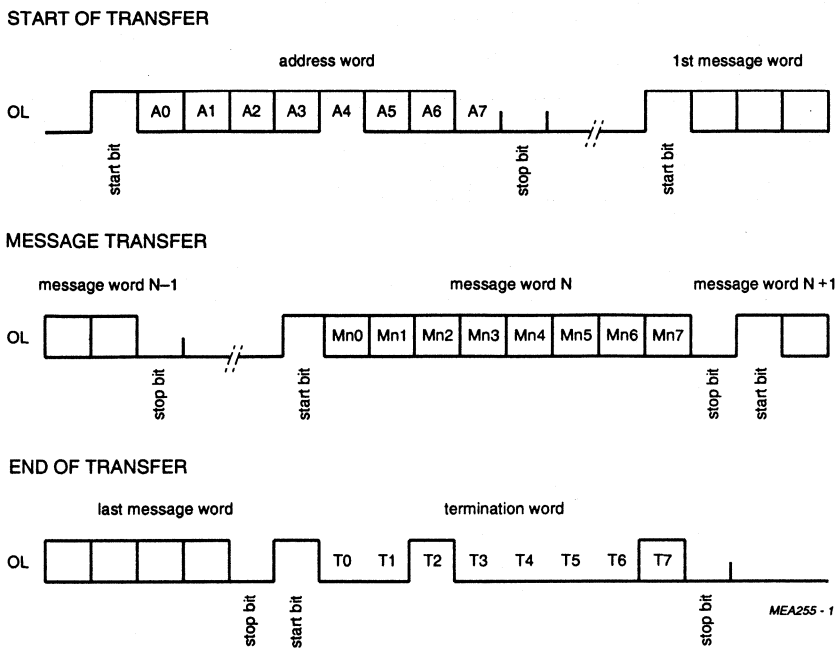


Fig.14 Call data transfer on the LED output.

Data conversion

The PCF5001T automatically converts message codewords received in numeric or alphanumeric format into ASCII format. Depending on SPF13 and the function bit setting in the received address codeword a conversion takes place as shown in Table 7.

When a conversion from alphanumeric format to ASCII takes place, the received message codewords are split into message blocks, seven bits in length. After adding the error flag they are transferred as message words.

When a conversion from numeric format to ASCII takes place, the received message codewords are split into blocks, four bits in length. Each four bit block is converted to a seven bit block as shown in Table 8. After adding the error flag they are transferred as message words.

Table 7 Message data conversion.

SFF 13	FUNCTION BITS		MESSAGE FORMAT
	BIT 20 (MSB)	BIT 21 (LSB)	
0	x	x	numeric
1	0	0	numeric
1	0	1	alphanumeric
1	1	0	alphanumeric
1	1	1	alphanumeric

Table 8 Numeric format to ASCII conversion.

4-BIT BLOCK				CHARACTER	7-BIT BLOCK						
LSB			MSB		LSB						MSB
0	0	0	0	'0'	0	0	0	0	1	1	0
1	0	0	0	'1'	1	0	0	0	1	1	0
0	1	0	0	'2'	0	1	0	0	1	1	0
1	1	0	0	'3'	1	1	0	0	1	1	0
0	0	1	0	'4'	0	0	1	0	1	1	0
1	0	1	0	'5'	1	0	1	0	1	1	0
0	1	1	0	'6'	0	1	1	0	1	1	0
1	1	1	0	'7'	1	1	1	0	1	1	0
0	0	0	1	'8'	0	0	0	1	1	1	0
1	0	0	1	'9'	1	0	0	1	1	1	0
0	1	0	1	'*'	0	1	0	1	0	1	0
1	1	0	1	'U'	1	0	1	0	1	0	1
0	0	1	1	' '	0	0	0	0	0	1	0
1	0	1	1	'-'	1	0	1	1	0	1	0
0	1	1	1	']'	1	0	1	1	1	0	1
1	1	1	1	'['	1	1	0	1	1	0	0

Memory Organization

The PCF5001T POCSAG decoder contains non-volatile EEPROM memory to store four user addresses, two frame numbers and specially programmed function bits (SPF01 to SPF32) for decoder application configuration. The EEPROM is organized as three arrays of 38 bits each as shown in Fig.15.

A user address (or RIC) in POCSAG code comprises of 21 bits, but three of them are coded in the frame number and therefore not explicitly transmitted. In the PCF5001T, addresses A/B and C/D must share the same frame number: addresses A and B reside in frame FR1 (FR10, FR11, FR12), addresses C and D reside in frame FR2 (FR20, FR21, FR22). Fig.16 shows an example of decimal address to EEPROM content conversion. Each address must be explicitly enabled by resetting of the associated enable bit.

EEPROM ARRAY 1

BIT18	BIT17	BIT16	BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
A17	A16	A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00	$\overline{ENA}$

BIT37	BIT36	BIT35	BIT34	BIT33	BIT32	BIT31	BIT30	BIT29	BIT28	BIT27	BIT26	BIT25	BIT24	BIT23	BIT22	BIT21	BIT20	BIT19
B17	B16	B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00	$\overline{ENB}$

EEPROM ARRAY 2

BIT18	BIT17	BIT16	BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
C17	C16	C15	C14	C13	C12	C11	C10	C09	C08	C07	C06	C05	C04	C03	C02	C01	C00	$\overline{ENC}$

BIT37	BIT36	BIT35	BIT34	BIT33	BIT32	BIT31	BIT30	BIT29	BIT28	BIT27	BIT26	BIT25	BIT24	BIT23	BIT22	BIT21	BIT20	BIT19
D17	D16	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00	$\overline{END}$

EEPROM ARRAY 3

BIT18	BIT17	BIT16	BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
SPF13	SPF12	SPF11	SPF10	SPF09	SPF08	SPF07	SPF06	SPF05	SPF04	SPF03	SPF02	SPF01	FR20	FR21	FR22	FR10	FR11	FR12

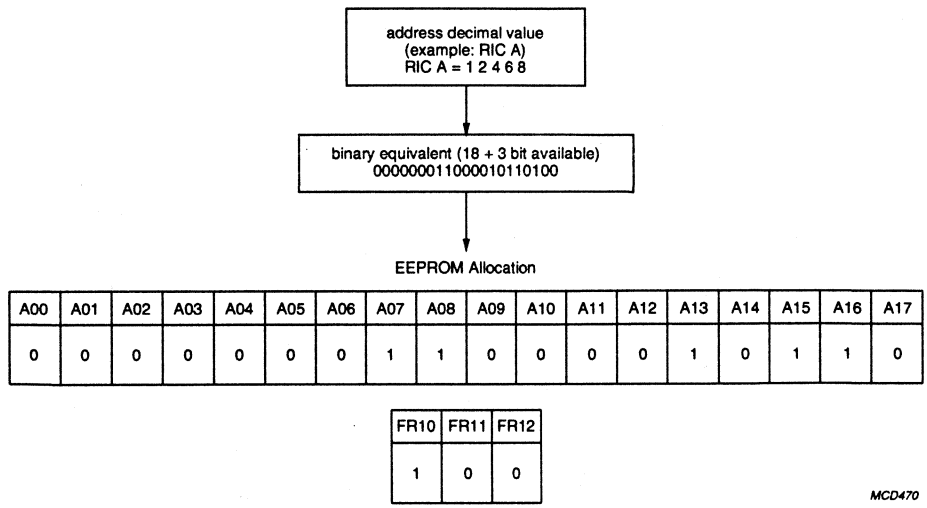
BIT37	BIT36	BIT35	BIT34	BIT33	BIT32	BIT31	BIT30	BIT29	BIT28	BIT27	BIT26	BIT25	BIT24	BIT23	BIT22	BIT21	BIT20	BIT19
SPF32	SPF31	SPF30	SPF29	SPF28	SPF27	SPF26	SPF25	SPF24	SPF23	SPF22	SPF21	SPF20	SPF19	SPF18	SPF17	SPF16	SPF15	SPF14

MCD469

Notes:

1. A00 represents the MSB of RIC A, B00 is the MSB of RIC B, etc.
2. FR10 represents the MSB of Frame 1 (valid for RICs A and B), FR20 is the MSB of Frame 2 (RICs C and D).

Fig.15 EEPROM memory organization.



Note: A00 is the MSB of RIC A, FR10 is the MSB of Frame 1.

Fig.16 Decimal address to memory contents conversion example.

Description of the Special Programmed Function (SPF) bits

The following features can be selected by appropriate programming of the special programmed function bits as shown in Table 9.

Table 9 Special Programmed Function (SPF) bits.

SPF	BIT	FUNCTION
SPF01	0	Alert-only mode
	1	Display pager mode
SPF02	0	512 bit/s data rate
	1	1200 bit/s data rate, possible with 76.8 kHz crystal only
SPF03	0	32768 Hz crystal configuration
	1	76800 Hz crystal configuration
SPF04, SPF05		Receiver establishment time (depending on data rate)
	0 0	7.8 ms/512 bps 53.3 ms/1200 bps
	0 1	15.6 ms/512 bps 6.7 ms/1200 bps
	1 0	31.3 ms/512 bps 13.3 ms/1200 bps
	1 1	62.5 ms/512 bps 26.7 ms/1200 bps

SPF	BIT	FUNCTION
SPF06, SPF07		Duplicate call suppression time out and out-of-range hold-off time out
	0 0	30 s
	0 1	60 s
	1 0	120 s
	1 1	240 s
SPF08	0	voltage converter disabled, if SPF01 = 1 (Display pager mode)
	1	voltage converter enabled, if SPF01 = 1 (Display pager mode)
SPF09	0	silent override on address C disabled
	1	silent override on address C enabled
SPF10	0	silent override on address D disabled
	1	silent override on address D enabled
SPF11	0	vibrator output disabled
	1	vibrator output enabled
SPF12	0	call termination criteria combination method (note 1)
	1	call termination criteria defined by SPF13
SPF13	0	numeric data deformatting, call termination on first uncorrectable codeword
	1	numeric data deformatting on function code 00 only, call termination on two uncorrectable codewords
SPF14	0	Duplicate call suppression disabled
	1	Duplicate call suppression enabled
SPF15	0	Out of range indication at OL output disabled, hold-off period is zero regardless of SPF06 and SPF07 setting
	1	Out of range indication at OL output enabled, hold-off period according to SPF06 and SPF07
SPF16	0	Repeat alert disabled
	1	Repeat alert enabled
SPF17	0	Call data output on OL disabled
	1	Call data output on OL enabled
SPF18		spare
SPF19		program always 0
SPF20 to SPF30		spares
SPF31	0	Alerter frequency 2048 Hz
	1	Alerter frequency 2731 Hz
SPF32	0	frequency reference output 16384 Hz if SPF01 = 1 (Display pager mode)
	1	frequency reference output 32768 Hz if SPF01 = 1 (Display pager mode)

Note to Table 9

1. Call termination on:
   - first codeword immediately following address codeword uncorrectable, or
   - two consecutive codewords uncorrectable.

EEPROM Write operation

The program mode is entered in OFF status by setting the PD input LOW and the PS input HIGH at any time. The program mode is left and normal operation resumed by either removing the power supply or setting the PD input HIGH after the 38th data bit while continuing to clock the PS input. The three EEPROM arrays can be programmed in any order. Selection of array is made during the second and third pulse on the PS input. The program mode has to be left after programming of each array.

After entering the program mode, keeping input PD LOW during the first pulse on PS selects Memory Write operation. After selection of the current array an erase cycle of duration t_{PEW} has to be carried out, during which the supply voltage at V_{SS} input must be at least V_{PG}. Program data for the selected array is entered bit by bit using PD as data input and the rising edge on PS as data strobe pulse. See Fig.17 for timing during an EEPROM write operation.

After the last bit a special write cycle of duration t_{PEW} has to be carried out again, during which the supply voltage at V_{SS} input must be V_{PG}.
During conditions when the supply voltage is increased to V_{PG} the maximum DC ratings at V_{REF} must not be exceeded. When the on-chip voltage converter is enabled a Zener diode or a damping resistor of sufficiently low impedance has to be connected between V_{REF} and V_{SS} to limit the voltage level at V_{REF} during program operation.

EEPROM Read operation

After entrance to the program mode, keeping input PD HIGH during the first pulse on PS selects Memory Read operation. After selection of the current array the programmed data is output bit-by-bit using PD as data output. A positive edge on PS input switches to the next bit. See Fig.17 for timing during an EEPROM read operation.

Read-Back operation via Microcontroller Interface

In display pager mode, the PCF5001T is capable of delivering the EEPROM contents to an external microcontroller using the serial interface outputs DO and DS. The EEPROM data transfer mode is selected by applying a LOW to input ON and a HIGH to input SK while pulsing the SR input, and the interface is enabled (IE is HIGH). The data transfer is triggered by the falling edge on input SR. The transfer is organized as 15-byte transfers. The contents of each array are extended to 40 bits by trailing zeros. The EEPROM data transfer starts with array 1, bit 0. A valid data bit at DO is indicated by a LOW level on DS as shown in Fig.18.

During EEPROM Read-Back operation, the PCF5001T configuration and the outputs FL, OL are undefined. After completion of the Read-Back operation, the PCF5001T will re-enter the programmed configuration.

Voltage converter

The PCF5001T contains a switched capacitor-type on-chip voltage converter, which can provide doubled supply voltage to the external microcontroller and display control devices. The microcontroller interface signals are level shifted accordingly.

A capacitor of 100 nF (C_S) must be connected between pins CP and CN while a load capacitor of 10 µF is connected to V_{REF} as shown in Fig.20. The voltage converter operates in display pager mode only, when enabled by programming SPF08 (see Table 9).

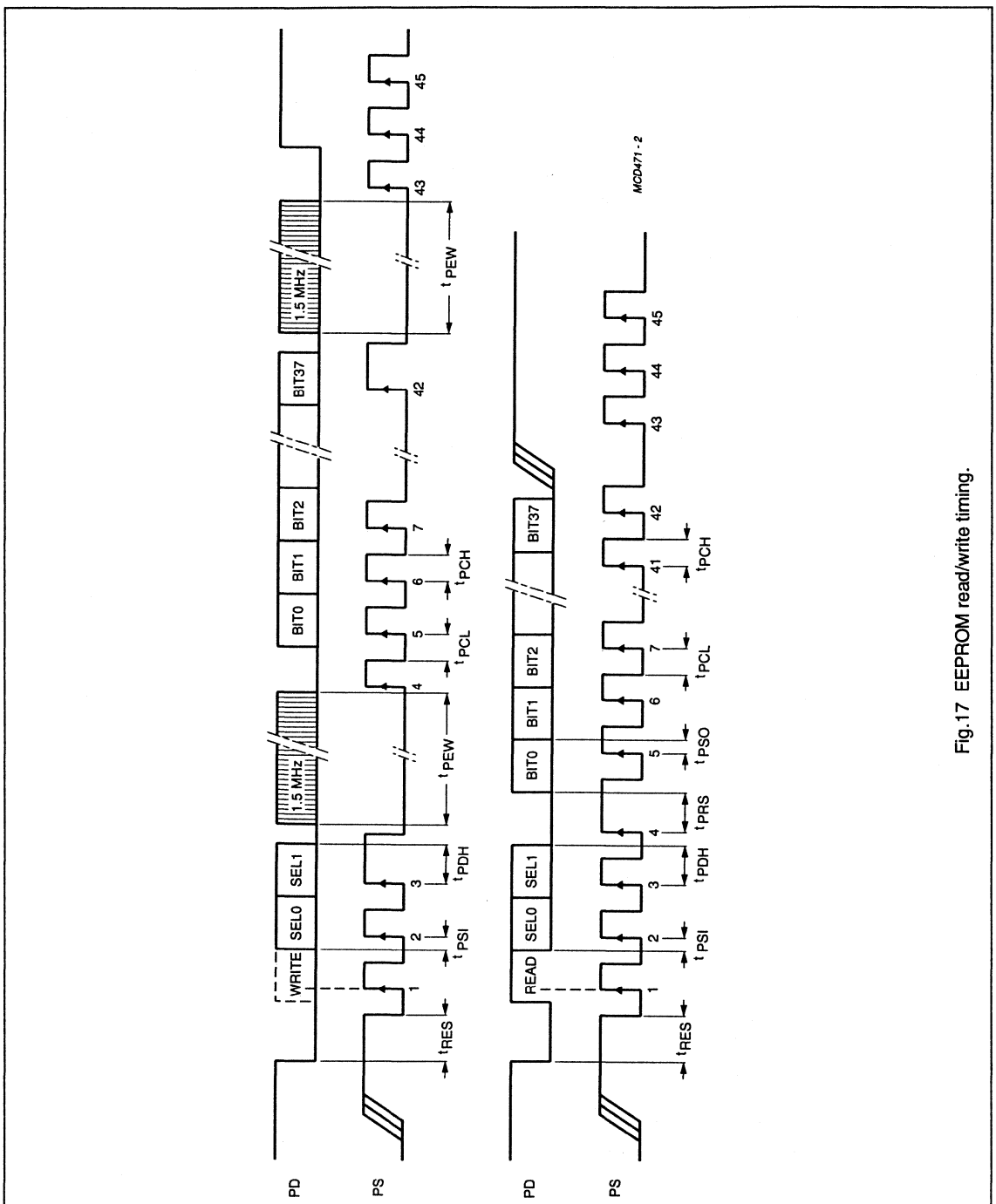


Fig.17 EEPROM read/write timing.

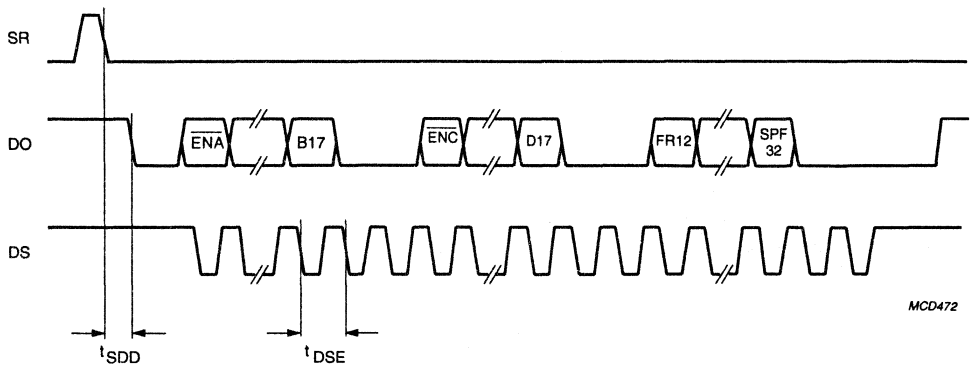


Fig.18 EEPROM data transfer to microcontroller timing.

Test modes of the decoder

The decoder supports two test modes, which are intended for use during pager production and type approval tests.

BOARD TEST MODE

Board test mode is selected by setting the PD input LOW at any time. In this test mode the following features are provided:

1. Receiver enable output is set constantly HIGH
2. Output AL is activated by a LOW level on ON input
3. Output AH is activated by a HIGH level on SR input
4. Outputs OL and OM are activated by a HIGH level on SK input.

Exit from board test mode is achieved by setting input PD HIGH.

PAGER TEST MODE (TYPE APPROVAL MODE)

Pager test mode is entered by reception of a valid call while board test mode is active, see above. In pager test mode:

1. Call alert cadences are terminated after 2 seconds
2. Duplicate call suppression is disabled.

Exit from pager test mode is achieved by disconnecting the power supply from the decoder.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{SS}	supply voltage (note 1)	+0.5	−8.0	V
V_{PG}	programming supply voltage	−5.5	−	V
V_I	input voltage on pins FL, DS, DO, OR, BL, AI, ON, SK, SR and IE	+0.8	V_{REF}−0.8	V
V_I	input voltage range on any other pin	+0.8	V_{SS}−0.8	V
P_{tot}	total power dissipation	-	250	mW
P_O	power dissipation per output	-	100	mW
I_I	maximum input current (any input)	−	10	mA
I_O	maximum output current (any output except AL)	−	20	mA
I_O	maximum output current (AL output)	−	70	mA
T_{stg}	storage temperature	−55	+125	°C
T_{amb}	operating ambient temperature	−40	+85	°C

Note to the Limiting values

1. Input V_{DD} is referred to as common, 0 V.

DC CHARACTERISTICS

V_{DD} = 0 V; V_{SS} = −2.7 V; V_{REF} = 2.7 V; T_{amb} = 25 °C.
Quartz crystal parameters: f = 76800 Hz; $R_{S(MAX)}$ = 40 kΩ, C_L = 12 pF.
Decoder Mode programmed as Alert-Only (SPF01 = 0).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{SS}	supply voltage	all outputs open-circuit	−1.5	−2.7	−6.0	V
I_{SS}	supply current	all inputs = V_{SS}; voltage converter off	–	−60	−100	µA
V_{PG}	programming supply voltage	note 1	−4.5	−5.0	−5.5	V
I_{PG}	programming supply current		–	−500	–	µA
Inputs						
V_{IL1}	LOW level input voltage PD, PS, DI, BS, TS, TT and X1		$0.7V_{SS}$	–	–	V
V_{IL2}	LOW level input voltage AI, ON, SR, SK and IE		$0.7V_{REF}$	–	–	V
V_{IH1}	HIGH level input voltage PD, PS, DI, BS, TS, TT and X1		–	–	$0.3V_{SS}$	V
V_{IH2}	HIGH level input voltage AI, ON, SR, SK and IE		–	–	$0.3V_{REF}$	V
I_I	Input current					
	BS, PS, TS and TT	$V_I = V_{DD}$	7.0	–	20.0	µA
	PD	$V_I = V_{SS}$	−9.0	–	−24.0	µA
	DI	$V_I = V_{DD}$; RE = 0	7.0	–	20.0	µA
	DI	$V_I = V_{DD}$; RE = 1	0	–	0.5	µA
	ON and SK	$V_I = V_{SS}$	−0.5	−0.8	−1.1	µA
	AI and SR	$V_I = V_{DD}$	7.0	–	20.0	µA
C_I	Input capacitance BS, DI, PD, PS, TS, TT, AI, ON, SR, SK, IE and X1		2	–	–	pF
Outputs						
I_{OL}	LOW level output current					
	OL, OM and AH	V_{OL} = −1.35 V	100	–	–	µA
	DO, DS, BL, FL and OR	V_{OL} = −1.35 V	100	–	–	µA
	AL	V_{OL} = −1.5 V	17.5	–	–	mA
	RE	V_{OL} = 2.2 V	200	–	–	µA
I_{OH}	HIGH level output current					
	OL, OM and AH	V_{OH} = −1.35 V	−0.8	–	−1.8	mA
	DO, DS, BL, FL and OR	V_{OH} = −1.35 V	−100	–	–	µA
	AL	AL HIGH impedance	–	–	−0.2	µA
	RE	V_{OH} = −0.5 V	−1.0	–	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Oscillator						
C_{XO}	output capacitance X2		–	40	–	pF
gm	oscillator transconductance					
		V_{SS} = –1.5 V	15	29	43	µS
		V_{SS} = –6.0 V	25	39	55	µS
V_{PU}	power-up reset threshold voltage		–	–1.20	–	V

Note to the DC characteristics

1. See section EEPROM Write operation and Limiting Values for limitations of V_{REF} when programming while the voltage converter is enabled.

DC CHARACTERISTICS (with Voltage Converter)

V_{DD} = 0 V;V_{SS} = –3.0 V; V_{REF} = –6.0 V; T_{amb} = 25 °C.
Quartz crystal parameters: f = 76800 Hz; $R_{s(max)}$ = 40 kΩ; C_L = 12 pF.
Decoder Mode programmed as Display Pager (SPF01 = 1).
Voltage converter enabled (SPF08 = 1); C_s = 100 nF.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{SS}	operating supply voltage		–1.5	–	–3.0	V
Voltage converter						
V_{REF0}	output voltage; no load	V_{SS} = –3.0 V	–5.8	–	–6.0	V
V_{REF}	output voltage	V_{SS} = –2.0 V; I_{REF} = 250 µA	–3.0	–3.5	–	V
I_{REF}	output current					
		V_{SS} = –2.0 V; V_{REF} = –2.7 V	400	600	–	µA
		V_{SS} = –3.0 V; V_{REF} = –4.5 V	600	900	–	µA
Inputs						
I_I	input current					
	AI, ON, SR and SK	$V_I = V_{REF}$	–	0	–0.5	µA
	ON and SK	$V_I = V_{DD}$	–	0	±0.5	µA
	SR	$V_I = V_{DD}$; V_{REF} = –6.0 V	–	17	–	µA

AC CHARACTERISTICS

V_{DD} = 0 V; V_{SS} = −2.7 V; T_{amb} = 25 °C.
Quartz crystal parameters: f = 32768 or 76800 Hz; $R_{S(MAX)}$ = 40 kΩ; C_L = 12 pF.
Decoder Mode programmed as Display or Alert-only pager (SPF01 = 1 or 0).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{AL}	alerter frequency	SPF31 = 0	–	2048	–	Hz
f_{AWH}	high alert warble frequency		–	1024	–	Hz
f_{AWL}	low alert warble frequency		–	16	–	Hz
f_{AL}	alerter frequency	SPF31 = 1	–	2731	–	Hz
f_{AWH}	high alert warble frequency		–	1365	–	Hz
f_{AWL}	low alert warble frequency		–	16	–	Hz
f_{FL}	frequency reference FL					
		SPF32 = 0	–	16384	–	Hz
		SPF32 = 1	–	32768	–	Hz
Call alert duration						
t_{ALT}	time out period		–	16	–	s
t_{ALL}	AL output only (LOW level)		–	4	–	s
t_{ALH}	AH and AL outputs (HIGH level)		–	12	–	s
t_{ALC}	call alert cycle period		–	1	–	s
t_{ALP}	call alert pulse duration		–	125	–	ms
t_{ALD}	call alert hold off period		52	–	–	ms
t_{RPT}	repeat alert duration		–	–	4	s
t_{RCR}	repeat alert recurrence		–	–	15	s
t_{RCP}	repeat alert cycle period		–	–	500	ms
t_{RPD}	repeat alert pulse duration		–	–	250	ms
t_{STON}	status alert period		–	–	62.5	ms
t_{STOF}	status alert delay		–	–	62.5	ms
t_{SUA}	start-up alert					
		SPF02 = 0	–	–	500	ms
		SPF02 = 1	–	–	453	ms
t_{ORA}	out-of-range alert width		–	–	62.5	ms
t_{ORD}	out-of range alert period		–	–	2	s
t_{BLAL}	battery low level alert		–	–	16	s
Receiver control						
t_{RXT}	RE transition time	C_L = 5 pF	–	–	100	ns
t_{RXON}	RE establishment time	SPF04 = 0; SPF05 = 1	–	7.8	62.5	ms
Data output						
f_{DO}	data output rate		–	2048	–	bps
t_{DSD}	strobe period call data		480	–	495	µs
t_{DSE}	strobe period EEPROM data		200	488	1150	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{DSW}	data strobe pulse width		230	–	250	µs
t_{TDO}	data output transition time	C_L = 10 pF	–	–	100	ns
t_{DOS}	data output set-up time		–	–	135	µs
t_{DOH}	data output hold time		115	–	–	µs
t_{BYD}	consecutive byte delay		1210	–	1225	µs
t_{CWD}	inter-codeword delay	1200 bps numeric message	3420	–	–	µs
t_{ST}	start condition set-up time		4750	–	–	µs
t_{SP}	stop condition set-up time		595	–	615	µs
t_{STL}	start bit period OL output		480	–	495	µs
t_{SPL}	stop bit period OL output		480	488	495	µs
t_{SDD}	SPF output delay time		1	–	10	ms

TIMING CHARACTERISTICS

V_{DD} = 0 V; V_{SS} = −2.7 V; T_{amb} = +25 °C.
Quartz crystal parameters: f = 32768 or 76800 Hz; $R_{S(MAX)}$ = 40 kΩ; C_L = 12 pF.
Decoder Mode programmed as Display or Alert-only pager (SPF01 = 1 or 0).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operating frequency dependent						
f_{OSC}	oscillator frequency					
		SPF03 = 0	–	32768	–	Hz
		SPF03 = 1	–	76800	–	Hz
t_{TDI}	data input transition time		–	–	100	µs
t_{DI1}	data input = logic 1 period		–	infinite	–	
t_{DI0}	data input = logic 0 period		–	infinite	–	
f_{DI}	data input rate	SPF02 = 0	–	512	–	bps
t_{BIT}	bit period		–	1.9531	–	ms
t_{CW}	codeword duration		–	62.5	–	ms
t_{PA}	preamble duration		1125	–	–	ms
t_{BAT}	batch duration		–	1062.5	–	ms
f_{DI}	data input rate	SPF02 = 1; f_{OSC} = 76800 Hz	–	1200	–	bps
t_{BIT}	bit period		–	833.3	–	µs
t_{CW}	codeword duration		–	26.7	–	ms
t_{PA}	preamble duration		480	–	–	ms
t_{BAT}	batch duration		–	453.3	–	ms
Alert-only mode (SPF01 = 0)						
t_{SDB}	switch debounce period		–	62.5	–	ms

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Display pager mode (SPF01 = 1)						
t_{STP}	status set-up time	f_{OSC} = 32768 Hz	35	–	–	µs
t_{STD}	status change delay time		–	–	35	µs
t_{IEH}	interface enable hold time		35	–	–	µs
t_{STH}	status hold time		35	–	–	µs
t_{SPD}	status pulse duration		35	–	–	µs
t_{STP}	status set-up time	SPF01 = 1; f_{OSC} = 76800 Hz	15	–	–	µs
t_{STD}	status change delay time		–	–	15	µs
t_{IEH}	interface enable hold time		15	–	–	µs
t_{STH}	status hold time		15	–	–	µs
t_{SPD}	status pulse duration		15	–	–	µs

PROGRAMMING CHARACTERISTICS

V_{DD} = 0 V; V_{SS} = V_{PG} = –5.0 V; (see notes 1, 2 and 3) V_{REF} = V_{SS}; pins 2 and 3 open-circuit; T_{amb} = +25 °C.
Quartz crystal parameters: f = 32768 Hz; $R_{S(MAX)}$ = 40 kΩ; C_L = 12 pF.
Decoder in OFF status.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Programming						
t_{RES}	power-up reset pulse width	note 4	35	–	–	µs
t_{PEW}	erase/write time		10	–	–	ms
f_{EW}	erase/write frequency		1.0	1.5	2.0	MHz
	erase/write cycles		100	10000	–	–
t_{DR}	data retention time	T_{amb} = 85 °C	10	–	–	yrs
t_{PCH}	data clock HIGH duration	note 4	65	–	–	µs
t_{PCL}	data clock LOW duration	note 4	65	–	–	µs
t_{PRS}	read set-up time	note 4	–	–	35	µs
t_{PSI}	data set-up time on input	note 4	35	–	–	µs
t_{PSO}	data set-up time on output	note 4	–	–	35	µs
t_{PDH}	data hold time	note 4	35	–	–	µs

Notes to the programming characteristics

1. V_{SS} = V_{PG} only required during erase/write (t_{PEW} in Fig.17), otherwise V_{SS} = –1.5 V minimum.
2. Maximum voltage for programming (V_{PG}) is –5.5 V.
3. See section EEPROM Write operation and Limiting Values for limitations of V_{REF} when programming while the voltage converter is enabled.
4. EEPROM programming is also possible at higher oscillator frequencies (76.8 kHz or 153.6 kHz). The timings shown then become proportionally smaller.

APPLICATION INFORMATION

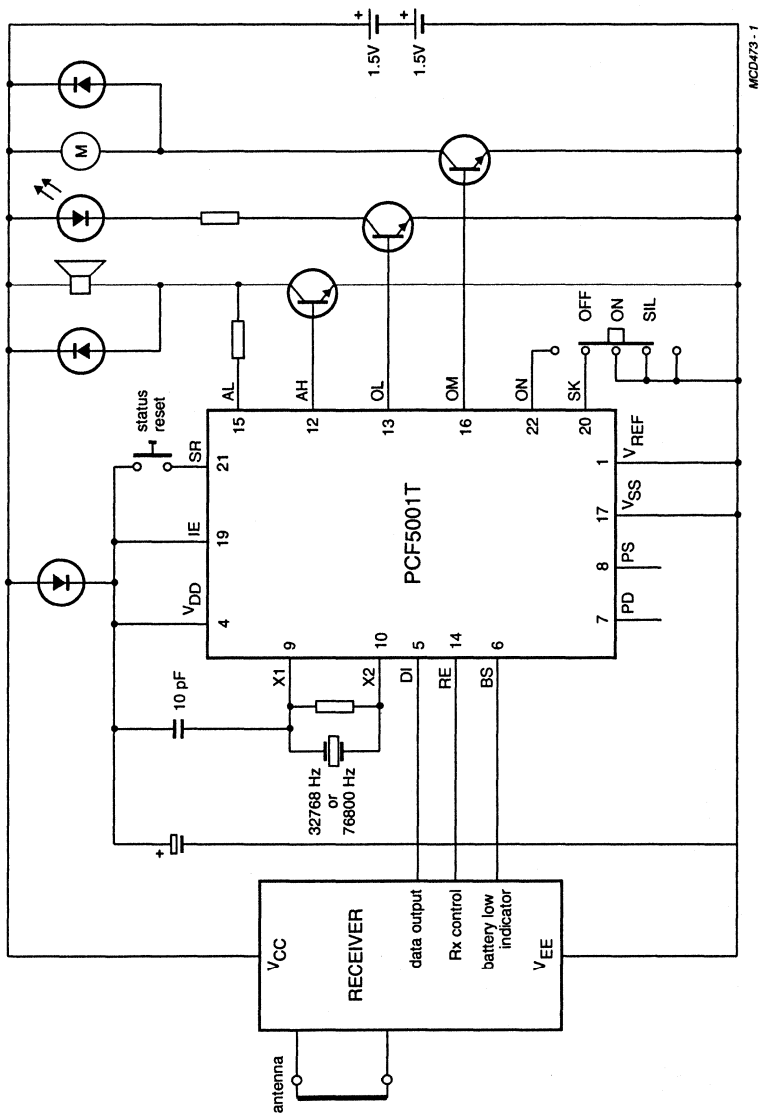


Fig.19 Alert-only pager application example.

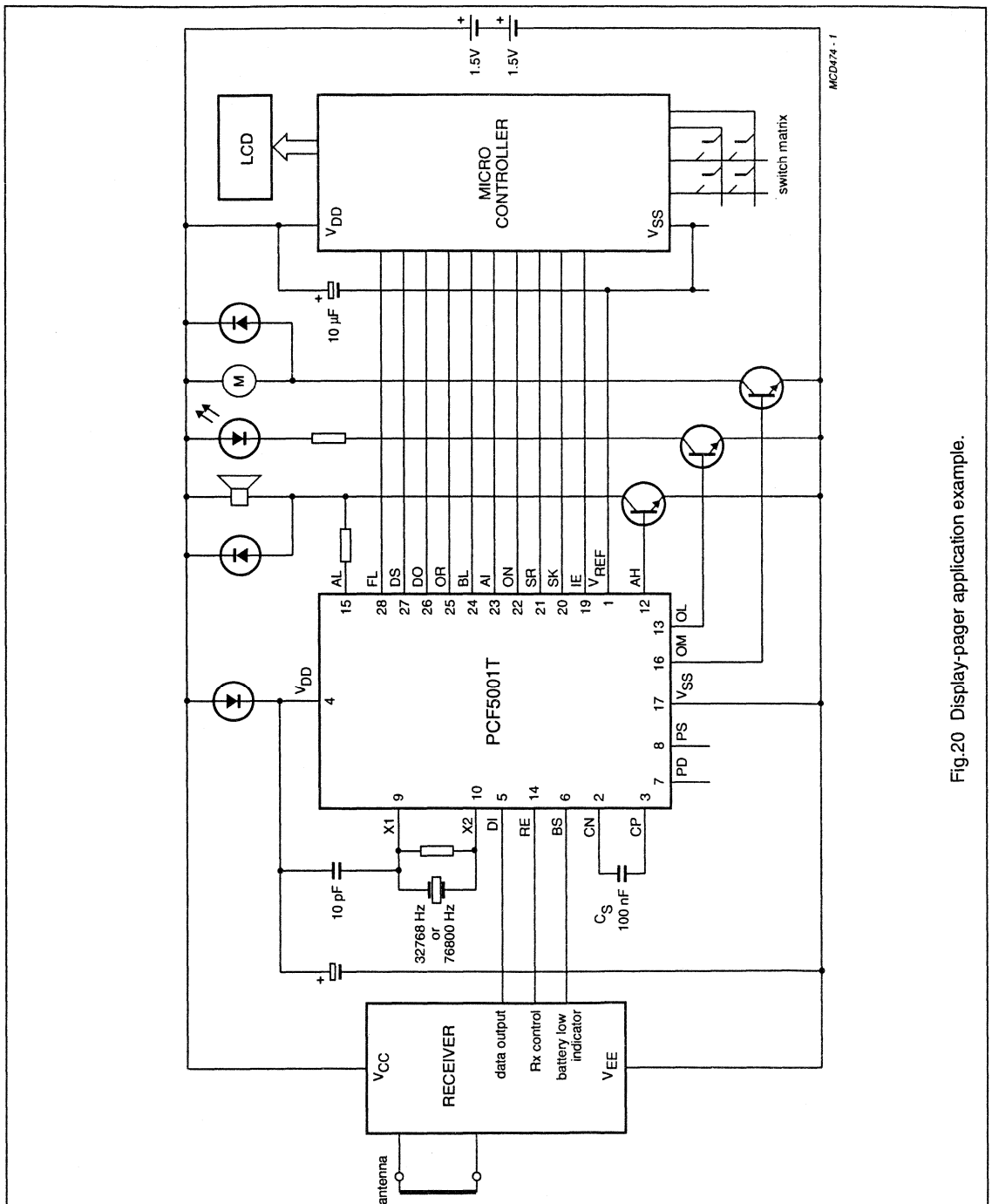
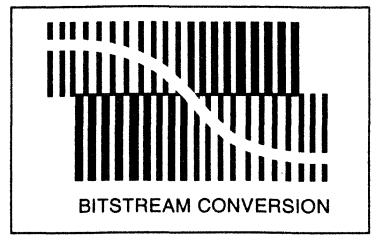


Fig.20 Display-pager application example.

14-bit AD/DA converter PCF5012A

FEATURES

- Complete analog-to-digital and digital-to-analog 14-bit conversion system
- Implemented using Philips 'Bit Stream' techniques
- Suitable for use in G.722 wideband speech CODECs
- No external sample-and-hold, simple/no analog pre and post filtering required: all filters are digitally integrated
- No need for internal trimming, no performance degradation
- Very high linearity
- Sampling rate in the range of 8 kHz to 16 kHz
- High bandwidth of the analog signal: 7 kHz (f_s = 16 kHz)
- Needs only a few external components
- Easily connectable to a DSP via a serial or parallel interface
- Low power consumption.



GENERAL DESCRIPTION

The PCF5012A is an integrated circuit which implements a full 14-bit analog-to-digital and digital-to-analog conversion system. It includes all band-limiting filters. The analog-to-digital and digital-to-analog converters operate according to the one-bit interpolative conversion principle, whereby quantization noise shaping is used.

The PCF5012A is optimized for use in combination with a digital signal processor. Telecom terminals is one of the application areas.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF5012AP	28	DIL28	plastic	SOT117
PCF5012AH	44	QFP44	plastic	SOT205A

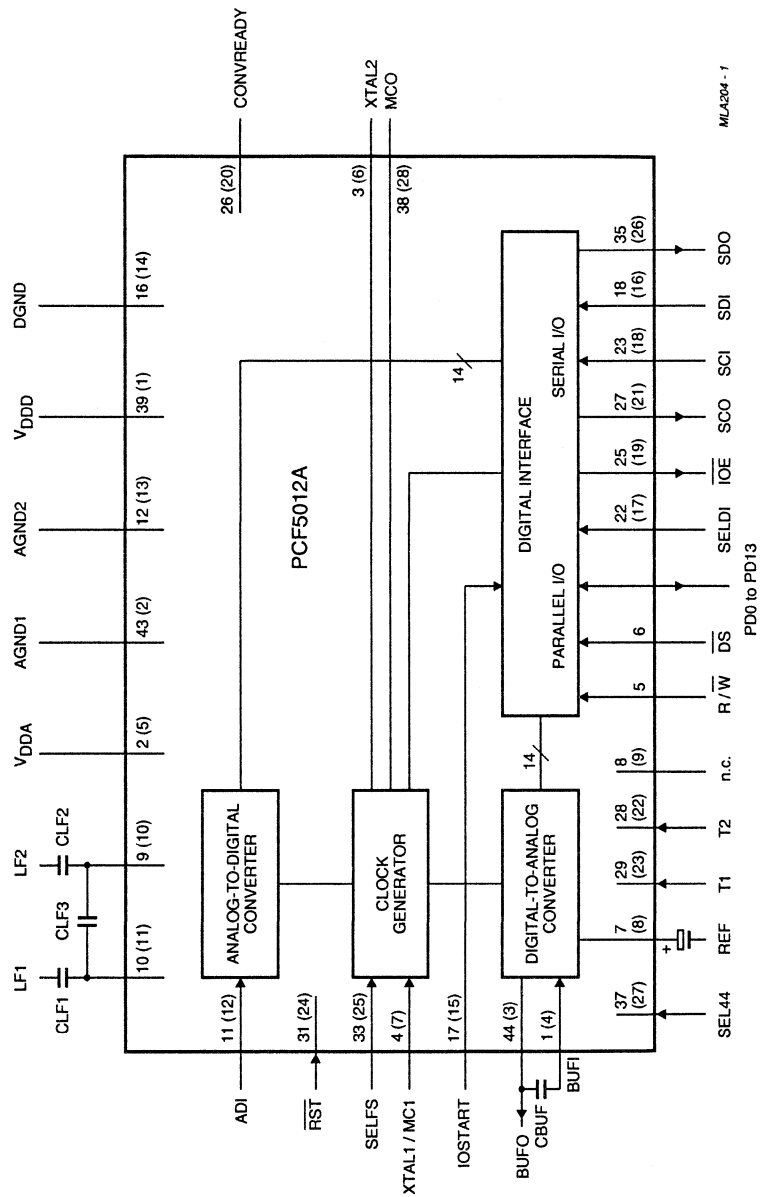


Fig.1 Block diagram.

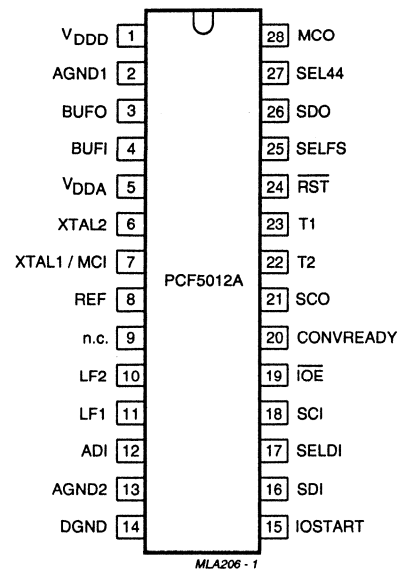


Fig.2 Pin configuration (DIL28).

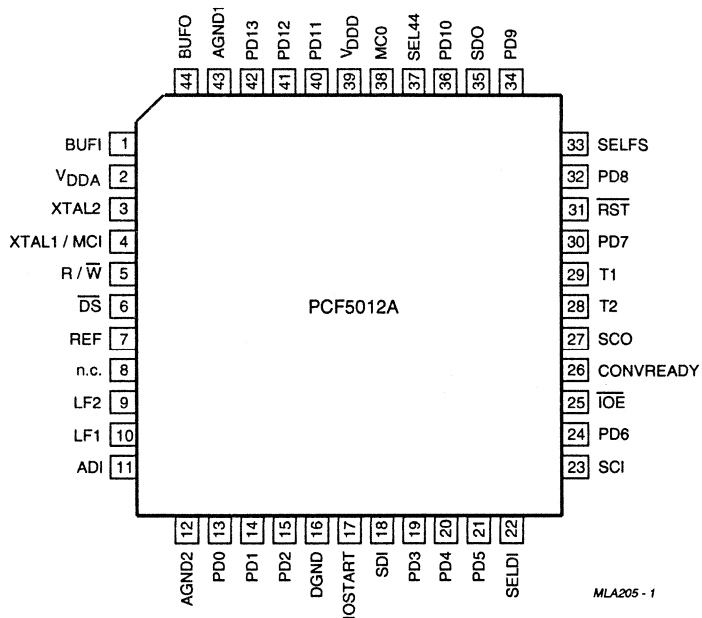


Fig.3 Pin configuration (QFP44).

PINNING

SYMBOL	PIN		DESCRIPTION
	SOT205A	SOT117	
BUFI	1	4	DAC buffer input. Used for external filter capacitor from BUFO
V_{DDA}	2	5	analog supply voltage connected to V_{DDD}
XTAL2	3	6	crystal connection
XTAL1/MC1	4	7	crystal connection or external system clock input
R/$\overline{W}$	5	–	defines the direction of the data transfer across the parallel interface. When R/$\overline{W}$ = HIGH processor reads from PCF5012A. When R/$\overline{W}$ = LOW processor writes to PCF5012A
$\overline{DS}$	6	–	data strobe signal to activate the data transfer across the parallel interface (active LOW)
REF	7	8	the reference for all internal analog signals is derived from the analog supply. Therefore a capacitor for external reference filtering should be connected to this pin
n.c.	8	9	not connected
LF2	9	10	external capacitor for ADC loop filter 2
LF1	10	11	external capacitor for ADC loop filter 1
ADI	11	12	analog signal input referenced to REF
AGND2	12	13	analog ground 2 connected to DGND
PD0	13	–	bidirectional parallel data line 0; LSB
PD1	14	–	bidirectional parallel data line 1
PD2	15	–	bidirectional parallel data line 2
DGND	16	14	digital ground
IOSTART	17	15	LOW-to-HIGH transition starts the I/O transfer. After a LOW-to-HIGH transition of CONVREADY the serial I/O can be started with IOSTART. This can be achieved externally or by connection to CONVREADY (Master PCF5012A). If several PCF5012As share a common multiplexed serial port they can be synchronized by connecting $\overline{IOE}$ to IOSTART of the next (Slave PCF5012A) in cascade
SDI	18	16	serial data input. Data shifted in MSB first with rising edge of SCI
PD3	19	–	bidirectional parallel data line 3
PD4	20	–	bidirectional parallel data line 4
PD5	21	–	bidirectional parallel data line 5
SELDI	22	17	selects between serial (SELDI = HIGH) or parallel (SELDI = LOW) interface
SCI	23	18	shift clock supply for the serial interface
PD6	24	–	bidirectional parallel data line 6
$\overline{IOE}$	25	19	input/output data transfer via the digital interfaces; starts when LOW
CONVREADY	26	20	clock with the frequency f_s. A LOW-to-HIGH transition indicates that the PCF5012A is ready for a new I/O procedure. This signal can be used to synchronize the whole system
SCO	27	21	buffered internal clock (128 x f_s) for the serial data interface in the "stand alone" operation. (independent of $\overline{RST}$)

SYMBOL	PIN		DESCRIPTION
	SOT205A	SOT117	
T2	28	22	test pin 2; must be connected to V_{DDD}
T1	29	23	test pin 1; must be connected to V_{DDD}
PD7	30	–	bidirectional parallel data line 7
$\overline{RST}$	31	24	reset signal. The internal sequencer starts at a defined position. Digital interfaces are muted for a time of $32/f_s$
PD8	32	–	bidirectional parallel data line 8
SELFS	33	25	selects the ratio of f_s and the system clock. SELFS = HIGH; f_s = MCO/1024 SELFS = LOW; f_s = MCO/512
PD9	34	–	bidirectional parallel data line 9
SDO	35	26	serial data output 3-state. Data shifted out MSB first with falling edge of SCI
PD10	36	–	bidirectional parallel data line 10
SEL44	37	27	has to be connected HIGH for 44-pin package; LOW for 28-pin package
MCO	38	28	buffered system clock output from MCI (independent from $\overline{RST}$)
V_{DDD}	39	1	digital supply voltage (+5 V)
PD11	40	–	bidirectional parallel data line 11
PD12	41	–	bidirectional parallel data line 12
PD13	42	–	bidirectional parallel data line 13; MSB
AGND1	43	2	analog ground 1 connected to DGND
BUF0	44	3	buffer for analog output. Output is referenced to REF

Note to the pinning

All SELect inputs are meant to be 'static' inputs to configure the system and can cause corruption of the system when they are switched during operation.

FUNCTIONAL DESCRIPTION

Figure 1 shows the functional block diagram of the PCF5012A.
The analog-to-digital and digital-to-analog converter, the digital interfaces and the clock generator are described separately in the subsequent sections.

Analog-to-digital converter (ADC)

The ADC consists of an analog input block which produces a 1-bit code, by means of oversampling (128 x f_s) and noise shaping, and a digital decimation filter, which converts the 1-bit code into a 14-bit signal and reduces the sampling rate to f_s. The 14-bit code is then transmitted via the digital interfaces.
It is possible to vary the sampling rate fs between 8 and 16 kHz by varying the system clock rate or the clock divider (SELFS).

Three external capacitors are required for the loop filter:

CLF1 = 220 pF x 16 kHz/f_s

CLF2 = 330 pF x 16 kHz/f_s

CLF3 = CLF2/10.7

Digital-to-analog converter (DAC)

The DAC consists of a digital interpolation filter, a noise shaping coder, a 1-bit DAC and a buffer amplifier.
The interpolation filter increases the sampling rate of the digital input signal and suppresses periodic spectral signal components within the audible range.

The noise shaping coder reduces the word length to 1 bit and feeds back the resulting quantization noise (noise shaping). This noise spectrum rises with 12 dB/octave above the audible range. A first-order filter can be included in the DAC by connecting one external capacitor (CBUF) between BUFI and BUFO (CBUF = 150 nF x 16 kHz/f_s). This filter is adequate for applications in which the ear is the receiver. For more critical applications, in which the DAC signal is resampled or mixed, further post-filtering of at least first order should be provided.

Digital interfaces

The PCF5012A has separate serial input and output ports. The data is transferred simultaneously on both serial ports. In the 44-pin version a parallel data exchange is provided for a 14-bit wide bidirectional parallel data interface. SELDI (Select Data Interface) determines whether the parallel or the serial interface is used.

The digital interfaces are arranged such that the PCF5012A can be directly connected to a signal processor (PCB5010/11) without the need for additional external "glue" logic. The number format is in two's complement notation.

Serial interfaces

Digital data transfer to and from the PCF5012A can take place via the serial I/O interfaces. The interface consists of two data lines SDI and SDO (Serial Data In and Serial Data Out) and two clock lines SCI and SCO (Serial Clock In and Serial Clock Out). The serial clock input (SCI) is common to both serial interfaces and must be supplied by the system.
For stand alone applications, SCI can be connected to the SCO output which supplies a buffered internal clock (128 x f_s). The maximum transfer rate is 4 Mbits/s.

The PCF5012A writes 14-bit serial data, on the falling edge of SCI, to the data output SDO and reads 14-bit serial data, on the rising edge of SCI, from the data input SDI. The MSB of a word is transferred in the first bit position, which is compatible to most converters and almost compatible to the I²S-Interface.

The serial I/O operation can be started after a LOW-to-HIGH transition of CONVREADY. It is triggered by a LOW-to-HIGH transition on the IOSTART pin which is detected at the LOW-to-HIGH transition of SCI.
IOSTART can be used to trigger the I/O either externally or internally by connecting it to CONVREADY. During the serial data transfer the $\overline{IOE}$ pin is held LOW for fourteen SCI cycles. The I/O operation has to be completed three SCO cycles before the next LOW-to-HIGH transition of CONVREADY to prevent data collision with the internal data exchange.
Should $\overline{IOE}$ become non-active (HIGH) then the output SDO will go to the 3-state condition and the input SDI will be inhibited. This allows the possibility to multiplex several serial I/Os on to a common serial port of a signal processor. In this situation, the arbitration of several serial interfaces has to be solved.

One simple solution is to connect the $\overline{IOE}$ output of one PCF5012A to the IOSTART input of the next PCF5012A. In this way a cascade of PCF5012As can be built so that the end of a transfer on one PCF5012A starts the beginning of the transfer of the next PCF5012A. The first PCF5012A can be configured as a master, (IOSTART = CONVREADY) or, started by an external trigger being applied to its IOSTART input.

Parallel interface (44-pin package only)

The parallel interface can be used instead of the serial interfaces for the digital transfer to and from the PCF5012A. The connections are bidirectional and do not require additional external "glue" logic.

The interface consists of the parallel data lines PD0 (LSB) to PD13 (MSB) and the control inputs R/$\overline{W}$ and $\overline{DS}$. After a LOW-to-HIGH transition of CONVREADY a parallel I/O operation can be started. It has to be completed three SCO cycles before the next LOW-to-HIGH transition of CONVREADY to prevent data collision with the internal data exchange. During this period the transfer can take place completely asynchronously and is controlled from the processor via the R/$\overline{W}$ and $\overline{DS}$ control lines.
The R/$\overline{W}$ signal switches the direction of the parallel data transfer from write to read and vice-versa. When R/$\overline{W}$ = HIGH a read operation from the PCF5012A to the processor is indicated, and when R/$\overline{W}$ = LOW a WRITE operation from the processor to the PCF5012A is indicated. The signal $\overline{DS}$ defines the time at which the data output is valid ($\overline{DS}$ = LOW), the data being accepted by the interface (LOW-to-HIGH transition of $\overline{DS}$). The 3-state buffers of the parallel interface are in a 3-state condition when $\overline{DS}$ is inactive ($\overline{DS}$ = HIGH). This enables the PCF5012A to be memory mapped into the address areas of the processor.

By means of a control signal SELDI (Select Data Interface) the user can define which of the digital interfaces (serial or parallel) is to be used for actual data exchange to the PCF5012A.

Clock generator

The PCF5012A can generate a system clock by connecting a crystal to the crystal oscillator (XTAL1 and XTAL2). Alternatively, an external clock generator can also be connected to the XTAL1/MCI input.
Since the timing of the analog blocks is derived from this clock it must not contain any clock jitter. Any low frequency jitter would modulate the analog signals and degrade the performance. The buffered master clock is available at the MCO output.

The PCF5012A derives the sampling rate, f_s, by dividing the master clock. The SELFS input can be used to set the division ratio either to 1024 (SELFS = HIGH) or to 512 (SELFS = LOW).

Reset (via $\overline{RST}$ pin)

A Reset ($\overline{RST}$ = LOW) stops most of the internal logic (except the clocks MCO and SCO) to enable a power-down operation. After a reset, the internal sequencer starts and the conversions begin. To prevent the output of corrupted data, the outputs BUFO, SDO and PD0 to 13 are muted for 32 sample periods ($1/f_s$).

System synchronization (via CONVREADY pin)

To synchronize the connected system, the PCF5012A provides a CONVREADY output. Its transition indicates that a new sample can be taken from the data output and supplied to the data input. The PCF5012A is thus always the master for the sampling rate.
To allow internal data exchange, all I/O actions have to be completed three SCO cycles before the next transition of CONVREADY.

Package selection (via SEL44 pin)

SEL44 has to be HIGH when the QFP44 package is used and LOW when the DIL28 package is used.

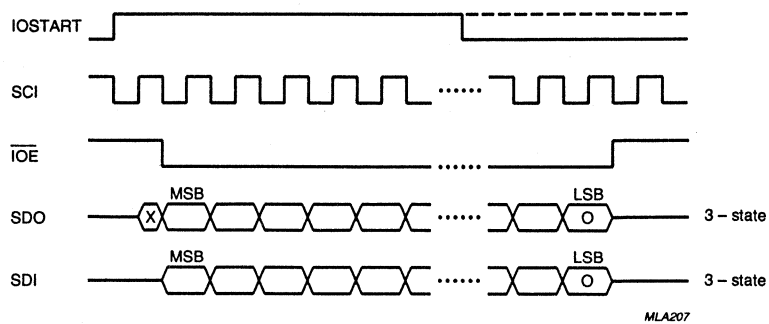


Fig.4 Functional timing diagram for the serial data transfer.

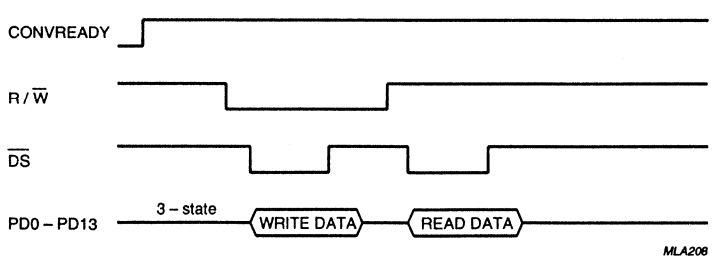


Fig.5 Functional timing diagram for the parallel data transfer.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDD}	digital supply voltage	−0.5	+7.0	V
V_{DDA}	analog supply voltage	−0.5	+7.0	V
V_O	DC output voltage	−0.5	V_{DD}+0.5	V
V_I	DC input voltage	−0.5	7.0	V
$I_{I(D)}$	DC input diode current	−10	+10	mA
V_O	DC output voltage	−0.5	V_{DD}+0.5	V
I_O	DC output current	−20	+20	mA
I_{DD}	DC supply current	−	60	mA
T_{amb}	operating ambient temperature	−40	+85	°C
T_{stg}	storage temperature	−55	+150	°C

DC CHARACTERISTICS

f_s = 16 kHz; T_{amb} = −40 to +85°C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
V_D	supply voltage difference V_{DDA}/V_{DDD}, AGND/DGND		–	–	0.25	V
P_{DA}	supply dissipation (analog)	in cascade at 5 V	–	20	–	mW
P_{DD}	supply dissipation (digital)	in cascade at 5 V	–	60	–	mW
P_{DD}	supply dissipation (V_{DDD})	in reset; in cascade at 5 V	–	10	–	mW
	standby supply current					
I_{DDA0}	analog		–	1.7	–	mA
I_{DDD0}	digital		–	50	–	µA
Reference generation						
V_{REF}	reference voltage (% of V_{DD})	note 1	48	50	52	
Z_{REF}	reference impedance		–	7.5	–	kΩ
Crystal oscillator						
gm	mutual conductance	T_{amb} = 25 °C; V_{DD} = 5 V	6	11	19	mA/V
C_I	input capacitance		–	10	–	pF
C_O	output capacitance		–	10	–	pF
C_{FB}	feedback capacitance		–	5	–	pF
Logic inputs						
V_{IL}	LOW level input voltage		–	–	+0.8	V
V_{IH}	HIGH level input voltage		2.0	–	–	V
I_{LI}	input leakage current		−1.0	–	+1.0	µA
C_I	input capacitance		–	10	–	pF
Master clock output (MCO)						
I_{OL}	LOW level output current	V_{OL} = 0.4 V	4	7	–	mA
I_{OH}	HIGH level output current	V_{OH} = V_{DD}−0.4 V	4	8	–	mA
Output $\overline{IOE}$ and SCO (with 50 pF load)						
I_{OL}	LOW level output current	V_{OL} = 0.4 V	2	4	–	mA
I_{OH}	HIGH level output current	V_{OH} = V_{DD}−0.4 V	2	5	–	mA
All other outputs (with 35 pF load)						
I_{OL}	LOW level output current	V_{OL} = 0.4 V	1	4	–	mA
I_{OH}	HIGH level output current	V_{OH} = V_{DD}−0.4 V	1	4	–	mA

Note

1. Any noise on V_{REF} directly modulates the analog signals.

AC CHARACTERISTICS

f_s = 16 kHz; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Crystal oscillator						
f_{XTAL}	crystal frequency		3.6	8.0	8.4	MHz
External clock input MCI (note 1)						
f_{XTAL}	crystal frequency		3.6	8.0	8.4	MHz
t_{IH}	input time HIGH (%1/f_{XTAL})		40	50	60	
t_r	rise time	0.8 to 2.0 V	–	–	15	ns
t_f	fall time	2.0 to 0.8 V	–	–	15	ns
Master clock output MCO (with 50 pF load)						
t_r	rise time	0.8 to 2.0 V	–	–	15	ns
t_f	fall time	2.0 to 0.8 V	–	–	15	ns
Output $\overline{IOE}$ (with 50 pF load)						
t_r	rise time	0.8 to 2.0 V	–	–	30	ns
t_f	fall time	2.0 to 0.8 V	–	–	30	ns
All other outputs (with 35 pF load)						
t_r	rise time	0.8 to 2.0 V	–	–	42	ns
t_f	fall time	2.0 to 0.8 V	–	–	42	ns
Delays referred to the appropriate clocks						
t_p	output propagation delay		5	–	–	ns
$t_{HD;DAT}$	output hold time		5	–	–	ns
$t_{SU;DAT}$	input set-up time		5	–	–	ns
$t_{HD;DAT}$	input hold time		0	–	–	ns
Clock inputs						
f_{SCI}	serial clock input frequency		–	2	4	MHz
t_{DS}	data strobe ($\overline{DS}$) LOW		50	–	–	ns

Note

1. Any clock jitter directly modulates the analog signals.

DYNAMIC PERFORMANCE OF THE ADC (note 1)

V_{DD} = 5 V; T_{amb} = 25 °C; f_s = 16 kHz; CLF1 = 220 pF ±10%; CLF2 = 330 pF ±10%; CLF3 = 30 pF unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{IREF(RMS)}$	analog input reference level to achieve –1 dBFS (RMS value)	V_{DD} = 5 V; input = 1 kHz	1.2	1.3	1.4	V
Z_I	input impedance		33	45	67	kΩ
SVRR	power supply rejection ratio	at 1 kHz; note 2	40	–	–	dB
f_{ch}	frequency characteristic	–1 dBFS input				
	0 to 6.8 kHz		–1.2	–	–0.8	dBFS
	7 kHz		–2.5	–	–	dBFS
att	anti-aliasing attenuation					
	8 to 9 kHz		25	–	–	dB
	9 to 100 kHz		70	–	–	dB
	> 100 kHz		85	–	–	dB
THD + N	total harmonic distortion plus noise					
	–1 dBFS at 1 kHz		–	–70	–65	dB
	–20 dBFS at 1 kHz		–	–61	–	dB
	–20 dBFS at 1 kHz	T_{amb} = 85 °C	–	–62	–	dB
α	crosstalk from DAC		–	–	–60	dB
f_s	sampling rate	coupled to DAC	7.2	–	16.4	kHz
t_d	constant group delay		–	–	18	$1/f_s$
Δt	group delay deviation	f_s = 16 kHz	–15	–	+15	µs
MUTE	muting after reset to suppress random data		–	–	32	$1/f_s$

Notes

1. All specifications are given relative to digital Full Scale (0 dBFS). Digital full scale is defined as an input sinewave whose peak value reaches the positive full scale.
2. Guaranteed by design.

DYNAMIC PERFORMANCE OF THE DAC

V_{DD} = 5 V; T_{amb} = 25 °C; f_s = 16 kHz; CBUF = 220 pF ±10% unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{REF(RMS)}$	analog output reference level (RMS value)	V_{DD} = 5 V; f =1 kHz at −1 dBFS	0.9	1.0	1.1	V
OL	overload level	digital; full scale	–	–	0	dBFS
Z_O	load impedance at output		1.2	–	–	kΩ
C_L	direct capacitive load to AGND on buffer		–	–	50	pF
R_{FB}	internal buffer feedback resistance	note 1	19	21	23	kΩ
SVRR	power supply rejection ratio	at 1 kHz; note 2	40	–	–	dB
f_{ch}	frequency characteristic	−1 dBFS				
	0 to 6.8 kHz		−1.2	–	−0.8	dBFS
	7 kHz		−2.5	–	–	dBFS
att	anti-imaging attenuation					
	8 to 9 kHz		25	–	–	dB
	9 to 119 kHz		70	–	–	dB
	> 119 kHz		30	–	–	dB
THD + N	total harmonic distortion plus noise					
	−1 dBFS at 1 kHz		–	−82	−70	dB
	−20 dBFS at 1 kHz		–	−61	–	dB
	−20 dBFS input	T_{amb} = 85 °C	–	−62	–	dB
N_{idle}	idle noise from 20 Hz to 7 kHz	unweighted	–	–	−84	dBFS
α	crosstalk from the ADC		–	–	−60	dB
f_s	sampling rate	coupled to ADC	7.2	–	16.4	kHz
t_d	constant group delay		–	–	18	$1/f_s$
Δt_d	group delay deviation	f_s = 16 kHz	−15	–	+15	μs
MUTE	muting after reset		–	–	32	$1/f_s$

Notes

1. This tolerance influences only the filter corner frequency, and not the output level.
2. Guaranteed by design.

DYNAMIC PERFORMANCE OF THE ADC/DAC IN CASCADE (ON THE SAME CHIP)

V_{DD} = 5 V; T_{amb} = 25 °C; f_s = 16 kHz unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	overload point	digital full scale	–	0	–	dBFS
THD + N	total harmonic distortion plus noise					
	–1 dBFS at 1 kHz		–	–70	–65	dB
	–20 dBFS at 1 kHz		–	–62	–	dB
f_N	single frequency noise from 20 Hz to 20 kHz	idle mode	–	–	–79	dBFS
N_{idle}	idle noise	unweighted				
	20 Hz to 7 kHz		–	–	–75	dBFS
	20 Hz to 20 kHz		–	–	–69	dBFS
t_d	absolute group delay		–	–	36	$1/f_s$
Δt_d	group delay deviation	f_s = 16 kHz	–0.3	–	+0.3	µs
ΔG	gain deviation from 0 dBFS to –65 dBFS	relative to –19 dBFS at 1 kHz	–0.3	–	+0.3	dB

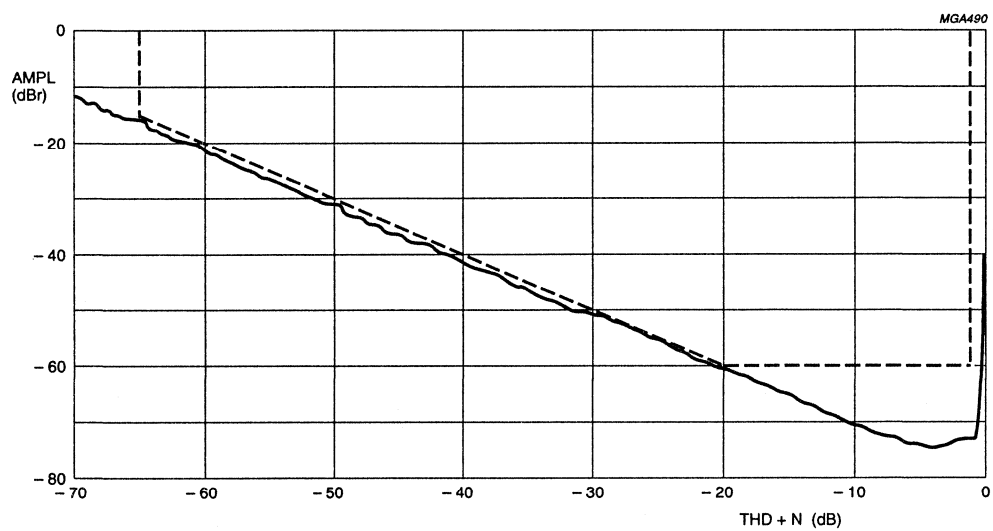


Fig.6 Typical performance of the ADC/DAC in cascade.

TYPICAL SYSTEM CONFIGURATIONS

Serial data transfer

Figure 7 illustrates a possible configuration of the PCF5012A with a PCB5010/11 using the serial interface. The data transfer is a single channel transfer.

In this configuration, the PCF5012A provides the PCB5010/11 with the system clock (MCO) and with the serial clock SCO = 128 x f_s for the serial data transmission. Therefore the system requires only one crystal for the clock supply.

For systems, where more than one channel can be multiplexed on to the same serial I/O of a processor, the allocation of transfer time slots has to be defined. Figure 8 shows a possible configuration for a two-channel cascaded system. In this configuration PCF5012A-1 starts the transfer of PCF5012A-2 and also provides the supply of clock signals to the other units.

Such a cascaded system operates as follows:

PCF5012A-1 is configured as a master (IOSTART = CONVREADY) and starts the transfer of a data byte after the availability of a new set of data. During the serial transfer, the signal $\overline{IOE}$ of the PCF5012A-1 is in the LOW state. After the end of the serial transfer, to and from PCF5012A-1, the signal $\overline{IOE}$ of PCF5012A-1 changes to the HIGH state.

PCF5012A-2 (slave PCF5012A) is triggered at the IOSTART input by the rising edge of $\overline{IOE}$ from PCF5012A-1. After PCF5012A-1 has finished its transfer PCF5012A-2 starts its own serial data transfer using the common serial data lines SDI and SDO. The transfer from PCF5012A-2 to PCF5012A-1 is therefore delayed by the transfer time of one data byte (15 SCI clock cycles). The signal processor detects, from the input flag IFA, which PCF5012A has transferred the data. Since the digital interfaces are asynchronous, in relation to the PCF5012A internal sequencing, only the transfer of the data blocks is delayed and not the actual conversion. To insure that all cascaded PCF5012As operate on the same sample, the first PCF5012A's transfer starts directly after its internal data exchange.

Figure 9 shows a functional timing diagram of the described relationships. Such a cascaded system could be extended to more than two channels. It is a necessary condition, however, that the transfer of the data of all channels is completed within one sampling period. The serial clock frequency has to be chosen sufficiently high.

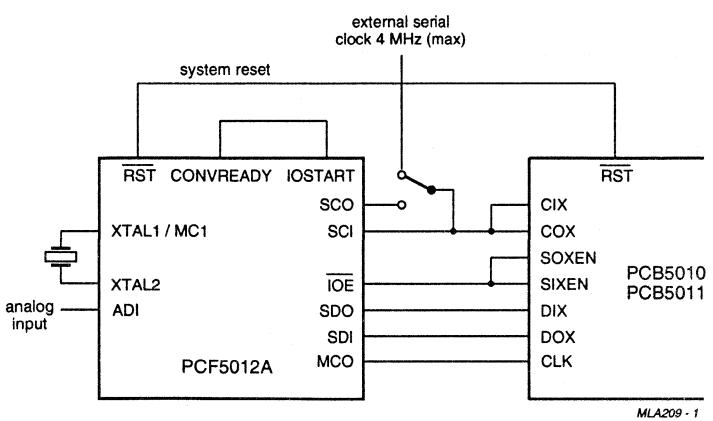


Fig.7 Single channel configuration PCF5012A and PCB5010/11.

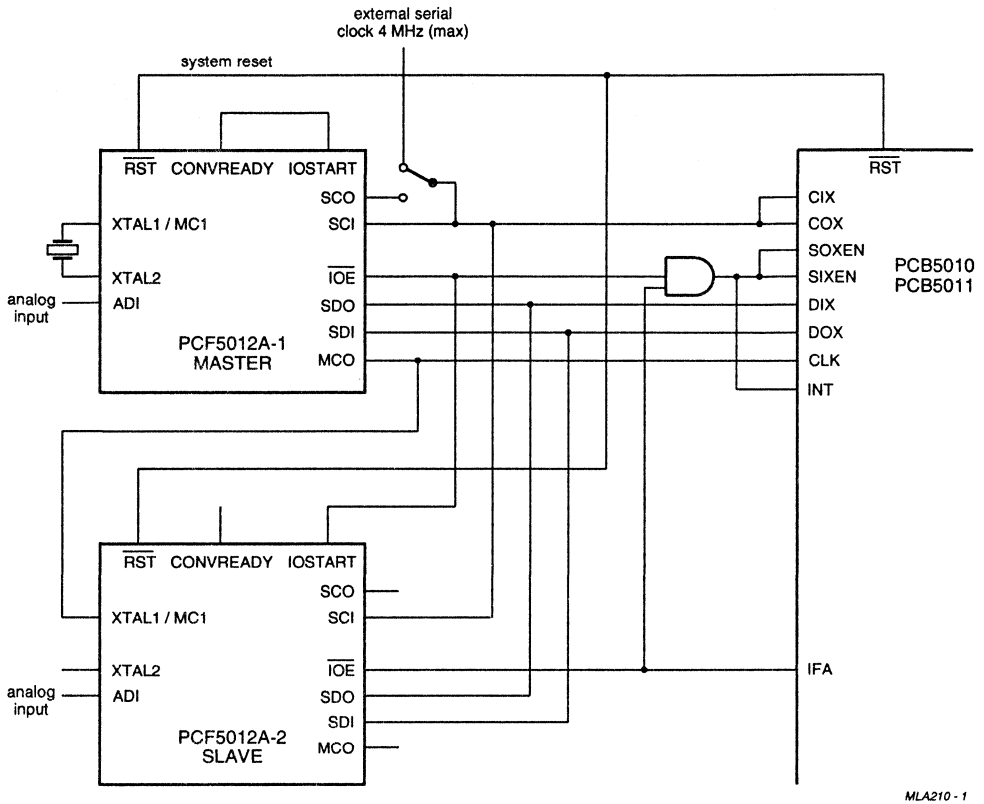


Fig.8 Cascaded two channel configuration.

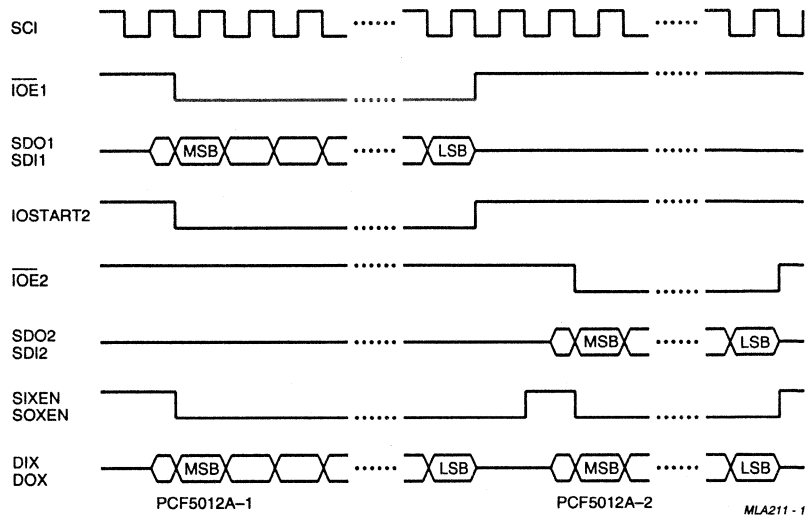


Fig.9 Timing of cascaded two channel configuration.

Parallel data transfer

Figure 10 illustrates a typical configuration for parallel data transfer.

In this configuration the signal processor PCB5010/11 communicates with a PCF5012A and, also, with an external DRAM via the parallel interface.

In this configuration the signal $\overline{DS}$ is gated with an address line (A15) from the signal processor (memory mapped). As can be seen from the signal processor, a choice is thus made between the PCF5012A and the RAM. The PCF5012A requests data transfer via the interrupt-input (INT) of the signal processor. The processor then controls the parallel data exchange via R/$\overline{W}$ and $\overline{DS}$.

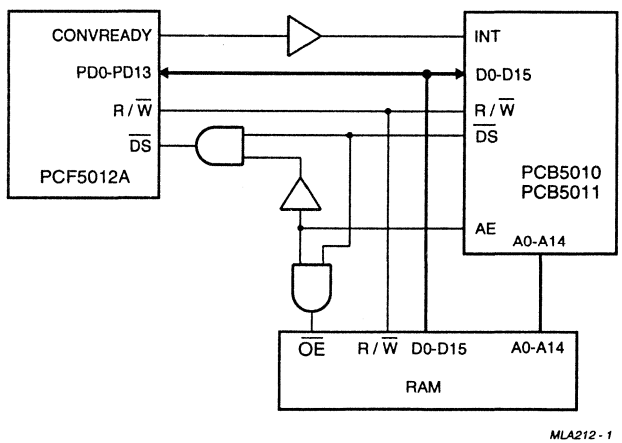


Fig.10 Possible configuration for parallel data transfer.

Single-chip 8-bit microcontroller — 80C562/83C562

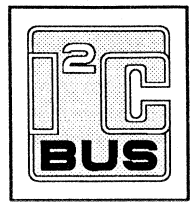
Single-chip 8-bit microcontroller with 8-bit A/D, capture/compare timer, high-speed outputs, PWM

DESCRIPTION

The 80C562/83C562 (hereafter generically referred to as 8XC562) Single-Chip 8-Bit Microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family. The 83C562/83C562 has the same instruction set as the 80C51.

The 8XC562 contains a non-volatile 256 × 8 read-only program memory, a volatile 256 × 8 read/write data memory (83C562) (the 80C562 is ROMless), a volatile 256 × 8 read/write data memory, six 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), an additional 16-bit timer coupled to capture and compare latches, a 15-source, two-priority-level, nested interrupt structure, an 8-input ADC, two pulse width modulated outputs, standard 80C51 UART, a "watchdog" timer and on-chip oscillator and timing circuits. For systems that require extra capability, the 83C562 can be expanded using standard TTL compatible memories and logic.

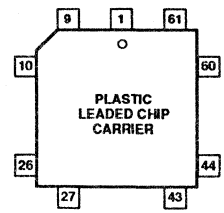
The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte and 17 three-byte. With a 12MHz crystal, 58% of the instructions are executed in 1μs and 40% in 2μs. Multiply and divide instructions require 4μs.



FEATURES

- 80C51 instruction set
- 8k × 8 ROM expandable externally to 64k bytes
- 256 × 8 RAM, expandable externally to 64k bytes
- Two standard 16-bit timer/counters
- An additional 16-bit timer/counter coupled to four capture registers and three compare registers
- Capable of producing eight synchronized, timed outputs
- An 8-bit ADC with eight multiplexed analog inputs
- Two 8-bit resolution, pulse width modulated outputs
- Five 8-bit I/O ports plus one 8-bit input port shared with analog inputs
- Full-duplex UART compatible with the standard 80C51
- On-chip watchdog timer
- Three temperature ranges
  - 0 to +70°C
  - –40 to +85°C
  - –40 to +125°C

PIN CONFIGURATION



Pin	Function	Pin	Function
1	P5.0/ADC0	35	XTAL1
2	V_{DD}	36	V_{SS}
3	STADC	37	V_{SS}
4	$\overline{PWM0}$	38	NC
5	$\overline{PWM1}$	39	P2.0/A08
6	$\overline{EW}$	40	P2.1/A09
7	P4.0/CMSR0	41	P2.2/A10
8	P4.1/CMRS1	42	P2.3/A11
9	P4.2CMSR2	43	P2.4/A12
10	P4.3/CMSR3	44	P2.5/A13
11	P4.4/CMSR4	45	P2.6/A14
12	P4.5/CMSR5	46	P2.7/A15
13	P4.6/CMT0	47	$\overline{PSEN}$
14	P4.7/CMT1	48	ALE
15	RST	49	$\overline{EA}$
16	P1.0/CT01	50	P0.7/AD7
17	P1.1/CT1I	51	P0.6/AD6
18	P1.2/CT2I	52	P0.5/AD5
19	P1.3/CT3I	53	P0.4/AD4
20	P1.4/T2	54	P0.3/AD3
21	P1.5/RT2	55	P0.2/AD2
22	P1.6	56	P0.1/AD1
23	P1.7	57	P0.0/AD0
24	P3.0/RxD	58	AVref–
25	P3.1TxD	59	AVref+
26	P3.2/$\overline{INT0}$	60	AV_{SS}
27	P3.3/$\overline{INT1}$	61	AV_{DD}
28	P3.4/T0	62	P5.7/ADC7
29	P3.5/T1	63	P5.6/ADC6
30	P3.6/$\overline{WR}$	64	P5.5/ADC5
31	P3.7/$\overline{RD}$	65	P5.4/ADC4
32	NC	66	P5.3/ADC3
33	NC	67	P5.2/ADC2
34	XTAL2	68	P5.1/ADC1

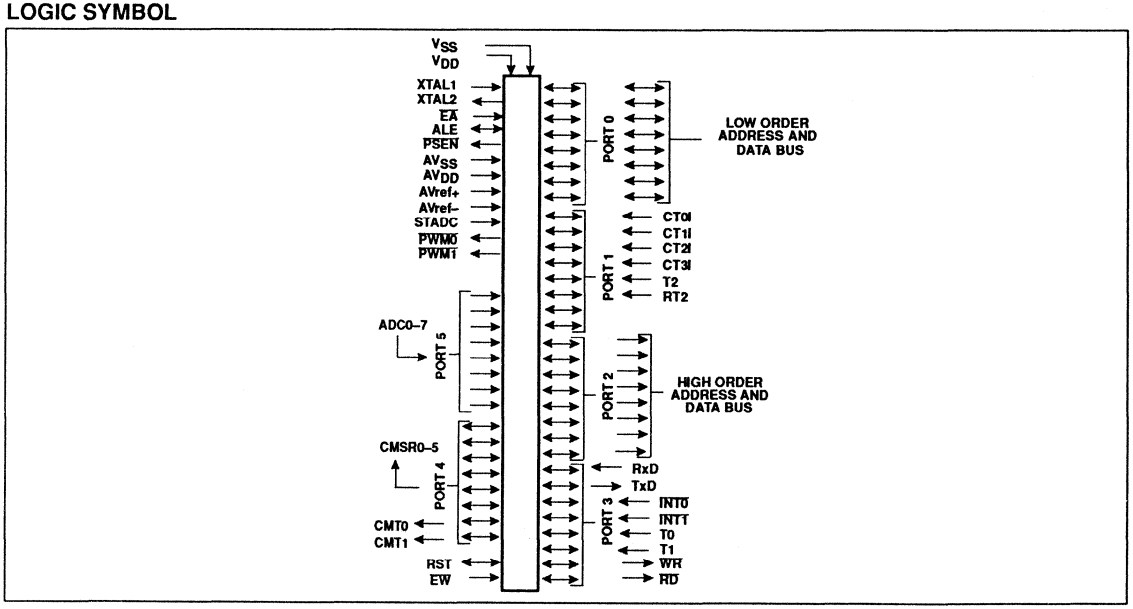
FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATA SHEET

ORDERING INFORMATION

PHILIPS PART ORDER NUMBER PART MARKING		PHILIPS NORTH AMERICA PART ORDER NUMBER					TEMPERATURE RANGE °C	
ROMless	ROM	ROMless	ROM	Drawing Number	EPROM	Drawing Number	AND PACKAGE	FREQ MHz
PCB80C562-16WP	PCB83C562-16WP/xxx	S80C562-4A68	S83C562-4A68	SOT188	S87C552-4A68[2]	0398E	0 to +70, Plastic Leaded Chip Carrier	16
					S87C552-4K68[2]	1473A	0 to +70, Plastic Leaded Chip Carrier w/Window	16
PCF80C562-12WP	PCF83C562-12WP/xxx	S80C562-2A68	S83C562-2A68	SOT188	S87C552-5A68[2]	0398E	–40 to +85, Plastic Leaded Chip Carrier	12
					S87C552-5K68[2]	1473A	–40 to +85, Plastic Leaded Chip Carrier w/Window	12
PCA80C562-12WP	PCA83C562-12WP/xxx	S80C562-6A68	S83C562-6A68	SOT188			–40 to +125, Plastic Leaded Chip Carrier	12

NOTES:
1. 80C562 and 83C562 frequency range is 1.2MHz–12MHz or 1.2MHz–16MHz.
2. 87C552 frequency range is 3.5MHz–16MHz. For full specification, see the 87C552 data sheets.
3. xxx denotes the ROM code number.

LOGIC SYMBOL



Single-chip 8-bit microcontroller P83C652; P80C652

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATA SHEET

1. FEATURES

- 80C51 central processing unit
- 8K ROM, expandable externally to 64K
- 256 bytes RAM, expandable externally to 64 kbytes
- ROM code protection
- Two standard 16-bit timer/counters
- Four 8-bit I/O ports
- I²C-bus serial I/O port with byte orientated master and slave functions
- Full-duplex UART compatible with the standard 80C51
- Extended frequency range: 1.2 to 24 MHz
- Three operating ambient temperature ranges:
  0 to +70 °C; –40 to +85 °C; –40 to +125 °C

2. GENERAL DESCRIPTION

The P80C652/P83C652 (hereafter generally referred to as 8XC652) are single-chip 8-bit microcontrollers manufactured in an advanced CMOS process; both are derivatives of the 80C51 microcontroller family. The 8XC652 has the same instruction set as the 80C51. Two versions exist:

- P83C652 - 8K mask-programmable ROM plus 256 bytes RAM
- P80C652 - ROMless version of the 83C652.

This device provides architectural enhancements that make it applicable in a variety of applications in general control systems.

The 8XC652 contains a non-volatile 8K read-only program memory, a volatile 256 bytes read/write data memory, four 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), a multi-source, two-priority-level, nested interrupt structure, two serial interfaces (UART and I²C-bus) and on-chip oscillator and timing circuits. For systems that require extra capability, the 8XC652 can be expanded using standard TTL compatible memories and logic.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte and 17 three-byte. With a 16 (24) MHz crystal, 58% of the instructions are executed in 0.75 (0.5) µs and 40% in 1.5 (1.0) µs. Multiply and divide instructions require 3 (2) µs.

3. ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			FREQUENCY RANGE (MHz)	V_{DD} RANGE (V)	TEMPERATURE RANGE (°C)
	PINS	PIN POSITION	CODE			
ROMless						
P80C652FBA	44	PLCC	SOT187	1.2 to 16	5 ±20%	0 to +70
P80C652FBB	44	QFP	SOT311	1.2 to 16	5 ±20%	0 to +70
P80C652FBP	40	DIL	SOT129	1.2 to 16	5 ±20%	0 to +70
P80C652FFA	44	PLCC	SOT187	1.2 to 16	5 ±20%	–40 to +85
P80C652FFB	44	QFP	SOT311	1.2 to 16	5 ±20%	–40 to +85
P80C652FFP	40	DIL	SOT129	1.2 to 16	5 ±20%	–40 to +85
P80C652FHA	44	PLCC	SOT187	1.2 to 16	5 ±10%	–40 to +125
P80C652FHB	44	QFP	SOT311	1.2 to 16	5 ±10%	–40 to +125
P80C652FHP	40	DIL	SOT129	1.2 to 16	5 ±10%	–40 to +125
P80C652IBA	44	PLCC	SOT187	1.2 to 24	5 ±10%	0 to +70
P80C652IBB	44	QFP	SOT311	1.2 to 24	5 ±10%	0 to +70
P80C652IBP	40	DIL	SOT129	1.2 to 24	5 ±10%	0 to +70
P80C652IFA	44	PLCC	SOT187	1.2 to 24	5 ±10%	–40 to +85
P80C652IFB	44	QFP	SOT311	1.2 to 24	5 ±10%	–40 to +85
P80C652IFP	40	DIL	SOT129	1.2 to 24	5 ±10%	–40 to +85
ROM coded						
P83C652FBA/YYY	44	PLCC	SOT187	1.2 to 16	5 ±20%	0 to +70
P83C652FBB/YYY	44	QFP	SOT311	1.2 to 16	5 ±20%	0 to +70
P83C652FBP/YYY	40	DIL	SOT129	1.2 to 16	5 ±20%	0 to +70
P83C652FFA/YYY	44	PLCC	SOT187	1.2 to 16	5 ±20%	–40 to +85
P83C652FFB/YYY	44	QFP	SOT311	1.2 to 16	5 ±20%	–40 to +85
P83C652FFP/YYY	40	DIL	SOT129	1.2 to 16	5 ±20%	–40 to +85
P83C652FHA/YYY	44	PLCC	SOT187	1.2 to 16	5 ±10%	–40 to +125
P83C652FHB/YYY	44	QFP	SOT311	1.2 to 16	5 ±10%	–40 to +125
P83C652FHP/YYY	40	DIL	SOT129	1.2 to 16	5 ±10%	–40 to +125
P83C652IBA/YYY	44	PLCC	SOT187	1.2 to 24	5 ±10%	0 to +70
P83C652IBB/YYY	44	QFP	SOT311	1.2 to 24	5 ±10%	0 to +70
P83C652IBP/YYY	40	DIL	SOT129	1.2 to 24	5 ±10%	0 to +70
P83C652IFA/YYY	44	PLCC	SOT187	1.2 to 24	5 ±10%	–40 to +85
P83C652IFB/YYY	44	QFP	SOT311	1.2 to 24	5 ±10%	–40 to +85
P83C652IFP/YYY	40	DIL	SOT129	1.2 to 24	5 ±10%	–40 to +85

Note

1. YYY = ROM code number; to be defined.

Single-chip 8-bit microcontroller P83C654

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATA SHEET

1. FEATURES

- 80C51 central processing unit
- 16K ROM, expandable externally to 64 kbytes
- 256 bytes RAM, expandable externally to 64 kbytes
- ROM code protection
- Two standard 16-bit timer/counters
- Four 8-bit I/O ports
- I²C-bus serial I/O port with byte orientated master and slave functions
- Full-duplex UART compatible with the standard 80C51
- Extended frequency range: 1.2 to 24 MHz
- Three operating ambient temperature ranges:
  0 to +70 °C; –40 to +85 °C; –40 to +125 °C

2. GENERAL DESCRIPTION

The P83C654 (hereafter generally referred to as 8XC654) is a single-chip 8-bit microcontroller manufactured in an advanced CMOS process; and is a derivative of the 80C51 microcontroller family. The 8XC654 has the same instruction set as the 80C51. One version exists:

- P83C654 - 16 kbytes mask-programmable ROM plus 256 bytes RAM

This device provides architectural enhancements that make it applicable in a variety of applications in general control systems.

The 8XC654 contains a non-volatile 16 kbytes read-only program memory, a volatile 256 byte read/write data memory, four 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), a multi-source, two-priority-level, nested interrupt structure, two serial interfaces (UART and I²C-bus) and on-chip oscillator and timing circuits. For systems that require extra capability, the 8XC654 can be expanded using standard TTL compatible memories and logic.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte and 17 three-byte. With a 16 (24) MHz crystal, 58% of the instructions are executed in 0.75 (0.5) µs and 40% in 1.5 (1.0) µs. Multiply and divide instructions require 3 (2) µs.

3. ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			FREQUENCY RANGE (MHz)	V_{DD} RANGE (V)	TEMPERATURE RANGE (°C)
	PINS	PIN POSITION	CODE			
ROM coded						
P83C654FBA/YYY	44	PLCC	SOT187	1.2 to 16	5 ±20%	0 to +70
P83C654FBB/YYY	44	QFP	SOT311	1.2 to 16	5 ±20%	0 to +70
P83C654FBP/YYY	40	DIL	SOT129	1.2 to 16	5 ±20%	0 to +70
P83C654FFA/YYY	44	PLCC	SOT187	1.2 to 16	5 ±20%	–40 to +85
P83C654FFB/YYY	44	QFP	SOT311	1.2 to 16	5 ±20%	–40 to +85
P83C654FFP/YYY	40	DIL	SOT129	1.2 to 16	5 ±20%	–40 to +85
P83C654FHA/YYY	44	PLCC	SOT187	1.2 to 16	5 ±10%	–40 to +125
P83C654FHB/YYY	44	QFP	SOT311	1.2 to 16	5 ±10%	–40 to +125
P83C654FHP/YYY	40	DIL	SOT129	1.2 to 16	5 ±10%	–40 to +125
P83C654IBA/YYY	44	PLCC	SOT187	1.2 to 24	5 ±10%	0 to +70
P83C654IBB/YYY	44	QFP	SOT311	1.2 to 24	5 ±10%	0 to +70
P83C654IBP/YYY	40	DIL	SOT129	1.2 to 24	5 ±10%	0 to +70
P83C654IFA/YYY	44	PLCC	SOT187	1.2 to 24	5 ±10%	–40 to +85
P83C654IFB/YYY	44	QFP	SOT311	1.2 to 24	5 ±10%	–40 to +85
P83C654IFP/YYY	40	DIL	SOT129	1.2 to 24	5 ±10%	–40 to +85

Note

1. YYY = ROM code number; to be defined.

CMOS single-chip 8-bit microcontroller with on-chip EEPROM

80C851/83C851

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATA SHEET

DESCRIPTION

The Philips 80C851/83C851 is a high-performance microcontroller fabricated with Philips high-density CMOS technology. The 80C851/83C851 has the same instruction set as the 80C51. The Philips CMOS technology combines the high speed and density characteristics of HMOS with the low power attributes of CMOS. The Philips epitaxial substrate minimizes latch-up sensitivity.

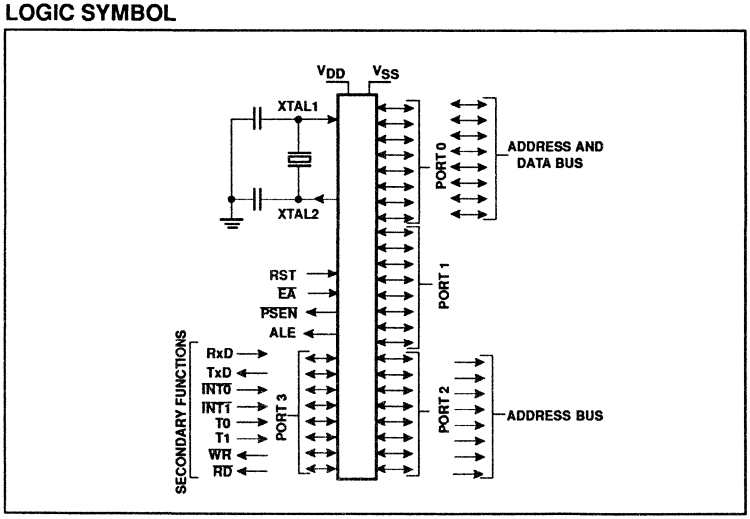
The 80C851/83C851 contains a 4k × 8 ROM with mask-programmable ROM code protection, a 128 × 8 RAM, 256 × 8 EEPROM, 32 I/O lines, two 16-bit counter/timers, a seven-source, five vector, two-priority level nested interrupt structure, a serial I/O port for either multi-processor communications, I/O expansion or full duplex UART, and on-chip oscillator and clock circuits.

In addition, the 80C851/83C851 has two software selectable modes of power reduction — idle mode and power-down mode. The idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. The power-down mode saves the RAM and EEPROM contents but freezes the oscillator, causing all other chip functions to be inoperative.

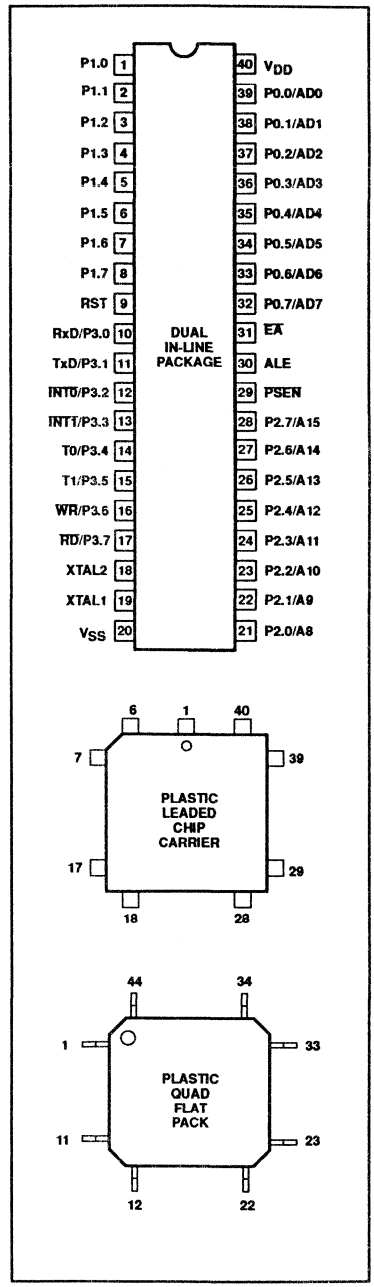
FEATURES

- 80C51 based architecture
  - 4k × 8 ROM
  - 128 × 8 RAM
  - Two 16-bit counter/timers
  - Full duplex serial channel
  - Boolean processor
- Non-volatile 256 × 8-bit EEPROM (electrically erasable programmable read only memory)
  - On-chip voltage multiplier for erase/write
  - 50,000 erase/write cycles per byte
  - 10 years non-volatile data retention
  - Infinite number of read cycles
  - User selectable security mode
  - Block erase capability
- Mask-programmable ROM code protection
- Memory addressing capability
  - 64k ROM and 64k RAM
- Power control modes:
  - Idle mode
  - Power-down mode
- CMOS and TTL compatible
- 1.2 to 16MHz
- Three package styles
- Three temperature ranges
- ROM code protection

LOGIC SYMBOL



PIN CONFIGURATIONS



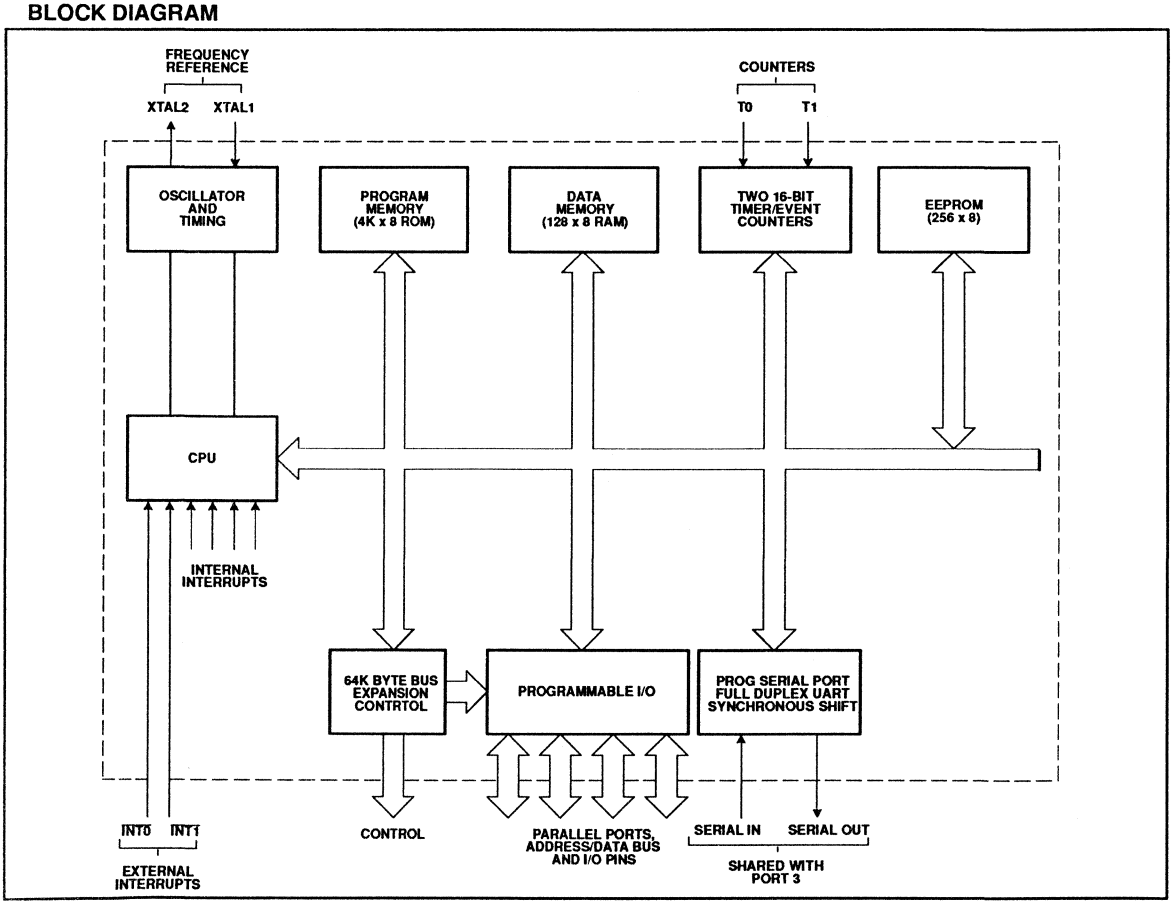
CMOS single-chip 8-bit microcontroller with on-chip EEPROM

80C851/83C851

ORDERING INFORMATION

PHILIPS PART ORDER NUMBER PART MARKING		NORTH AMERICA PHILIPS PART ORDER NUMBER		TEMPERATURE RANGE °C AND PACKAGE	FREQ. (MHz)	DRAWING NUMBER
ROMless Version	ROM Version	ROMless Version	ROM Version			
P80C851 FBP	P83C851 FBP	S80C851-4N40	S83C851-4N40	0 to +70, Plastic Dual In-line Package	1.2 to 16	SOT129
P80C851 FBA	P83C851 FBA	S80C851-4A44	S83C851-4A44	0 to +70, Plastic Leaded Chip Carrier	1.2 to 16	SOT187
P80C851 FBB	P83C851 FBB	S80C851-4B44	S83C851-4B44	0 to +70, Plastic Quad Flat Pack	1.2 to 16	SOT311
P80C851 FFP	P83C851 FFP	S80C851-5N40	S83C851-5N40	–40 to +85, Plastic Dual In-line Package	1.2 to 16	SOT129
P80C851 FFA	P83C851 FFA	S80C851-5A44	S83C851-5A44	–40 to +85, Plastic Leaded Chip Carrier	1.2 to 16	SOT187
P80C851 FFB	P83C851 FFB	S80C851-5B44	S83C851-5B44	–40 to +85, Plastic Quad Flat Pack	1.2 to 16	SOT311
P80C851 FHP	P83C851 FHP	S80C851-6N40	S83C851-6N40	–40 to +125, Plastic Dual In-line Package	1.2 to 16	SOT129
P80C851 FHA	P83C851 FHA	S80C851-6A44	S83C851-6A44	–40 to +125, Plastic Leaded Chip Carrier	1.2 to 16	SOT187
P80C851 FHB	P83C851 FHB	S80C851-6B44	S83C851-6B44	–40 to +125, Plastic Quad Flat Pack	1.2 to 16	SOT311

BLOCK DIAGRAM



Single-chip 8-bit microcontroller PCF84CXXXA Family

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC14 OR DATA SHEET

INTRODUCTION

This datasheet describes the shared properties of the PCF84CXXXA family of microcontrollers and its quickly growing number of derivative microcontrollers. For a particular microcontroller, this datasheet should be read in conjunction with the individual datasheet of the specific device.

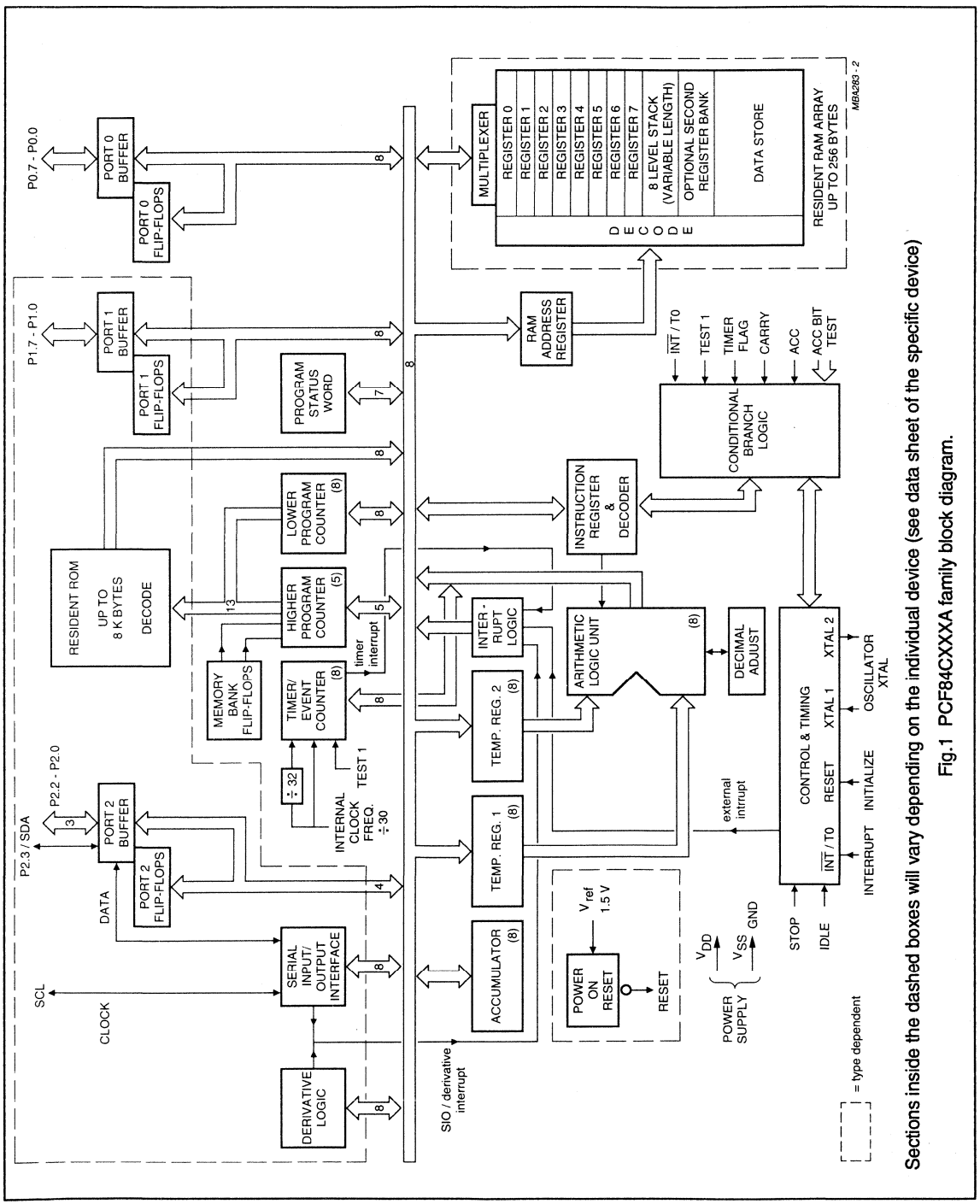
FEATURES

- 8-bit CPU, ROM, RAM, I/O all in one package
- Up to 8K ROM bytes
- Up to 256 RAM bytes
- Over 100 instructions (based on MAB8048) all of 1 or 2 cycles
- 8 or more quasi-bidirectional I/O port lines
- 8-bit programmable timer/event counter 1
- 3 single-level vectored interrupts: external, timer/event counter, SIO/derivative
- Two test inputs, one of which also serves as the external interrupt input
- Serial I/O interface (some devices only)
- Power-on-reset, stop and idle modes
- Supply range V_{DD}: 2.5 V to 6 V
- Clock frequency: 1 MHz to 16 MHz
- Operating temperature range: –40 °C to +85 °C
- Manufactured in silicon gate CMOS process.

GENERAL DESCRIPTION

The PCF84CXXXA family of microcontrollers provide up to 8k bytes of program memory and up to 256 bytes of RAM. All devices include flexible I/O ports, an 8-bit programmable timer/event counter and a choice of single-level vectored interrupts. The instruction set is based on that of the well-known MAB8048. Being similar to the MAB8400 family of NMOS controllers, some devices can serve as CMOS replacements, especially where the lower power consumption and higher speed provide advantages.

A range of prototyping devices with external program memory and 'piggy backs', as well as emulation probes and prototyping systems are available.



Sections inside the dashed boxes will vary depending on the individual device (see data sheet of the specific device)

Fig.1 PCF84CXXXA family block diagram.

Table 1 Pin functions (for the individual pinning configuration consult the datasheet of the specific device)

SYMBOL	TYPE	FUNCTION
V_{SS}	P	ground
V_{DD}	P	positive supply voltage
XTAL1	I	crystal oscillator/external clock input
XTAL2	O	crystal oscillator output
RESET	I	reset input
INT/T0	I	interrupt/test 0
T1	I	test 1/count input of 8-bit timer/event counter 1
P0.0 - P0.7	I/O	Port 0: quasi-bidirectional I/O lines
P1.0 - P1.7	I/O	Port 1: quasi-bidirectional I/O lines
P2.0 - P2.2	I/O	Port 2: quasi-bidirectional I/O line
SDA/P2.3	I/O	bidirectional data line of the serial I/O interface/Port 2: quasi-bidirectional I/O line
SCLK	I/O	bidirectional clock line of the serial I/O interface

DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC11 OR DATA SHEET

8-BIT A/D AND D/A CONVERTER

GENERAL DESCRIPTION

The PCF8591 is a single chip, single supply low power 8-bit CMOS data acquisition device with four analogue inputs, one analogue output and a serial I^2C bus interface. Three address pins A0, A1 and A2 are used for programming the hardware address, allowing the use of up to eight devices connected to the I^2C bus without additional hardware. Address, control and data to and from the device are transferred serially via the two-line bidirectional bus (I^2C).

The functions of the device include analogue input multiplexing, on-chip track and hold function, 8-bit analogue-to-digital conversion and an 8-bit digital-to-analogue conversion. The maximum conversion rate is given by the maximum speed of the I^2C bus.

Features

- Single power supply
- Operating supply voltage 2,5 V to 6 V
- Low standby current
- Serial input/output via I^2C bus
- Address by 3 hardware address pins
- Sampling rate given by I^2C bus speed
- 4 analogue inputs programmable as single-ended or differential inputs
- Auto-incremented channel selection
- Analogue voltage range from V_{SS} to V_{DD}
- On-chip track and hold circuit
- 8-bit successive approximation A/D conversion
- Multiplying DAC with one analogue output

APPLICATIONS

Closed loop control systems; low power converter for remote data acquisition; battery operated equipment; acquisition of analogue values in automotive, audio and TV applications.

PACKAGE OUTLINES

PCF8591P:16-lead DIL; plastic (SOT38).
PCF8591T:16-lead mini-pack; plastic (SO16L; SOT162A).

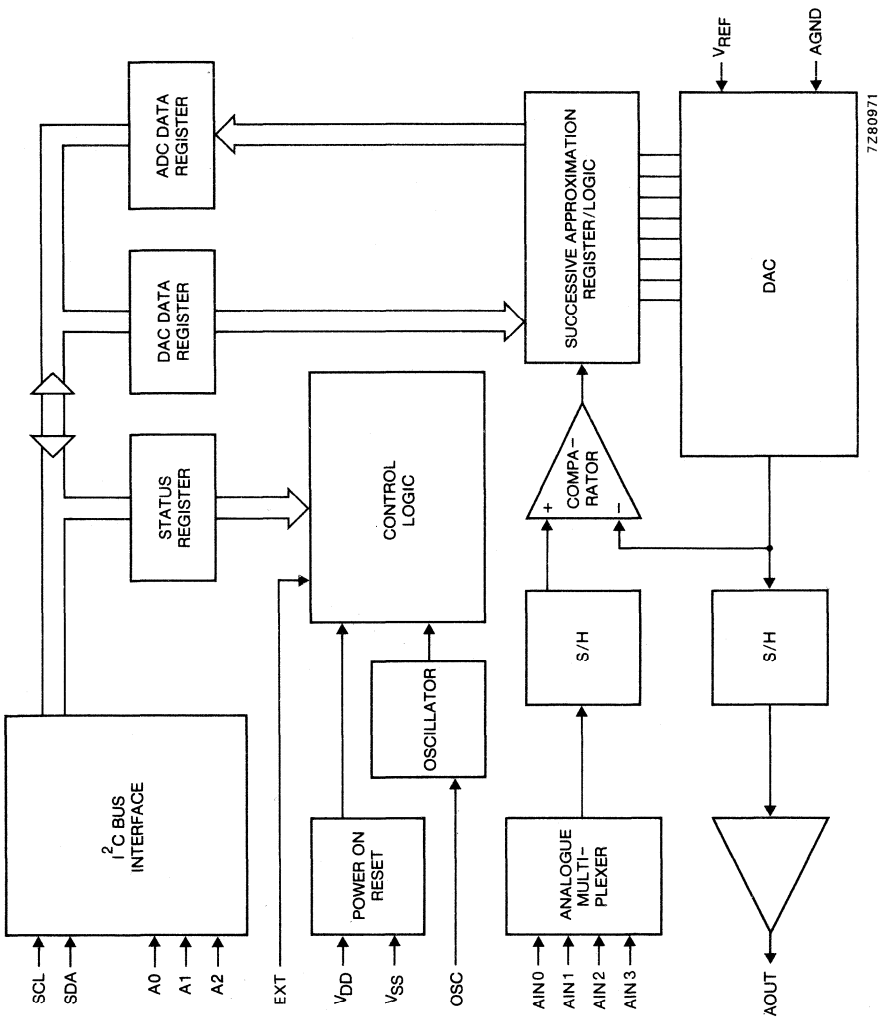


Fig. 1 Block diagram.

Low voltage high performance mixer FM IF system — SA607

DESCRIPTION

The SA607 is a low voltage high performance monolithic FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), voltage regulator and audio and RSSI op amps. The SA607 is available in 20-lead dual-in-line plastic, 20-lead SOL (surface-mounted miniature package) and 20-lead SSOP package.

The SA607 was designed for portable communication applications and will function down to 2.7V. The RF section is similar to the famous NE605. The audio output has an internal amplifier with the feedback pin accessible. The RSSI output is buffered. The SA607 also has an extra limiter output. This signal is buffered from the output of the limiter and can be used to perform frequency check. This is accomplished by comparing a reference frequency with the frequency check signal using a comparator to a varactor or PLL at the oscillator inputs.

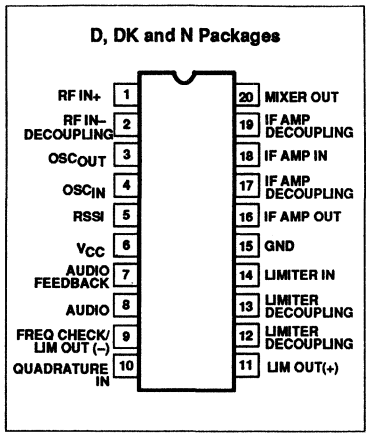
FEATURES

- Low power consumption: 3.5mA typical at 3V
- Mixer input to >150MHz
- Mixer conversion power gain of 17dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator or external oscillator can be used at higher frequencies)
- 102dB of IF Amp/Limiter gain
- 2MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a 90dB dynamic range
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.31μV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone, 8kHz deviation with RF at 45MHz and IF at 455kHz
- SA607 meets cellular radio specifications
- Audio output internal op amp
- RSSI output internal op amp
- Buffered frequency check output
- Internal op amps with rail-to-rail outputs
- ESD protection: Human Body Model 2kV
  Robot Model 200V

APPLICATIONS

- Portable cellular radio FM IF
- Cordless phones
- Narrow band cellular applications (NAMPS/NTACS)
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Portable high performance communication receivers
- Single conversion VHF receivers
- Wireless systems

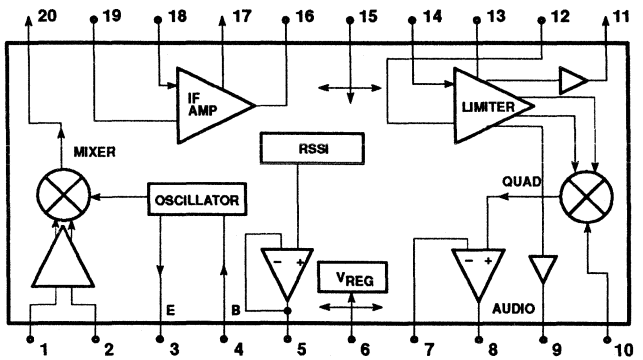
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic DIP	-40 to +85°C	SA607N	0408B
20-Pin Plastic SOL (Surface-mount)	-40 to +85°C	SA607D	0172D
20-Pin Plastic SSOP (Surface-mount)	-40 to +85°C	SA607DK	1563

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	7	V
T_{STG}	Storage temperature range	–65 to +150	°C
T_A	Operating ambient temperature range SA607	–40 to +85	°C
θ_{JA}	Thermal impedance D package DK package N package	90 117 75	°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA607			
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		2.7		7.0	V
I_{CC}	DC current drain			3.5	4.2	mA

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +3V, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step-up; IF frequency = 455kHz; R17 = 2.4k; R18 = 3.3k; RF level = –45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with de-emphasis filter and C-message weighted filter. Test circuit 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS SA607 MIN	LIMITS SA607 TYP	LIMITS SA607 MAX	UNITS
Mixer/Osc section (ext LO = 220mV$_{RMS}$)						
f_{IN}	Input signal frequency			150		MHz
f_{OSC}	Crystal oscillator frequency			150		MHz
	Noise figure at 45MHz			6.2		dB
	Third–order input intercept point (50Ω source)	f1 = 45.0; f2 = 45.06MHz Input RF Level = –52dBm		–9		dBm
	Conversion power gain	Matched 14.5dBV step–up	13.5	17	19.5	dB
		50Ω source		+2.5		dB
	RF input resistance	Single–ended input		8		kΩ
	RF input capacitance			3.0	4.0	pF
	Mixer output resistance	(Pin 20)	1.25	1.5		kΩ
IF section						
	IF amp gain	50Ω source		44		dB
	Limiter gain	50Ω source		58		dB
	Input limiting –3dB, R_{17} = 2.4k	Test at Pin 18		–109		dBm
	AM rejection	80% AM 1kHz		45		dB
	Audio level	Gain of two (2kΩ AC load)	70	120	160	mV
	SINAD sensitivity	RF level –110dB		17		dB
THD	Total harmonic distortion		–35	–50		dB
S/N	Signal–to–noise ratio	No modulation for noise		62		dB
	IF RSSI output, R_9 = 2kΩ[1]	IF level = –118dBm		0.3	0.8	V
		IF level = –68dBm	.70	1.1	1.80	V
		IF level = –23dBm	1.2	1.8	2.5	V
	RSSI range			90		dB
	RSSI accuracy			±1.5		dB
	IF input impedance		1.3	1.5		kΩ
	IF output impedance			0.3		kΩ
	Limiter input impedance		1.30	1.5		kΩ
	Limiter output impedance	(Pin 11)		200		Ω
	Limiter output level	(Pin 11) No load 5kΩ load		130 115		mV$_{RMS}$
	Frequency check/limiter output impedance	(Pin 9)		200		Ω
	Frequency check/limiter output level	(Pin 9) No load 5kΩ load		130 115		mV$_{RMS}$
RF/IF section (Int LO)						
	Audio level	3V = V_{CC}, RF level = –27dBm		120		mV$_{RMS}$
	System RSSI output	3V = V_{CC}, RF level = –27dBm		2.2		V
	System SINAD sensitivity	RF level = –117dBm		12		dB

NOTE:

1. The generator source impedance is 50Ω, but the SA607 input impedance at Pin 18 is 1500Ω. As a result, IF level refers to the actual signal that enters the SA607 input (Pin 18) which is about 21dB less than the "available power" at the generator.

CIRCUIT DESCRIPTION

The SA607 is an IF signal processing system suitable for second IF systems with input frequency as high as 150MHz. The bandwidth of the IF amplifier and limiter is at least 2MHz with 90dB of gain. The gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 6.2dB, conversion gain of 17dB, and input third-order intercept of –9dBm. The oscillator will operate in excess of 200MHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

The output impedance of the mixer is a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. The IF amplifier has 43dB of gain and 5.5MHz bandwidth. The IF limiter has 60dB of gain and 4.5MHz bandwidth. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor or an L pad for simultaneous loss and impedance matching can be added between the first IF output (Pin 16) and the interstage network. The overall gain will then be 90dB with 2MHz bandwidth.

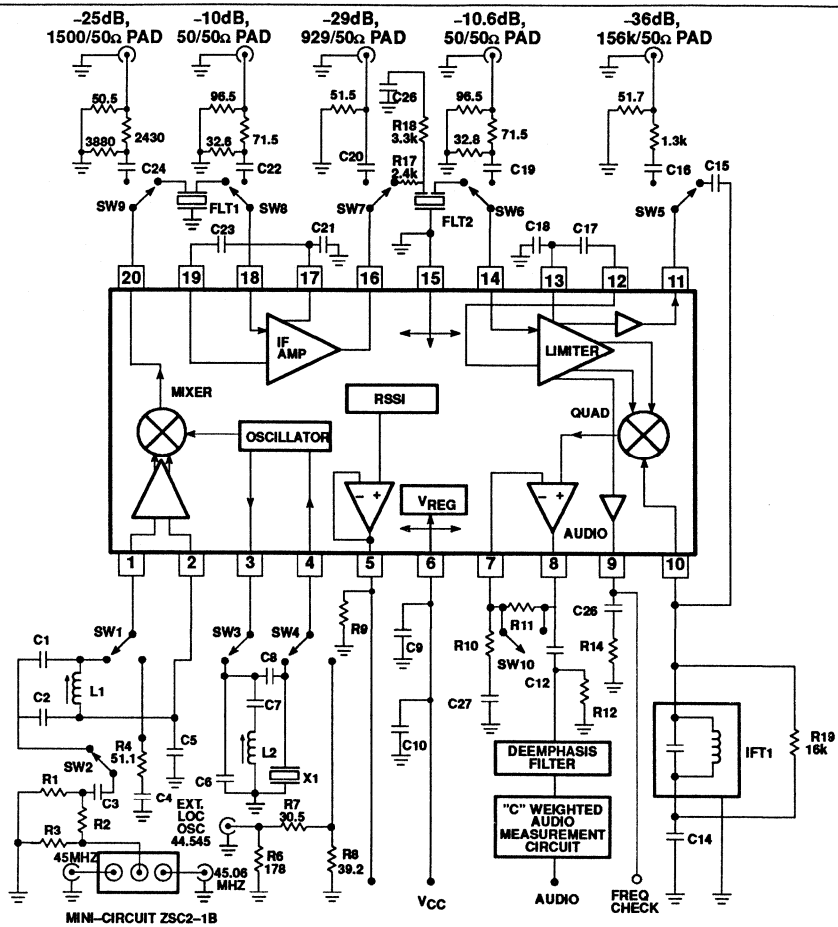
The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

The demodulated output of the quadrature drives an internal op amp. This op amp can be configured as a unity gain buffer, or for simultaneous gain, filtering, and 2nd-order temperature compensation if needed. It can drive an AC load as low as 5kΩ with a rail-to-rail output.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone. This signal is buffered through an internal unity gain op amp. The frequency check pin provides a buffered limiter output. This is useful for implementing an AFC (Automatic Frequency Check) function. This same output can also be used in conjunction with limiter output (Pin 11) for demodulating FSK (Frequency Shift Keying) data. Both pins are of the same amplitude, but 180° out of phase.

NOTE: Limiter output or Frequency Check output has drive capability of a load minimum of 2kΩ or higher to obtain 115mV output level.

NOTE: $dB(v) = 20\log V_{OUT}/V_{IN}$

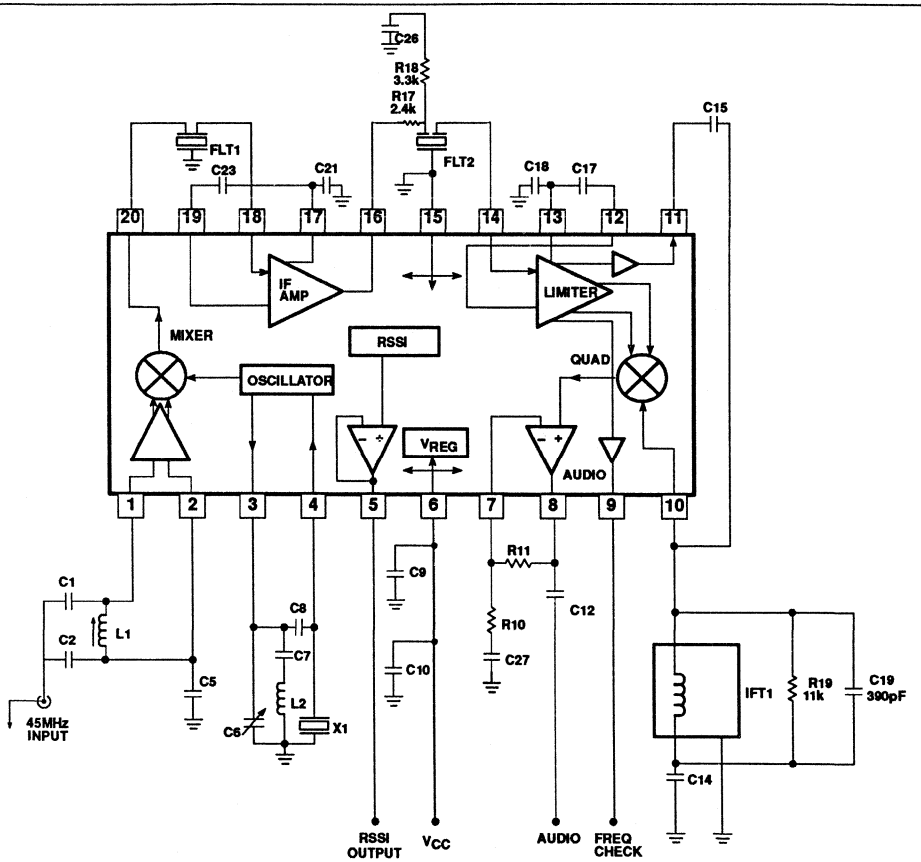


Automatic Test Circuit Component List

C1	100pF NPO Ceramic
C2	390pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	10μF Tantalum (minimum) *
C12	2.2μF
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
C26	0.1μF ±10% Monolithic Ceramic
C27	2.2μF
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	455kHz (Ce = 180pF) Toko RMC-2A6597H
L1	147-160nH Coilcraft UNI-10/142-04J08S
L2	0.8μH nominal Toko 292CNS-T1038Z
X1	44.545MHz Crystal ICM4712701
R9	2kΩ ±1% 1/4W Metal Film
R10	8.2kΩ ±1%
R11	10kΩ ±1%
R12	2kΩ ±1%
R14	5kΩ ±1%
R17	2.4kΩ ±5% 1/4W Carbon Composition
R18	3.3kΩ ±5% 1/4W Carbon Composition
R19	16kΩ ±5% 1/4W Carbon Composition

*NOTE: This value can be reduced when a battery is the power source.

Figure 1. SA607 45MHz Test Circuit (Relays as shown)



SA607D/DK
Application Component List

C1	51pF NPO Ceramic
C2	220pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	5-30pF trim cap
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	10μF Tantalum (minimum) *
C12	2.2μF ±10% Tantalum
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C19	390pF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C26	100nF ±10% Monolithic Ceramic
C27	2.2μF Tantalum
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	330μH TOKO 303LN-1130
L1	.33μH TOKO SCB-1320Z
L2	1.2μH Coilcraft 1008C S-122
X1	44.545MHz Crystal Hy-Q
R5	Not Used in Application Board (see Note 8, pg 8)
R10	8.2k ±5% 1/4W Carbon Composition
R11	10k ±5% 1/4W Carbon Composition
R17	2.4k ±5% 1/4W Carbon Composition
R18	3.3k ±5% 1/4W Carbon Composition
R19	11k ±5% 1/4W Carbon Composition

*NOTE: This value can be reduced when a battery is the power source.

Figure 2. SA607 45MHz Application Circuit

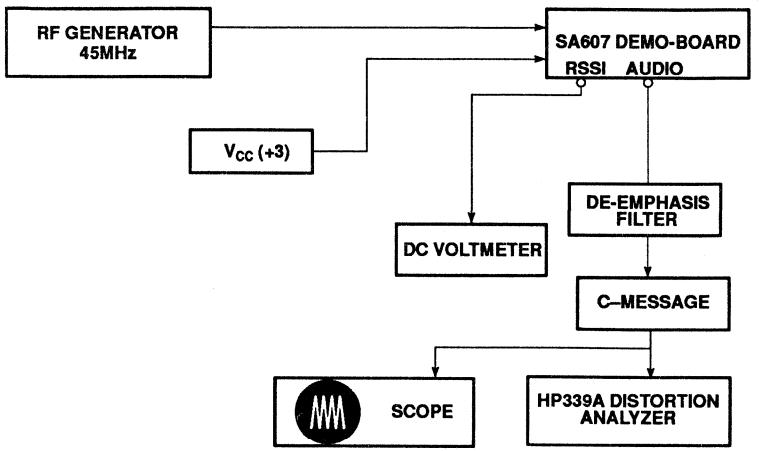


Figure 3. SA607 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message and de-emphasis filter combination has a peak gain of 10 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer. The de-emphasis filter has a fixed -6dB/Octave slope between 300Hz and 3kHz.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.35μV or –116dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 500mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10-15μF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1μF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2-3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 22kΩ, but should not be below 10kΩ.

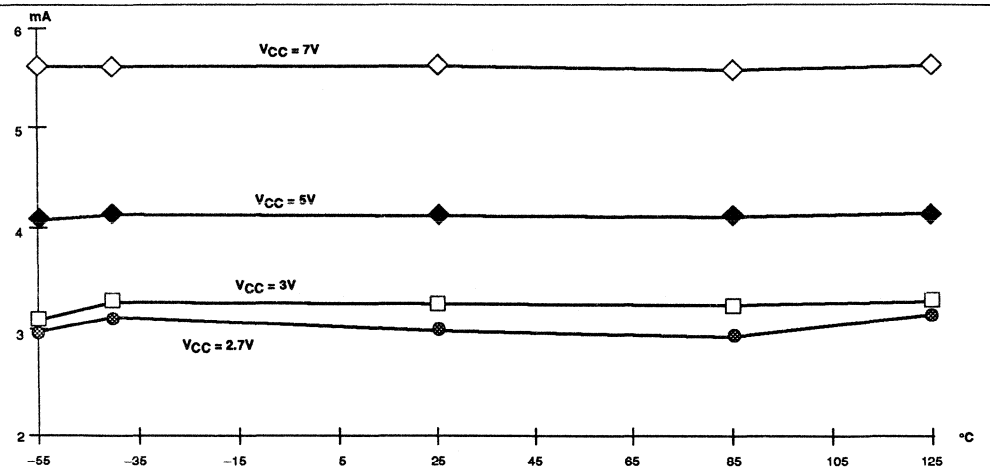


Figure 4. I_{CC} vs Temperature

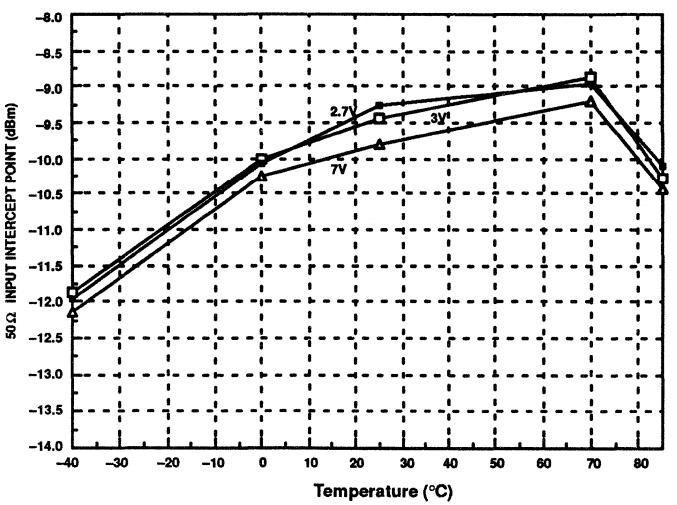


Figure 5. Third Order Intercept Point vs Supply Voltage

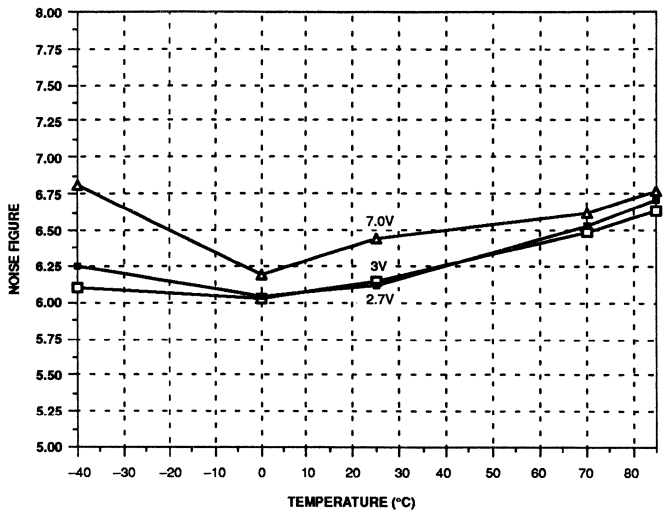


Figure 6. Mixer Noise Figure vs Supply Voltage

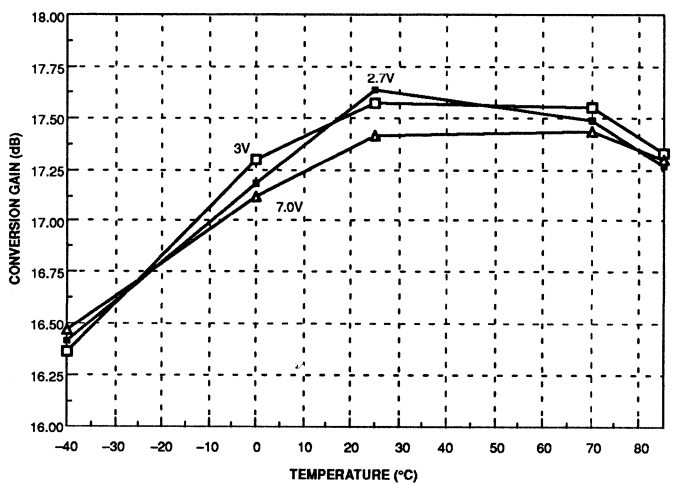


Figure 7. Conversion Gain vs Supply Voltage

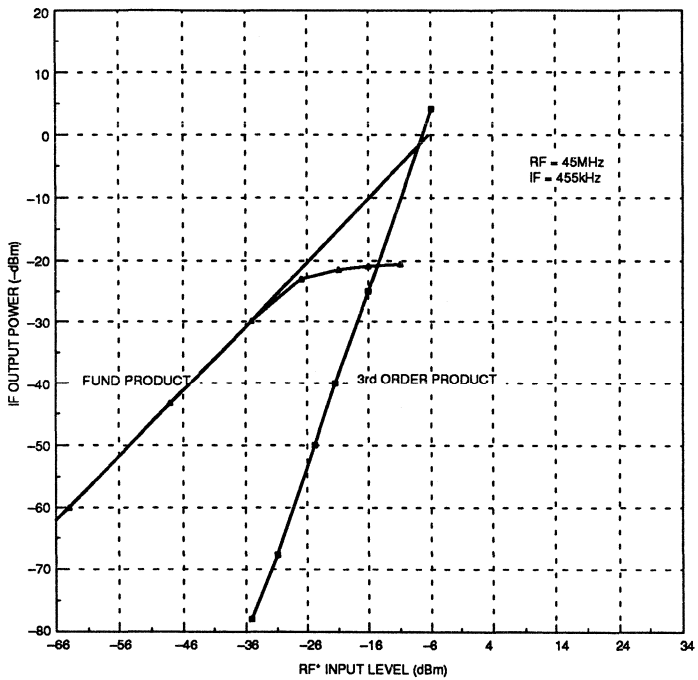


Figure 8. Mixer Third Order Intercept and Compression

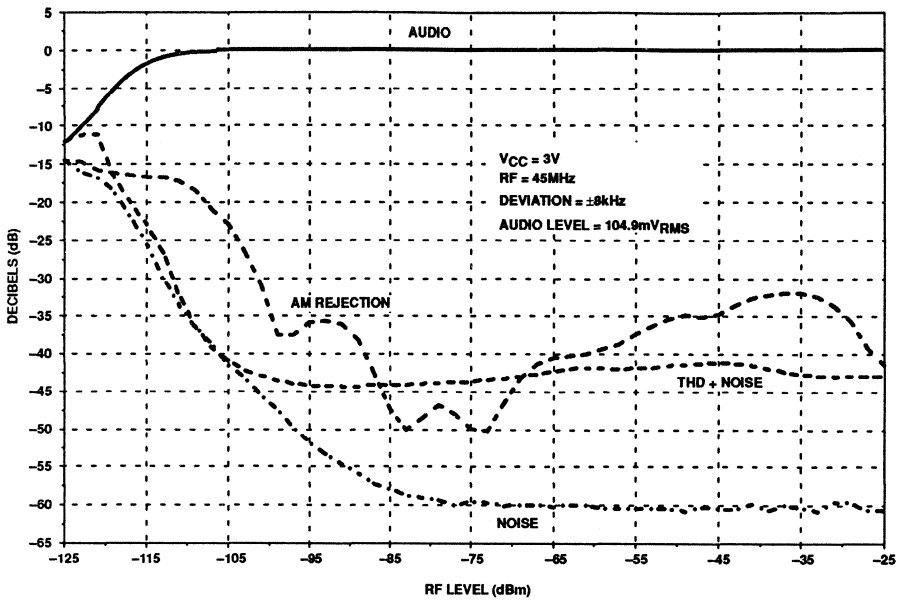


Figure 9. Sensitivity vs RF Level (–40°C)

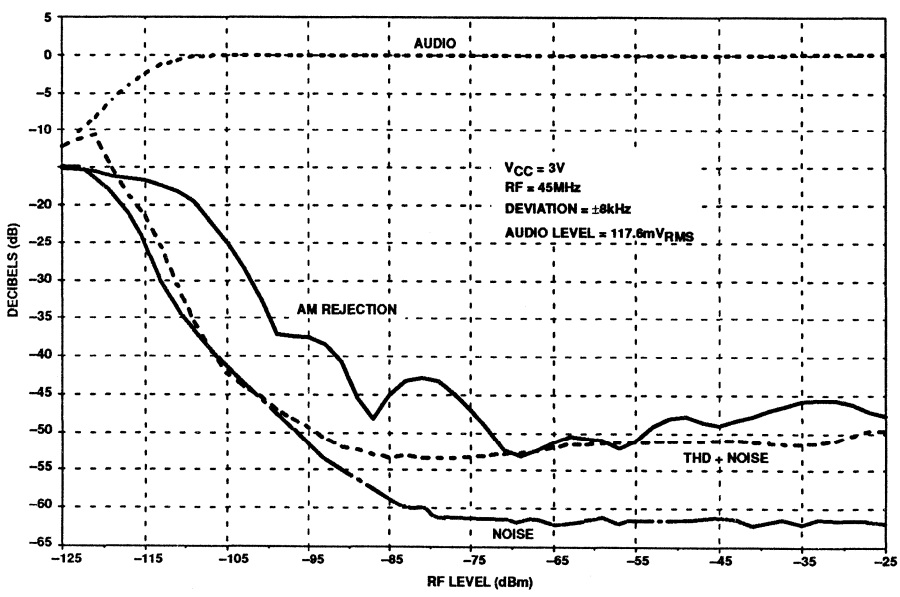


Figure 10. Sensitivity vs RF Level (+25°C)

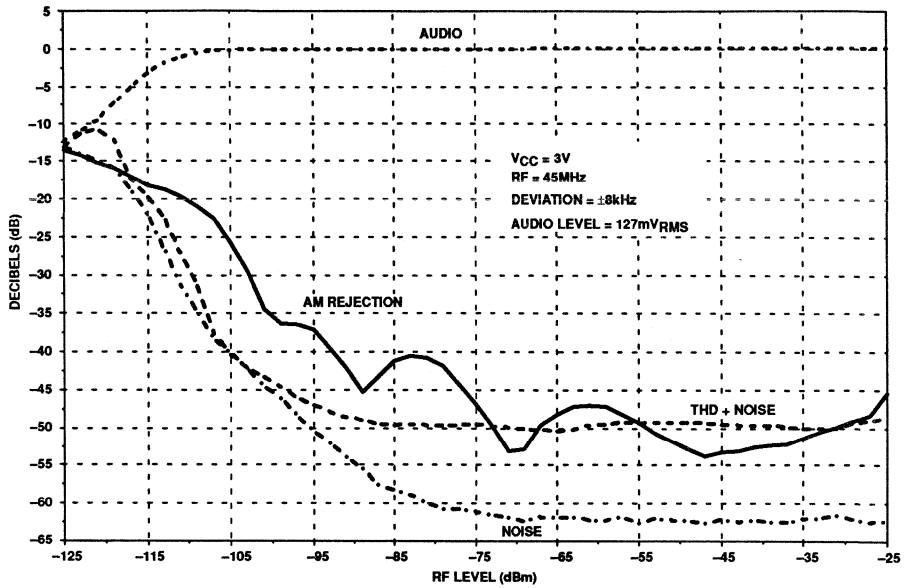


Figure 11. Sensitivity vs RF Level (Temperature 85°C)

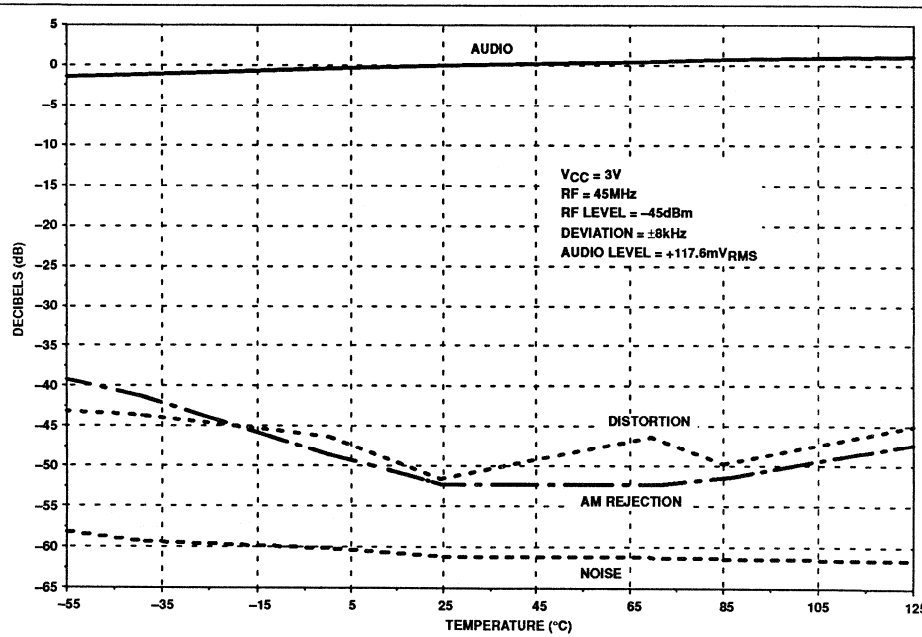


Figure 12. Relative Audio Level, Distortion, AM Rejection and Noise vs Temperature

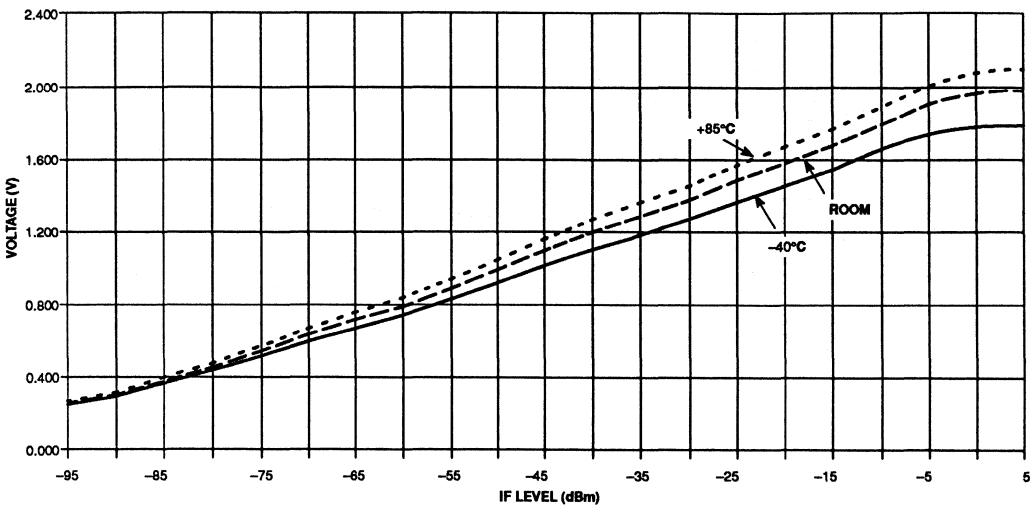


Figure 13. RSSI (455kHz IF @ 3V)

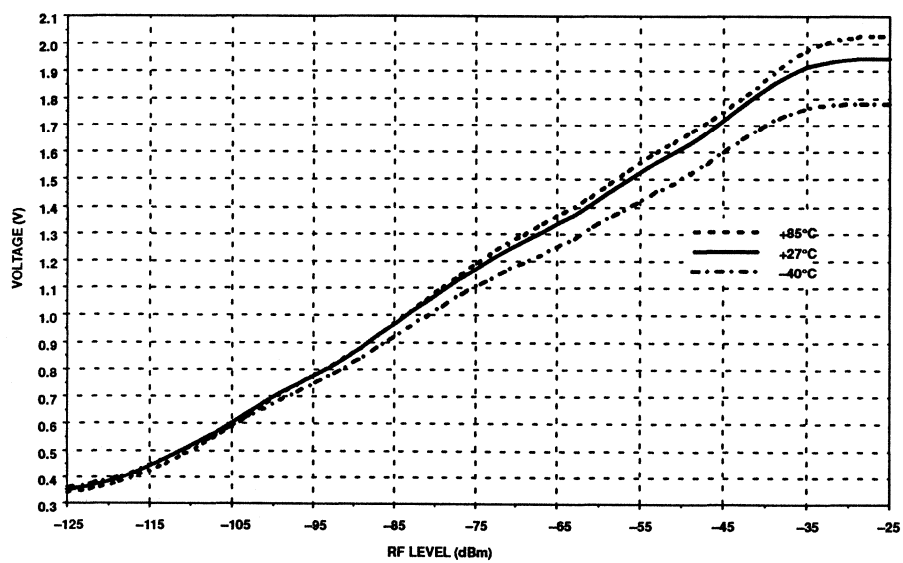


Figure 14. RSSI vs RF Level and Temperature - V_{CC} = 3V

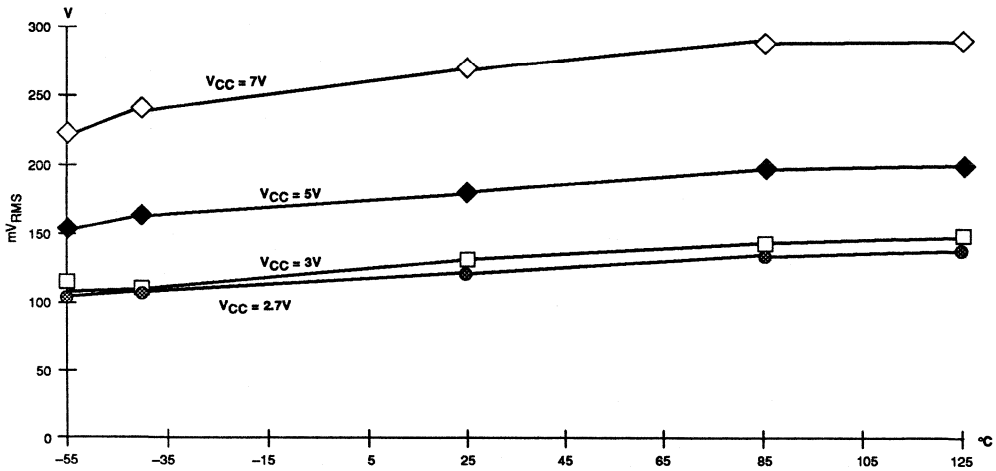
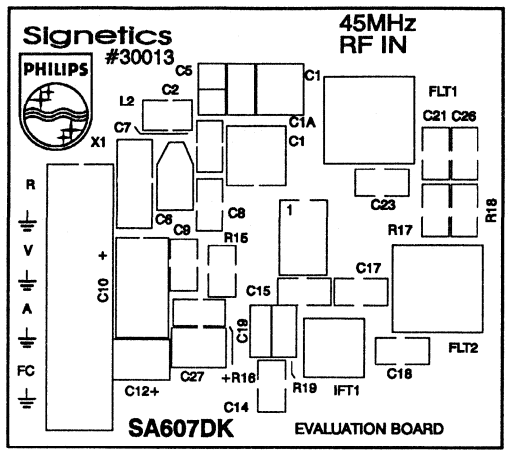
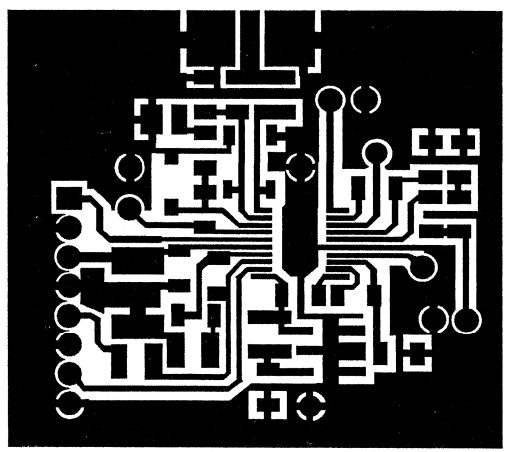


Figure 15. Audio Output vs Temperature

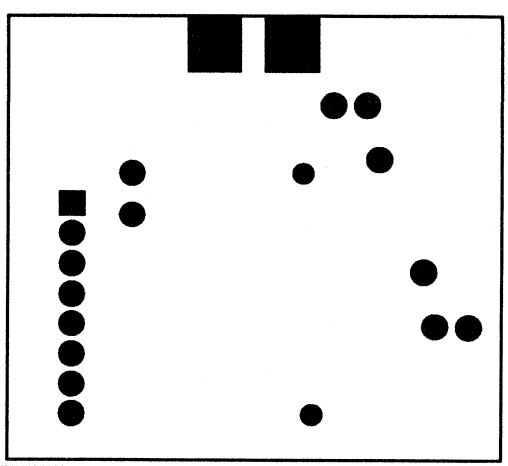
607 Silk Screen



607 TOP



607 BOTTOM



NOTE;
All views are TOP VIEW and not actual size. For reference only.

Low voltage high performance mixer FM IF system — SA608

DESCRIPTION

The SA608 is a low voltage high performance monolithic FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), voltage regulator and audio and RSSI op amps. The SA608 is available in 20-lead dual-in-line plastic, 20-lead SOL (surface-mounted miniature package) and 20-lead SSOP package.

The SA608 was designed for portable communication applications and will function down to 2.7V. The RF section is similar to the famous NE605. The audio output is buffered. The RSSI output has an internal amplifier with the feedback pin accessible. The SA608 also has an extra limiter output. This signal is buffered from the output of the limiter and can be used to perform frequency check. This is accomplished by comparing a reference frequency with the frequency check signal using a comparator to a varactor or PLL at the oscillator inputs.

FEATURES

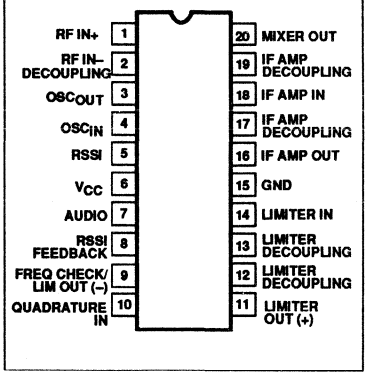
- Low power consumption: 3.5mA typical at 3V
- Mixer input to >150MHz
- Mixer conversion power gain of 17dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator or external oscillator can be used at higher frequencies)
- 102dB of IF Amp/Limiter gain
- 2MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a 90dB dynamic range
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.31μV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone, 8kHz deviation with RF at 45MHz and IF at 455kHz
- SA608 meets cellular radio specifications
- Audio output internal op amp
- RSSI output internal op amp
- Buffered frequency check output
- Internal op amps with rail-to-rail outputs
- ESD protection: Human Body Model 2kV
  Robot Model 200V

APPLICATIONS

- Portable cellular radio FM IF
- Cordless phones
- Narrow band cellular applications (NAMPS/NTACS)
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Portable high performance communication receivers
- Single conversion VHF receivers
- Wireless systems

PIN CONFIGURATION

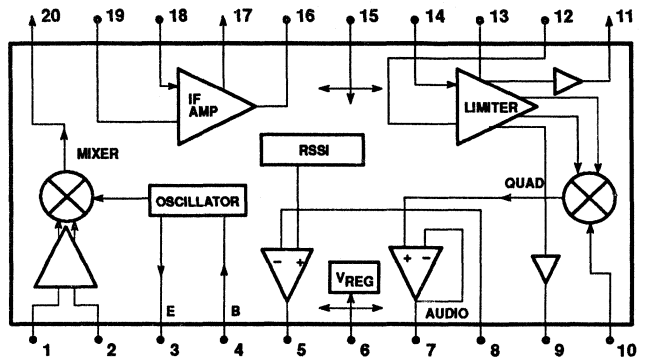
D, DK and N Packages



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic DIP	-40 to +85°C	SA608N	0408B
20-Pin Plastic SOL (Surface-mount)	-40 to +85°C	SA608D	0172D
20-Pin Plastic SSOP (Surface-mount)	-40 to +85°C	SA608DK	1563

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	7	V
T_{STG}	Storage temperature range	–65 to +150	°C
T_A	Operating ambient temperature range SA608	–40 to +85	°C
θ_{JA}	Thermal impedance D package DK package N package	90 117 75	°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA608			
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		2.7		7.0	V
I_{CC}	DC current drain			3.5	4.2	mA

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +3V, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step-up; IF frequency = 455kHz; R17 = 2.4k; R18 = 3.3k; RF level = –45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with de-emphasis filter and C-message weighted filter. Test circuit 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS SA608			UNITS
			MIN	TYP	MAX	
Mixer/Osc section (ext LO = 220mV$_{RMS}$)						
f_{IN}	Input signal frequency			150		MHz
f_{OSC}	Crystal oscillator frequency			150		MHz
	Noise figure at 45MHz			6.2		dB
	Third–order input intercept point (50Ω source)	f1 = 45.0; f2 = 45.06MHz Input RF Level = –52dBm		–9		dBm
	Conversion power gain	Matched 14.5dBV step–up	13.5	17	19.5	dB
		50Ω source		+2.5		dB
	RF input resistance	Single–ended input		8		kΩ
	RF input capacitance			3.0	4.0	pF
	Mixer output resistance	(Pin 20)	1.25	1.5		kΩ
IF section						
	IF amp gain	50Ω source		44		dB
	Limiter gain	50Ω source		58		dB
	Input limiting –3dB, R_{17} = 2.4k	Test at Pin 18		–109		dBm
	AM rejection	80% AM 1kHz		45		dB
	Audio level[2]		35	60	80	mV
	SINAD sensitivity	RF level –110dB		17		dB
THD	Total harmonic distortion		–35	–50		dB
S/N	Signal–to–noise ratio	No modulation for noise		62		dB
	IF RSSI output, R_9 = 2kΩ[1]	IF level = –118dBm		0.3	0.8	V
		IF level = –68dBm	.70	1.1	1.80	V
		IF level = –23dBm	1.2	1.8	2.5	V
	RSSI range			90		dB
	RSSI accuracy			±1.5		dB
	IF input impedance		1.3	1.5		kΩ
	IF output impedance			0.3		kΩ
	Limiter input impedance		1.30	1.5		kΩ
	Limiter output impedance	(Pin 11)		200		Ω
	Limiter output level	(Pin 11) no load 5kΩ load		130 115		mV$_{RMS}$
	Frequency check/lim (–) output impedance	(Pin 9)		200		Ω
	Frequency check/lim (–) output level	(Pin 9) no load 5kΩ load		130 115		mV$_{RMS}$
RF/IF section (int LO)						
	Audio level	3V = V_{CC}, RF level = –27dBm		120		mV$_{RMS}$
	System RSSI output	3V = V_{CC}, RF level = –27dBm		2.2		V
	System SINAD sensitivity	RF level = –117dBm		12		dB

NOTE:

1. The generator source impedance is 50Ω, but the SA608 input impedance at Pin 18 is 1500Ω. As a result, IF level refers to the actual signal that enters the SA608 input (Pin 18) which is about 21dB less than the "available power" at the generator.
2. By using 45kΩ load across the Quad detector coil, you will have Audio output at 115mV with –42dB distortion.

CIRCUIT DESCRIPTION

The SA608 is an IF signal processing system suitable for second IF systems with input frequency as high as 150MHz. The bandwidth of the IF amplifier and limiter is at least 2MHz with 90dB of gain. The gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 6.2dB, conversion gain of 17dB, and input third-order intercept of –9dBm. The oscillator will operate in excess of 200MHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

The output impedance of the mixer is a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. The IF amplifier has 43dB of gain and 5.5MHz bandwidth. The IF limiter has 60dB of gain and 4.5MHz bandwidth. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor or an L pad for simultaneous loss and impedance matching can be added between the first IF output (Pin 16) and the interstage network. The overall gain will then be 90dB with 2MHz bandwidth.

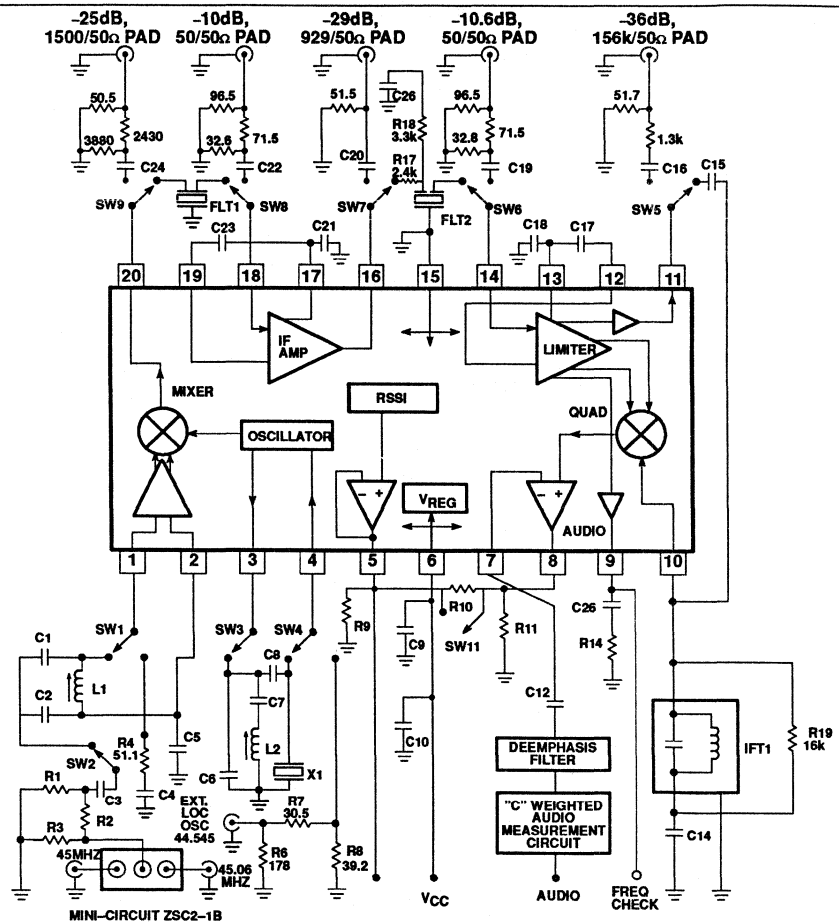
The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

The demodulated output of the quadrature drives an internal op amp. This op amp can be configured as a unity gain buffer.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone. This signal is buffered through an internal unity gain op amp. The frequency check pin provides a buffered limiter output. This is useful for implementing an AFC (Automatic Frequency Check) function. This same output can also be used in conjunction with limiter output (Pin 11) for demodulating FSK (Frequency Shift Keying) data. Both pins are of the same amplitude, but 180° out of phase.

NOTE: Limiter or Frequency Check output has drive capability of a 5kΩ minimum or higher in order to obtain 120mV_{RMS} output level.

NOTE: dB(v) = 20log V_{OUT}/V_{IN}

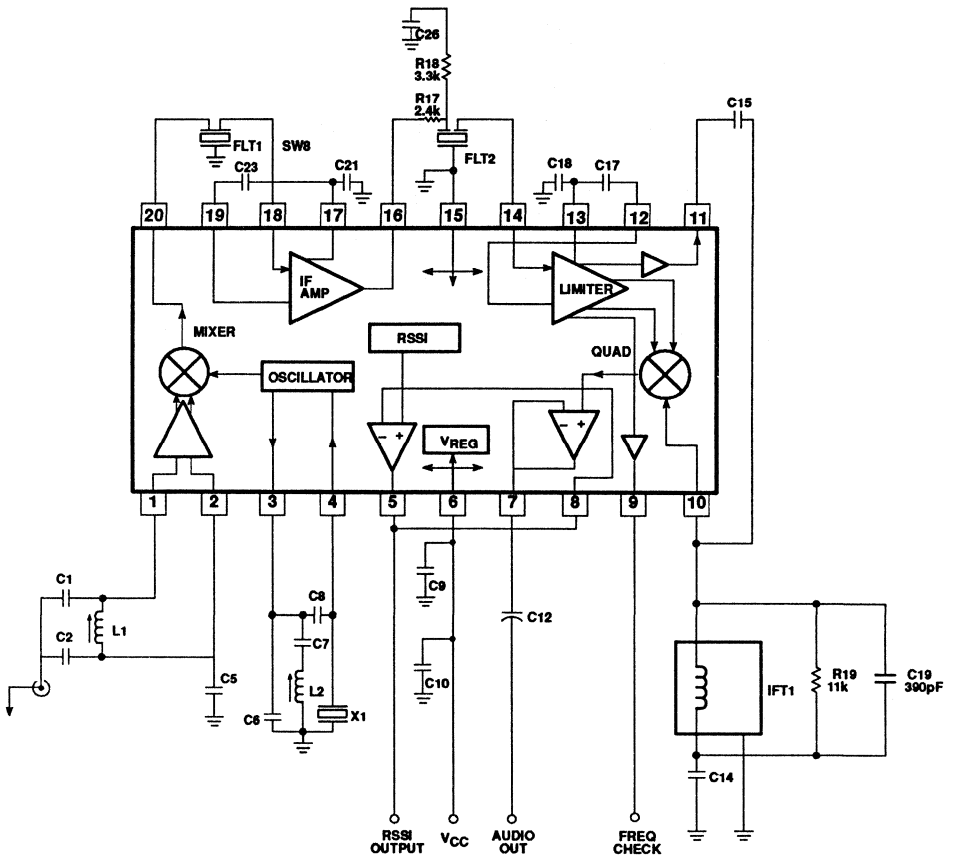


Automatic Test Circuit Component List

C1	100pF NPO Ceramic
C2	390pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	10μF Tantalum (minimum) *
C12	2.2μF
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
C26	0.1μF ±10% Monolithic Ceramic
C27	2.2μF
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	455kHz (Ce = 180pF) Toko RMC-2A6597H
L1	147-160nH Coilcraft UNI-10/142-04J08S
L2	0.8μH nominal Toko 292CNS-T1038Z
X1	44.545MHz Crystal ICM4712701
R9	2kΩ ±1% 1/4W Metal Film
R10	10kΩ ±1%
R11	10kΩ ±1%
R14	5kΩ ±1%
R17	2.4kΩ ±5% 1/4W Carbon Composition
R18	3.3kΩ ±5% 1/4W Carbon Composition
R19	16kΩ ±5% 1/4W Carbon Composition

*NOTE: This value can be reduced when a battery is the power source.

Figure 1. SA607 45MHz Test Circuit (Relays as shown)



Product Board SA608D/DK Component List

C1	51pF NPO Ceramic
C2	220pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	5-30pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	10μF Tantalum (minimum) *
C12	2.2μF
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C19	390pF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
C26	0.1μF ±10% Monolithic Ceramic
C27	2.2μF
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	330μH TOKO 303LN–1130
L1	0.33μH TOKO SCB–1320Z
L2	1.2μH Coilcraft 1008CS–122
X1	44.545MHz Crystal Hy-Q
R9	2kΩ ±1% 1/4W Metal Film
R10	8.2kΩ ±1%
R11	10kΩ ±1%
R14	10kΩ ±1%
R17	2.4kΩ ±5% 1/4W Carbon Composition
R18	3.3kΩ ±5% 1/4W Carbon Composition
R19	16kΩ ±5% 1/4W Carbon Composition

*NOTE: This value can be reduced when a battery is the power source.

Figure 2. SA608 45MHz Test Circuit (Relays as shown)

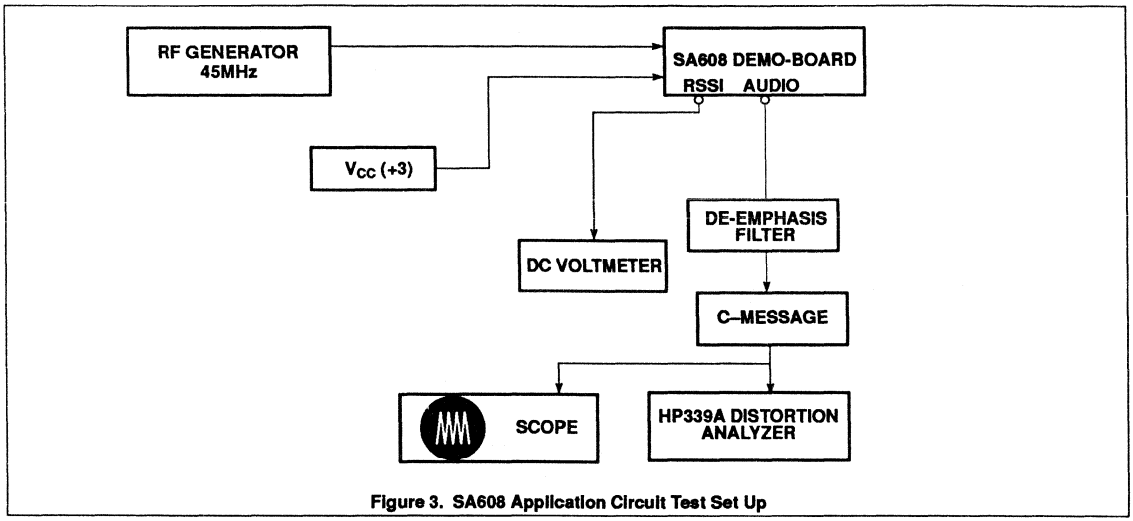


Figure 3. SA608 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message and de-emphasis filter combination has a peak gain of 10 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer. The de-emphasis filter has a fixed -6dB/Octave slope between 300Hz and 3kHz.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.35μV or –116dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 500mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10-15μF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1μF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2-3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 22kΩ, but should not be below 10kΩ.

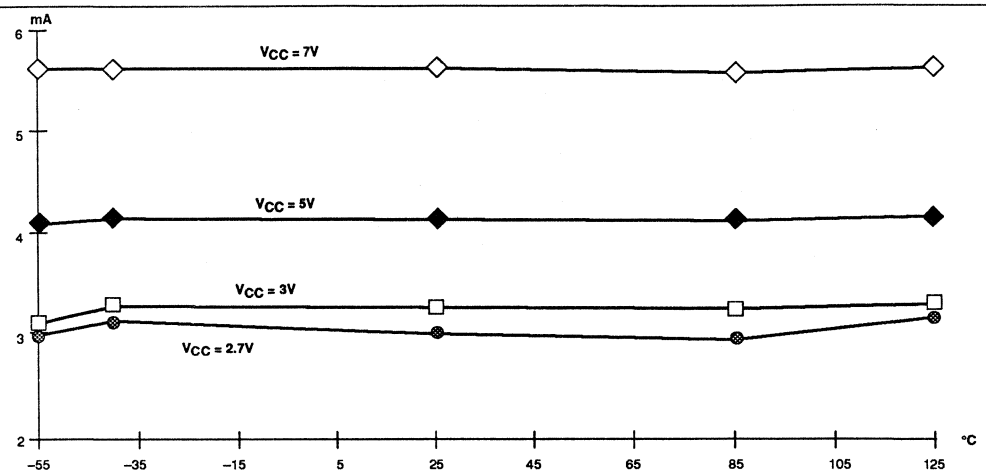


Figure 4. I_{CC} vs Temperature

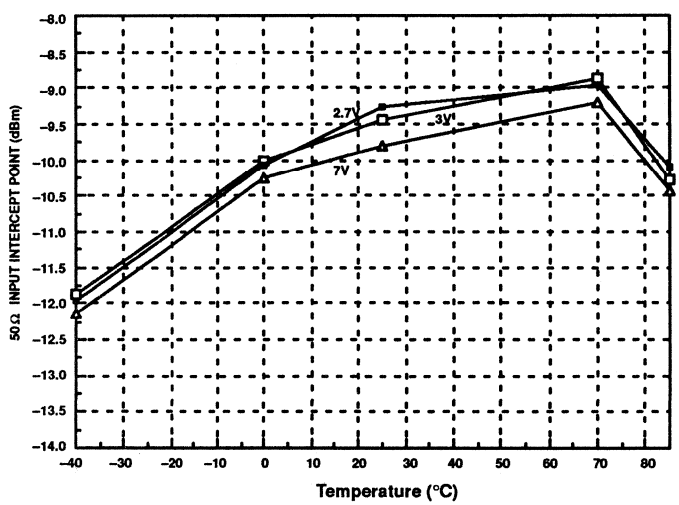


Figure 5. Third Order Intercept Point vs Supply Voltage

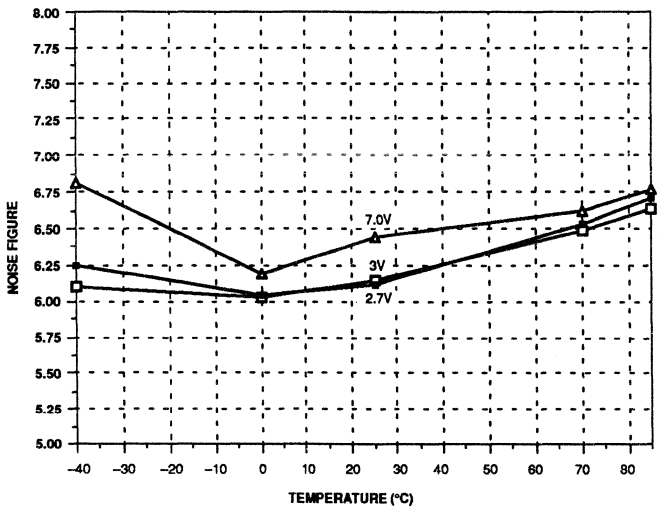


Figure 6. Mixer Noise Figure vs Supply Voltage

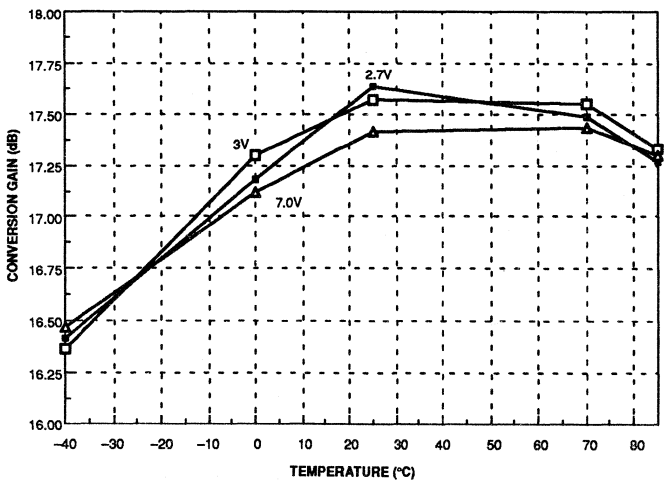


Figure 7. Conversion Gain vs Supply Voltage

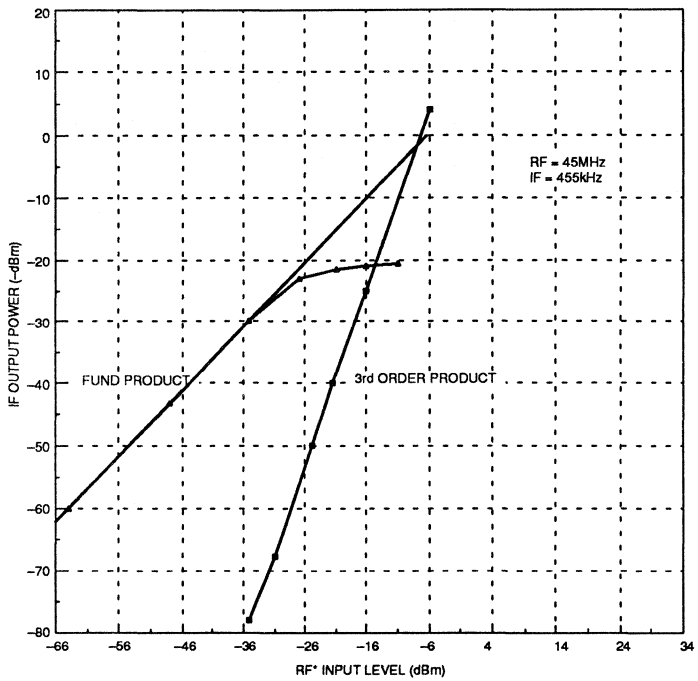


Figure 8. Mixer Third Order Intercept and Compression

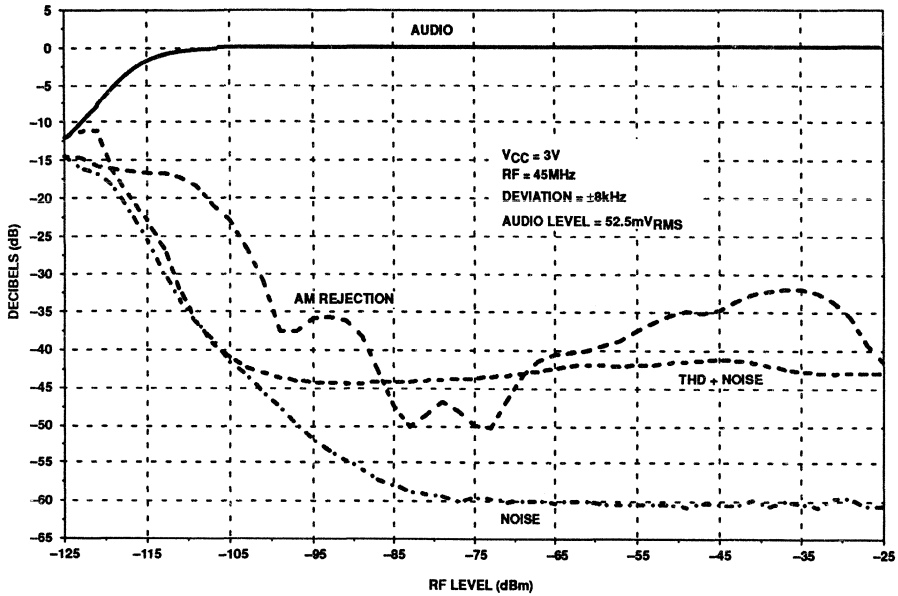


Figure 9. Sensitivity vs RF Level (–40°C)

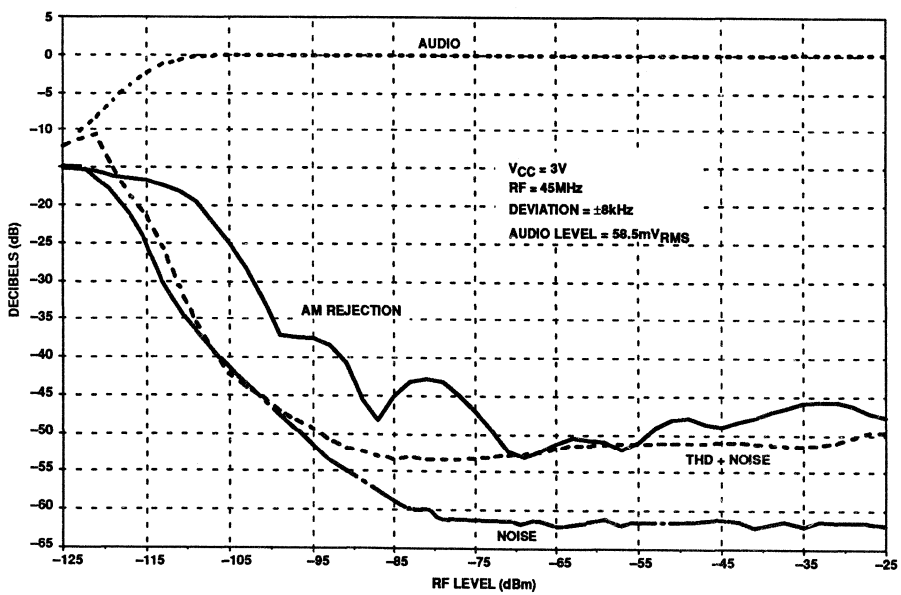


Figure 10. Sensitivity vs RF Level (+25°C)

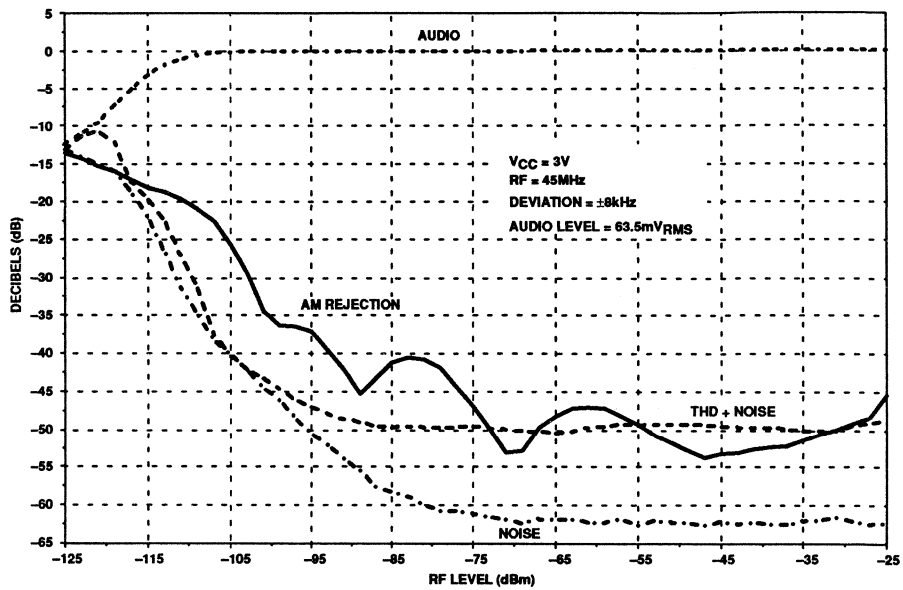


Figure 11. Sensitivity vs RF Level (Temperature 85°C)

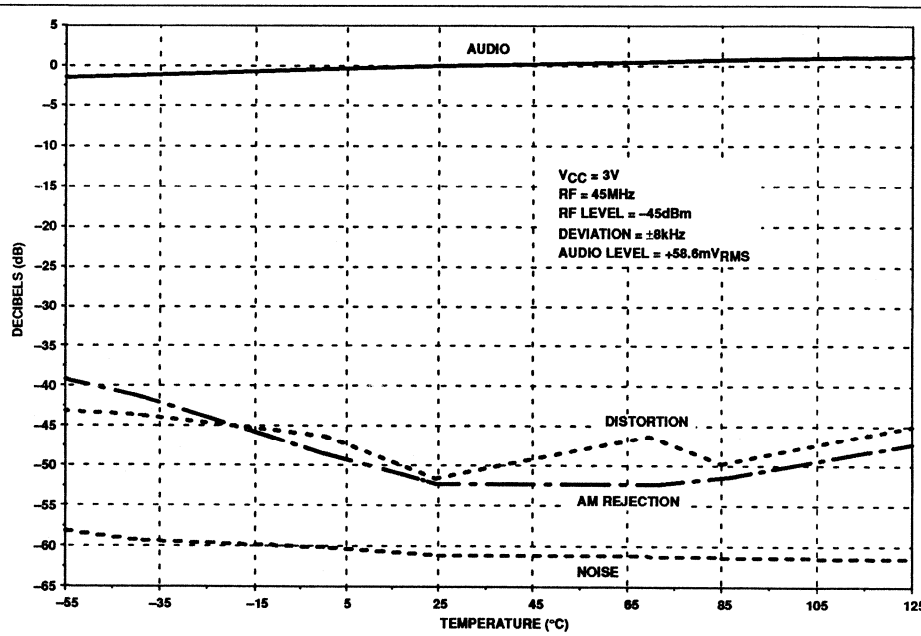


Figure 12. Relative Audio Level, Distortion, AM Rejection and Noise vs Temperature

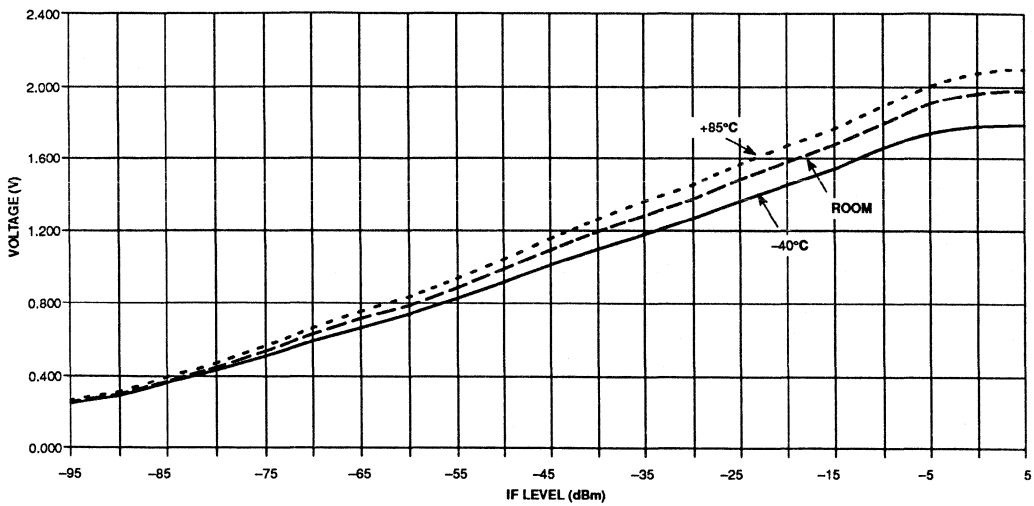


Figure 13. RSSI (455kHz IF @ 3V)

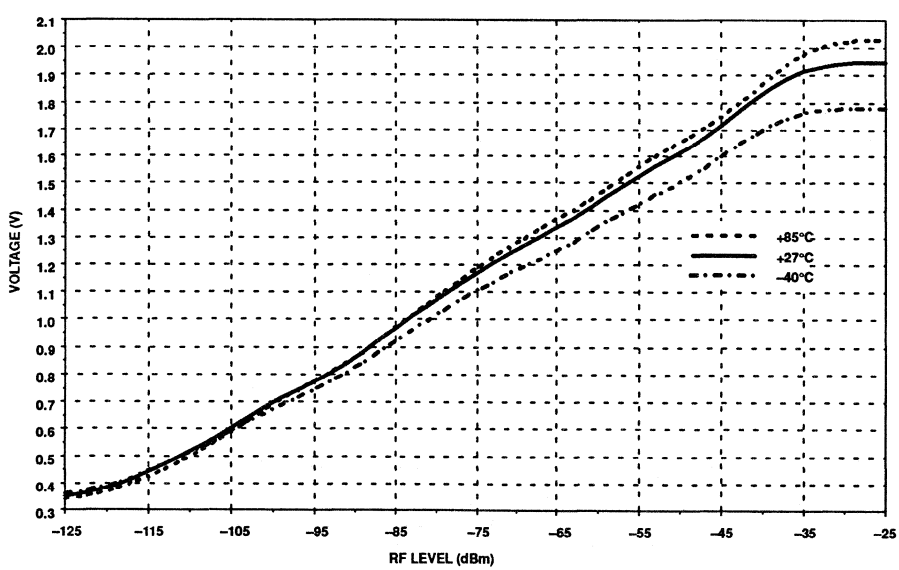


Figure 14. RSSI vs RF Level and Temperature - V_{CC} = 3V

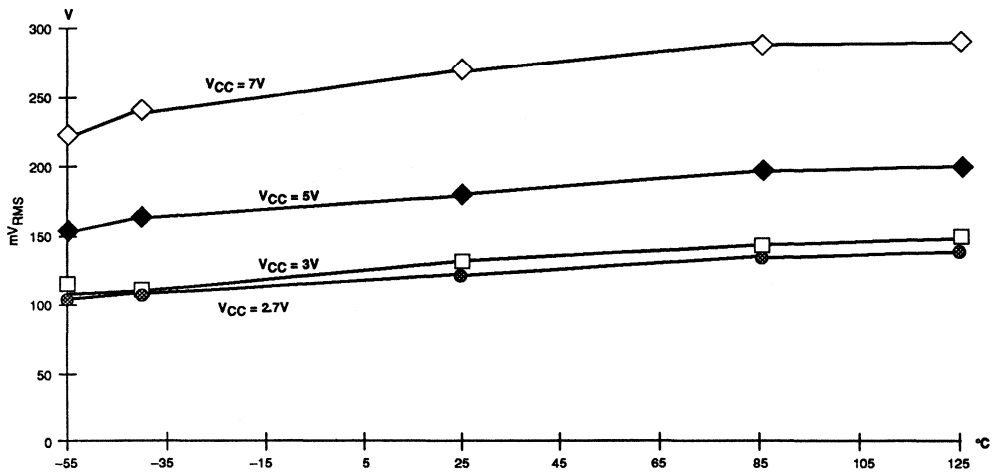


Figure 15. Audio Output vs Temperature

Low-voltage high performance mixer FM IF system — SA617

DESCRIPTION

The SA617 is a low voltage high performance monolithic FM IF system incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), voltage regulator and audio and RSSI op amps. The SA617 is available in 20-lead dual-in-line plastic, 20-lead SOL (surface-mounted miniature package) and 20-lead SSOP package.

The SA617 was designed for portable communication applications and will function down to 2.7V. The RF section is similar to the famous NE605. The audio output has an internal amplifier with the feedback pin accessible. The RSSI output is buffered. The SA617 also has an extra limiter output. This signal is buffered from the output of the limiter and can be used to perform frequency check. This is accomplished by comparing a reference frequency with the frequency check signal using a comparator to a varactor or PLL at the oscillator inputs.

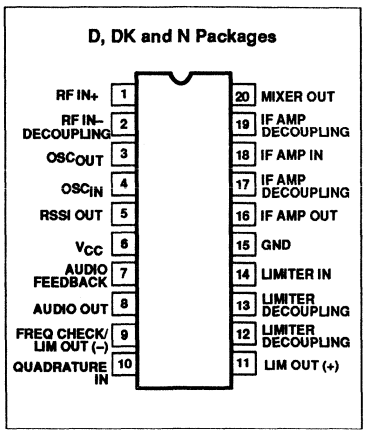
FEATURES

- Low power consumption: 3.5mA typical at 3V
- Mixer input to >150MHz
- Mixer conversion power gain of 17dB at 45MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator or external oscillator can be used at higher frequencies)
- 102dB of IF Amp/Limiter gain
- 2MHz IF amp/limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a 80dB dynamic range
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.31μV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone, 8kHz deviation with RF at 45MHz and IF at 455kHz
- SA617 meets cellular radio specifications
- Audio output internal op amp
- RSSI output internal op amp
- Buffered frequency check output
- Internal op amps with rail-to-rail outputs
- ESD protection: Human Body Model 2kV
  Robot Model 200V

APPLICATIONS

- Portable cellular radio FM IF
- Cordless phones
- Narrow band cellular applications (NAMPS/NTACS)
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Portable high performance communication receivers
- Single conversion VHF receivers
- Wireless systems

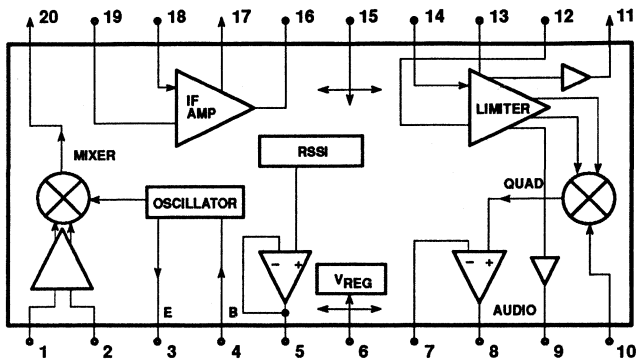
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic DIP	-40 to +85°C	SA617N	0408B
20-Pin Plastic SOL (Surface-mount)	-40 to +85°C	SA617D	0172D
20-Pin Plastic SSOP (Surface-mount)	-40 to +85°C	SA617DK	1563

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Single supply voltage	7	V
T_{STG}	Storage temperature range	–65 to +150	°C
T_A	Operating ambient temperature range SA617	–40 to +85	°C
θ_{JA}	Thermal impedance D package DK package N package	90 117 75	°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS SA617			UNITS
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		2.7		7.0	V
I_{CC}	DC current drain			3.5	5.0	mA

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +3V, unless otherwise stated. RF frequency = 45MHz + 14.5dBV RF input step-up; IF frequency = 455kHz; R17 = 2.4k; R18 = 3.3k; RF level = –45dBm; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with de-emphasis filter and C-message weighted filter. Test circuit NO TAG. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS SA617 MIN	LIMITS SA617 TYP	LIMITS SA617 MAX	UNITS
Mixer/Osc section (ext LO = 220mV$_{RMS}$)						
f_{IN}	Input signal frequency			150		MHz
f_{OSC}	Crystal oscillator frequency			150		MHz
	Noise figure at 45MHz			6.8		dB
	Third–order input intercept point (50Ω source)	f1 = 45.0; f2 = 45.06MHz Input RF Level = –52dBm		–9		dBm
	Conversion power gain	Matched 14.5dBV step–up	11.0	17		dB
		50Ω source		+2.5		dB
	RF input resistance	Single–ended input		8		kΩ
	RF input capacitance			3.0	4.0	pF
	Mixer output resistance	(Pin 20)	1.25	1.5		kΩ
IF section						
	IF amp gain	50Ω source		44		dB
	Limiter gain	50Ω source		58		dB
	Input limiting –3dB, R_{17} = 2.4k	Test at Pin 18		–105		dBm
	AM rejection	80% AM 1kHz		40		dB
	Audio level	Gain of two (2kΩ AC load)	60	114		mV
	SINAD sensitivity	RF level –110dB		13		dB
THD	Total harmonic distortion		–30	–45		dB
S/N	Signal–to–noise ratio	No modulation for noise		62		dB
	IF RSSI output, R_9 = 2kΩ[1]	IF level = –118dBm		0.3	0.8	V
		IF level = –68dBm	.70	1.1	2.0	V
		IF level = –23dBm	1.0	1.8	2.5	V
	RSSI range			80		dB
	RSSI accuracy			±2.0		dB
	IF input impedance		1.3	1.5		kΩ
	IF output impedance			0.3		kΩ
	Limiter input impedance		1.30	1.5		kΩ
	Limiter output impedance	(Pin 11)		200		Ω
	Limiter output level	(Pin 11) No load 2.4kΩ load		130 115		mV$_{RMS}$
	Frequency Check/limiter output impedance	(Pin 9)		200		Ω
	Frequency Check/limiter output level	(Pin 9) No load 2.4kΩ load		130 115		mV$_{RMS}$
RF/IF section (Int LO)						
	Audio level	3V = V_{CC}, RF level = –27dBm		240		mV$_{RMS}$
	System RSSI output	3V = V_{CC}, RF level = –27dBm		2.2		V
	System SINAD sensitivity	RF level = –117dBm		12		dB

NOTE:

1. The generator source impedance is 50Ω, but the SA617 input impedance at Pin 18 is 1500Ω. As a result, IF level refers to the actual signal that enters the SA617 input (Pin 18) which is about 21dB less than the "available power" at the generator.

CIRCUIT DESCRIPTION

The SA617 is an IF signal processing system suitable for second IF systems with input frequency as high as 150MHz. The bandwidth of the IF amplifier and limiter is at least 2MHz with 90dB of gain. The gain/bandwidth distribution is optimized for 455kHz, 1.5kΩ source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 6.2dB, conversion gain of 17dB, and input third-order intercept of –9dBm. The oscillator will operate in excess of 200MHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

The output impedance of the mixer is a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The input resistance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. The IF amplifier has 43dB of gain and 5.5MHz bandwidth. The IF limiter has 60dB of gain and 4.5MHz bandwidth. To achieve optimum linearity of the log signal strength indicator, there must be a 12dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 12dB(v) insertion loss, a fixed or variable resistor or an L pad for simultaneous loss and impedance matching can be added between the first IF output (Pin 16) and the interstage network. The overall gain will then be 90dB with 2MHz bandwidth.

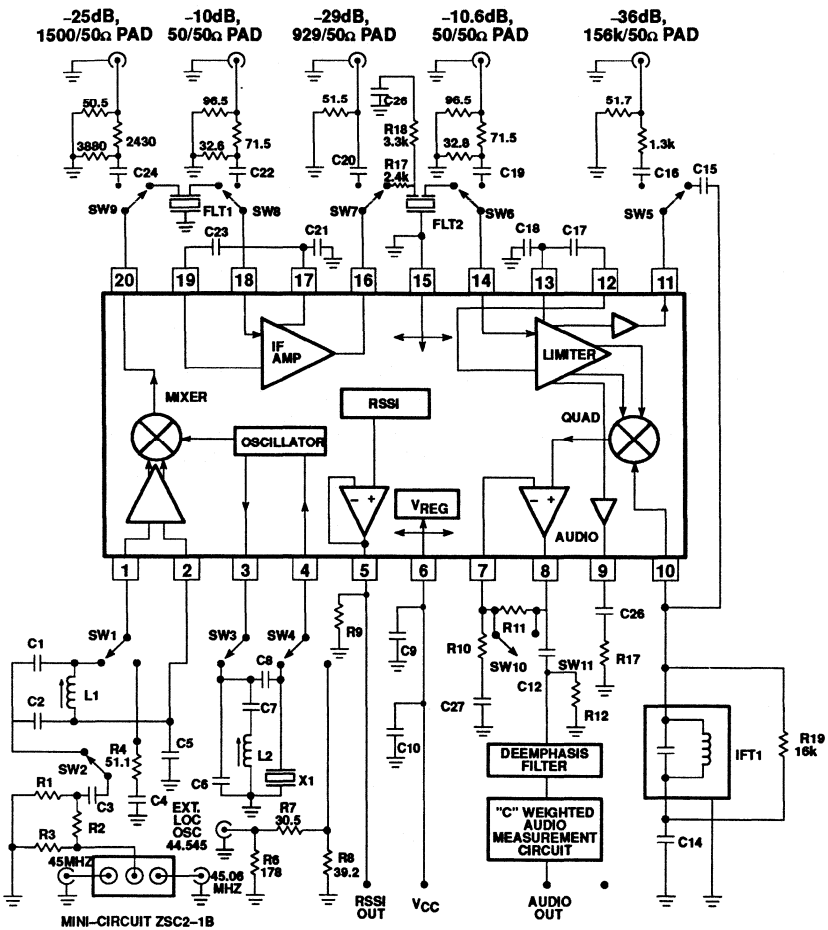
The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

The demodulated output of the quadrature drives an internal op amp. This op amp can be configured as a unity gain buffer, or for simultaneous gain, filtering, and 2nd-order temperature compensation if needed. It can drive an AC load as low as 2kΩ with a rail-to-rail output.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone. This signal is buffered through an internal unity gain op amp. The frequency check pin provides a buffered limiter output. This is useful for implementing an AFC (Automatic Frequency Check) function. This same output can also be used in conjunction with limiter output (Pin 11) for demodulating FSK (Frequency Shift Keying) data. Both pins are of the same amplitude, but 180° out of phase.

NOTE: Limiter output or Frequency Check output has drive capability of a load minimum of 2kΩ or higher to obtain 115mV output level.

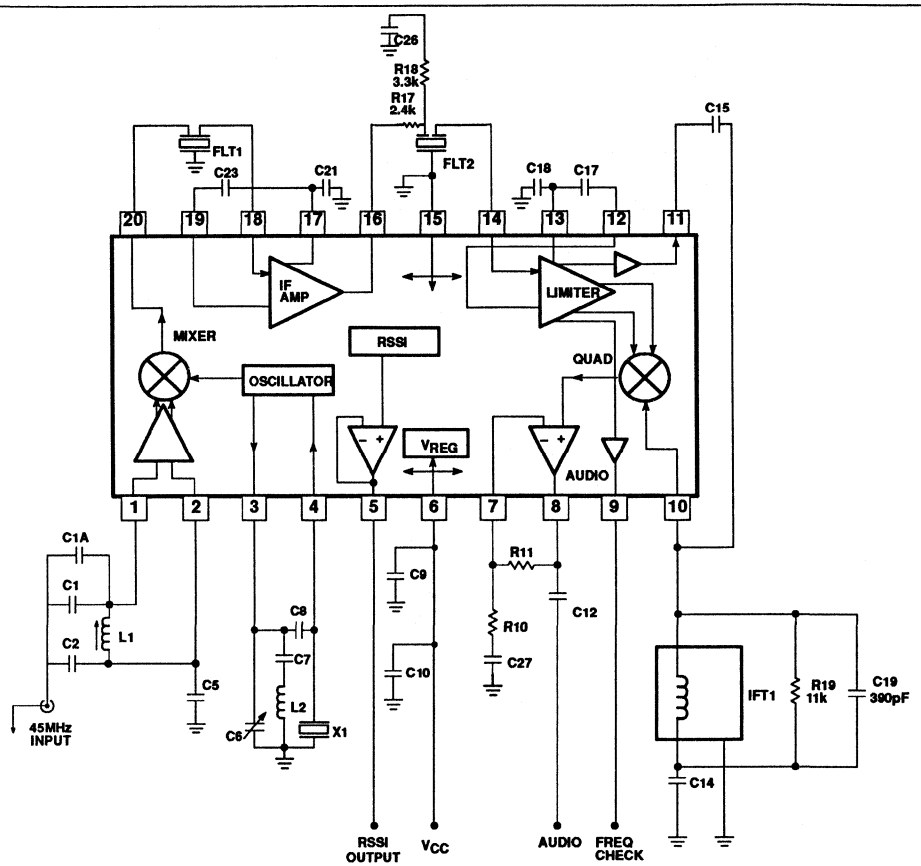
NOTE: $dB(v) = 20\log V_{OUT}/V_{IN}$



Automatic Test Circuit Component List

C1	100pF NPO Ceramic
C2	390pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	22pF NPO Ceramic
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	15μF Tantalum (minimum)
C12	2.2μF
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C25	100nF ±10% Monolithic Ceramic
C26	0.1μF ±10% Monolithic Ceramic
C27	2.2μF
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	455kHz (Ce = 180pF) Toko RMC-2A6597H
L1	147-160nH Coilcraft UNI-10/142-04J08S
L2	3.3μH nominal Toko 292CNS-T1046Z
X1	44.545MHz Crystal ICM4712701
R9	2kΩ ±1% 1/4W Metal Film
R10	8.2kΩ ±1%
R11	10kΩ ±1%
R12	2kΩ ±1%
R14	10kΩ ±1%
R17	2.4kΩ ±5% 1/4W Carbon Composition
R18	3.3kΩ ±5% 1/4W Carbon Composition
R19	16kΩ ±5% 1/4W Carbon Composition

Figure 1. SA617 45MHz Test Circuit (Relays as shown)



SA617DK
Application Component List

C1A	18pF NPO Ceramic
C1	33pF NPO Ceramic
C2	220pF NPO Ceramic
C5	100nF ±10% Monolithic Ceramic
C6	30pF trim cap
C7	1nF Ceramic
C8	10.0pF NPO Ceramic
C9	100nF ±10% Monolithic Ceramic
C10	15µF Tantalum (minimum)
C12	2.2µF ±10% Tantalum
C14	100nF ±10% Monolithic Ceramic
C15	10pF NPO Ceramic
C17	100nF ±10% Monolithic Ceramic
C18	100nF ±10% Monolithic Ceramic
C19	390pF ±10% Monolithic Ceramic
C21	100nF ±10% Monolithic Ceramic
C23	100nF ±10% Monolithic Ceramic
C26	100nF ±10% Monolithic Ceramic
C27	2.2µF Tantalum
Flt 1	Ceramic Filter Murata SFG455A3 or equiv
Flt 2	Ceramic Filter Murata SFG455A3 or equiv
IFT 1	330µH TOKO 303LN-1130
L1	.33µH TOKO SCB-1320Z
L2	1.2µH
X1	44.545MHz Crystal ICM4712701
R5	Not Used in Application Board (see Note 8, pg 8)
R10	8.2k ±5% 1/4W Carbon Composition
R11	10k ±5% 1/4W Carbon Composition
R17	2.4k ±5% 1/4W Carbon Composition
R18	3.3k ±5% 1/4W Carbon Composition
R19	11k ±5% 1/4W Carbon Composition

Figure 2. SA617 45MHz Application Circuit

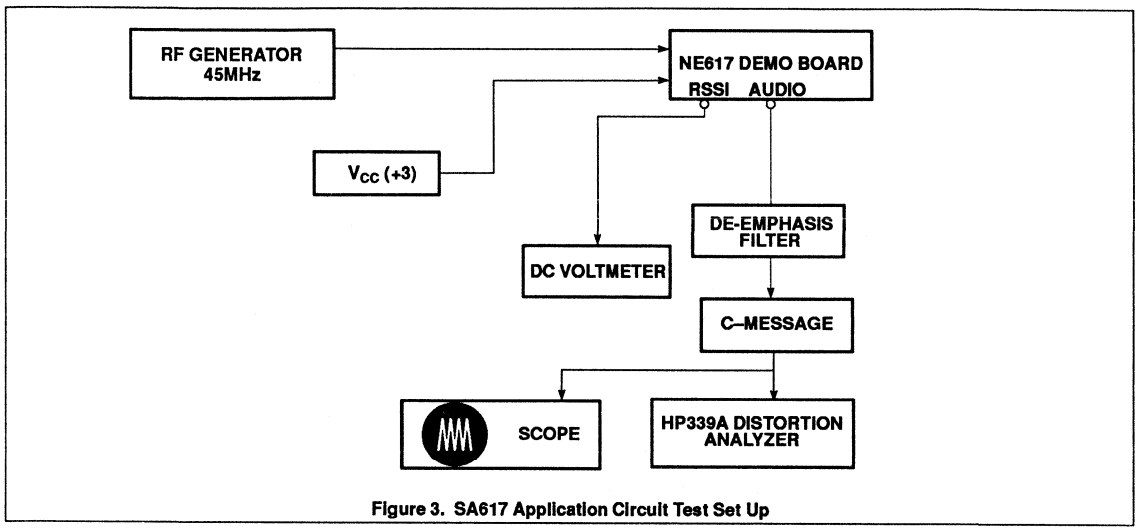


Figure 3. SA617 Application Circuit Test Set Up

NOTES:

1. C-message: The C-message and de-emphasis filter combination has a peak gain of 10 for accurate measurements. Without the gain, the measurements may be affected by the noise of the scope and HP339 analyzer. The de-emphasis filter has a fixed -6dB/Octave slope between 300Hz and 3kHz.
2. Ceramic filters: The ceramic filters can be 30kHz SFG455A3s made by Murata which have 30kHz IF bandwidth (they come in blue), or 16kHz CFU455Ds, also made by Murata (they come in black). All of our specifications and testing are done with the more wideband filter.
3. RF generator: Set your RF generator at 45.000MHz, use a 1kHz modulation frequency and a 6kHz deviation if you use 16kHz filters, or 8kHz if you use 30kHz filters.
4. Sensitivity: The measured typical sensitivity for 12dB SINAD should be 0.35μV or –116dBm at the RF input.
5. Layout: The layout is very critical in the performance of the receiver. We highly recommend our demo board layout.
6. RSSI: The smallest RSSI voltage (i.e., when no RF input is present and the input is terminated) is a measure of the quality of the layout and design. If the lowest RSSI voltage is 500mV or higher, it means the receiver is in regenerative mode. In that case, the receiver sensitivity will be worse than expected.
7. Supply bypass and shielding: All of the inductors, the quad tank, and their shield must be grounded. A 10-15μF or higher value tantalum capacitor on the supply line is essential. A low frequency ESR screening test on this capacitor will ensure consistent good sensitivity in production. A 0.1μF bypass capacitor on the supply pin, and grounded near the 44.545MHz oscillator improves sensitivity by 2-3dB.
8. R5 can be used to bias the oscillator transistor at a higher current for operation above 45MHz. Recommended value is 22kΩ, but should not be below 10kΩ.

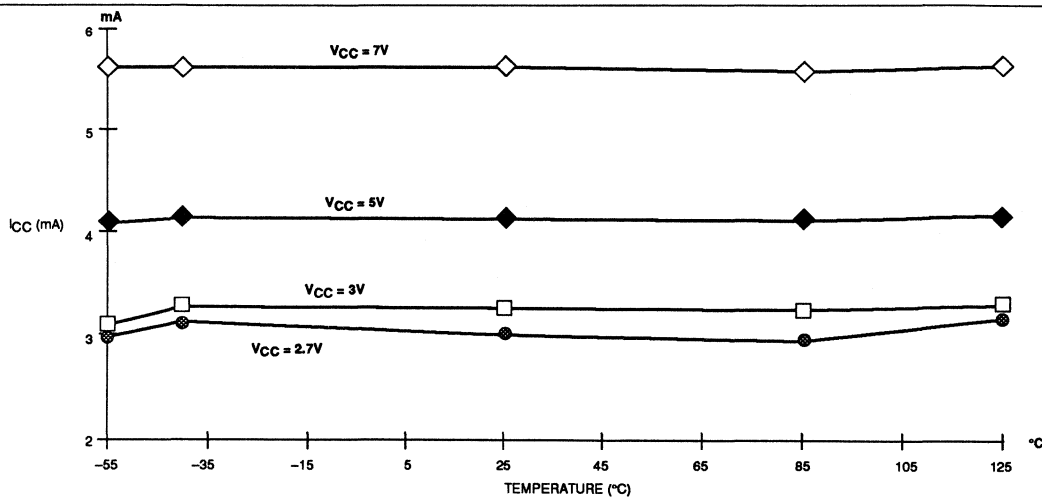


Figure 4. I_{CC} vs Temperature

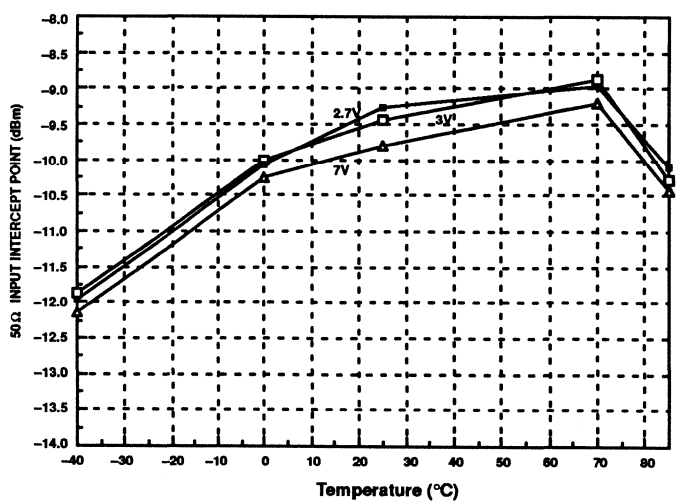


Figure 5. Third Order Intercept Point vs Supply Voltage

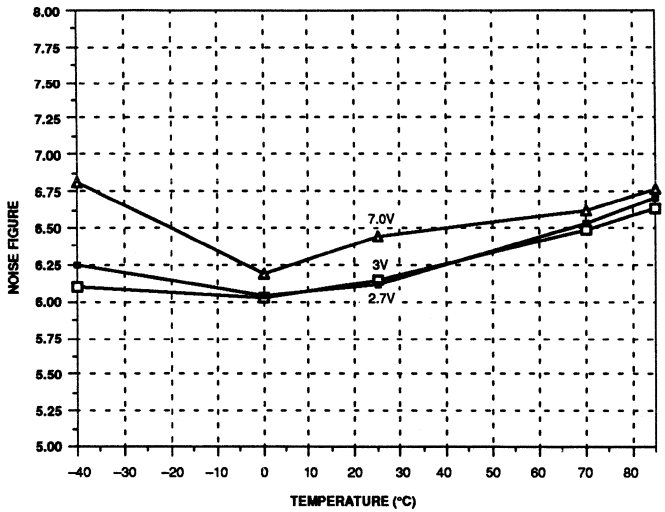


Figure 6. Mixer Noise Figure vs Supply Voltage

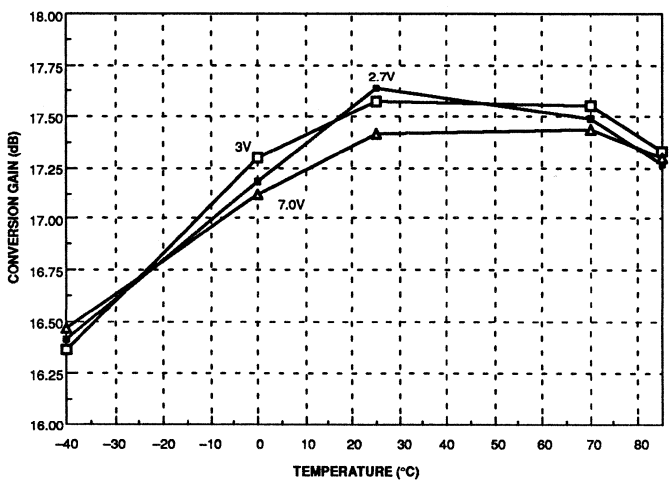


Figure 7. Conversion Gain vs Supply Voltage

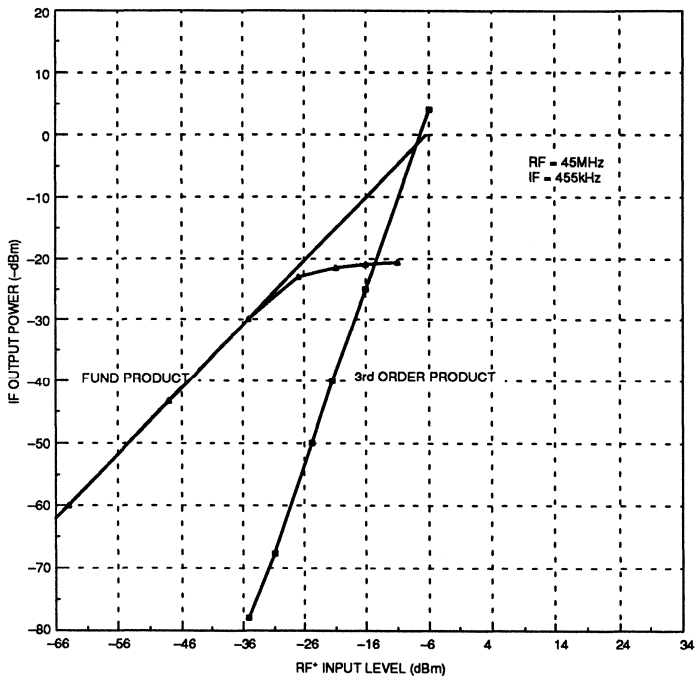


Figure 8. Mixer Third Order Intercept and Compression

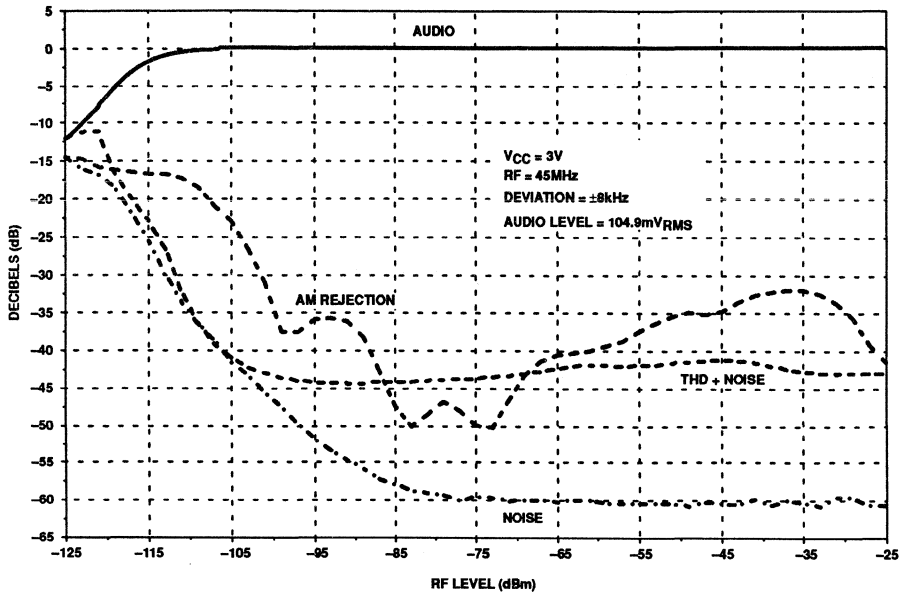


Figure 9. Sensitivity vs RF Level (–40°C)

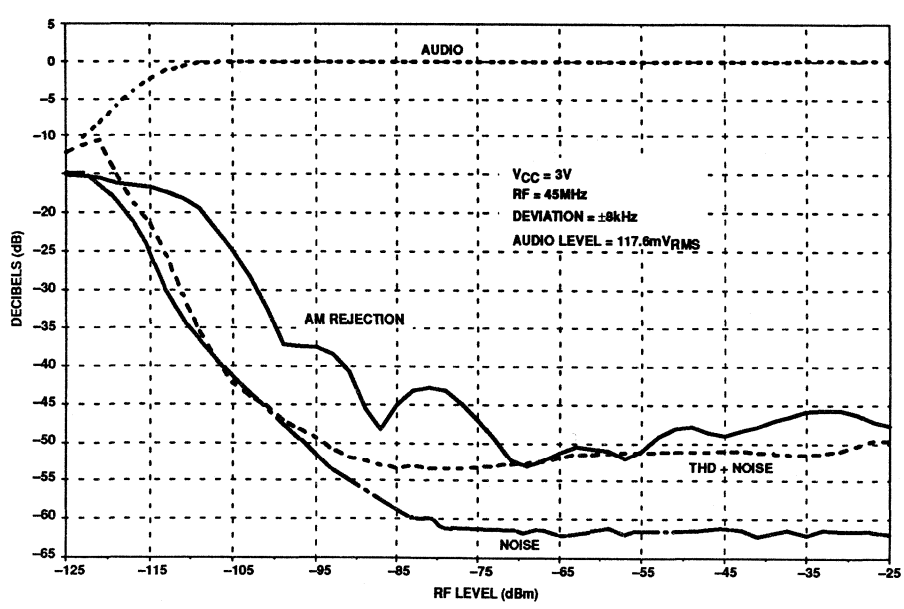


Figure 10. Sensitivity vs RF Level (+25°C)

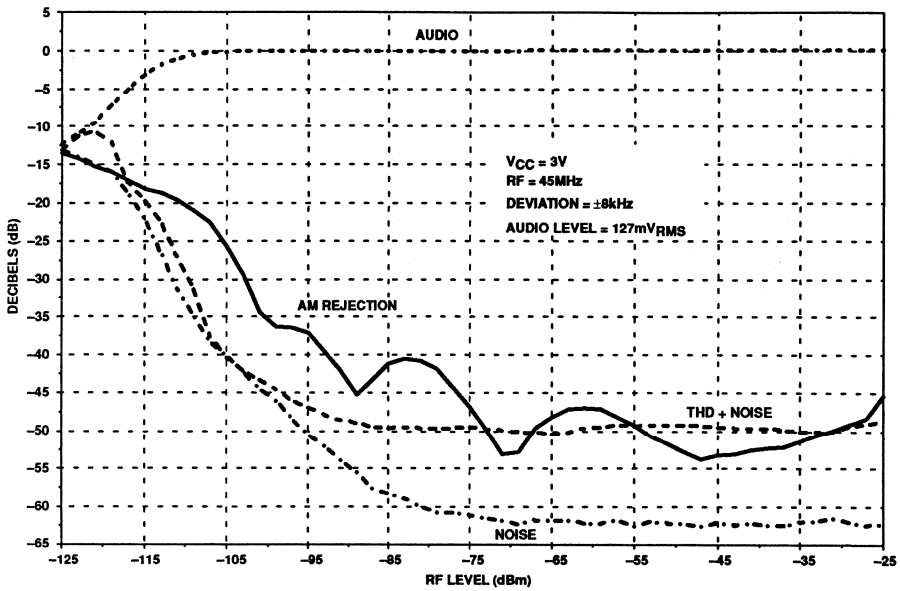


Figure 11. Sensitivity vs RF Level (Temperature 85°C)

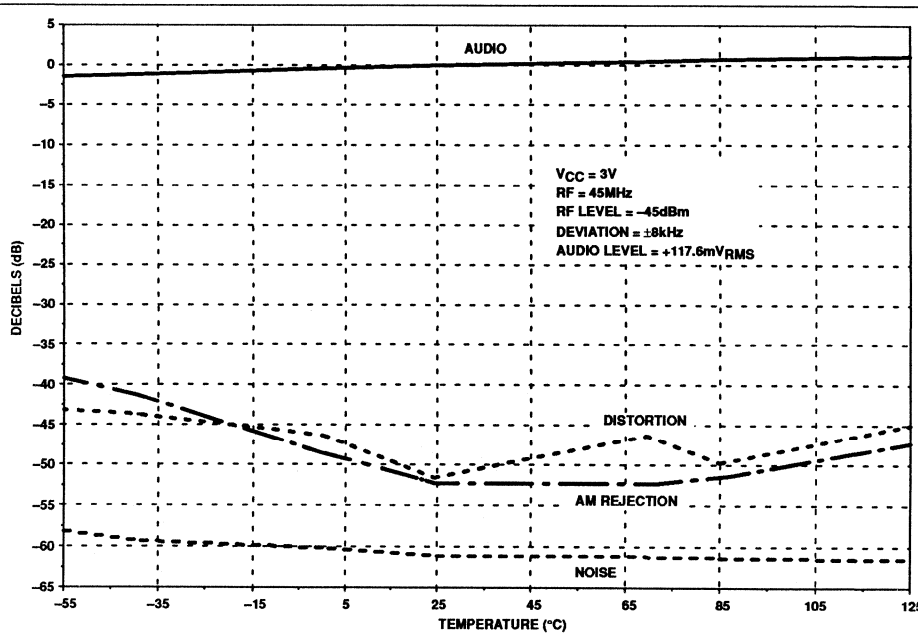


Figure 12. Relative Audio Level, Distortion, AM Rejection and Noise vs Temperature

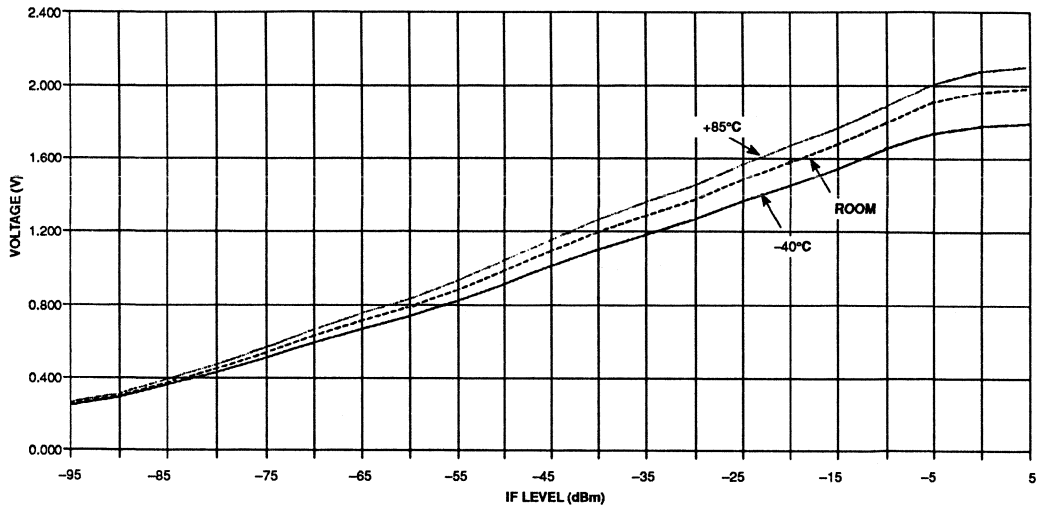


Figure 13. RSSI (455kHz IF @ 3V)

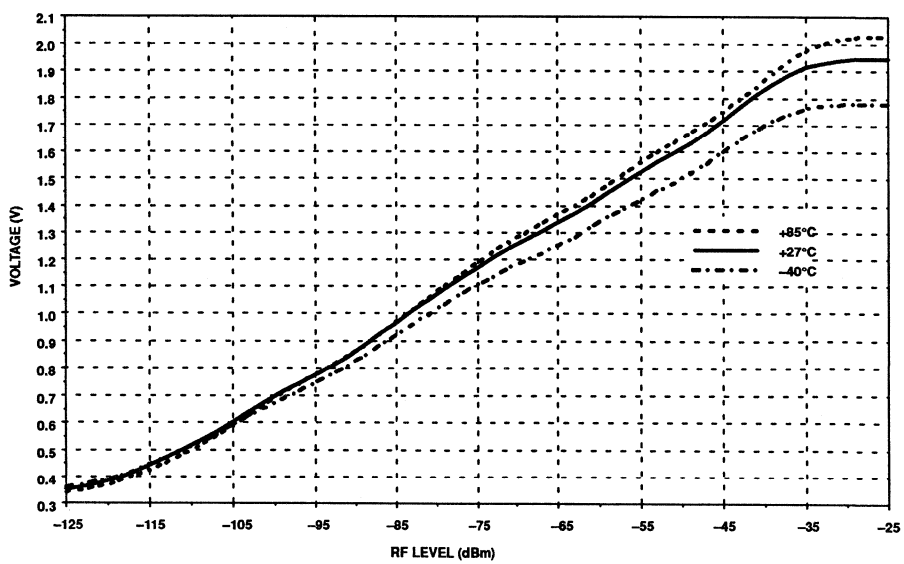


Figure 14. RSSI vs RF Level and Temperature - V_{CC} = 3V

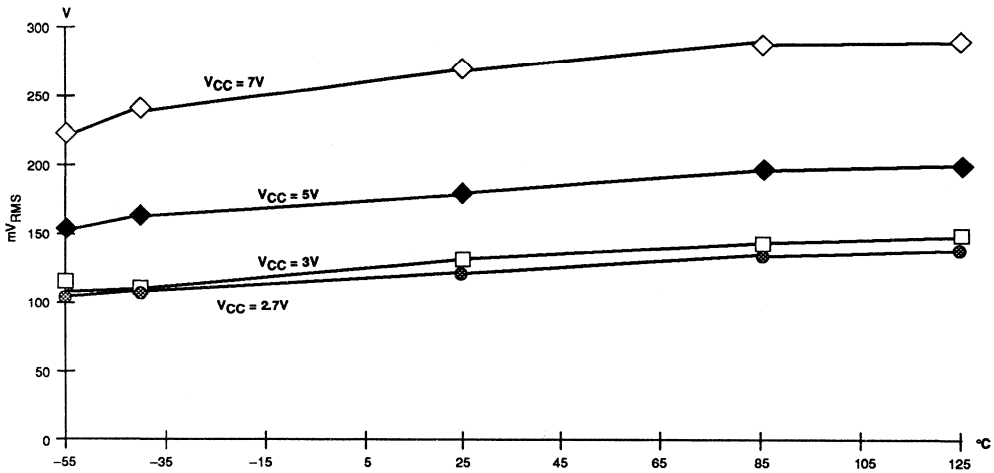


Figure 15. Audio Output vs Temperature

Low voltage high performance mixer FM IF system with high-speed RSSI

SA626

DESCRIPTION

The SA626 is a low-voltage high performance monolithic FM IF system with high-speed RSSI incorporating a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, logarithmic received signal strength indicator (RSSI), voltage regulator and audio and fast RSSI op amps. The SA626 is available in 20-lead SOL (surface-mounted small outline large package) and 20-lead SSOP (shrink samll outline package).

The SA626 was designed for high bandwidth portable communication applications and will function down to 2.7V. The RF section is similar to the famous NE605. The audio and RSSI outputs have amplifiers. The RSSI output has access to the feedback pin. This enables the designer to level adjust the outputs or add filtering.

SA626 incorporates a power down mode which powers down the device when Pin 8 is low. Power down logic level are CMOS and TTL compatible with high input impedance.

APPLICATIONS

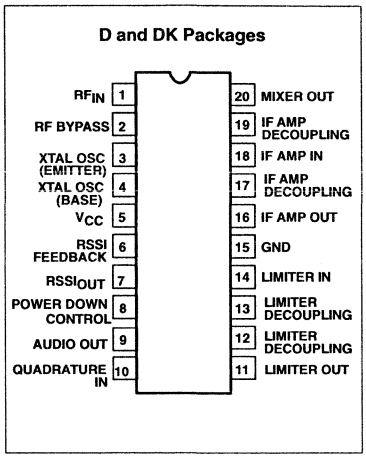
- Digital cordless telephones
- Digital cellular telephones
- Digital cellular base stations
- Portable high performance communications receivers
- Single conversion VHF/UHF receivers
- SCA receivers
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers
- Log amps
- Wideband low current amplification

FEATURES

- Fast RSSI rise and fall times
- Low power consumption: 6.5mA typ at 3V
- Mixer input to >500MHz
- Mixer conversion power gain of 13dB at 240MHz
- Mixer noise figure of 11dB at 240MHz
- XTAL oscillator effective to 150MHz (L.C. oscillator to 1GHz local oscillator can be injected)
- 102dB of IF Amp/Limiter gain
- 25MHz limiter small signal bandwidth
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- Audio output internal op amp
- RSSI output internal op amp
- Internal op amps with rail-to-rail outputs
- Low external component count; suitable for crystal/ceramic/LC filters
- Excellent sensitivity: 0.54μV into 50Ω matching network for 12dB SINAD (Signal to Noise and Distortion ratio) for 1kHz tone with RF at 240MHz and IF at 10.7MHz
- SA626 meets cellular radio specifications
- ESD hardened
- 10.7MHz filter matching (330Ω)
- Power down mode (I_{CC} = 200μA)

PIN CONFIGURATION

D and DK Packages



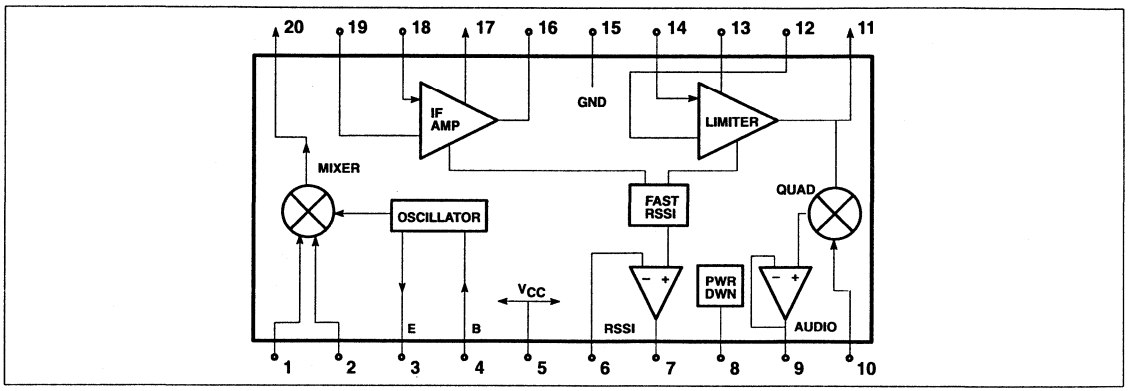
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic SOL (Surface-mount)	-40 to +85°C	SA626D
20-Pin Plastic SSOP (Surface-mount)	-40 to +85°C	SA626DK

Low voltage high performance mixer FM IF system with high-speed RSSI

SA626

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		RATING	UNITS
V_{CC}	Single supply voltage		0.3 to 7	V
V_{IN}	Voltage applied to any other pin		–0.3 to (V_{CC}+0.3)	V
T_{STG}	Storage temperature range		-65 to +150	°C
T_A	Operating ambient temperature range SA626		–40 to +85	°C
θ_{JA}	Thermal impedance	D package	90	°C/W
		DK package	117	°C/W

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA626			
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		2.7	3.0	5.5	V
I_{CC}	DC current drain	Pin 8 = HIGH		6.5		mA
I_{CC}	Standby	Pin 8 = LOW		200		µA
t_{ON}	Power up time	RSSI valid (10% to 90%)		10		µs
t_{OFF}	Power down time	RSSI invalid (90% to 10%)		5		µs

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +3V, unless otherwise stated. RF frequency = 240.05MHz + 14.5dBV RF input step-up; IF frequency = 10.7MHz; RF level = -45dBm; FM modulation = 1kHz with ±125kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 1. The parameters listed below are tested using automatic test equipment to assure consistent electrical characterristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA626			
			MIN	TYP	MAX	
Mixer/Osc section (ext LO = 160mV$_{RMS}$)						
f_{IN}	Input signal frequency			500		MHz
f_{OSC}	External oscillator (buffer)			500		MHz
	Noise figure at 240MHz			11		dB
	Third-order input intercept point	Matched f1=240.05; f2=240.35MHz		-18		dBm
	Conversion power gain	Matched 14.5dBV step-up		14		dB
	RF input resistance	Single-ended input		800		Ω
	RF input capacitance			3.5		pF
	Mixer output resistance	(Pin 20)		330		Ω
IF section						
	IF amp gain			44		dB
	Limiter gain			58		dB
	Input limiting -3dB	Test at Pin 18		–105		dBm
	AM rejection	80% AM 1kHz		34		dB
	Audio level	Unity gain		145		mV$_{RMS}$
	SINAD sensitivity	RF level = -111dBm		16		dB
THD	Total harmonic distortion			-42		dB
S/N	Signal-to-noise ratio	No modulation for noise		60		dB
	IF RSSI output with buffer	IF level = -118dBm		0.2		V
		IF level = -68dBm		1.1		V
		IF level = -18dBm		1.8		V
	IF RSSI output rise time	IF frequency = 10.7MHz				
	(10kHz pulse, no 10.7MHz filter)	RF level = -56dBm		1.2		µs
	(no RSSI bypass capacitor)	RF level = -28dBm		1.1		µs
	IF RSSI output fall time	IF frequency = 10.7MHz				
	(10kHz pulse, no 10.7MHz filter)	RF level = -56dBm		2.0		µs
	(no RSSI bypass capacitor)	RF level = -28dBm		7.3		µs
	RSSI range			90		dB
	RSSI accuracy			±1.5		dB
	IF input impedance			330		Ω
	IF output impedance			330		Ω
	Limiter intput impedance			330		Ω
	Limiter output impedance			300		Ω
	Limiter output level with no load			130		mV$_{RMS}$
RF/IF section (int LO)						
	Audio level	RF level = -27dBm		145		mV$_{RMS}$
	System RSSI output	RF level = -27dBm		2.0		V
	System SINAD	RF level = -110dBm		12		dB

Low voltage high performance mixer FM IF system with high-speed RSSI

SA626

CIRCUIT DESCRIPTION

The SA626 is an IF signal processing system suitable for second IF or single conversion systems with input frequency as high as 1GHz. The bandwidth of the IF amplifier is about 40MHz, with 44dB(v) of gain from a 50Ω source. The bandwidth of the limiter is about 28MHz with about 58dB(v) of gain from a 50Ω source. However, the gain/bandwidth distribution is optimized for 10.7MHz, 330Ω source applications. The overall system is well-suited to battery operation as well as high performance and high quality products of all types, such as cordless and cellular hand-held phones.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 11dB, conversion gain of 13dB, and input third-order intercept of -11dBm. The oscillator will operate in excess of 1GHz in L/C tank configurations. Hartley or Colpitts circuits can be used up to 100MHz for xtal configurations. Butler oscillators are recommended for xtal configurations up to 150MHz.

The output of the mixer is internally loaded with a 330Ω resistor permitting direct connection to a 10.7MHz ceramic filter. The input resistance of the limiting IF amplifiers is also 330Ω. With most 10.7MHz ceramic filters and many crystal filters, no impedance matching network is necessary. To achieve optimum linearity of the log signal strength indicator, there must be a 6dB(v) insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 6dB(v) insertion loss, a fixed or variable resistor can be added between the first IF output (Pin 16) and the interstage network.

The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

Overall, the IF section has a gain of 90dB. For operation at intermediate frequency at 10.7MHz. Special care must be given to layout, termination, and interstage loss to avoid instability.

The demodulated output of the quadrature drives an internal op amp. This op amp can be configured as a unity gain buffer, or for simultaneous gain, filtering, and 2nd-order temperature compensation if needed. It can drive an AC load as low as 5kΩ with a rail-to-rail output.

A log signal strength completes the circuitry. The output range is greater than 90dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone, and RCR;28 cordless telephone. This signal drives an internal op amp. The op amp is capable of rail-to-rail output. It can be used for gain, filtering, or 2nd-order temperature compensation of the RSSI, if needed.

NOTE: $dB(v) = 20\log V_{OUT}/V_{IN}$

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATA SHEET

6 W AUDIO POWER AMPLIFIER IN CAR APPLICATIONS
10 W AUDIO POWER AMPLIFIER IN MAINS-FED APPLICATIONS

The TDA1010A is a monolithic integrated class-B audio amplifier circuit in a 9-lead single in-line (SIL) plastic package. The device is primarily developed as a 6 W car radio amplifier for use with 4 Ω and 2 Ω load impedances. The wide supply voltage range and the flexibility of the IC make it an attractive proposition for record players and tape recorders with output powers up to 10 W.

Special features are:

- single in-line (SIL) construction for easy mounting
- separated preamplifier and power amplifier
- high output power
- low-cost external components
- good ripple rejection
- thermal protection

QUICK REFERENCE DATA

Supply voltage range	V_P		6 to 24 V
Repetitive peak output current	I_{ORM}	max.	3 A
Output power at pin 2; d_{tot} = 10%			
V_P = 14,4 V; R_L = 2 Ω	P_o	typ.	6,4 W
V_P = 14,4 V; R_L = 4 Ω	P_o	typ.	6,2 W
V_P = 14,4 V; R_L = 8 Ω	P_o	typ.	3,4 W
V_P = 14,4 V; R_L = 2 Ω; with additional bootstrap resistor of 220 Ω between pins 3 and 4	P_o	typ.	9 W
Total harmonic distortion at P_o = 1 W; R_L = 4 Ω	d_{tot}	typ.	0,2 %
Input impedance			
preamplifier (pin 8)	$\lvert Z_i \rvert$	typ.	30 kΩ
power amplifier (pin 6)	$\lvert Z_i \rvert$	typ.	20 kΩ
Total quiescent current at V_P = 14,4 V	I_{tot}	typ.	31 mA
Sensitivity for P_o = 5,8 W; R_L = 4 Ω	V_i	typ.	10 mV
Operating ambient temperature	T_{amb}		−25 to + 150 °C
Storage temperature	T_{stg}		−55 to + 150 °C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT110B).

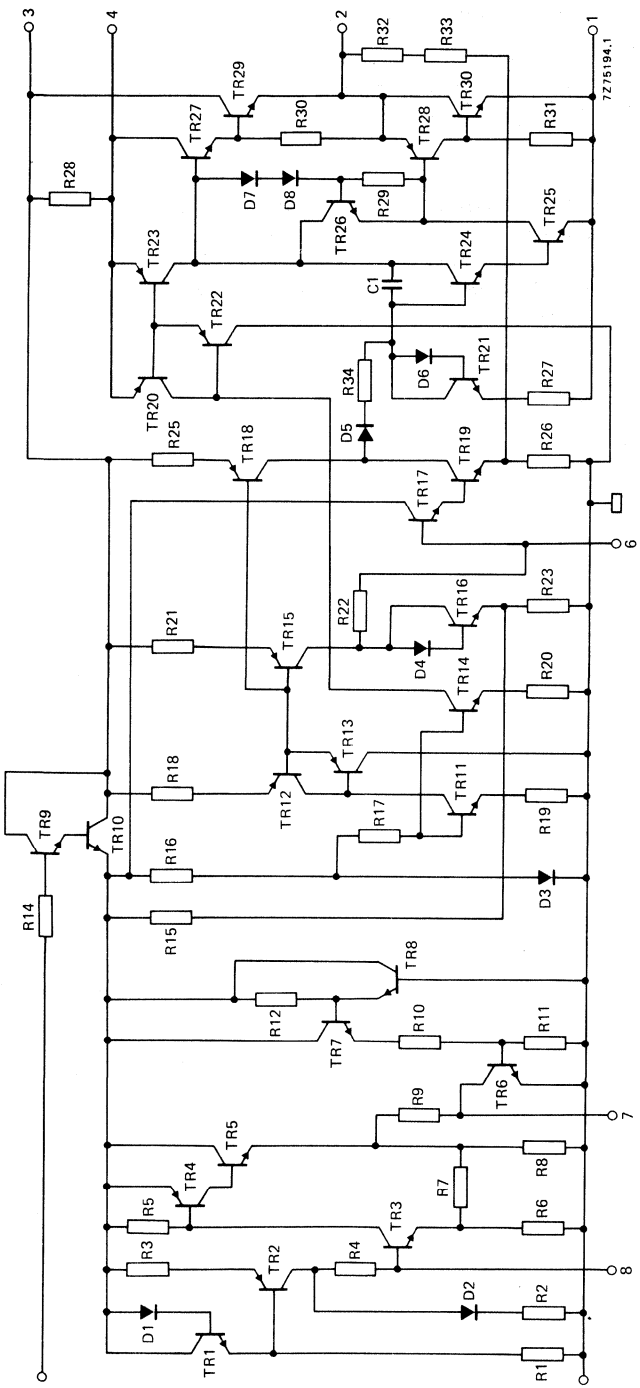


Fig. 1 Circuit diagram.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATA SHEET

2 TO 6 W AUDIO POWER AMPLIFIER

The TDA1011 is a monolithic integrated audio amplifier circuit in a 9-lead single in-line (SIL) plastic package. The device is especially designed for portable radio and recorder applications and delivers up to 4 W in a 4 Ω load impedance. The device can deliver up to 6 W into 4 Ω at 16 V loaded supply in mains-fed applications. The maximum permissible supply voltage of 24 V makes this circuit very suitable for d.c. and a.c. apparatus, while the very low applicable supply voltage of 3,6 V permits 6 V applications.
Special features are:

- single in-line (SIL) construction for easy mounting
- separated preamplifier and power amplifier
- high output power
- thermal protection
- high input impedance
- low current drain
- limited noise behaviour at radio frequencies

QUICK REFERENCE DATA

Supply voltage range	V_P		3,6 to 20 V
Peak output current	I_{OM}	max.	3 A
Output power at d_{tot} = 10%			
V_P = 16 V; R_L = 4 Ω	P_o	typ.	6,5 W
V_P = 12 V; R_L = 4 Ω	P_o	typ.	4,2 W
V_P = 9 V; R_L = 4 Ω	P_o	typ.	2,3 W
V_P = 6 V; R_L = 4 Ω	P_o	typ.	1,0 W
Total harmonic distortion at P_o = 1 W; R_L = 4 Ω	d_{tot}	typ.	0,2 %
Input impedance			
preamplifier (pin 8)	$\lvert Z_i \rvert$	>	100 kΩ
power amplifier (pin 6)	$\lvert Z_i \rvert$	typ.	20 kΩ
Total quiescent current	I_{tot}	typ.	14 mA
Operating ambient temperature	T_{amb}		−25 to + 150 °C
Storage temperature	T_{stg}		−55 to + 150 °C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT110B).

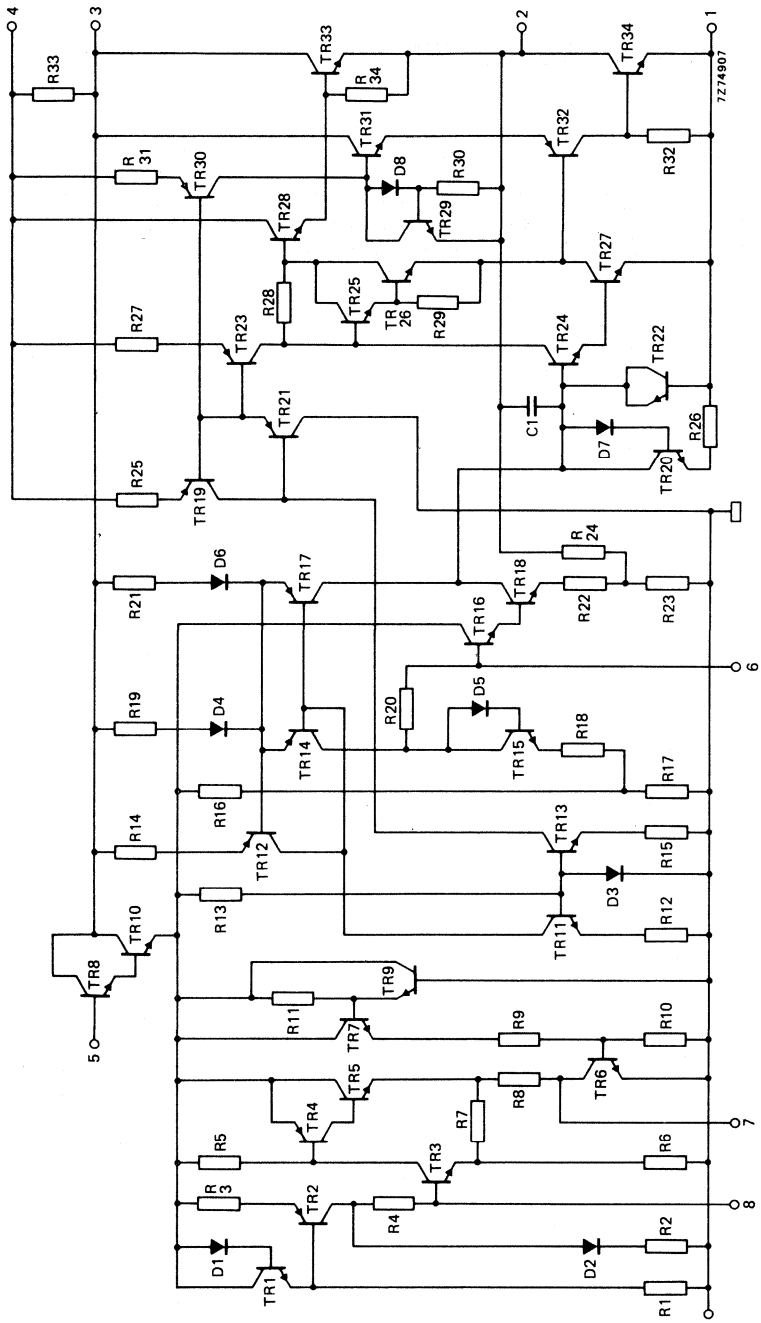


Fig. 1 Circuit diagram.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATA SHEET

0,5 W AUDIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1015T is a low-cost audio amplifier which can deliver up to 0,5 W output power into a 16 Ω load impedance at a supply voltage of 9 V. The amplifier is specially designed for portable applications such as radios and recorders. The IC has a very low supply voltage requirement (3,6 V min.).

Features

- High input impedance
- Separated preamplifier and power amplifier
- Limited noise behaviour at radio frequencies
- Short-circuit protected
- Miniature encapsulation

QUICK REFERENCE DATA

Supply voltage range	V_P		3,6 to 12	V
Peak output current	I_{OM}	max.	1	A
Output power	P_o	typ.	0,5	W
Voltage gain power amplifier	G_{v1}	typ.	29	dB
Voltage gain preamplifier	G_{v2}	typ.	23	dB
Total quiescent current	I_{tot}	max.	22	mA
Operating ambient temperature range	T_{amb}		−25 to +150	°C
Storage temperature range	T_{stg}		−55 to +150	°C

PACKAGE OUTLINE

8-lead mini-pack; plastic (SO8; SOT96A).

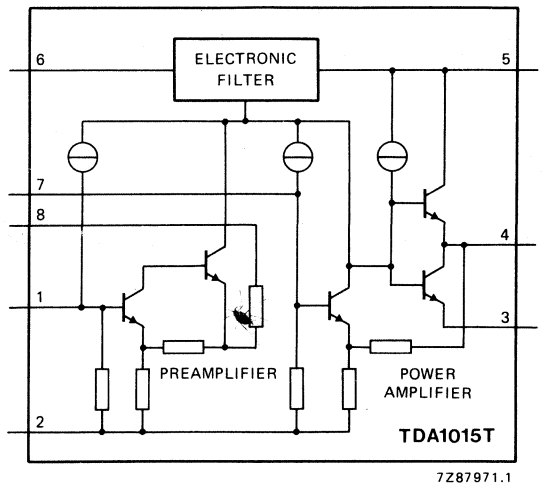


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	12 V
Peak output current	I_{OM}	max.	1 A
Total power dissipation	see derating curve Fig. 2		
Storage temperature range			−55 to +150 °C
A.C. short-circuit duration of load during sine-wave drive at V_P = 9 V	t_{sc}	max.	1 hour

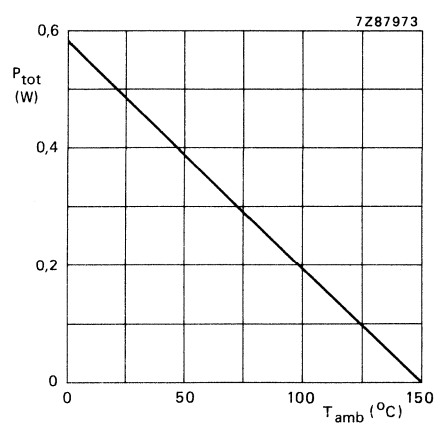


Fig. 2 Power derating curve.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATA SHEET

FM/IF AMPLIFIER CIRCUIT

The TDA1576 is a monolithic integrated f.m./i.f. amplifier circuit provided with the following functions:

- symmetrical limiting i.f. amplifier
- symmetrical quadrature demodulator
- internal muting circuit
- symmetrical a.f.c. output
- field-strength indication output
- detune-detector
- reference voltage output
- electronic smoothing of the supply voltage
- standby on/off switching circuit.

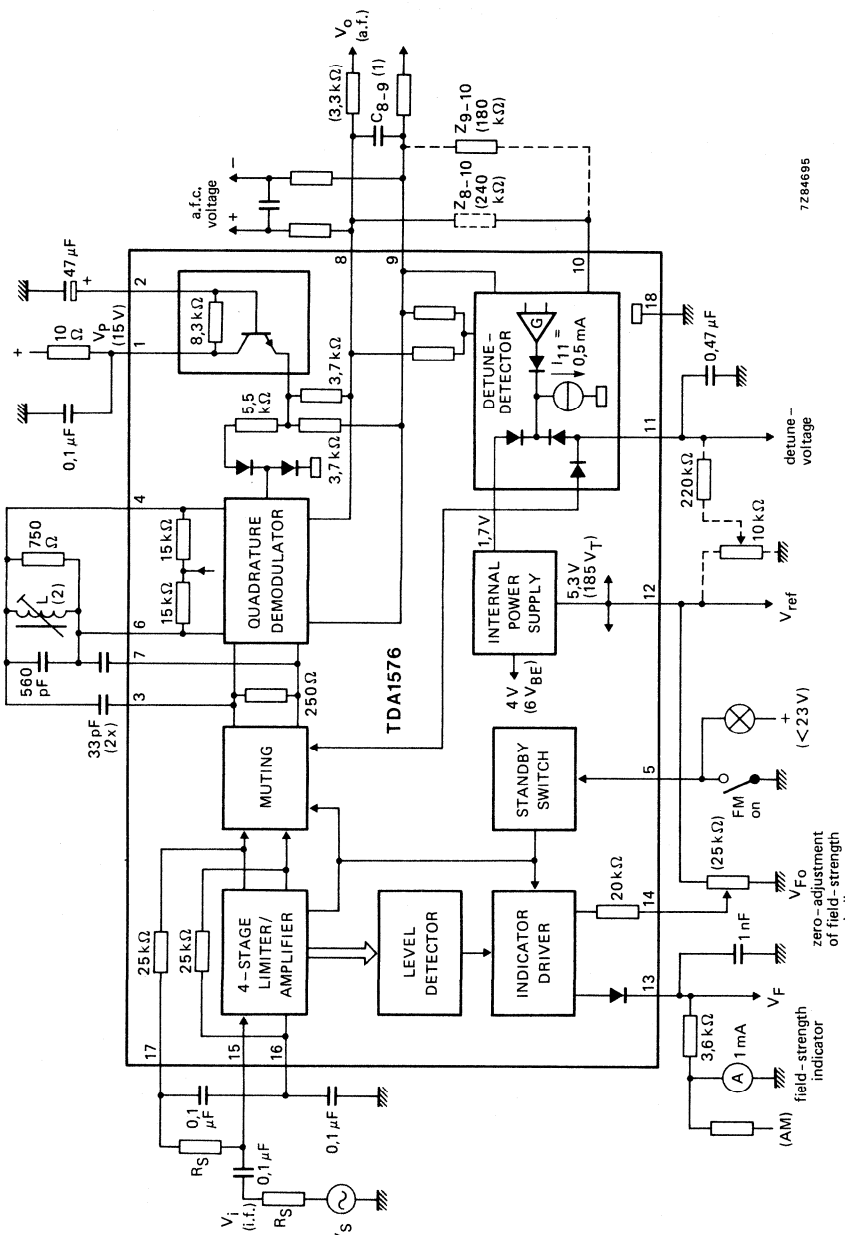
QUICK REFERENCE DATA

f_o = 10,7 MHz; Δf = ± 22,5 kHz; f_m = 400 Hz; Q_L = 20; de-emphasis τ = 50 μs

Supply voltages (pin 1)	V_P		8,5	15	V
Supply current	I_P	typ.	16	18	mA
Sensitivity at −3 dB before limiting	V_i	typ.	22		μV
I.F. sensitivity for					
S + N/N = 26 dB	V_i	typ.	8		μV
S + N/N = 46 dB	V_i	typ.	35		μV
A.F. output voltage	V_o	typ.	67	135	mV
Total distortion					
single tuned circuit	d_{tot}	typ.	0,1		%
two tuned circuits	d_{tot}	typ.	0,02		%
Signal plus noise-to-noise ratio; $V_i > 1$ mV	S + N/N	typ.	76	80	dB
A.M. rejection	α	typ.	50		dB
A.F.C. offset drift	$\pm \Delta f$	typ.	3		kHz
		<	6		kHz
Field-strength indication range	ΔV_i	typ.	90		dB
Permissible indicator (load) current	I_L	<	2		mA
Supply voltage range (pin 1)	V_P		7,5 to 20		V
Ambient temperature range	T_{amb}		−30 to +80		°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).



(1) For de-emphasis $\tau = 50\ \mu s$: $C_{8\text{-}9} = 6{,}8$ nF.
For stereo operation: $C_{8\text{-}9} = 56$ pF.

(2) L = 0,38 μH; $Q_o = 70$; $Q_L = 20$; adjusted to minimum 2nd harmonic distortion (d_2); at $V_i = 1$ mV; coil: 6 turns CuL (0,25 mm) on coil former KAN (C).

Fig. 1 Block diagram and test circuit.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATA SHEET

LOW VOLTAGE MONO/STEREO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA7050 is a low voltage audio amplifier for small radios with headphones (such as watch, pen and pocket radios) in mono (bridge-tied load) or stereo applications.

Features

- Limited to battery supply application only (typ. 3 and 4 V)
- Operates with supply voltage down to 1,6 V
- No external components required
- Very low quiescent current
- Fixed integrated gain of 26 dB, floating differential input
- Flexibility in use – mono BTL as well as stereo
- Small dimension of encapsulation (see package design example)

QUICK REFERENCE DATA

Supply voltage range	V_P	1,6 to 6,0		V
Total quiescent current (at V_P = 3 V)	I_{tot}	typ.	3,2	mA
Bridge tied load application (BTL)				
Output power at R_L = 32 Ω V_P = 3 V; d_{tot} = 10%	P_o	typ.	140	mW
D.C. output offset voltage between the outputs	$\|\Delta V\|$	max.	70	mV
Noise output voltage (r.m.s. value) at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ.	140	μV
Stereo application				
Output power at R_L = 32 Ω d_{tot} = 10%; V_P = 3 V	P_o	typ.	35	mW
d_{tot} = 10%; V_P = 4,5 V	P_o	typ.	75	mW
Channel separation at R_S = 0 Ω; f = 1 kHz	α	typ.	40	dB
Noise output voltage (r.m.s. value) at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ.	100	μV

PACKAGE OUTLINE

8-lead DIL; plastic (SOT97).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	6 V
Peak output current	I_{OM}	max.	150 mA
Total power dissipation	see derating curve Fig. 1		
Storage temperature range	T_{stg}	−55 to + 150	°C
Crystal temperature	T_c	max.	100 °C
A.C. and d.c. short-circuit duration at V_P = 3,0 V (during mishandling)	t_{sc}	max.	5 s

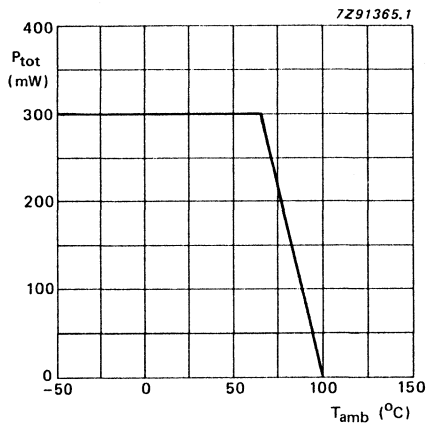


Fig. 1 Power derating curve.

THERMAL RESISTANCE

From junction to ambient $R_{thj\text{-}a}$ = 110 K/W

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATA SHEET

LOW VOLTAGE MONO/STEREO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA7050T is a low voltage audio amplifier for small radios with headphones (such as watch, pen and pocket radios) in mono (bridge-tied load) or stereo applications.

Features

- Limited to battery supply application only (typ. 3 and 4 V)
- Operates with supply voltage down to 1,6 V
- No external components required
- Very low quiescent current
- Fixed integrated gain of 26 dB, floating differential input
- Flexibility in use — mono BTL as well as stereo
- Small dimension of encapsulation (see package design example)

QUICK REFERENCE DATA

Supply voltage range	V_P	1,6 to 6,0	V
Total quiescent current (at V_P = 3 V)	I_{tot}	typ. 3,2	mA
Bridge tied load application (BTL)			
Output power at R_L = 32 Ω V_P = 3 V; d_{tot} = 10%	P_o	typ. 140	mW
D.C. output offset voltage between the outputs	$\|\Delta V\|$	max. 70	mV
Noise output voltage (r.m.s. value) at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ. 140	μV
Stereo application			
Output power at R_L = 32 Ω d_{tot} = 10%; V_P = 3 V	P_o	typ. 35	mW
d_{tot} = 10%; V_P = 4,5 V	P_o	typ. 75	mW
Channel separation at R_S = 0 Ω; f = 1 kHz	α	typ. 40	dB
Noise output voltage (r.m.s. value) at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ. 100	μV

PACKAGE OUTLINE

8-lead mini-pack; plastic (SO8; SOT96A).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	6 V
Peak output current	I_{OM}	max.	150 mA
Total power dissipation	see derating curve Fig. 1		
Storage temperature range	T_{stg}	−55 to + 150	°C
Crystal temperature	T_c	max.	100 °C
A.C. and d.c. short-circuit duration at V_P = 3,0 V (during mishandling)	t_{sc}	max.	5 s

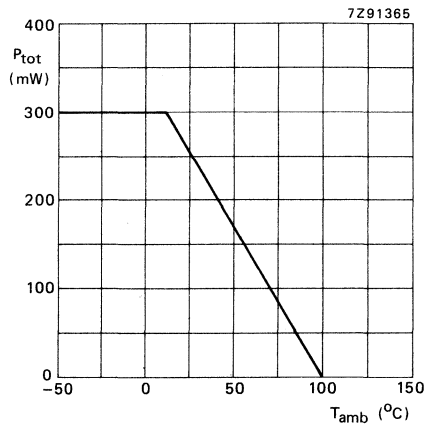


Fig. 1 Power derating curve.

SO PACKAGE DESIGN EXAMPLE

To achieve the small dimension of the encapsulation the SO package is preferred with only 8 pins. Because a heatsink is not applicable, the dissipation is limited by the thermal resistance of the 8-pin SO encapsulation until:

$$\frac{T_{j\ max} - T_{amb}}{R_{th\ j\text{-}a}} = \frac{100-60}{300} = 0{,}1\ W.$$

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATA SHEET

1 W BTL MONO AUDIO AMPLIFIER

GENERAL DESCRIPTION

The TDA7052 is a mono output amplifier in a 8-lead dual-in-line (DIL) plastic package. The device is designed for battery-fed portable audio applications.

Features:

- No external components
- No switch-on or switch-off clicks
- Good overall stability
- Low power consumption
- No external heatsink required
- Short-circuit proof

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	3	6	15	V
Total quiescent current	$R_L = \infty$	I_{tot}	–	4	8	mA
Voltage gain		G_v	38	39	40	dB
Output power	THD = 10%; 8 Ω	P_o	–	1,2	–	W
Total harmonic distortion	P_o = 0,1 W	THD	–	0,2	1,0	%

PACKAGE OUTLINE

8-lead DIL; plastic (SOT97).

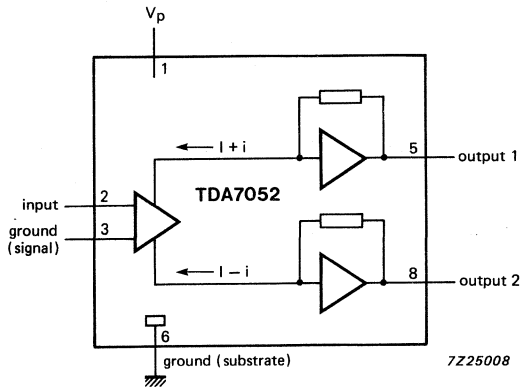


Fig. 1 Block diagram.

PINNING

1	V_P	supply voltage	5	OUT1	output 1
2	IN	input	6	GND2	ground (substrate)
3	GND1	ground (signal)	7	n.c.	not connected
4	n.c.	not connected	8	OUT2	output 2

True logarithmic amplifier TDA8781T

FEATURES

- 55 dB true logarithmic dynamic range
- Small-signal gain-adjust facility
- Constant limiting output voltage
- Temperature and DC power supply voltage compensation
- Easy interfacing to TDA8703 analog-to-digital converter
- Output DC level shift facility
- Additional received signal-strength indication (RSSI) output.

APPLICATIONS

- Dynamic range compression
- IF signal dynamic range reduction in GSM900 and DCS1800 receivers
- Compressive receivers.

GENERAL DESCRIPTION

The TDA8781T is a true logarithmic amplifier intended for dynamic range reduction of IF signals at 10.7 MHz in GSM900 and DCS1800 receivers. It offers true logarithmic characteristics over a 55 dB input dynamic range and has a small-signal gain-adjust facility and a constant limiting output voltage for large input levels. It is manufactured in an advanced BICMOS process which enables high performance to be obtained with low DC power supply consumption. The true logarithmic amplifier can be driven by single-ended or differential inputs and the DC operating point is set by overall on-chip feedback decoupled by two off-chip capacitors which define the low-frequency cut-off point. The performance of the true logarithmic amplifier is stabilized against temperature and DC power supply voltage variations. The differential output is converted internally to a single-ended output by an on-chip operational amplifier arrangement in which the DC output level is set by an externally-supplied reference voltage. An additional received signal-strength indication (RSSI) output is available and a power-down facility allows the circuit to be disabled from a TTL-level compatible control input.

The device can be used to compress IF signals prior to being digitized in digital radio systems. It allows the usage of low-cost, low-power 8-bit DACs instead of the 10 or 12-bit types. In GSM systems decompression is performed by the digital signal processor such as the PCD5080. The TDA8781T interfaces directly with the ADC which is integrated on the Base Band Interface PCD5070.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	DC power supply voltage	4.5	5.0	5.5	V
I_{CC}	DC power supply current	–	–	10	mA
I_{OFF}	I_{CC} in power-down mode	–	250	400	µA
f_i	operating input frequency	0.1	10.7	15.0	MHz
T_{amb}	operating ambient temperature	−20	–	+75	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8781T	14	SO14	plastic	SOT108A

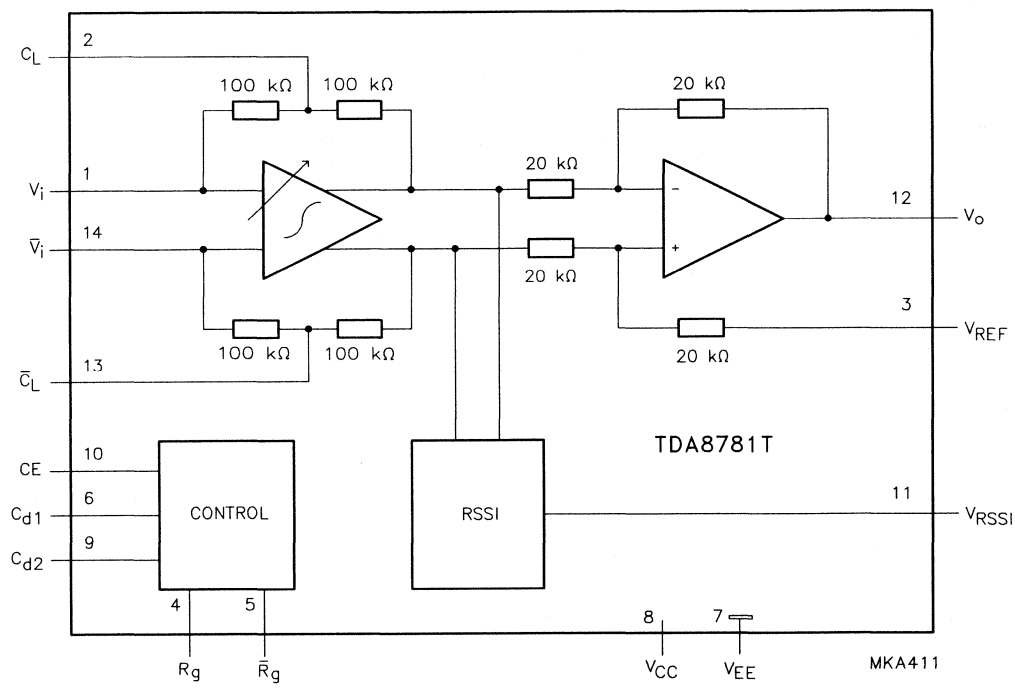


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_i	1	signal input
C_L	2	low-frequency cut-off point setting capacitor connection
V_{REF}	3	external reference voltage input
R_g	4	small-signal gain-setting resistor connection
$\overline{R}_g$	5	complementary small-signal gain-setting resistor connection
C_{d1}	6	first control circuit decoupling capacitor and optional start-up capacitor connection
V_{EE}	7	ground
V_{CC}	8	DC power supply voltage
C_{d2}	9	second control circuit decoupling capacitor and optional start-up capacitor connection
CE	10	TTL-level-compatible circuit enable input
V_{RSSI}	11	received signal-strength indication output (RSSI)
V_o	12	true logarithmic output
$\overline{C}_L$	13	complementary low-frequency cut-off point setting capacitor connection
$\overline{V}_i$	14	complementary signal input

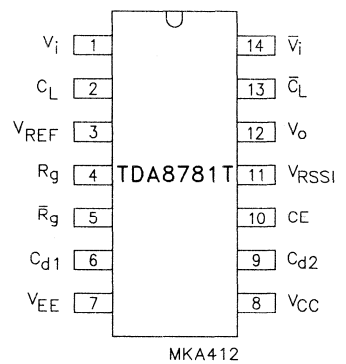


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

A true logarithmic amplifier can be realized from a cascade of similar stages each of which consists of a pair of amplifiers whose inputs and outputs are connected in parallel. One of these amplifiers can be formed by an undegenerated long-tailed pair which provides high gain but a limited linear input signal-handling capability. The other amplifier can be formed by a degenerated long-tailed pair which provides a gain of unity and a much larger linear input signal-handling capability. The overall cascade amplifies very small input signals linearly but, once these reach the level at which the undegenerated long-tailed pair in the last stage is at the limit of its linear input signal-handling capability, the output voltage becomes logarithmically dependent on the input signal level. This behavior continues until the input signal reaches the level at which the undegenerated long-tailed pair in the first stage is at the limit of its linear input signal-handling capability. The transfer characteristic beyond this point then depends on the exact configuration of the degenerated long-tailed pair in the first stage.

Three stages are used in the TDA8781T to provide a 55 dB true logarithmic dynamic range. The DC bias current in the undegenerated long-tailed pair in the first stage is made externally adjustable, by means of an off-chip resistor, to provide a small-signal gain-adjust facility. A high-level limiter is inserted between the first and second stages to provide a constant limiting output voltage which is essentially independent of the value of the gain-setting resistor. These stages can be driven by single-ended or differential inputs and the DC operating point is set by overall on-chip feedback decoupled by two off-chip capacitors which define the low-frequency cut-off point. The performance of these stages is stabilized against temperature and DC power supply voltage variations. The input to the true logarithmic amplifier is protected against damage due to excessive differential input signals by diodes.

The differential output from the true logarithmic amplifier is converted internally to a single ended output by an on-chip operational amplifier arrangement in which the DC output level is set by an externally-supplied reference voltage. The output is capable of driving loads down to 10 kΩ in parallel with 20 pF. The limiting output voltage and this output drive capability have been chosen to facilitate interfacing to a TDA8703 analog-to-digital converter. A major proportion of the DC power supply current consumption of the device is associated with provision of this output drive capability. The DC power supply consumption is significantly less when the device is driving less-highly capacitive loads.

An additional received signal-strength indication (RSSI) output is available from the true logarithmic amplifier. This output is protected against damage due to excessive current being drawn by means of a series resistor. A power-down facility allows the circuit to be disabled from a TTL-level-compatible control input.

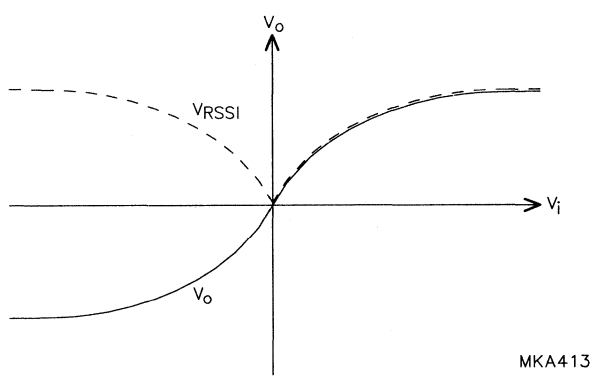


Fig.3 Transfer function.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	DC power supply voltage	−0.3	+5.5	V
V_I	DC voltage at all other pins with respect to ground	−0.3	V_{CC} + 0.3	V
T_{stg}	storage temperature	−55	+125	°C
T_{amb}	operating ambient temperature	−20	+75	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

CHARACTERISTICS

V_{CC} = 5.0 V; V_{REF} = 2.5 V; V_i at f_i = 10.7 MHz; T_{amb} = 25 °C; nominal small-signal gain setting resistor in use; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pin 8)						
V_{CC}	operating DC power supply voltage		4.5	5.0	5.5	V
I_{CC}	DC power supply current	V_{CC} = 5.5 V; V_i = 1 V (peak)	–	8	10	mA
I_{OFF}	DC power supply current in power-down mode	10 µs after V_{CE} changes from $V_{CE(ON)}$ to $V_{CE(OFF)}$	–	250	400	µA
Control: CE, R_g, $\overline{R}_g$, C_{d1}, C_{d2} (pins 10, 4, 5, 6 and 9)						
$V_{CE(ON)}$	circuit enable input voltage		2.0	–	V_{CC}	V
$V_{CE(OFF)}$	circuit enable input voltage in power-down mode		0	–	0.8	V
R_g	small-signal gain-setting resistor	nominal small-signal gain setting	–	3.3	–	kΩ
		total adjustment range	0	–	–	kΩ
C_{d1}, C_{d2}	control circuit decoupling capacitors		–	560	–	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs: V_I, V_{REF}, C_L, $\overline{C}_L$ (pins 1, 3, 2 and 13)						
f_i	operating input frequency		0.1	10.7	15	MHz
R_i	small-signal input resistance	differential input at f_i = 10.7 MHz; V_i = 10 mV (peak)	–	10	–	kΩ
C_i	input capacitance	differential input at f_i = 10.7 MHz	–	3	–	pF
$V_{i(min)}$	peak input voltage at start of true logarithmic characteristic		–	800	–	μV
$V_{i(max)}$	peak input at end of true logarithmic characteristic		–	450	–	mV
$V_{i(limit)}$	maximum peak input signal	input protection diodes not conducting	–	1	–	V
ΔV_i	spread in true logarithmic output amplitude transfer characteristic across true logarithmic range over whole temperature and DC power supply voltage range	input spread for fixed output	–	±2.5	–	dB
ΔG_v	small-signal gain-adjustment range		±6	–	–	dB
C_L, $\overline{C}_L$	low-frequency cut-off point setting capacitors	f = 100 kHz at 3 dB	–	560	–	pF
R_{REF}	external reference input resistance		–	40	–	kΩ
V_{REF}	external reference voltage		2.0	2.5	V_{CC} – 2.0	V
Outputs: V_o, V_{RSSI} (pins 12 and 13)						
$V_{o(min)}$	peak true logarithmic output voltage relative to V_{REF} at start of true logarithmic characteristic	V_i = 800 μV (peak)	–	90	–	mV
$V_{o(max)}$	peak true logarithmic output voltage relative to V_{REF} at end of true logarithmic characteristic	V_i = 450 mV (peak)	–	900	–	mV
V_o	true logarithmic peak output voltage across true logarithmic range	V_i = 1 mV (peak)	55	100	145	mV
		V_i = 10 mV (peak)	340	410	480	mV
		V_i = 100 mV (peak)	630	730	830	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{o(limit)}$	limiting peak output voltage	V_i = 1 V (peak)	800	950	1100	mV
$V_o - V_{REF}$	DC offset voltage	V_i = 0 V	−100	+35	+100	mV
ΔG_{vo}	change in small-signal true logarithmic gain referred to V_o at V_i = 10 mV (peak); R_g = 3.3 kΩ	V_i = 5 mV (peak); R_g = 0	0	–	+2	dB
		V_i = 20 mV (peak); R_g = ∞	−2	–	0	dB
ΔV_o	change in small-signal true logarithmic output voltage with frequency	V_i = 10 mV (peak); f_i = 100 kHz and 15 MHz referenced to 1 MHz	–	0.4	1.5	dB
$\Delta\phi$	spread in true logarithmic output phase transfer characteristic across true logarithmic range		–	15	–	deg
V_{RSSI}	RSSI output across true logarithmic range	V_i = 1 mV (peak)	1.85	2.0	2.15	V
		V_i = 10 mV (peak)	2.05	2.2	2.35	V
		V_i = 100 mV (peak)	2.25	2.4	2.55	V

APPLICATION INFORMATION

The circuit is connected as shown in the typical application circuit diagram (Fig.4). The single-ended 10.7 MHz input IF signal is applied (arbitrarily) to one of the two input pins via a ceramic filter. These inputs should not be DC coupled as this will disable the on-chip feedback which sets the DC operating point of the true logarithmic amplifier. The relatively high input impedance of these inputs facilitates correct termination of the ceramic filter by means of an off-chip resistor.

The low-frequency cut-off point is determined by the value of the capacitors which decouple the overall DC feedback as well as the value of the input coupling capacitors. The output is AC coupled to a TDA8703 analog-to-digital converter in order that the value of the voltage fed to the reference voltage input is not critical. It could be useful in other applications, where the output might be DC coupled to an alternative analog-to-digital converter, to derive this reference voltage from the centre of the input resistor chain of the analog-to-digital converter.

The additional RSSI output is required only in applications where this is not derived in subsequent digital signal processing stages. The capacitor connected to this output provides a simple peak-hold and averaging function. Excessively large values of capacitance may lead to distortion of the true logarithmic output.

It may be found advantageous to add two small capacitors to speed up the re-enabling of the circuit after it has been in power-down mode. These should be connected between the circuit enable input and the control circuit decoupling capacitors. The size of these capacitors will be related to the size of the control circuit decoupling capacitors which are required both for stability and to prevent degradation of the noise figure.

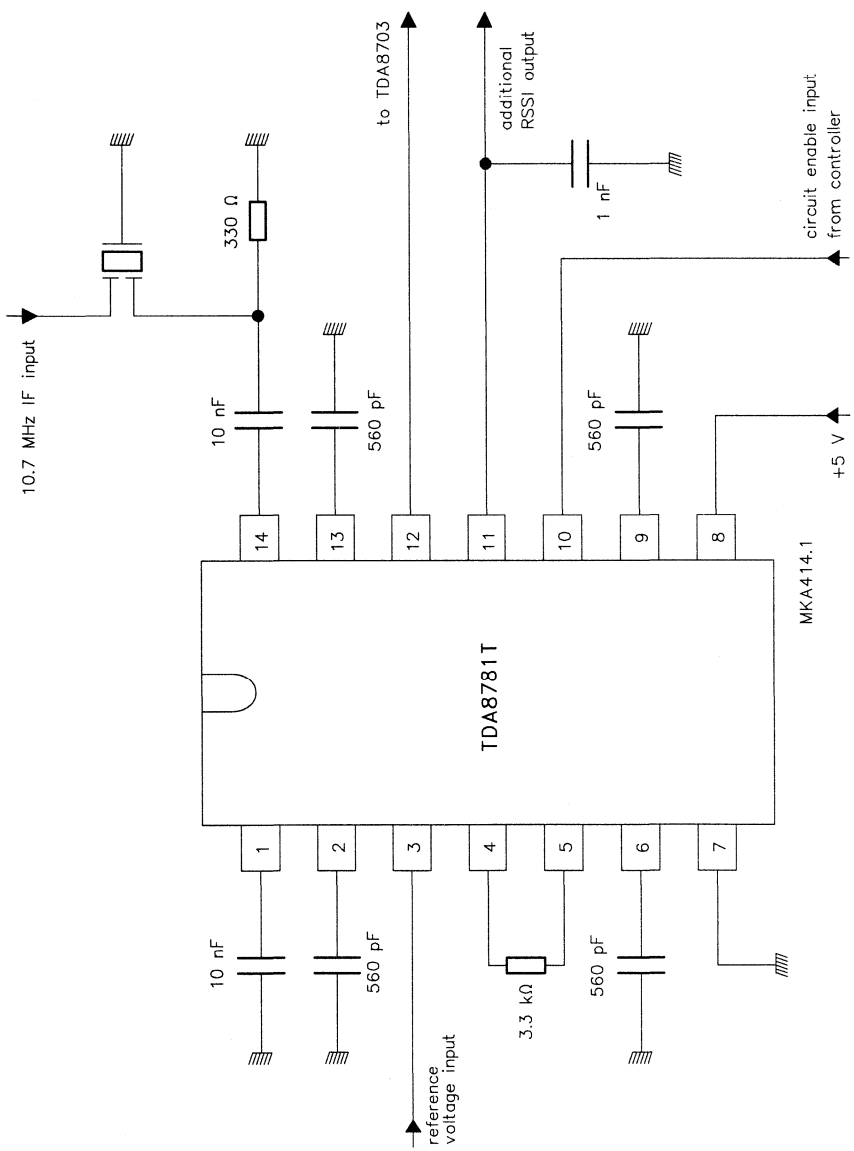
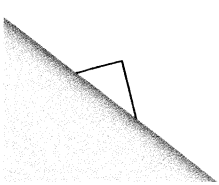


Fig.4 Typical application diagram.



LOW POWER FREQUENCY SYNTHESIZER (LOPSY)

GENERAL DESCRIPTION

The TDD1742T is a low power, high-performance frequency synthesizer in local oxidation CMOS (LOCMOS) technology. The device is designed for use in channelized VHF/UHF applications especially portable and mobile radios.

The circuit incorporates many of the features of the HEF4750V (frequency synthesizer) and HEF4751 (universal divider), including a high-gain phase comparator together with an on-chip sample-and-hold capacitor and phase modulator.

A multiplexed or bus-structured programming sequence allows interface to a microcontroller or external memory (ROM/PROM); power is applied to the memory only when it is required for programming via additional on-chip circuitry.

Operation is possible with a minimum supply voltage of 7 V and a maximum input frequency of 8,5 MHz.

Encapsulation in a 28-lead mini-pack enables the construction of small, low power consumption synthesizers with low noise performance and high side-band attenuation.

Features

- On-chip sample-and-hold capacitor
- Low power consumption
- High-gain phase comparator with low levels of noise and spurious outputs
- Auxiliary digital phase comparator for fast locking
- On-chip phase modulator
- Simple interfacing to external memory
- Microcontroller compatible
- Power-on reset circuitry

QUICK REFERENCE DATA

Supply voltage ranges			
pin 14	$V_{DD1} = V_{14-6}$		7 to 10 V
pin 8	$V_{DD2} = V_{8-6}$		4,5 to 5 V
pin 1	$V_{DD3} = V_{1-6}$		7 to 10 V
Supply current			
(at T_{amb} = 25 °C; $V_{DD1} = V_{DD3}$ = 7,4 V; V_{DD2} = 5 V)			
pin 14 (phase modulator OFF)	$I_{DD1} = I_{14}$	max.	1,5 mA
pin 8	$I_{DD2} = I_8$	max.	100 μA

PACKAGE OUTLINE

28-lead mini-pack; plastic (SO28; SOT136A).

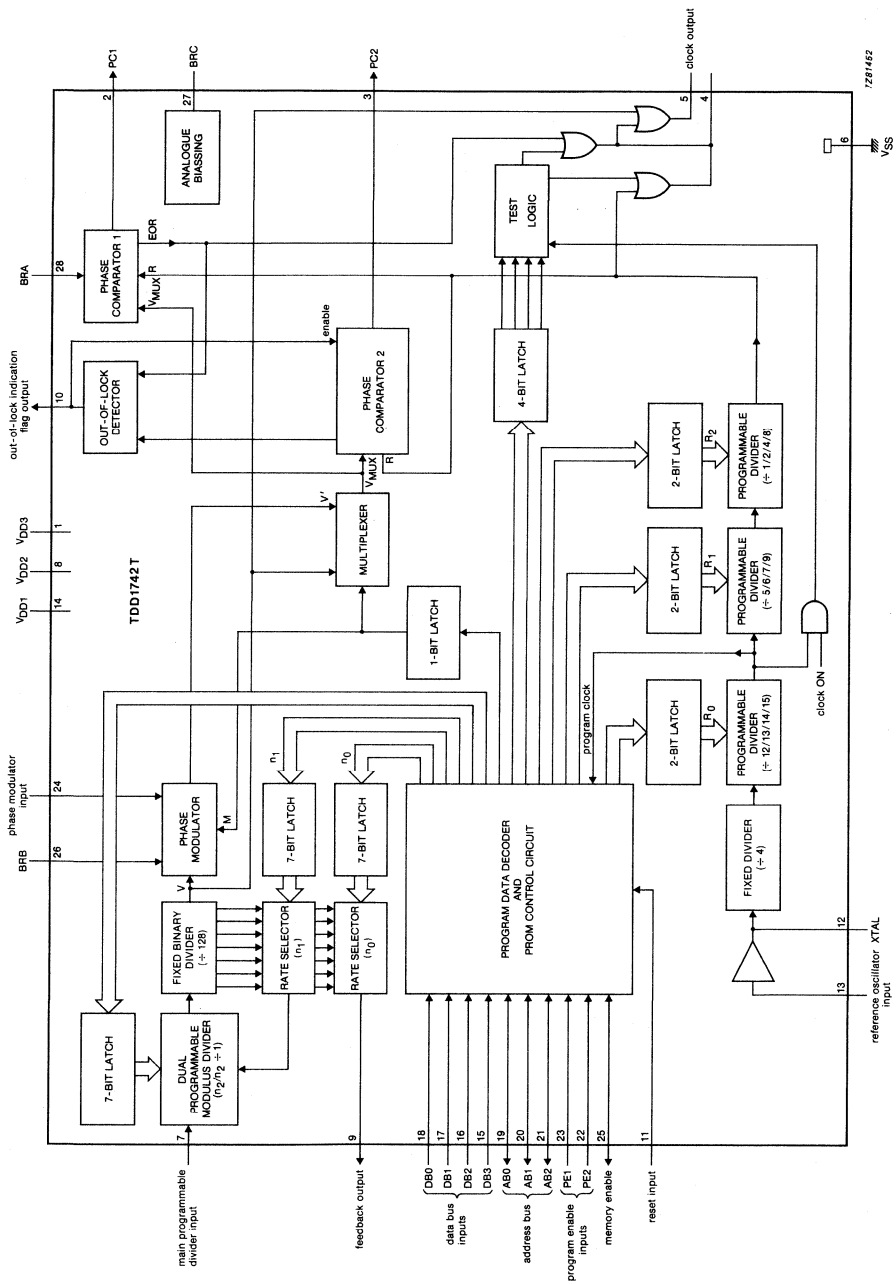


Fig. 1 Block diagram.

PINNING

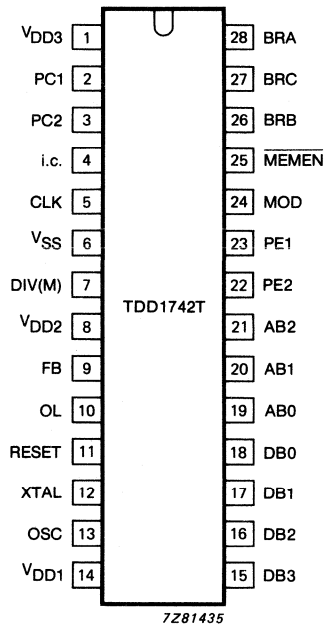


Fig. 2 Pinning diagram.

Pin functions

pin no.	mnemonic	description
1	V_{DD3}	**Power Supply 3:** analogue supply voltage (7 to 10 V).
2	PC1	**Phase Comparator 1:** high-gain analogue phase comparator output which is used when the system is in-lock to give low levels of noise and spurious outputs.
3	PC2	**Phase Comparator 2:** low-gain digital phase comparator 3-state output which enables the achievement of fast lock times when the system is initially out-of-lock. Phase comparator 2 is inhibited when the phase is within the locking range of phase comparator 1.
4	i.c.	**internally connected** (must be left floating).
5	CLK	**Clock:** clock output.
6	V_{SS}	**Ground:** circuit earth potential.
7	DIV(M)	**Divider:** input to the main programmable divider (8,5 MHz max.), usually from prescaler.
8	V_{DD2}	**Power Supply 2:** supply voltage for TTL-compatible stages (+ 5 V ± 10%).
9	FB	**Feedback:** feedback output to control the modulus of the external prescaler.
10	OL	**Out-of-lock:** out-of-lock indication flag output. This output is HIGH when phase comparator 2 is in operation (when the system is out-of-lock).
11	RESET	**Power-on-Reset:** Following power up an initial pulse is applied to this input pin to set the internal counters.

Pin functions (continued)

pin no.	mnemonic	description
12	XTAL	**Crystal:** output to external crystal to form the oscillator circuit in combination with the OSC input. Alternatively this pin may be used as a buffer output.
13	OSC	**Oscillator:** input to reference oscillator which together with the XTAL output and an external crystal is used to generate the reference frequency. Alternatively to OSC input may be used as a buffer amplifier for an external reference oscillator.
14	V_{DD1}	**Power Supply 1:** digital supply voltage (7 to 10 V).
15-18	DB3-DB0	**Data Bus:** Data Bus inputs (TTL compatible).
19-21	AB0-AB2	**Address Bus:** TTL compatible bidirectional address bus. Provides address output to an external memory or input from microcontroller. The outputs are 3-state with internal pull-downs.
22	PE2	**Program Enable 2:** TTL compatible inputs to initiate the programming cycle or strobe the internal data latches.
23	PE1	**Program Enable 1:**
24	MOD	**Modulator:** high impedance linear phase modulator input, which applies a voltage controlled delay to the programmable divider output to the phase comparator.
25	$\overline{\text{MEMEN}}$	**Memory Enable:** mode control and memory enable bidirectional pin. If pin 25 is LOW at general reset the TDD1742T is set to the microcontroller mode; if pin 25 is HIGH at general reset the TDD1742T is set to the memory mode and the ROM/PROM is enabled.
26	BRB	**Bias Resistor B:** current mirror which acts as gain control for the phase modulator.
27	BRC	**Bias Resistor C:** current mirror pin which provides analogue biassing.
28	BRA	**Bias Resistor A:** current mirror pin which acts as gain control for phase comparator 1.

FUNCTIONAL DESCRIPTION

Reference oscillator chain

The reference oscillator chain comprises a crystal oscillator and dividers to give the required frequency to drive the phase comparators.
The oscillator stage is a single inverter connected between pin 12 (XTAL) and pin 13 (OSC). Satisfactory operation is achieved with crystals up to 9 MHz. Alternatively, the OSC input may be used as a buffer amplifier for an external reference oscillator.
The reference divider chain comprises a fixed divide by 4-stage followed by three cascaded programmable dividers of ratios ÷ 12/13/14/15, ÷ 5/6/7/9 and ÷ 1/2/4/8. The output of the last stage is applied as one input (R) to the two phase comparators. Thus a number of division ratios between 240 and 4320 are possible which provides all the required VHF and UHF channel spacings with reference crystals in a 1 to 9 MHz range.

Main programmable divider

The main programmable divider is a rate feedback binary divider. As shown in figure 1 it comprises a fixed 7-bit binary divider (÷ 128) and two rate selectors (n_1 and n_0). One rate selector controls a 7-bit fully programmable dual modulus divider (÷ $n_2/n_2 + 1$) and the other controls the external dual modulus prescaler (÷ A/A + 1).

The overall division rate (N) is given by:

$$N = (128\, n_2 + n_1)\, A + n_0$$

Where:

$$0 \leqslant n_0 \leqslant 127$$
$$0 \leqslant n_1 \leqslant 127$$
$$1 \leqslant n_2 \leqslant 127.$$

The output from the programmable divider is fed to the phase comparators via the phase modulator and the multiplexer. The phase modulator is bypassed if not selected.

Phase comparison

The TDD1742T contains 2 phase comparators which act in close co-operation. Phase comparator 1 is the main comparator. It is designed to have a high-gain analogue output, 4500 volts/cycle at 10 kHz (typ.). This enables a low noise performance to be achieved. However, the output of phase comparator 1 will saturate at high or low levels for very small phase excursions.
Phase comparator 2 is an auxiliary comparator with a wide range, which enables faster lock times to be achieved than otherwise would be possible. This digital phase comparator has a linear $\pm 2\pi$ radians phase range, which corresponds to a gain of $\frac{V_{DD}}{2}$ volts/cycle.

To avoid degrading the noise performance of the system by the relatively low gain of phase comparator 2, once a small phase error has been achieved an internal switch disconnects phase comparator 2, leaving only phase comparator 1 connected. Thus the low noise properties of phase comparator 1 are obtained once phase-lock has been achieved.

FUNCTIONAL DESCRIPTION (continued)

Phase comparator 1 (see Fig. 3)

Phase comparator 1 is comprised of a linear ramp generator and a sample and hold circuit.

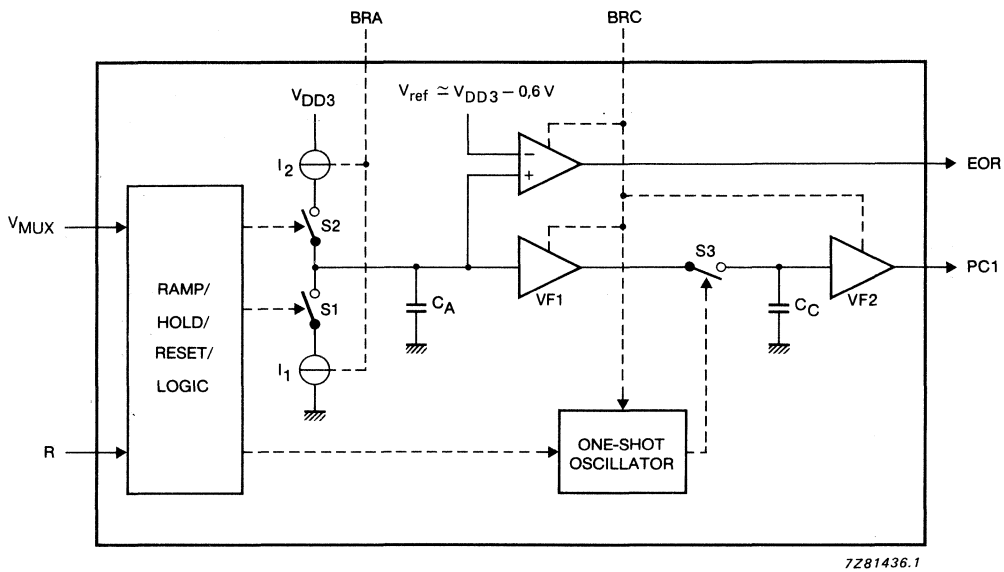


Fig. 3 Simplified block diagram of phase comparator 1.

A negative-going transition at the V_{MUX} input causes the hold capacitor C_A to be discharged via switch S1 and constant current source I_1.
A positive-going transition at the V_{MUX} input causes the hold capacitor C_A to be charged via switch S2 and constant current source I_2, which produces a linear ramp.
A negative-going transition at the R input terminates the linear ramp.
Capacitor C_A holds the voltage that the ramp has attained, and is buffered by the voltage follower VF1. After the output of VF1 is stable (2 μs), the sample switch S3 is closed for approximately 1 μs by the one-shot oscillator. This enables the capacitor C_C to charge to the voltage level of VF1 and in turn buffered by voltage follower VF2 made available at output PC1.
The construction and small duty cycle of the sample switch S3 provides a low hold step, resulting in a minimum side-band level.
If the linear ramp terminates before a negative-going transition at the R input is present, an end of ramp (EOR) signal is produced, generating in turn an out-of-lock (OL) signal. OL enables phase comparator 2 via the out-of-lock detector.

These actions are illustrated in the waveforms of Fig. 4 and Fig. 5.

The gain of phase comparator 1 as measured at PC1 is given by:

$$\text{PC gain} \simeq \frac{446\, I_{BRA}}{F_R}$$

Where:

I_{BRA} is in μA
F_R is the phase comparator reference frequency in kHz

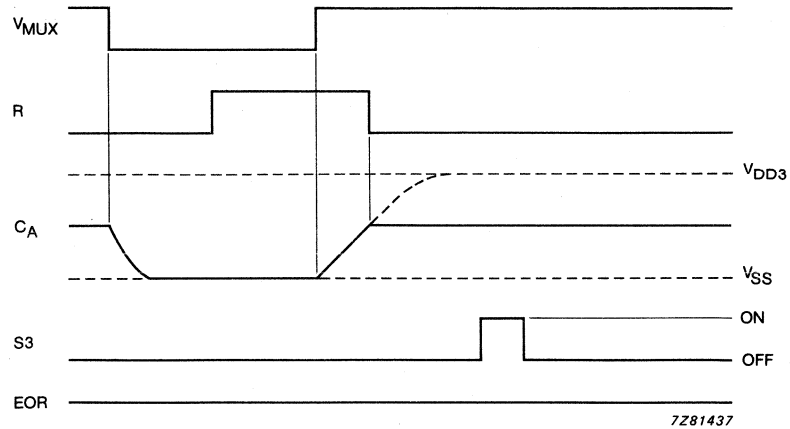


Fig. 4 Waveforms of phase comparator 1; in-lock condition.

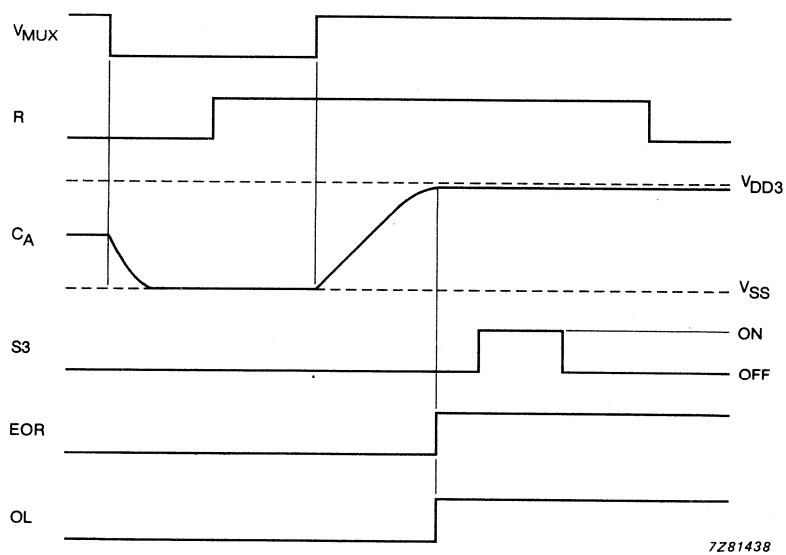


Fig. 5 Waveforms of phase comparator 1; out-of-lock condition.

When V_{MUX} leads R the output signal at pin 2 (PC1) is proportional to the phase difference (in-lock condition) or HIGH (out-of-lock condition).
When R leads V_{MUX} the output signal at pin 2 (PC1) remains LOW.

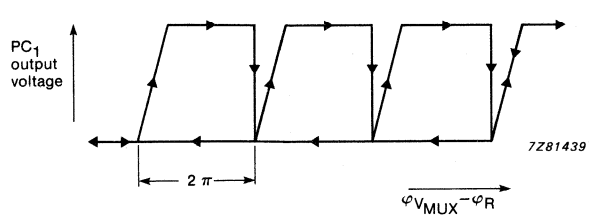


Fig. 6 Phase characteristic of output PC1.

FUNCTIONAL DESCRIPTION (continued)

Phase comparator 2 (see Fig. 7)

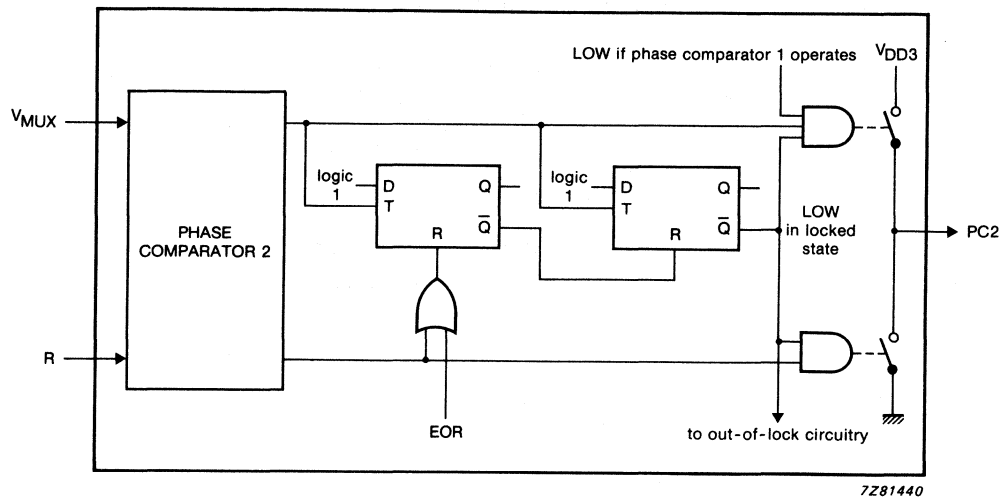


Fig. 7 Simplified block diagram of phase comparator 2.

The digital phase comparator (PC2) has three stable states:

- Reset
- V_{MUX} leads R
- R leads V_{MUX}

Table 1 Phase comparator 2: stable states and corresponding output levels

state	V_{MUX} leads R	R leads V_{MUX}
reset	0	0
V_{MUX} leads R	1	0
R leads V_{MUX}	0	1

Transition from one state to another takes place on command of either an active V_{MUX}-edge or an active R-edge as shown in Fig. 8.

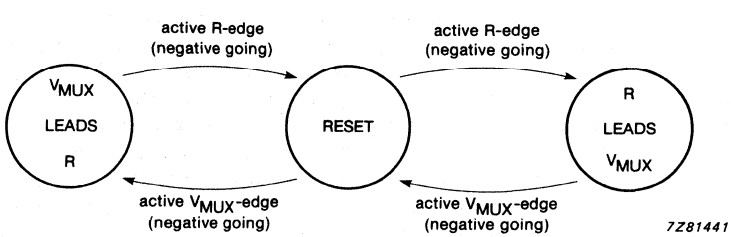


Fig. 8 Transition of state; phase comparator 2.

The output of phase comparator 2 produces positive or negative going pulses with variable width, dependent on the phase relationship of R and V_{MUX}.
The average output voltage is a linear function of the phase difference. Output at pin 3 (PC2) remains in the high impedance OFF-state in the region in which phase comparator 1 operates

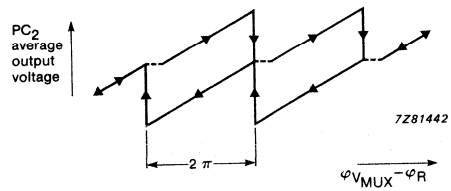


Fig. 9 Phase characteristic of output PC2.

To reach the reset state of phase comparator 2 it is necessary to apply:

- $2V_{MUX} + R^*$
  or
- $2R + V_{MUX}$

Thus to achieve the R leads V_{MUX} state 2R must be applied; to achieve the V_{MUX1} leads R state $2V_{MUX}$ must be applied.

Out-of-lock function

There are several situations when the system goes from the locked to the out-of-lock state (OL output goes HIGH):

- V_{MUX} leads R, however out of the range of phase comparator 1
- R leads V_{MUX}
- R-pulse is missing
- V_{MUX}-pulse is missing

In the first three situations the locked state can be reset by applying two successive cycles within the range of phase comparator 1.
In the fourth situation the locked state can be reset by applying a V_{MUX} pulse followed by two successive cycles within the range of phase comparator 1.

Phase modulator (see Fig. 10)

The linear phase modulator applies a voltage controlled delay to the signal from the programmable divider to the phase comparator input. The gain of the phase modulator is adjustable via an external bias resistor (BRB) which is connected between pin 26 and ground.
The time delay introduced into the V path to the phase modulator is:

$$\frac{909}{I_{BRB}} \text{ ns/volt of input applied to pin 24 (MOD)}$$

When a positive-going transition appears at the V-input, the D type flip-flop produces a HIGH V′ level and causes capacitor C_B to produce a positive-going ramp via switch S1 and constant current source I_1 starting at the V_{SS} potential. When the ramp has reached a value equal to the modulation input voltage (at MOD), the comparator resets the D type flip-flop, which terminates the V pulse. C_B now discharges to V_{SS} via switch S1 and constant current source I_2 and the circuit returns to the start position. Because the trailing edge of the V′ pulse is the active edge for the phase comparators, a linear phase modulation is achieved. The associated waveforms are shown in Fig. 11. The phase modulator can be switched OFF, via the programming logic, to avoid superfluous dissipation. To achieve, this the M signal must be programmed to logic 0. The V pulse will then be connected via switch S2 to V_{MUX}.

* This means apply two successive active V_{MUX} edges followed by one active R edge.

FUNCTIONAL DESCRIPTION (continued)

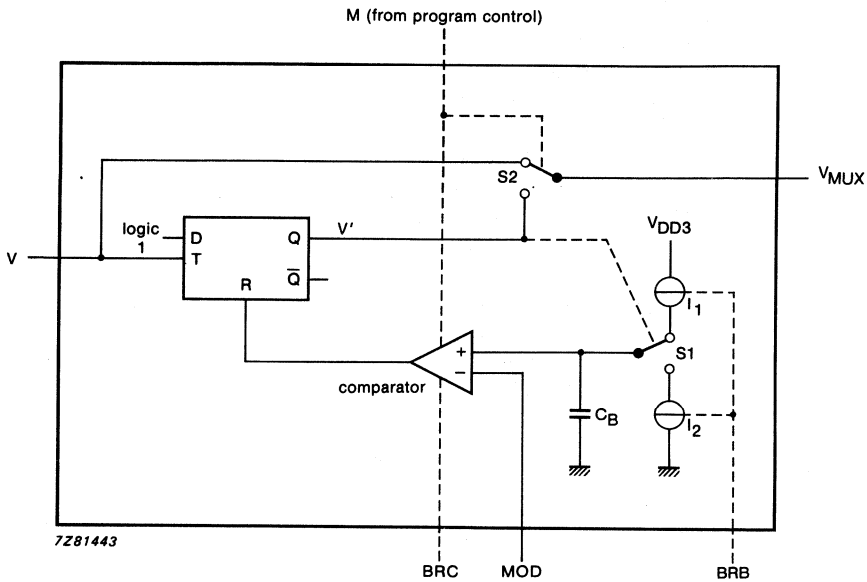


Fig. 10 Simplified block diagram of the phase modulator.

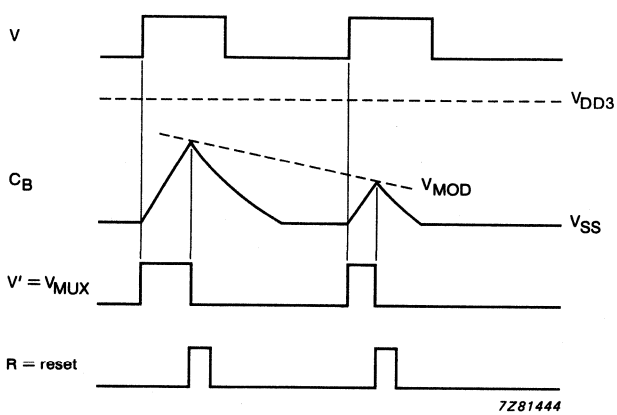


Fig. 11 Phase modulator waveforms; M = 1.

Program control

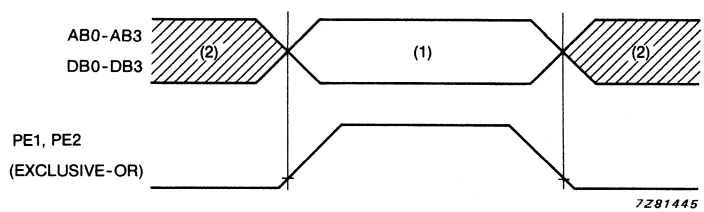
A multiplexed or bus structured sequence allows the TDD1742T to be interfaced to a microcontroller or a PROM.
The device is fully programmable in terms of:

- 6 bits to define the reference divider ratio
- 21 bits to define the main divider ratio
- 1 bit to switch the modulator
- 4 bits to determine the test status

Thus the TDD1742T is programmed with a total of 32 bits which are organized as eight 4-bit words. The address bus is 3 bits wide and the data bus is 4 bits wide. Both buses are TTL compatible. The data words are described in detail in Tables 3 to 7.

Microcontroller mode

If pin 25 ($\overline{\text{MEMEN}}$) is LOW at general reset, the device is set to the micro-controller mode. In this mode a 7-bit word, comprised of 3 address bits (AB0 to AB2) and 4 data bits (DB0 to DB3), may be strobed into the TDD1742T when the program enable pins PE1 and PE2 are set to opposite state (EXCLUSIVE -OR condition; see Fig. 12 and Table 2). One frame of 8 words is necessary to completely program the TDD1742T. Incoming data is not clocked into the internal counter latches until after the receipt of data corresponding to address 111. Upon subsequent reprogramming it is not necessary to change all eight words but a reprogramming sequence must always finish with the data corresponding to address 111.



(1) Address and data valid.
(2) Address and data not valid.

Fig. 12 Waveforms for program enable function; microcontroller mode.

Table 2 Truth table for program enable function; microcontroller mode

PE1	PE2	load
0	0	NO
1	0	YES
0	1	YES
1	1	NO

Program control (continued)

Memory mode (PROM)

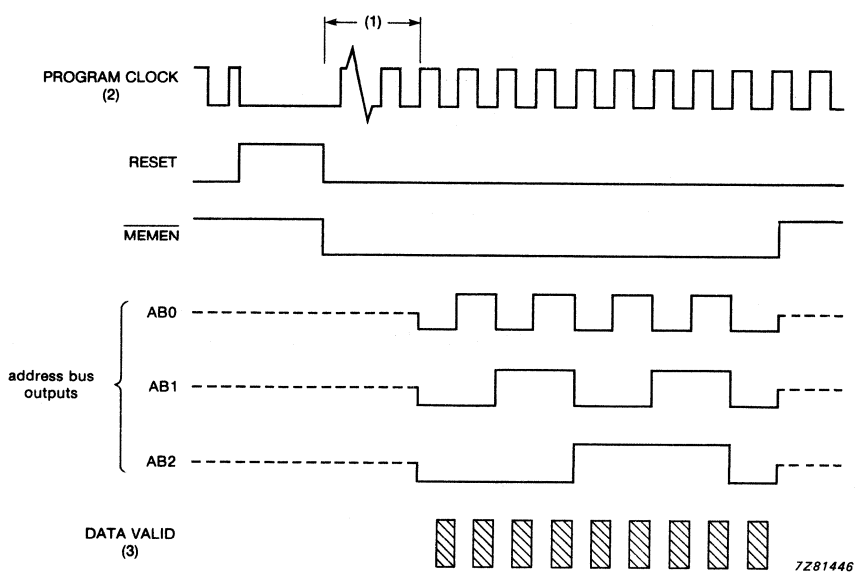
If pin 25 ($\overline{\text{MEMEN}}$) is HIGH at general reset, TDD1742T is set to the memory mode and a programming cycle is initiated. Subsequent reprogramming is performed by applying a pulse to program enable PE1 (pin 23) or PE2 (pin 22). If PE1 is LOW, programming will occur on the LOW-to-HIGH transition of PE2. If PE1 is HIGH, programming will occur on the HIGH-to-LOW transition of PE2. PE1 and PE2 are interchangeable. Reprogramming will also occur by applying a pulse to RESET (pin 11).

At the start of a programming sequence pin 25 goes LOW and may be used to apply power to the memory via an external driver. After a settling time the address bus outputs 000 followed by the remaining seven addresses. During the second half of each address period data, from the memory is latched into the TDD1742T so that the access time of the PROM is not critical.

Note

The program clock is derived from the reference divider chain and its frequency equals $f_{OSC}/4R_0$.

After the full 32 bits have been read the address returns to address 000 before going 3-state. This step transfers data from the internal data latches to the appropriate divider latches. Pin 25 now returns to a high impedance state and power is removed from the memory. Fig. 13 shows the timing for a reset initiated programming sequence; the timing is similar for program enable initiated sequence.



(1) Delay time for PROM settling.
(2) The program clock is derived from the reference divider chain.
(3) Data is valid during the shaded period.

Fig. 13 Timing diagram for TDD1742T PROM control.

Data memory maps

Table 3 Bit programming of the eight 4-bit words

address			data			
AB2	AB1	AB0	DB3	DB2	DB1	DB0
0	0	0	see Table 4			
0	0	1	$n_0 3$	$n_0 2$	$n_0 1$	$n_0 0$
0	1	0	$R_0 0$	$n_0 6$	$n_0 5$	$n_0 4$
0	1	1	$n_1 3$	$n_1 2$	$n_1 1$	$n_1 0$
1	0	0	$R_0 1$	$n_1 6$	$n_1 5$	$n_1 4$
1	0	1	$n_2 3$	$n_2 2$	$n_2 1$	$n_2 0$
1	1	0	M	$n_2 6$	$n_2 5$	$n_2 4$
1	1	1	$R_2 1$	$R_2 0$	$R_1 1$	$R_1 0$

In Table 3

n_0, n_1 and n_2 comprises the main programmable divider.

$n_0 0$ is the LSB of n_0, $n_0 6$ the MSB and so forth.

If M is 1 the modular is ON.

Table 4 Memory map for address 000

DB3	DB2	DB1	DB0	program clock to output CLK	mode
0	0	X	X	yes	idle
0	1	0	0	no	idle
all other combinations				not defined	not defined

Where

X = don't care.

For optimum performance (minimum crosstalk) 0100 should be programmed into address 000.

Memory maps (continued)

Table 5 Reference divider control; part 1

R_01	R_00	division ratio
0	0	12
0	1	13
1	0	14
1	1	15

In Table 5:

R_00 and R_01 control the ÷ 12/13/14/15 portion of the reference divider.

Table 6 Reference divider control; part 2

R_11	R_10	division ratio
0	0	9
0	1	5
1	0	6
1	1	7

In Table 6:

R_10 and R_11 control the ÷ 5/6/7/9 portion of the reference divider.

Table 7 Reference divider control; part 3

R_21	R_20	division ratio
0	0	1
0	1	2
1	0	4
1	1	8

In Table 7:

R_20 and R_21 control the ÷ 1/2/4/8 portion of the reference divider.

Current biassing

Current biassing is provided by 3 external bias resistors A, B and C.

Bias Resistor A: is connected between pin 28 (BRA) and ground. The value of the resistor must be such that $I_{BRA} = 20\ \mu A$, which acts as gain control for analogue phase comparator 1.
Bias Resistor B: is connected between pin 26 (BRB) and ground. The value of the resistor must be such that $I_{BRB} = 3$ to $25\ \mu A$, which acts as gain control for the phase modulator.
Bias Resistor C: is connected between pin 27 (BRC) and ground. The value of the resistor must be such that $I_{BRC} = 5$ to $30\ \mu A$, which provides biassing for the remainder of the analogue circuitry.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage ranges			
pin 14	V_{DD1}		−0,5 to + 15 V
pin 8	V_{DD2}		−0,5 to + 15 V
pin 1	V_{DD3}		−0,5 to + 15 V
Voltage on any input	V_I		−0,5 to V_{DD1} + 0,5 V
Relative supply voltage	V_{DD2}-V_{DD1}	max.	0,5 V
Relative supply voltage	V_{DD3}-V_{DD1}	max.	0,5 V
D.C. current into any input or output	± I	max.	10 mA
Power dissipation per package for T_{amb} = 0 to + 85 °C	P_{tot}	max.	400 mW
Power dissipation per output for T_{amb} = 0 to + 85 °C	P_O	max.	100 mW
Storage temperature range	T_{stg}		−65 to 150 °C
Operating ambient temperature range	T_{amb}		−40 to 85 °C

D.C. CHARACTERISTICS

$V_{DD1} = V_{DD3} = 7{,}4$ V; $V_{DD2} = 5$ V; $V_{SS} = 0$ V; $T_{amb} = 25\ ^{o}C$ unless otherwise specified; for definitions see note 1.

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage					
pin 14	V_{DD1}	7	–	10	V
pin 8	V_{DD2}	4,5	–	5	V
pin 1	V_{DD3}	7	–	10	V
Supply current					
pin 14 (phase modulator OFF)	I_{DD1}	–	–	1,5	mA
pin 8	I_{DD2}	–	–	100	μA
pin 1 (phase modulator OFF)	I_{DD3}	–	–	1,5	mA
Input leakage current (notes 2 and 3)					
logic inputs, MOD	$\pm I_{LI}$	–	–	300	nA
Output leakage current (notes 2 and 3) at ½ V_{DD}					
PC2 high impedance OFF state	$\pm I_{LO}$	–	–	50	nA
$\overline{\text{MEMEN}}$ high impedance state	$\pm I_{LO}$	–	–	1,6	μA
I/O current					
AB0 to AB2 high impedance state	$I_{I/O}$	5	–	30	μA
Logic input voltage LOW					
CMOS inputs; CMOS I/Os	V_{IL}	–	–	$0{,}3V_{DD1}$	V
TTL inputs; TTL I/Os	V_{IL}	–	–	0,8	V
Logic input voltage HIGH					
CMOS inputs; CMOS I/Os	V_{IH}	$0{,}7V_{DD1}$	–	–	V
TTL inputs; TTL I/Os	V_{IH}	2	–	–	V
Logic output voltage LOW (note 2)					
at $\lvert I_O \rvert < 1$ μA	V_{OL}	–	–	50	mV
Logic output voltage HIGH (note 2)					
at $\lvert I_O \rvert < 1$ μA	V_{OH}	V_{DD1}-50	–	–	mV

parameter	symbol	min.	typ.	max.	unit
Logic output voltage LOW (note 2)					
$\overline{MEMEN}$ at I_{OL} = 4 mA	V_{OL}	–	–	1	V
PC2 at I_{OL} = 1,5 mA	V_{OL}	–	–	0,5	V
CLK; OL at I_{OL} = 1 mA	V_{OL}	–	–	0,5	V
XTAL at I_{OL} = 3 mA	V_{OL}	–	–	0,5	V
FB at I_{OL} = 1 mA	V_{OL}	–	–	0,5	V
AB0; AB1; AB2 at I_{OL} = 0,2 mA	V_{OL}	–	–	0,4	V
Logic output voltage HIGH (notes 2 and 3)					
PC2 at $-I_{OH}$ = 1,5 mA	V_{OH}	$V_{DD1}-0,5$	–	–	V
CLK; OL at $-I_{OH}$ = 1 mA	V_{OH}	$V_{DD1}-0,5$	–	–	V
XTAL at $-I_{OH}$ = 3 mA	V_{OH}	$V_{DD1}-1$	–	–	V
FB at $-I_{OH}$ = 1 mA	V_{OH}	$V_{DD2}-1$	–	–	V
AB0; AB1 at I_{OH} = 0,2 mA	V_{OH}	2,4	–	–	V
AB2 at I_{OH} = 0,8 mA	V_{OH}	2,4	–	–	V
Output PC1					
sink current (notes 2, 3 and Fig. 15)	I_O	1	–	–	mA
source current (notes 2, 3 and Fig. 16)	$-I_O$	1	–	–	mA
Internal resistance of phase comparator 1 (notes 2 and 3) locked state |output swing| < 200 mV specified output range: 0,5 V_{DD} –0,5 V to 0,5 V_{DD} + 0,5 V	R_i	–	2,0	–	Ω

A.C. CHARACTERISTICS

A dynamic specification is given for the circuit, built-up with external components as shown in Fig. 14, under the following conditions; for definitions see note 1; V_{DD} = 7,4 ± 0,4 V; T_{amb} = 25 °C; input transition times ⩽ 40 ns; $C_A = C_B = C_C$ = 10 nF; R_A chosen so that I_{RA} = 20 μA ± 1 μA; R_B chosen so that I_{RB} = 3 to 25 μA; R_C chosen so that I_{RC} = 5 to 30 μA; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Main programmable divider (DIV(M); pin 7)					
input frequency all divider ratios (square wave input)	$f_{DIV(M)}$	8,5	–	–	MHz
Reference divider					
input frequency all divider ratios (square wave input)	$f_{DIV(R)}$	9	–	–	MHz
Oscillator frequency (OSC; pin 13)	f_{OSC}	9	12	–	MHz
Input capacitance					
DIV(M); OSC	C_I	–	–	3	pF
DB0 to DB3; PE1; PE2; AB0 to AB2	C_I	–	–	5	pF
Propagation delay (see Fig. 17)					
Feedback output to external prescaler					
DIV(M) → FB at C_L = 10 pF					
HIGH to LOW*	t_{PHL}	–	35	70	ns
LOW to HIGH*	t_{PLH}	–	35	70	ns
Average power supply current (notes 3 and 4)					
in-lock state	I_{DD1}	–	2	–	mA
	I_{DD2}	–	0,15	–	mA
	I_{DD3}	–	0,45	–	mA

* Measured from 30% point of negative-going edge at DIV(M) to 50% point of either output edge of FB.

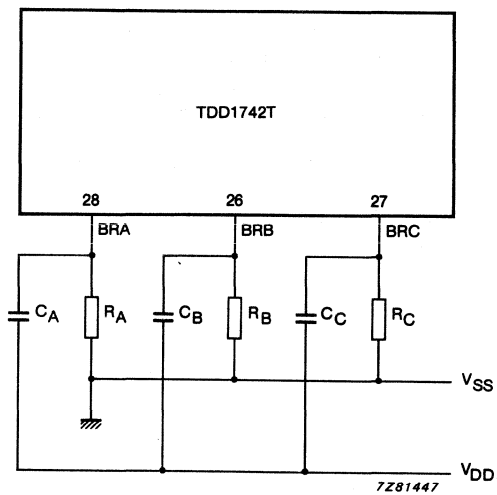


Fig. 14 Test circuit for measuring a.c. characteristics.

Notes to the characteristics

1. Definitions:
   R_A = external biassing resistor between pins BRA and V_{SS}.
   R_B = external biassing resistor between pins BRB and V_{SS}.
   R_C = external biassing resistor between pins BRC and V_{SS}.
   C_A = decoupling capacitor between pins BRA and V_{DD}.
   C_B = decoupling capacitor between pins BRB and V_{DD}.
   C_C = decoupling capacitor between pins BRC and V_{DD}.
   CMOS logic inputs: RESET, OSC.
   CMOS logic outputs: PC2, CLK, OL, XTAL.
   CMOS logic I/O: $\overline{\text{MEMEN}}$.
   TTL logic inputs: DB0 to DB3, PE2, PE1.
   TTL logic output: FB.
   TTL logic I/O: AB0 to AB2.
   Analogue inputs: DIV(M), MOD.
   Analogue output: PC1.
   Analogue biassing pins: BRA, BRB, BRC.
2. All logic inputs at V_{SS} or V_{DD}.
3. R_A connected; its value chosen such that $I_{BRA} = 20\ \mu A$.
   R_B connected; its value chosen such that $I_{BRB} = 20\ \mu A$.
   R_C connected; its value chosen such that $I_{BRC} = 20\ \mu A$.
4. Average power supply current measured at:
   f_{OSC} = 5 MHz, external clock, divider ratio 420;
   $f_{DIV(M)}$ = 2 MHz, divider ratio 168.

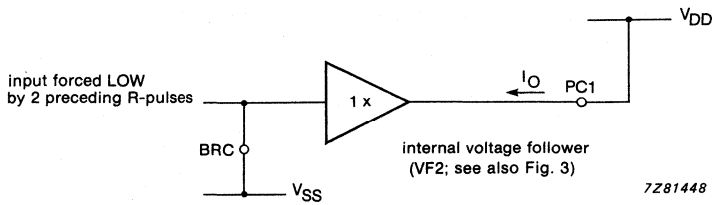


Fig. 15 Equivalent circuit for output PC1 sink current.

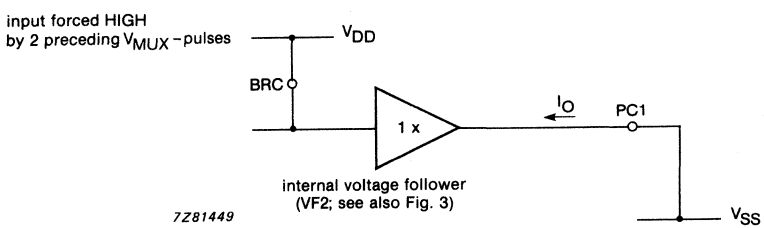


Fig. 16 Equivalent circuit for output PC1 source current.

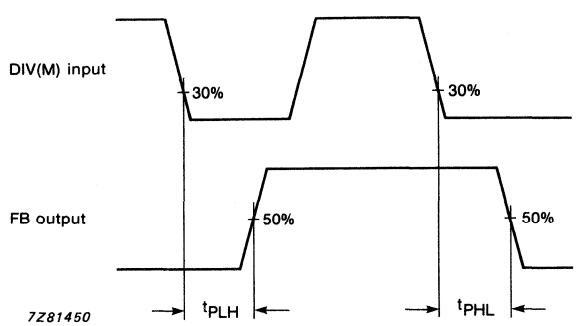


Fig. 17 Waveforms showing propagation delay; DIV (M) → FB.

APPLICATION INFORMATION

Fig. 18 shows a typical application circuit using the TDD1742T in the memory mode with the following design parameters:

Frequency range	150 to 155 MHz
VCO sensitivity	1 MHz/V
Reference frequency	12,5 kHz
Prescaler	÷ 80/81
Reference crystal frequency	5,25 MHz
Reference divider chain	÷ 15; ÷ 7; ÷ 1
Total division ratio	12000 to 12400
Loop bandwidth	300 Hz

APPLICATION INFORMATION (continued)

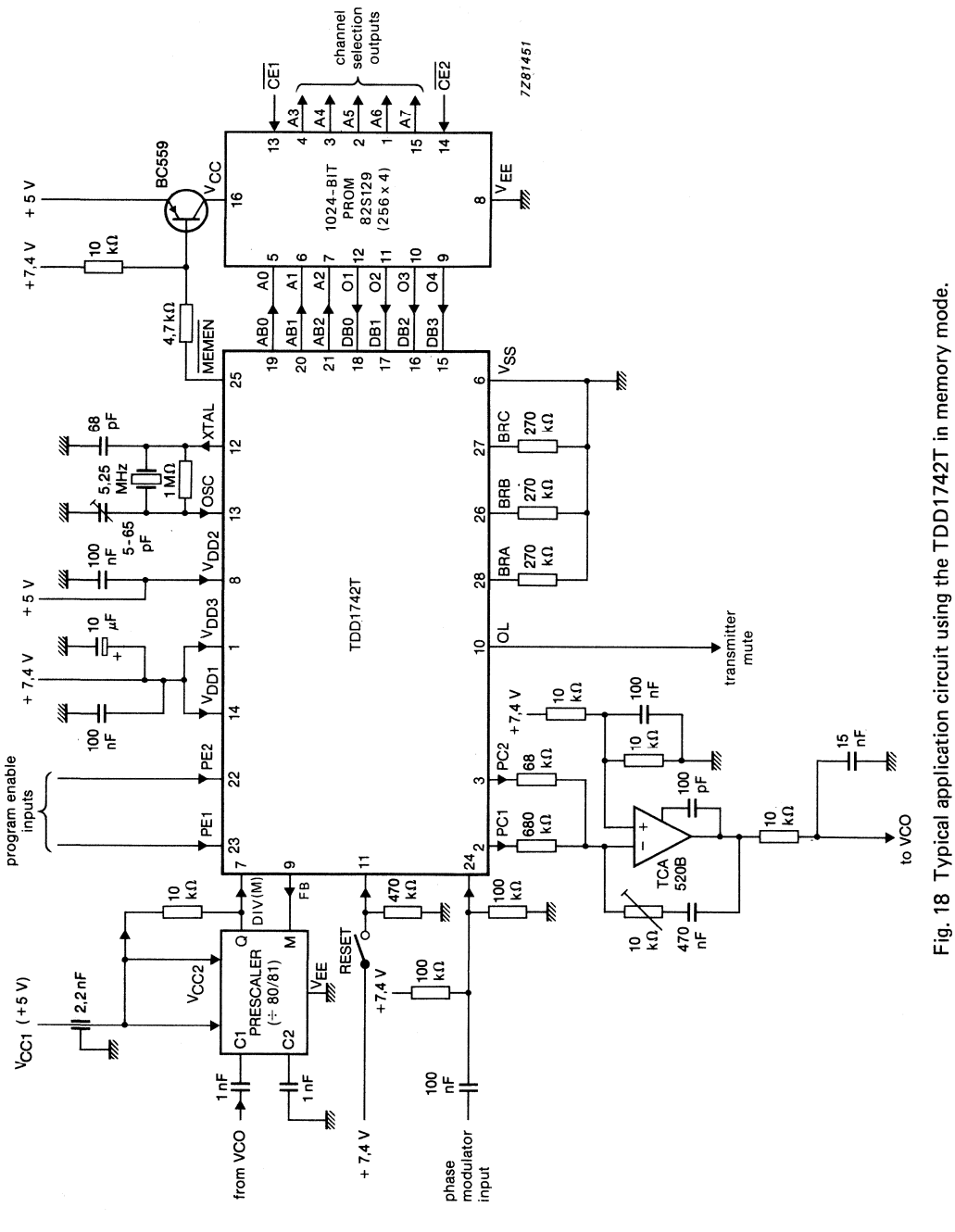


Fig. 18 Typical application circuit using the TDD1742T in memory mode.

Battery low-level indicator TEA1041T

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC11 OR DATA SHEET

FEATURES

- Optical signal following battery low-level detection
- Additional warning ('recharge needed') at end of system operation
- One or two LED indication
- Trigger level adjustable
- Low stand-by current
- Insensitive to interference
- Few external components

APPLICATIONS

- Battery operated systems

GENERAL DESCRIPTION

Intended for use with battery operated systems, the TEA1041T generates an optical alarm via one or two LEDs when the battery supply voltage falls below a preset threshold level.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_p	supply voltage	1.8	-	4.0	V
I_{sb}	stand-by current	-	-	10	µA
P_{tot}	total power dissipation	-	-	150	mW
I_L	output current LED outputs	-	-	59	mA

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA1041T	8	SO8	plastic	SOT96A

FUNCTIONAL DESCRIPTION

Supply (pin 8)

The supply voltage, which may range from 1.8 to 4.0 V, is connected to pin 8.

Voltage sense input (pin 1)

Pin 1 is connected to a trigger circuit consisting of a trigger amplifier and a Schmitt trigger.

An up / down counter in the control and timing logic is enabled when the potential at pin 1 falls below 1.25 V. Unless this voltage increases above 1.25 V the counter will operate for approximately two seconds. When the voltage increases or the count is timed-out, the counter will then begin counting-down. The circuit is thus protected from any disturbance of less than two seconds duration. LED 1 becomes lit on the next occasion that for two seconds the potential on pin 1 is less than 1.25 V.

Following low level detection the circuit is de-activated by operation of S1. For a period of 4 seconds LEDs 1 and 2 will then each be alternately lit for a duration of approximately 500 ms.

LED 1 and LED 2 connections (pin 7, 6)

The cathodes of LEDs 1 and 2 must be connected respectively to pins 7 and 6. The circuit will also function with only LED 1 connected.

Oscillator capacitor connection (pin 4)

Circuit timing is provided by the internal oscillator, the frequency of which is determind by a capacitor connected to pin 4.

Forcing a current (max. 5 mA) into pin 4 permits direct monitoring of the trigger circuit at pins 6 and 7. When V_I is above 1.25 V, pin 7 will be LOW and pin 6 will be HIGH. Alternatively, when V_I is below the 1.25 V threshold level pin 7 will be HIGH while pin 6 will be rendered LOW. This feature facilitates easier circuit adjustment.

Pin 2 Test Pin

An external clock signal may be connected to pin 2 for test purposes. This may be used to shorten the test time (see also test and application information).

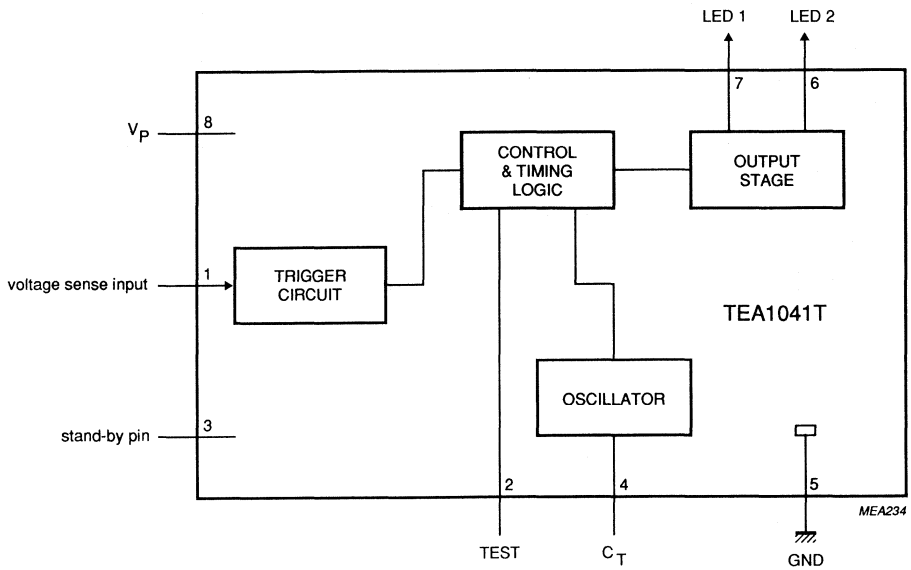


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_I	1	voltage sense input
TEST	2	test pin
V_{sw}	3	stand-by
C_T	4	oscillator capacitor
GND	5	ground
L2	6	LED 2
L1	7	LED 1
V_p	8	supply voltage

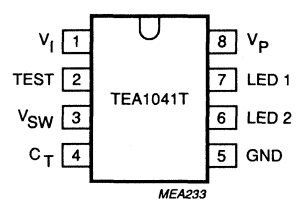


Fig.2 Pin configuration.

VERSATILE TELEPHONE TRANSMISSION CIRCUITS WITH DIALLER INTERFACE

GENERAL DESCRIPTION

The TEA1060 and TEA1061 are bipolar integrated circuits performing all speech, and line interface functions required in fully electronic telephone sets. The circuits internally perform electronic switching between dialling and speech.

Features

- Voltage regulator with adjustable static resistance
- Provides supply for external circuitry
- Symmetrical low-impedance inputs for dynamic and magnetic microphones (TEA1060)
- Symmetrical high-impedance inputs for piezoelectric microphone (TEA1061)
- Asymmetrical high-impedance input for electret microphone (TEA1061)
- DTMF signal input with confidence tone
- Mute input for pulse or DTMF dialling
- Power down input for pulse dial or register recall
- Receiving amplifier for magnetic, dynamic or piezoelectric earpieces
- Large amplification setting range on microphone and earpiece amplifiers
- Line loss compensation facility, line current dependent (microphone and earpiece amplifiers)
- Gain control adaptable to exchange supply
- DC line voltage adjustment facility

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Line voltage	I_{line} = 15 mA	V_{LN}	4.25	4.45	4.65	V
Line current operating range (pin 1)		I_{line}	10	–	140	mA
Internal supply current						
power down input LOW		I_{CC}	–	0.96	1.3	mA
power down input HIGH		I_{CC}	82	55	–	μA
Supply voltage for peripherals	I_{line} = 15 mA; MUTE input HIGH					
	I_P = 1.2 mA	V_{CC}	2.8	3.05	–	V
	I_P = 1.7 mA	V_{CC}	2.5	–	–	V
Voltage gain range						
microphone amplifier						
TEA1060		G_v	44	–	60	dB
TEA1061		G_v	30	–	46	dB
receiving amplifier		G_v	17	–	39	dB
Line loss compensation gain control range		ΔG_v	5.5	5.9	6.3	dB
Exchange supply voltage range		V_{exch}	24	–	60	V
Exchange feeding bridge resistance range		R_{exch}	400	–	1000	Ω
Operating ambient temperature range		T_{amb}	−25	–	+75	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

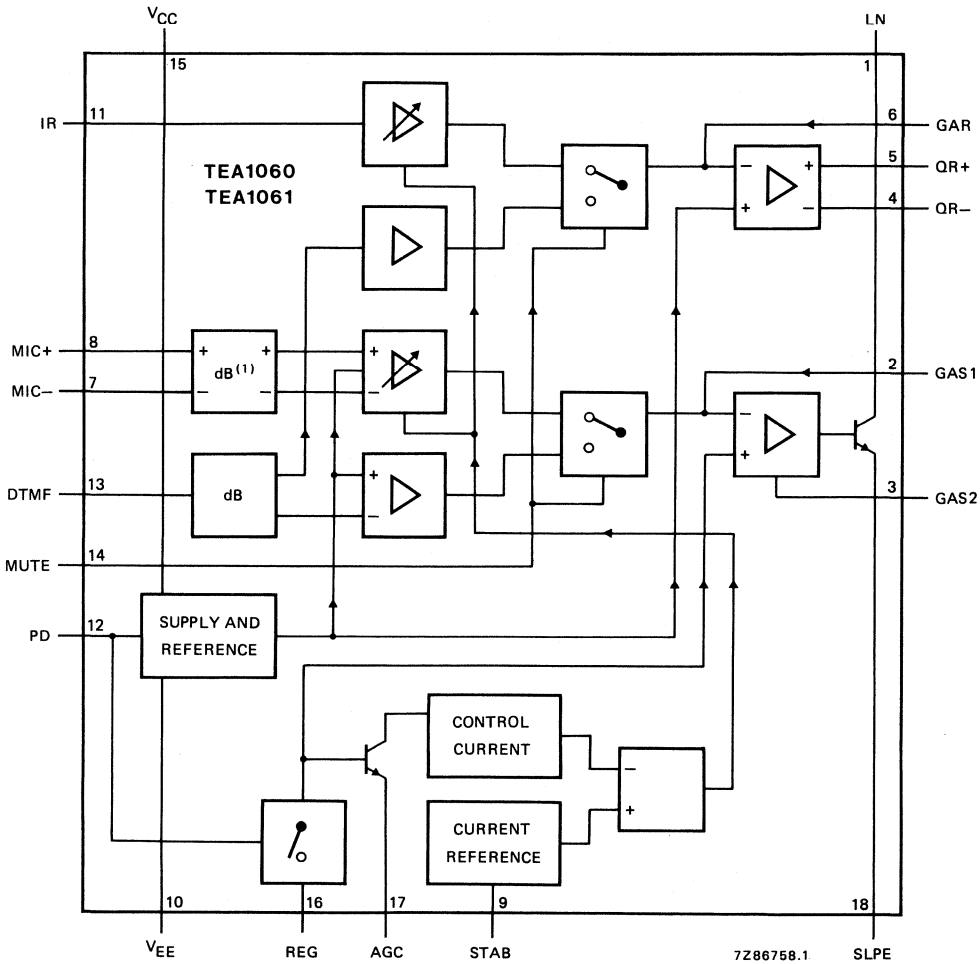


Fig.1 Block diagram.

The blocks marked "dB" are attenuators. The block marked (1) is only present in the TEA1061.

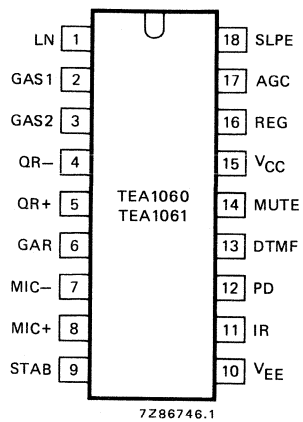


Fig.2 Pinning diagram.

PINNING

1	LN	positive line terminal
2	GAS1	gain adjustment; transmitting amplifier
3	GAS2	gain adjustment; transmitting amplifier
4	QR–	inverting output, receiving amplifier
5	QR+	non-inverting output, receiving amplifier
6	GAR	gain adjustment; receiving amplifier
7	MIC–	inverting microphone input
8	MIC+	non-inverting microphone input
9	STAB	current stabilizer
10	V_{EE}	negative line terminal
11	IR	receiving amplifier input
12	PD	power-down input
13	DTMF	dual-tone multi-frequency input
14	MUTE	mute input
15	V_{CC}	positive supply decoupling
16	REG	voltage regulator decoupling
17	AGC	automatic gain control input
18	SLPE	slope (DC resistance) adjustment

FUNCTIONAL DESCRIPTION

Supply: V_{CC}, LN, SLPE, REG and STAB

The circuit and its peripheral circuits are usually supplied from the telephone line. The circuit develops its own supply voltage at V_{CC} and regulates its voltage drop. The supply voltage V_{CC} may also be used to supply external peripheral circuits, e.g. dialling and control circuits.

The supply has to be decoupled by connecting a smoothing capacitor between V_{CC} and V_{EE}; the internal voltage regulator has to be decoupled by a capacitor from REG to V_{EE}. An internal current stabilizer is set by a resistor of 3.6 kΩ between STAB and V_{EE}.

The DC current flowing into the set is determined by the exchange supply voltage (V_{exch}), the feeding bridge resistance (R_{exch}), the DC resistance ot the subscriber line (R_{line}) and the DC voltage on the subscriber set (see Fig.4).

If the line current (I_{line}) exceeds the current I_{CC} + 0.5 mA required by the circuit itself (I_{CC} ca. 1 mA), plus the current I_P required by the peripheral circuits connected to V_{CC}, then the voltage regulator diverts the excess current via LN.
The voltage regulator adjusts the average voltage on LN to:
$V_{LN} = V_{ref} + I_{SLPE} \times R9 = V_{ref} + (I_{line} - I_{CC} - 0.5 \times 10^{-3} A - I_P) \times R9$.

V_{ref} being an internally generated temperature compensated reference voltage of 4.2 V and R9 being an external resistor connected between SLPE and V_{EE}. The preferred value of R9 is 20 Ω. Changing R9 will have influence on microphone gain, DTMF gain, gain control characteristics, side tone and maximum output swing on LN.
Under normal conditions $I_{SLPE} \geqslant I_{CC}$ + 0.5 mA + I_P. The static behaviour of the circuit then equals a 4.2 V voltage regulator diode with an internal resistance R9. In the audio frequency range the dynamic impedance equals R1. The internal reference voltage can be adjusted by means of an external resistor R_{VA}. This resistor connected between pins 1 and 16 (LN and REG) will decrease the internal reference voltage. R_{VA} connected between pins 16 and 18 (REG and SLPE) will increase the internal reference voltage.

Supply: V_{CC}, LN, SLPE, REG and STAB (continued)

The current Ip available from V_{CC} for supplying peripheral circuits depends on external components and on the line current. Fig.5 shows this current for $V_{CC} > 2.2$ V and for $V_{CC} > 3$ V, of which 3 V is the minimum supply voltage for most CMOS circuits including a diode voltage drop for an enable diode. If MUTE is LOW the available current is further reduced when the receiving amplifier is driven.

Microphone inputs MIC+ and MIC– and gain adjustment connections GAS1 and GAS2

The TEA1060 and TEA1061 have symmetrical microphone inputs.
The TEA1060 is intended for low-sensitivity low-impedance dynamic or magnetic microphones. Its input impedance is 8.2 kΩ (2 x 4.1 kΩ) and its voltage amplification is typ. 52 dB.
The TEA1061 is intended for a piezoelectric microphone or an electret microphone with built-in FET source follower. Its input impedance is 40.8 kΩ (2 x 20.4 kΩ) and its voltage amplification is typ. 38 dB.
The arrangements with the microphone types mentioned are shown in Fig.6.

The gain of the microphone amplifier in both types can be adjusted over a range of + and –8 dB to suit the sensitivity of the transducer used. The gain is proportional to external resistor R7 connected between GAS1 and GAS2.

An external capacitor (C6) of 100 pF between GAS1 and SLPE is required to ensure stability. A larger value may be chosen to obtain a first-order low-pass filter. The cut-off frequency corresponds with the time constant R7 x C6.

Mute input MUTE

A HIGH level at MUTE enables the DTMF input and inhibits the microphone inputs and the receiving amplifier, a LOW level or an open circuit does the reverse. Switching the mute input will cause negligible clicks at the telephone outputs and on the line.

Dual-tone multi-frequency input DTMF

When the DTMF input is enabled, dialling tones may be sent onto the line. The voltage gain from DTMF to LN is typ. 25.5 dB and varies with R7 in the same way as the gain of the microphone amplifier. The signalling tones can be heard in the earpiece at a low level (confidence tone).

Receiving amplifier: IR, QR+, QR– and GAR

The receiving amplifier has one input IR and two complementary outputs, a non-inverting output QR+ and an inverting output QR–. These outputs may be used for single-ended or for differential drive, depending on the sensitivity and type of earpiece used (see Fig.7). The gain from IR to QR+ is typ. 25 dB. This will be sufficient for low-impedance magnetic or dynamic earpieces; these are suited for single-ended drive. By using both outputs (differential drive) the gain is increased by 6 dB and differential drive becomes possible.
This feature can be used in case the earpiece impedance exceeds 450 Ω (high-impedance dynamic, magnetic or piezoelectric earpieces).

The output voltage of the receiving amplifier is specified for continuous-wave drive. The maximum output voltage will be higher under speech conditions, where the ratio of peak and RMS value is higher.

The gain of the receiving amplifier can be adjusted over a range of + and –8 dB to suit the sensitivity of the transducer used. The gain is proportional to external resistor R4 connected from GAR to QR+.

Two external capacitors C4 = 100 pF and C7 = 10 x C4 = 1 nF are necessary to ensure stability.
A larger value of C4 may be chosen to obtain a first-order low-pass filter. The "cut-off" frequency corresponds with the time constant R4 x C4.

Automatic gain control input AGC

Automatic line loss compensation will be obtained by connecting a resistor R6 from AGC to V_{EE}. This automatic gain control varies the gain of the microphone amplifier and the receiving amplifier in accordance with the DC line current. The control range is 6 dB. This corresponds with a line length of 5 km for a 0.5 mm diameter copper twisted-pair cable with a DC resistance of 176 Ω/km and an average attenuation of 1.2 dB/km.

Resistor R6 should be chosen in accordance with the exchange supply voltage and its feeding bridge resistance (see Fig.8 and Table 1). Different values of R6 give the same ratio of line currents for begin and end of the control range. If automatic line loss compensation is not required AGC may be left open. The amplifiers then all give their maximum gain as specified.

Power-down input PD

During pulse dialling or register recall (timed loop break) the telephone line is interrupted, as a consequence it provides no supply for the transmission circuit and the peripherals connected to V_{CC}. These gaps have to be bridged by the charge in the smoothing capacitor C1. The requirements on this capacitor are relaxed by applying a HIGH level to the PD input during the time of the loop break, which reduces the supply current from typ. 1 mA to typ. 55 μA.

A HIGH level at PD further disconnects the capacitor at REG, with the effect that the voltage stabilizer will have no switch-on delay after line interruptions. This results in no contribution of the IC to the current waveform during pulse dialling or register recall.
When this facility is not required PD may be left open.

Side-tone suppression

Suppression of the transmitted signal in the earpiece is obtained by the antiside-tone network consisting of $R1//Z_{line}$, R2, R3, R8 and Z_{bal} (see Fig.11). Maximum compensation is obtained when the following conditions are fulfilled:

$$a)\ R9.R2 = R1[R3 + (R8//Z_{bal})]$$

$$b)\ [Z_{bal}/(Z_{bal} + R8)] = [Z_{line}/(Z_{line} + R1)]$$

If fixed values are chosen for R1, R2, R3 and R9, then condition a) will always be fulfilled provided that $|R8//Z_{bal}| \ll R3$.

To obtain optimum side-tone-suppression, condition (b) has to be fulfilled resulting in:

$$Z_{bal} = (R8/R1)Z_{line} = k.Z_{line}$$

where k is a scale factor; $k = (R8/R1)$

Scale factor k (value of R8) must be chosen to meet the following criteria:

- compatibility with a standard capacitor from the E6 or E12 range for Z_{bal}
- $|Z_{bal}//R8| \ll R3$
- $|Z_{bal} + R8| \gg R9$

In practice Z_{line} varies strongly with line length and cable type; consequently an average value has to be chosen for Z_{bal}. The suppression further depends on the accuracy with which Z_{bal} equals the average line impedance.

The anti-side-tone network as used in the standard application (Fig.11) attenuates the signal from the line with 32 dB. The attenuation is nearly flat over the audio-frequency range.
Instead of the above described special bridge, the conventional Wheatstone bridge configuration can be used as an alternative anti-side tone circuit. Both bridges can be used with either a resistive set impedance or with a complex set impedance.

RATINGS

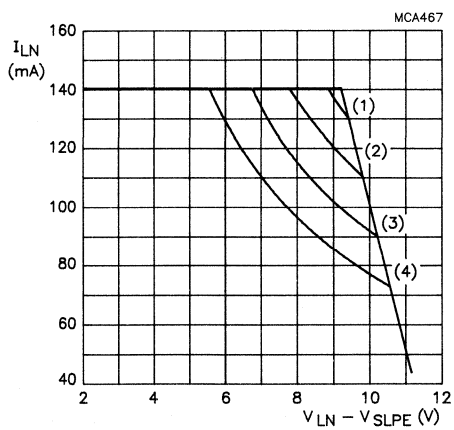
Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Positive continuous line voltage		V_{LN}	–	12	V
Repetitive line voltage during switch-on or line interruption		V_{LN}	–	13.2	V
Repetitive peak line voltage for a 1 ms pulse per 5 s	R10 = 13 Ω; R9 = 20 Ω; (see Fig.11)	V_{LN}	–	28	V
Line current TEA1060 (1)	R9 = 20 Ω	I_{line}	–	140	mA
Line current TEA1061 (1)	R9 = 20 Ω	I_{line}	–	140	mA
Voltage on all other pins		V_i	–	$V_{CC}+0.7$	V
		$-V_i$	–	0.7	V
Total power dissipation (2)		P_{tot}	–	769	mW
Storage temperature range		T_{stg}	−40	+125	°C
Operating ambient temperature range		T_{amb}	−25	+75	°C
Junction temperature		T_j	–	+125	°C

1. Mostly dependent on the maximum required T_{amb} and the voltage between LN and SLPE (see Fig.3).
2. Calculated for the maximum ambient temperature specified T_{amb} = 75 °C and a maximum junction temperature of 125 °C.

THERMAL RESISTANCE

From junction to ambient in free air
TEA1060 and TEA1061 $R_{th\ j\text{-}a}$ = 65 K/W



	T_{amb}	P_{tot}
(1)	45 °C	1231 mW
(2)	55 °C	1077 mW
(3)	65 °C	923 mW
(4)	75 °C	769 mW

Fig.3 TEA1060/1061 safe operating area.

CHARACTERISTICS

I_{line} = 10 to 140 mA; V_{EE} = 0 V; f = 800 Hz; T_{amb} = 25 °C, R9 = 20 Ω; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply: LN and V_{CC} (pins 1 and 15)						
Voltage drop over circuit	I_{line} = 5 mA	V_{LN}	3.95	4.25	4.55	V
	I_{line} = 15 mA	V_{LN}	4.25	4.45	4.65	V
	I_{line} = 100 mA	V_{LN}	5.4	6.1	6.7	V
	I_{line} = 140 mA	V_{LN}	–	–	7.5	V
Variation with temperature	I_{line} = 15 mA	$\Delta V_{LN}/\Delta T$	−4	−2	0	mV/K
Voltage drop over circuit	I_{line} = 15 mA; $R_{VA} = R_{1\text{-}16}$ = 68 kΩ	V_{LN}	3.5	3.8	4.05	V
	I_{line} = 15 mA; $R_{VA} = R_{16\text{-}18}$ = 39 kΩ	V_{LN}	4.7	5.0	5.3	V
Supply current	PD = LOW; V_{CC} = 2.8 V	I_{CC}	–	0.96	1.30	mA
	PD = HIGH; V_{CC} = 2.8 V	I_{CC}	–	55	82	μA
Supply voltage available for peripheral circuits	I_{line} = 15 mA; MUTE = HIGH; I_P = 0 mA	V_{CC}	3.5	3.75	–	V
	I_P = 1.2 mA	V_{CC}	2.8	3.05	–	V
Microphone inputs MIC+ and MIC− (pins 7 and 8)						
Input impedance						
TEA1060		$\lvert Z_i \rvert$	3.3	4.1	4.9	kΩ
TEA1061		$\lvert Z_i \rvert$	16.5	20.4	24.5	kΩ
Common-mode rejection ratio						
TEA1060		k_{CMR}	–	82	–	dB
Voltage gain	I_{line} = 15 mA; R7 = 68 kΩ					
TEA1060		G_v	51	52	53	dB
TEA1061		G_v	37	38	39	dB
Variation with frequency referred to 800 Hz	f = 300 and 3400 kHz	ΔG_{vf}	−0.5	±0.2	+0.5	dB
Variation with temperature referred to +25 °C	I_{line} = 50 mA; T_{amb} = −25 and +75 °C	ΔG_{vT}	–	±0.2	–	dB

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Dual-tone multi-frequency input DTMF (pin 13)						
Input impedance		$\|Z_i\|$	16.8	20.7	24.6	kΩ
Voltage gain	I_{line} = 15 mA; R7 = 68 kΩ	G_v	24.5	25.5	26.5	dB
Variation with frequency referred to 800 Hz	f = 300 and 3400 kHz	ΔG_{vf}	−0.5	±0.2	+0.5	dB
Variation with temperature referred to 800 Hz	I_{line} = 50 mA; T_{amb} = −25 and +75 °C	ΔG_{vT}	−	±0.2	−	dB
Gain adjustment GAS1 and GAS2 (pins 2 and 3)						
Gain variation with R7 connected between pins 2 and 3; transmitting amplifier		ΔG_v	−8	−	+8	dB
Transmitting amplifier output LN (pin 1)						
Output voltage	I_{line} = 15 mA; d_{tot} = 2%	$V_{LN(rms)}$	1.9	2.3	−	V
	d_{tot} = 10%	$V_{LN(rms)}$	−	2.6	−	V
Noise output voltage	I_{line} = 15 mA; R7 = 68 kΩ; pins 7 and 8 open circuit psophometrically weighted (P53 curve)	$V_{no(rms)}$	−	−70	−	dBmp
Receiving amplifier input IR (pin 11)						
Input impedance		$\|Z_i\|$	17	21	25	kΩ
Receiving amplifier outputs QR+ and QR− (pins 4 and 5)						
Output impedance; single-ended		$\|Z_o\|$	−	4	−	Ω
Voltage gain from pin 11 to pin 4 or 5	I_{line} = 15 mA; R4 = 100 kΩ					
single-ended	R_L = 300 Ω	G_v	24	25	26	dB
differential	R_L = 600 Ω	G_v	30	31	32	dB

parameter	conditions	symbol	min.	typ.	max.	unit
Variation with frequency referred to 800 Hz	f = 300 and 3400 Hz	ΔG_{vf}	−0.5	±0.2	+0.5	dB
Variation with temperature referred to 800 Hz	I_{line} = 15 mA T_{amb} = −25 and +75 °C	ΔG_{vT}	–	±0.2	–	dB
Output voltage	I_P = 0 mA; d_{tot} = 2%;					
sine-wave drive	R4 = 100 kΩ					
single-ended	R_L = 150 Ω	$V_{o(rms)}$	0.3	0.38	–	V
single-ended	R_L = 450 Ω	$V_{o(rms)}$	0.4	0.52	–	V
differential	C_L = 47 nF					
R_{series} = 100 Ω	f = 3400 Hz	$V_{o(rms)}$	0.8	1.0	–	V
Noise output voltage	I_{line} = 15 mA; R4 = 100 kΩ; pin 11 open circuit psophometrically weighted (P53 curve)					
single-ended	R_L = 300 Ω	$V_{no(rms)}$	–	50	–	μV
differential	R_L = 600 Ω	$V_{no(rms)}$	–	100	–	μV
Gain adjustment GAR (pin 6)						
Gain variation with R4 connected between pins 6 and 5; receiving amplifier		ΔG_v	−8	–	+8	dB
MUTE input (pin 14)						
Input voltage HIGH		V_{IH}	1.5	–	V_{CC}	V
Input voltage LOW		V_{IL}	–	–	0.3	V
Input current		I_{MUTE}	–	8	15	μA
Reduction of voltage gain from MIC+ and MIC− to LN	MUTE = HIGH	ΔG_v	–	70	–	dB
Voltage gain from DTMF to QR+ or QR−	MUTE = HIGH R4 = 100 kΩ					
single-ended load	R_L = 300 Ω	G_v	−21	−19	−17	dB
Power-down input PD (pin 12)						
Input voltage HIGH		V_{IH}	1.5	–	V_{CC}	V
Input voltage LOW		V_{IL}	–	–	0.3	V
Input current		I_{PD}	–	5	10	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Automatic gain control input AGC (pin 17)						
Controlling the gain from IR to QR+/QR− and the gain from MIC+/MIC− to LN; R6 = 110 kΩ (connected between pins 17 and 10)						
Gain control range	I_{line} = 70 mA	$-\Delta G_v$	5.5	5.9	6.3	dB
Highest line current for maximum gain		I_{line}	–	23	–	mA
Lowest line current for lowest gain		I_{line}	–	61	–	mA
Reduction of gain between I_{line} = 15 mA and I_{line} = 35 mA		$-\Delta G_v$	1.0	1.5	2.0	dB

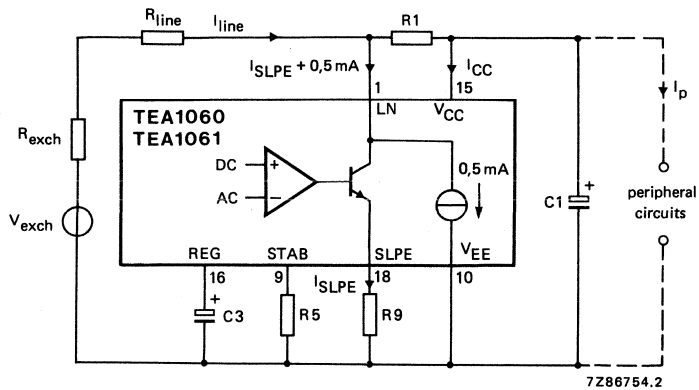
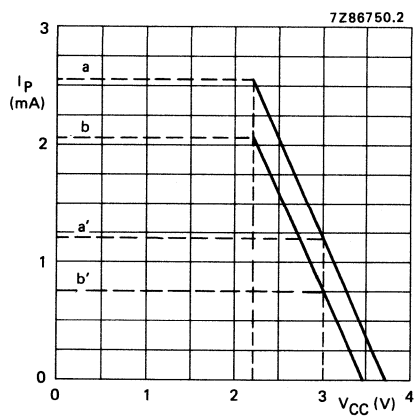


Fig.4 Supply arrangement.



I_{line} = 15 mA at
V_{LN} = 4.45 V;
R1 = 620 Ω, R9 = 20 Ω

Fig.5 Maximum current I_P available from V_{CC} for external (peripheral) circuitry with $V_{CC} > 2.2$ V and $V_{CC} > 3$ V. Curves (a) and (a') are valid when the receiving amplifier is not driven or when MUTE = HIGH. Curves (b) and (b') are valid when MUTE = LOW and the receiving amplifier is driven. $V_{o(rms)}$ = 150 mV, R_L = 150 Ω (asymmetrical).

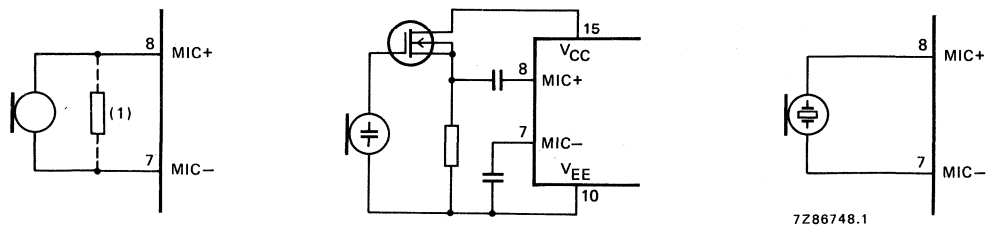


Fig.6 Alternative microphone arrangements: (a) magnetic or dynamic microphone for TEA1060, the resistor marked (1) may be connected to lower the terminating impedance, (b) electret microphone and (c) piezoelectric microphone for TEA1061.

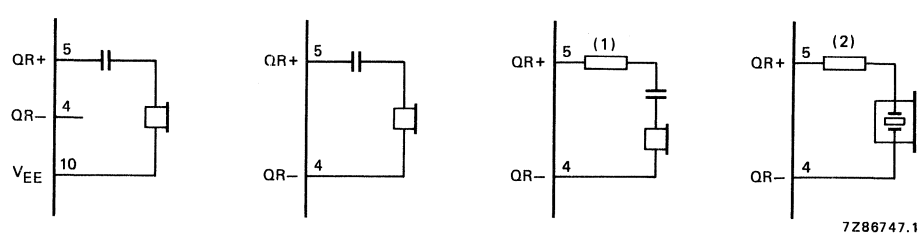


Fig.7 Alternative receiver arrangements: (a) dynamic earpiece with less than 450 Ω impedance, (b) dynamic earpiece with more than 450 Ω impedance, (c) magnetic earpiece. The resistor marked (1) may be connected to prevent distortion [inductive load (d)] piezoelectric earpiece. The resistor marked (2) is required to increase the phase margin (capacitive load).

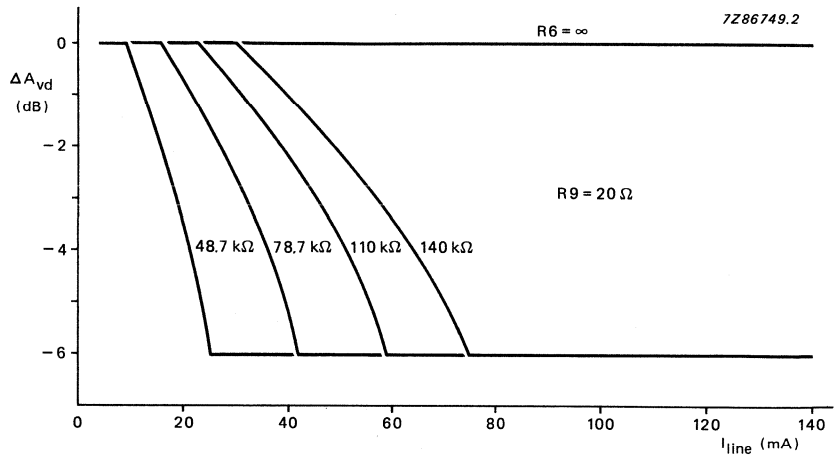


Fig.8 Variation of gain with line current with R6 as a parameter.

Table 1 Values of resistor R6 for optimum line loss compensation, for various usual values of exchange supply voltage V_{exch} and exchange feeding bridge resistance R_{exch}; R9 = 20 Ω.

		R_{exch} (Ω)			
		400	600	800	1000
		R6 (kΩ)			
V_{exch} (V)	24	61.9	48.7	X	X
	36	100	78.7	68	60.4
	48	140	110	93.1	82
	60	X	X	120	102

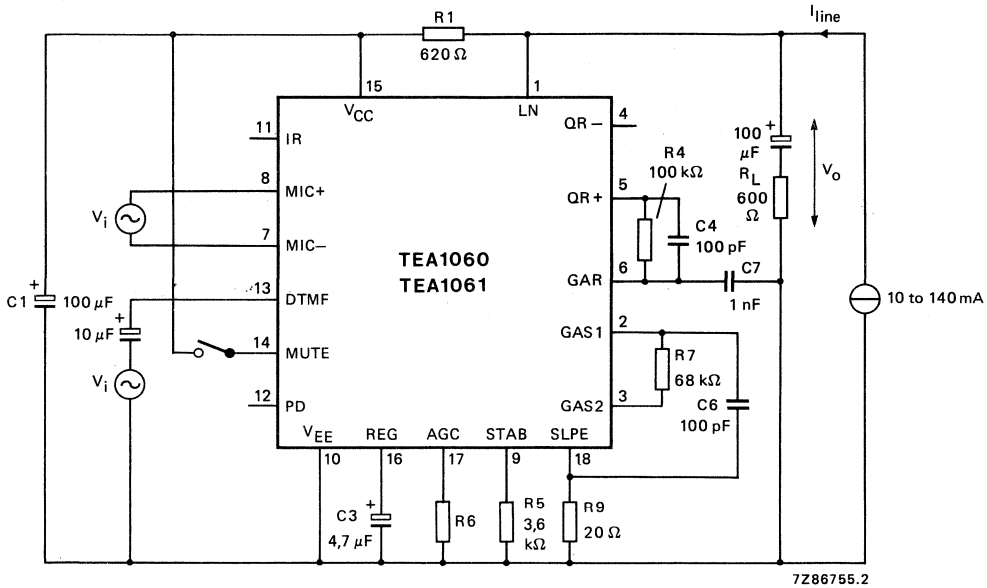


Fig.9 Test circuit for defining voltage gain of MIC+, MIC– and DTMF inputs. Voltage gain is defined as; $G_v = 20 \log |V_o/V_i|$. For measuring the gain from MIC+ and MIC– the MUTE input should be LOW or open circuit. For measuring the DTMF input MUTE should be HIGH. Inputs not under test should be open circuit.

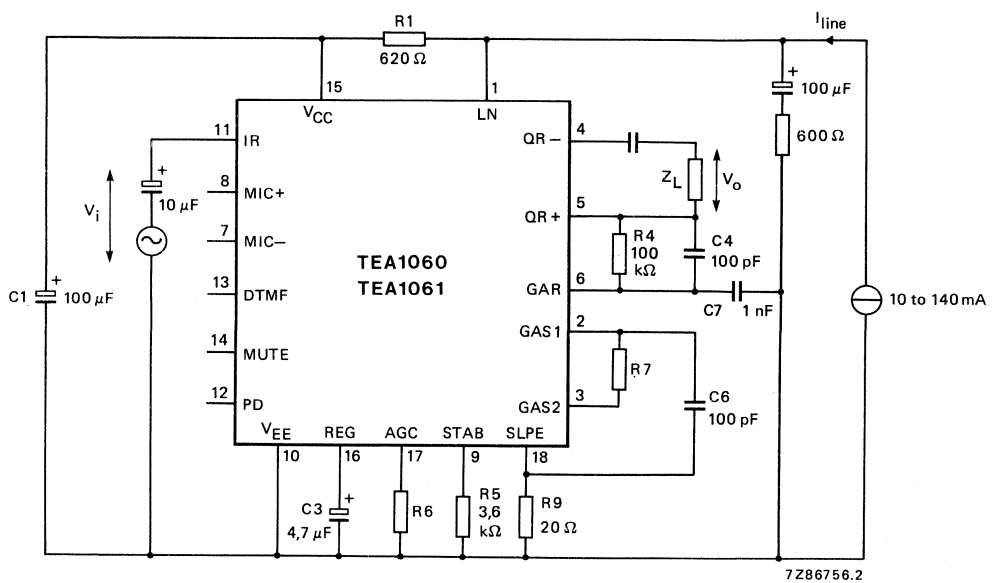


Fig.10 Test circuit for defining voltage gain of the receiving amplifier. Voltage gain is defined as; $G_v = 20 \log |V_o/V_i|$.

APPLICATION INFORMATION

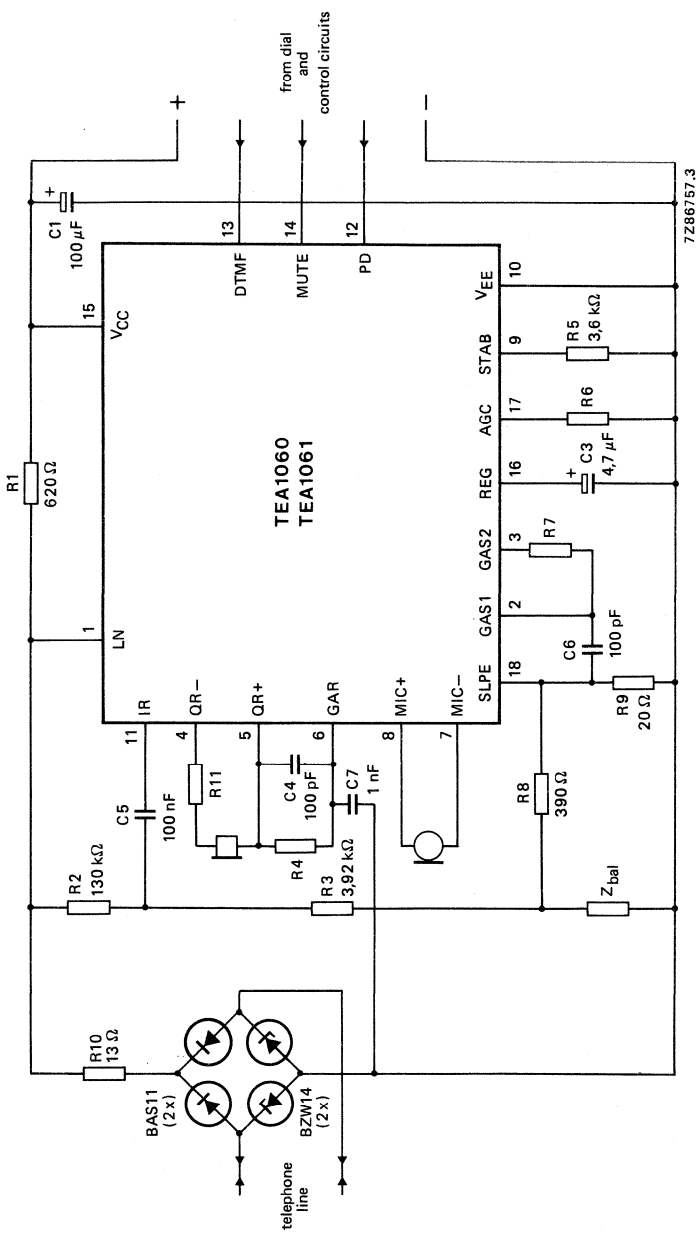


Fig.11 Typical application of the TEA1060 or TEA1061, shown here with a piezoelectric earpiece and DTMF dialling. The bridge to the left and R10 limit the current into the circuit and the voltage across the circuit during line transients. Pulse dialling or register recall require a different protection arrangement.

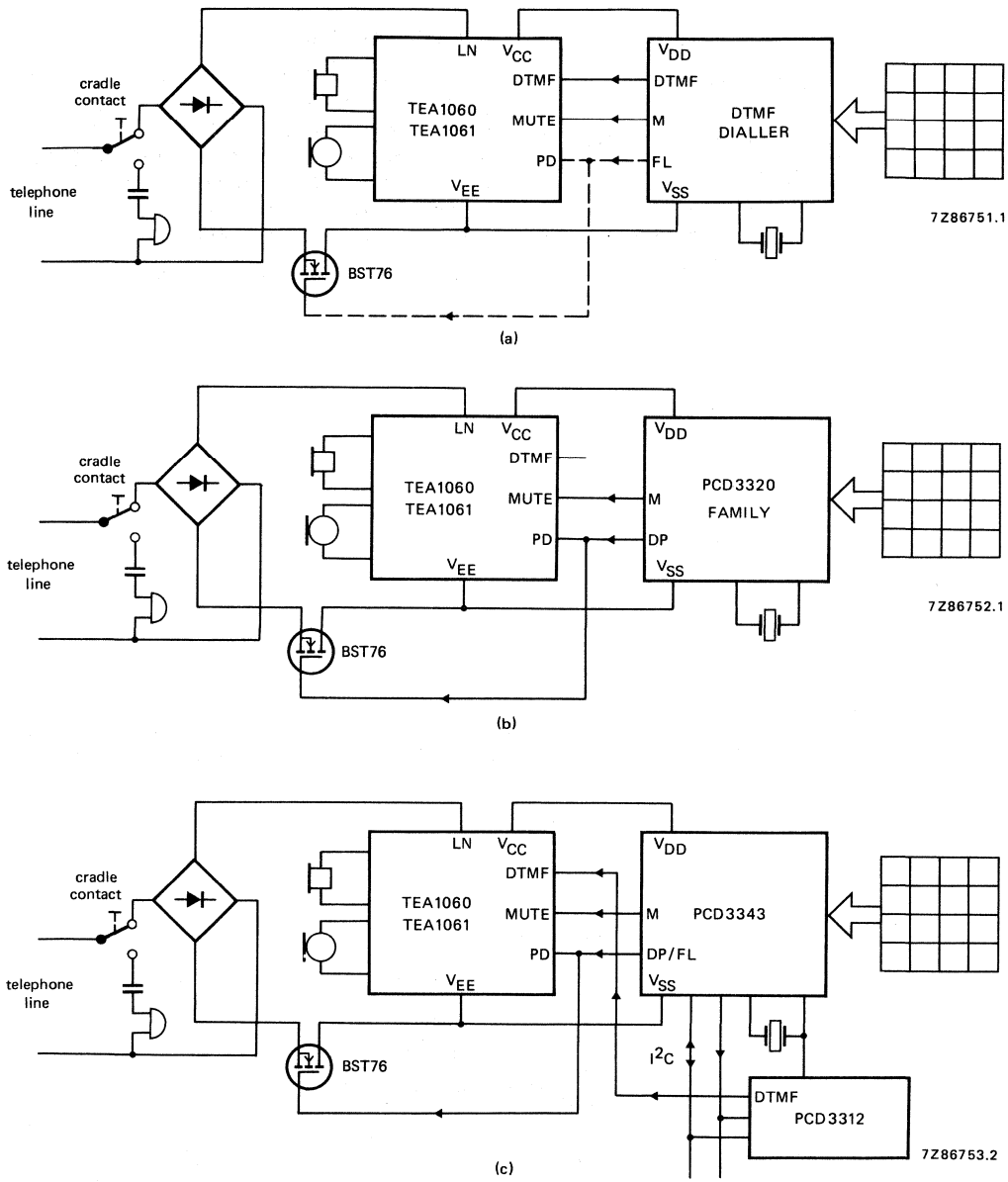


Fig.12 Typical applications of the TEA1060 or TEA1061 (simplified): (a) DTMF set with a CMOS DTMF dialling circuit, the dashed lines show an optional flash (register recall by timed loop break); (b) Pulse dial set with the one of the PCD3320 family of CMOS interrupted current-loop dialling circuits; (c) Dual-standard (pulse and DTMF) feature phone with the PCD3343 CMOS telephone controller and the PCD3312 CMOS DTMF generator with I^2C-bus.

Low voltage versatile telephone transmission circuits with dialler interface

TEA1062; TEA1062A

FEATURES

- Low DC line voltage; operates down to 1.6 V (excluding polarity guard)
- Voltage regulator with adjustable static resistance
- Provides a supply for external circuits
- Symmetrical high-impedance inputs (64 kΩ) for dynamic, magnetic or piezo-electric microphones
- Asymmetrical high-impedance input (32 kΩ) for electret microphones
- DTMF signal input with confidence tone
- Mute input for pulse or DTMF dialling (TEA1062)
- $\overline{\text{Mute}}$ input for pulse or DTMF dialling (TEA1062A)
- Receiving amplifier for dynamic, magnetic or piezo-electric earpieces
- Large gain setting ranges on microphone and earpiece amplifiers
- Line loss compensation (line current dependent) for microphone and earpiece amplifiers
- Gain control curve adaptable to exchange supply
- DC line voltage adjustment facility.

GENERAL DESCRIPTION

The TEA1062 and TEA1062A are bipolar integrated circuits that perform all speech and line interface functions required in fully electronic telephone sets. They perform electronic switching between dialling and speech. The ICs operate at line voltage down to 1.6 V DC (with reduced performance) to facilitate the use of more telephone sets connected in parallel.

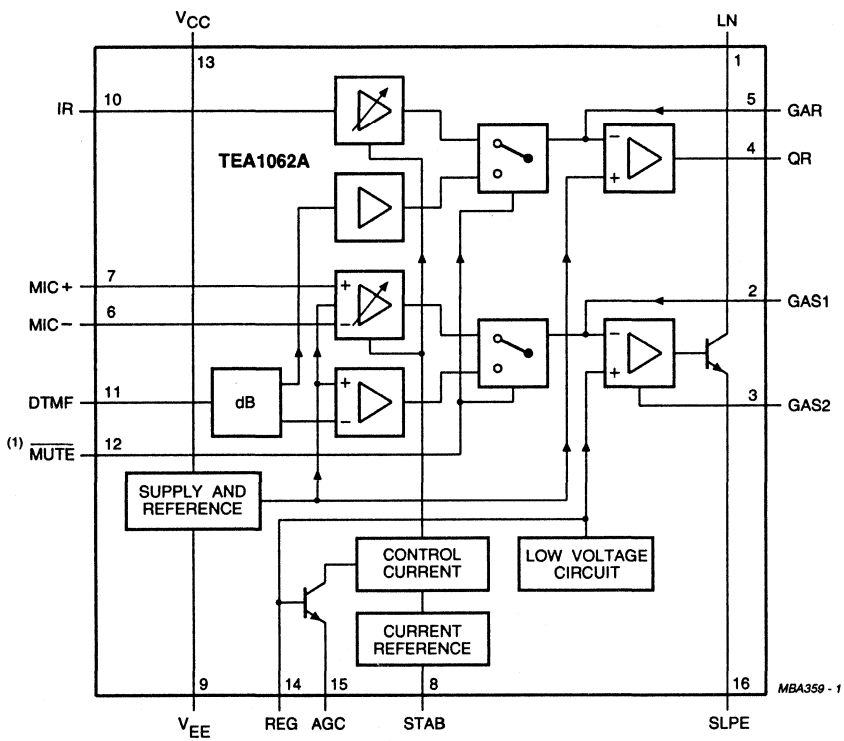
All statements and values refer to all versions unless otherwise specified.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{LN}	line voltage	I_{line} = 15 mA	3.55	4.0	4.25	V
I_{line}	line current operating range					
	normal operation		11	–	140	mA
	with reduced performance		1	–	11	mA
I_{CC}	internal supply current		–	0.9	–	mA
V_{CC}	supply for peripherals	I_{line} = 15 mA				
	TEA1062	I_p = 1.2 mA; MUTE = HIGH	2.2	2.7	–	V
		I_p = 0 mA; MUTE = HIGH	–	3.4	–	V
	TEA1062A	I_p = 1.2 mA; $\overline{\text{MUTE}}$ = LOW	2.2	2.7	–	V
		I_p = 0 mA; $\overline{\text{MUTE}}$ = LOW	–	3.4	–	V
G_v	voltage gain range					
	microphone amplifier		44	–	52	dB
	receiving amplifier		20	–	31	dB
	line loss compensation range					
ΔG_v	gain control		–	5.8	–	dB
V_{exch}	exchange supply voltage		36	–	60	V
R_{exch}	exchange feeding bridge resistance		0.4	–	1	kΩ
T_{amb}	operating ambient temperature		–25	–	+75	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA1062	16	DIL	plastic	SOT38
TEA1062A	16	DIL	plastic	SOT38
TEA1062T	16	SO	plastic	SOT109A
TEA1062AT	16	SO	plastic	SOT109A



(1) Pin 12 is active HIGH (MUTE) for TEA1062.

Fig.1 Block diagram for TEA1062A.

SYMBOL	PIN	DESCRIPTION
LN	1	positive line terminal
GAS1	2	gain adjustment; transmitting amplifier
GAS2	3	gain adjustment; transmitting amplifier
QR	4	non-inverting output; receiving amplifier
GAR	5	gain adjustment; receiving amplifier
MIC–	6	inverting microphone input
MIC+	7	non-inverting microphone input
STAB	8	current stabilizer
V_{EE}	9	negative line terminal
IR	10	receiving amplifier input
DTMF	11	dual-tone multi-frequency input
$\overline{MUTE}$	12	mute input (see note 1)
V_{CC}	13	positive supply decoupling
REG	14	voltage regulator decoupling
AGC	15	automatic gain control input
SLPE	16	slope (DC resistance) adjustment

PINNING

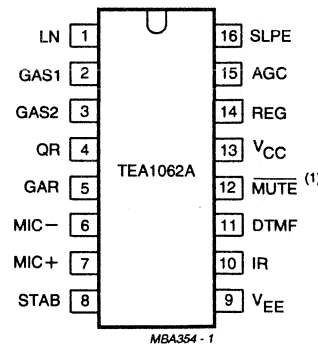


Fig.2 Pin configuration for TEA1062A.

Note to Fig.2 and pinning description

1. Pin 12 is active HIGH (MUTE) for TEA1062.

FUNCTIONAL DESCRIPTION

Supplies V_{CC}, LN, SLPE, REG and STAB

Power for the IC and its peripheral circuits is usually obtained from the telephone line. The supply voltage is derived from the line via a dropping resistor and regulated by the IC. The supply voltage V_{CC} may also be used to supply external circuits e.g. dialling and control circuits.

Decoupling of the supply voltage is performed by a capacitor between V_{CC} and V_{EE}. The internal voltage regulator is decoupled by a capacitor between REG and V_{EE}.

The DC current flowing into the set is determined by the exchange supply voltage V_{exch}, the feeding bridge resistance R_{exch} and the DC resistance of the telephone line R_{line}.

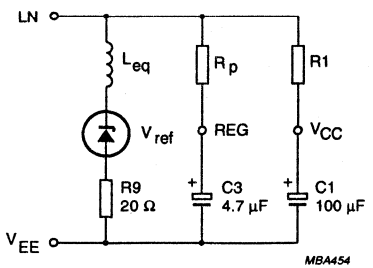
The circuit has an internal current stabilizer operating at a level determined by a 3.6 kΩ resistor connected between STAB and V_{EE} (see Fig.8). When the line current (I_{line}) is more than 0.5 mA greater than the sum of the IC supply current (I_{CC}) and the current drawn by the peripheral circuitry connected to V_{CC} (I_p) the excess current is shunted to V_{EE} via LN.

The regulated voltage on the line terminal (V_{LN}) can be calculated as:

$V_{LN} = V_{ref} + I_{SLPE} \times R9$ or;

$V_{LN} = V_{ref} + \{(I_{line} - I_{CC} - 0.5 \times 10^{-3}\ A) - I_p\} \times R9$

V_{ref} is an internally generated temperature compensated reference voltage of 3.7 V and R9 is an external resistor connected between SLPE and V_{EE}.
In normal use the value of R9 would be 20 Ω.
Changing the value of R9 will also affect microphone gain, DTMF gain, gain control characteristics, sidetone level, maximum output swing on LN and the DC characteristics (especially at the lower voltages).



L_{eq} = C3 x R9 x R_p
R_p = 16.2 kΩ

Fig.3 Equivalent impedance circuit.

Under normal conditions, when $I_{SLPE} >> I_{CC}$ + 0.5 mA + I_p, the static behaviour of the circuit is that of a 3.7 V regulator diode with an internal resistance equal to that of R9. In the audio frequency range the dynamic impedance is largely determined by R1. Fig.3 shows the equivalent impedance of the circuit.

At line currents below 9 mA the internal reference voltage is automatically adjusted to a lower value (typically 1.6 V at 1 mA). This means that more sets can be operated in parallel with DC line voltages (excluding the polarity guard) down to an absolute minimum voltage of 1.6 V. At line currents below 9 mA the circuit has limited sending and receiving levels. The internal reference voltage can be adjusted by means of an external resistor (R_{VA}). This resistor when connected between LN and SLPE will decrease the internal reference voltage and when connected between REG and SLPE will increase the internal reference voltage.

Current (I_p) available from V_{CC} for peripheral circuits depends on the external components used. Fig.9 shows this current for V_{CC} > 2.2 V. If MUTE is LOW (TEA1062) or $\overline{\text{MUTE}}$ is HIGH (TEA1062A) when the receiving amplifier is driven, the available current is further reduced. Current availability can be increased by connecting the supply IC (TEA1081) in parallel with R1 as shown in Figures 18(c) and 19(c), or by increasing the DC line voltage by means of an external resistor (R_{VA}) connected between REG and SLPE.

Microphone inputs MIC+ and MIC– and gain pins GAS1 and GAS2

The circuit has symmetrical microphone inputs. Its input impedance is 64 kΩ (2 x 32 kΩ) and its voltage gain is typicallly 52 dB (when R7 = 68 kΩ, see Figures 13 and 14). Dynamic, magnetic, piezo-electric or electret (with built-in FET source followers) can be used. Microphone arrangements are illustrated in Fig.10.

The gain of the microphone amplifier can be adjusted between 44 dB and 52 dB to suit the sensitivity of the transducer in use. The gain is proportional to the value of R7 which is connected between GAS1 and GAS2.

Stability is ensured by two external capacitors, C6 connected between GAS1 and SLPE and C8 connected between GAS1 and V_{EE}. The value of C6 is 100 pF but this may be increased to obtain a first-order low-pass filter. The value of C8 is 10 times the value of C6. The cut-off frequency corresponds to the time constant R7 x C6.

Mute input MUTE (TEA1062)

When MUTE is HIGH the DTMF input is enabled and the microphone and receiving amplifier inputs are inhibited. The reverse is true when MUTE is LOW or open-circuit. MUTE switching causes only negligible clicking on the line and earpiece output. If the number of parallel sets in use causes a drop in line current to below 6 mA the speech amplifiers remain active independent to the DC level applied to the MUTE input.

Mute input $\overline{\text{MUTE}}$ (TEA1062A)

When $\overline{\text{MUTE}}$ is LOW or open-circuit, the DTMF input is enabled and the microphone and receiving amplifier inputs are inhibited. The reverse is true when $\overline{\text{MUTE}}$ is HIGH. $\overline{\text{MUTE}}$ switching causes only negligible clicking on the line and earpiece output. If the number of parallel sets in use causes a drop in line current to below 6 mA the DTMF amplifier becomes active independent to the DC level applied to the $\overline{\text{MUTE}}$ input.

Dual-tone multi-frequency input DTMF

When the DTMF input is enabled dialling tones may be sent on to the line. The voltage gain from DTMF to LN is typically 25.5 dB (when R7 = 68 kΩ) and varies with R7 in the same way as the microphone gain. The signalling tones can be heard in the earpiece at a low level (confidence tone).

Receiving amplifier IR, QR and GAR

The receiving amplifier has one input (IR) and a non-inverting output (QR). Earpiece arrangements are illustrated in Fig.11. The IR to QR gain is typically 31 dB (when R4 = 100 kΩ). It can be adjusted between 20 and 31 dB to match the sensitivity of the transducer in use. The gain is set with the value of R4 which is connected between GAR and QR. The overall receive gain, between LN and QR, is calculated by subtracting the anti-sidetone network attenuation (32 dB) from the amplifier gain. Two external capacitors, C4 and C7, ensure stability. C4 is normally 100 pF and C7 is 10 times the value of C4. The value of C4 may be increased to obtain a first-order low-pass filter. The cut-off frequency will depend on the time constant R4 x C4.

The output voltage of the receiving amplifier is specified for continuous-wave drive. The maximum output voltage will be higher under speech conditions where the peak to RMS ratio is higher.

Automatic gain control input AGC

Automatic line loss compensation is achieved by connecting a resistor (R6) between AGC and V_{EE}. The automatic gain control varies the gain of the microphone amplifier and the receiving amplifier in accordance with the DC line current. The control range is 5.8 dB which corresponds to a line length of 5 km for a 0.5 mm diameter twisted-pair copper cable with a DC resistance of 176 Ω/km and average attenuation of 1.2 dB/km). Resistor R6 should be chosen in accordance with the exchange supply voltage and its feeding bridge resistance (see Fig.12 and Table 1). The ratio of start and stop currents of the AGC curve is independent of the value of R6. If no automatic line-loss compensation is required the AGC pin may be left open-circuit. The amplifiers, in this condition, will give their maximum specified gain.

Sidetone suppression

The anti-sidetone network, $R1//Z_{line}$, R2, R3, R8, R9 and Z_{bal}, (see Fig.4) suppresses the transmitted signal in the earpiece. Maximum compensation is obtained when the following conditions are fulfilled:

(a) $R9 \times R2 = R1 \times \{R3 + (R8//Z_{bal})\}$

(b) $\{Z_{bal}/(Z_{bal} + R8)\} = \{Z_{line}/(Z_{line} + R1)\}$

If fixed values are chosen for R1, R2, R3 and R9, then condition (a) will always be fulfilled when $|R8//Z_{bal}| \ll R3$.

To obtain optimum sidetone suppression, condition (b) has to be fulfilled which results in:

$$Z_{bal} = (R8/R1) \times Z_{line} = k \times Z_{line}$$

Where k is a scale factor; k = (R8/R1).

The scale factor k, dependent on the value of R8, is chosen to meet the following criteria:

- compatibility with a standard capacitor from the E6 or E12 range for Z_{bal}
- $|Z_{bal}//R8| \ll R3$ fulfilling condition (a) and thus ensuring correct anti-sidetone bridge operation
- $|Z_{bal} + R8| \gg R9$ to avoid influencing the transmit gain

In practise Z_{line} varies considerably with the line type and length. The value chosen for Z_{bal} should therefore be for an average line length thus giving optimum setting for short or long lines.

EXAMPLE

The balance impedance Z_{bal} at which the optimum suppression is present can be calculated by:

Suppose Z_{line} = 210 Ω + (1265 Ω//140 nF) representing a 5 km line of 0.5 mm diameter, copper, twisted-pair cable matched to 600 Ω (176 Ω/km; 38 nF/km).

When k = 0.64 then R8 = 390 Ω; Z_{bal} = 130 Ω + (820 Ω//220 nF).

The anti-sidetone network for the TEA1060 family shown in Fig.4 attenuates the signal received from the line by 32 dB before it enters the receiving amplifier. The attenuation is almost constant over the whole audio-frequency range.

Fig.5 shows a conventional Wheatstone bridge anti-sidetone circuit that can be used as an alternative. Both bridge types can be used with either resistive or complex set impedances. (More information on the balancing of anti-sidetone bridges can be obtained in our publication 'TEA1060 Family versatile speech transmission ICs for electronic telephone sets', order number 9398 341 10011).

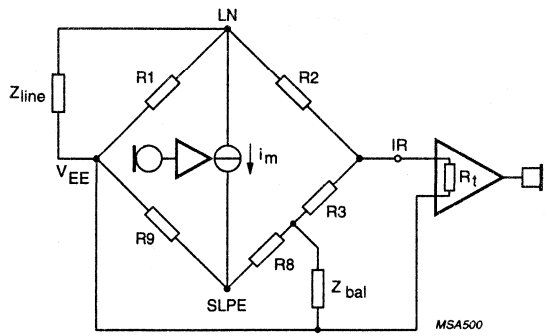


Fig.4 Equivalent circuit of TEA1060 family anti-sidetone bridge.

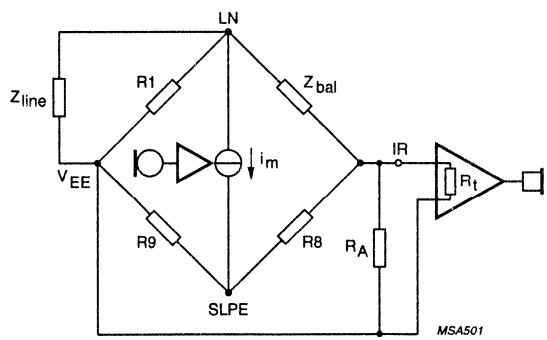


Fig.5 Equivalent circuit of an anti-sidetone network in a Wheatstone bridge configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{LN}	positive continuous line voltage		–	12	V
V_{LN}	repetitive line voltage during switch-on or line interruption		–	13.2	V
V_{LN}	repetitive peak line voltage for a 1 ms pulse per 5 s	R9 = 20 Ω; R10 = 13 Ω; see Fig.17	–	28	V
I_{line}	line current	R9 = 20 Ω; note 1			
	TEA1062; TEA1062A		–	140	mA
	TEA1062T; TEA1062AT		–	140	mA
V_i	input voltage on all other pins				
		positive input voltage	–	V_{CC}+0.7	V
		negative input voltage	–	–0.7	V
P_{tot}	total power dissipation	R9 = 20 Ω; note 2			
	TEA1062; TEA1062A		–	666	mW
	TEA1062T; TEA1062AT		–	454	mW
T_{amb}	operating ambient temperature		–25	+75	°C
T_{stg}	storage temperature		–40	+125	°C
T_j	junction temperature		–	+125	°C

Notes to the Limiting values

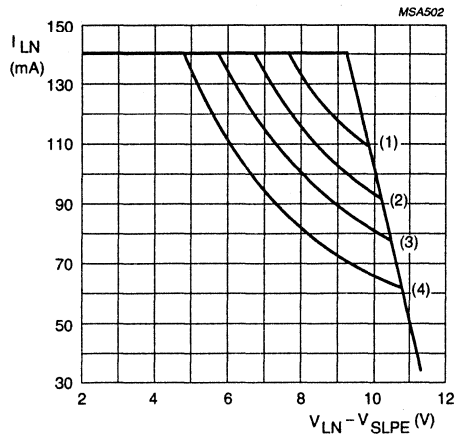
1. Mostly dependent on the maximum required T_{amb} and on the voltage between LN and SLPE (see Fig.6 and Fig.7).
2. Calculated for the maximum ambient temperature specified T_{amb} = 75 °C and a maximum junction temperature of 125 °C.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	TEA1062; TEA1062A	75 K/W
	TEA1062T; TEA1062AT (note 1)	110 K/W

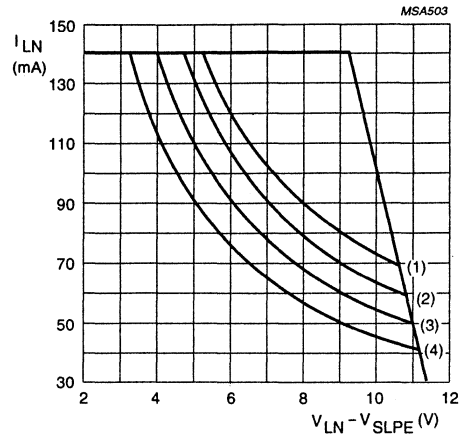
Note to Thermal resistance

1. Mounted on glass epoxy board 28.5 x 19.1 x 1.5 mm.



(1) T_{amb} = 45 °C; P_{tot} = 1068 mW.
(2) T_{amb} = 55 °C; P_{tot} = 934 mW.
(3) T_{amb} = 65 °C; P_{tot} = 800 mW.
(4) T_{amb} = 75 °C; P_{tot} = 666 mW.

Fig.6 TEA1062 and TEA1062A safe operating area.



(1) T_{amb} = 45 °C; P_{tot} = 727 mW.
(2) T_{amb} = 55 °C; P_{tot} = 636 mW.
(3) T_{amb} = 65 °C; P_{tot} = 545 mW.
(4) T_{amb} = 75 °C; P_{tot} = 454 mW.

Fig.7 TEA1062T and TEA1062AT safe operating area.

CHARACTERISTICS

I_{line} = 11 to 140 mA; V_{EE} = 0 V; f = 800 Hz; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies LN and V_{CC} (pins 1 and 13)						
V_{LN}	voltage drop over circuit between LN and V_{EE}	MIC inputs open-circuit				
		I_{line} = 1 mA	–	1.6	–	V
		I_{line} = 4 mA	–	1.9	–	V
		I_{line} = 15 mA	3.55	4.0	4.25	V
		I_{line} = 100 mA	4.9	5.7	6.5	V
		I_{line} = 140 mA	–	–	7.5	V
$\Delta V_{LN}/\Delta T$	variation with temperature	I_{line} = 15 mA	–	–0.3	–	mV/K
V_{LN}	voltage drop over circuit between LN and V_{EE} with external resistor R_{VA}	I_{line} = 15 mA				
		R_{VA} (LN to REG) = 68 kΩ	–	3.5	–	V
		R_{VA} (REG to SLPE) = 39 kΩ	–	4.5	–	V
I_{CC}	supply current	V_{CC} = 2.8 V	–	0.9	1.35	mA
V_{CC}	supply voltage available for peripheral circuitry	I_{line} = 15 mA				
	TEA1062	MUTE = HIGH				
		I_p = 1.2 mA	2.2	2.7	–	V
		I_p = 0 mA	–	3.4	–	V
	TEA1062A	$\overline{MUTE}$ = LOW				
		I_p = 1.2 mA	2.2	2.7	–	V
		I_p = 0 mA	–	3.4	–	V
Microphone inputs MIC– and MIC+ (pins 6 and 7)						
$\lvert Z_i \rvert$	input impedance					
	differential	between MIC– and MIC+	–	64	–	kΩ
	single-ended	MIC– or MIC+ to V_{EE}	–	32	–	kΩ
CMRR	common mode rejection ratio		–	82	–	dB
G_v	voltage gain MIC+ or MIC– to LN	I_{line} = 15 mA; R7 = 68 kΩ	50.5	52.0	53.5	dB
ΔG_{vf}	gain variation with frequency referred to 800 Hz	f = 300 and 3400 Hz	–	±0.2	–	dB
ΔG_{vT}	gain variation with temperature referred to 25 °C	without R6; I_{line} = 50 mA; T_{amb} = –25 and +75 °C	–	±0.2	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DTMF input (pin 11)						
$\|Z_i\|$	input impedance		–	20.7	–	kΩ
G_v	voltage gain from DTMF to LN	I_{line} = 15 mA; R7 = 68 kΩ	24.0	25.5	27.0	dB
ΔG_{vf}	gain variation with frequency referred to 800 Hz	f = 300 and 3400 Hz	–	±0.2	–	dB
ΔG_{vT}	gain variation with temperature referred to 25 °C	I_{line} = 50 mA; T_{amb} = –25 and +75 °C	–	±0.2	–	dB
Gain adjustment inputs GAS1 and GAS2 (pins 2 and 3)						
ΔG_v	transmitting amplifier gain variation by adjustment of R7 between GAS1 and GAS2		–8	–	0	dB
Sending amplifier output LN (pin 1)						
$V_{LN(RMS)}$	output voltage (RMS value)	THD = 10%				
		I_{line} = 4 mA	–	0.8	–	V
		I_{line} = 15 mA	1.7	2.3	–	V
$V_{no(RMS)}$	noise output voltage (RMS value)	I_{line} = 15 mA; R7 = 68 kΩ; 200 Ω between MIC– and MIC+; psophometrically weighted (P53 curve)	–	–69	–	dBmp
Receiving amplifier input IR (pin 10)						
$\|Z_i\|$	input impedance		–	21	–	kΩ
Receiving amplifier output QR (pin 4)						
$\|Z_o\|$	output impedance		–	4	–	Ω
G_v	voltage gain from IR to QR	I_{line} = 15 mA; R_L = 300 Ω (from pin 9 to pin 4)	29.5	31	32.5	dB
ΔG_{vf}	gain variation with frequency referred to 800 Hz	f = 300 and 3400 Hz	–	±0.2	–	dB
ΔG_{vT}	gain variation with temperature referred to 25 °C	without R6; I_{line} = 50 mA; T_{amb} = –25 and +75 °C	–	±0.2	–	dB
$V_{o(RMS)}$	output voltage (RMS value)	THD = 2%; sinewave drive; R4 = 100 kΩ; I_{line} = 15 mA; I_p = 0 mA				
		R_L = 150 Ω	0.22	0.33	–	V
		R_L = 450 Ω	0.3	0.48	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{o(RMS)}$	output voltage (RMS value)	THD = 10%; R4 = 100 kΩ; R_L = 150 Ω; I_{line} = 4 mA	–	15	–	mV
$V_{no(RMS)}$	noise output voltage (RMS value)	I_{line} = 15 mA; R4 = 100 kΩ; IR open-circuit psophometrically weighted (P53 curve); R_L = 300 Ω	–	50	–	μV
Gain adjustment input GAR (pin 5)						
ΔG_v	receiving amplifier gain variation by adjustment of R4 between GAR and QR		−11	–	0	dB
Mute input (pin 12)						
V_{IH}	HIGH level input voltage		1.5	–	V_{CC}	V
V_{IL}	LOW level input voltage		–	–	0.3	V
I_{MUTE}	input current		–	8	15	μA
Reduction of gain						
ΔG_v	MIC+ or MIC− to LN					
	TEA1062	MUTE = HIGH	–	70	–	dB
	TEA1062A	$\overline{MUTE}$ = LOW	–	70	–	dB
G_v	voltage gain from DTMF to QR	R4 = 100 kΩ; R_L = 300 Ω				
	TEA1062	MUTE = HIGH	–	−19	–	dB
	TEA1062A	$\overline{MUTE}$ = LOW	–	−19	–	dB
Automatic gain control input AGC (pin 15)						
	controlling the gain from IR to QR and the gain from MIC+, MIC− to LN	R6 = 110 kΩ (between AGC and V_{EE})				
ΔG_v	gain control range	I_{line} = 70 mA	–	−5.8	–	dB
I_{line}	highest line current for maximum gain		–	23	–	mA
I_{line}	lowest line current for minimum gain		–	61	–	mA

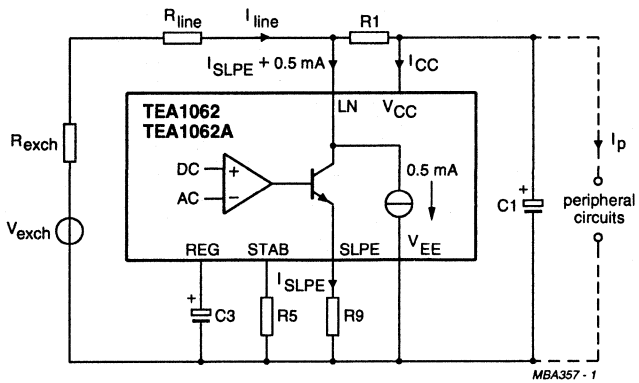
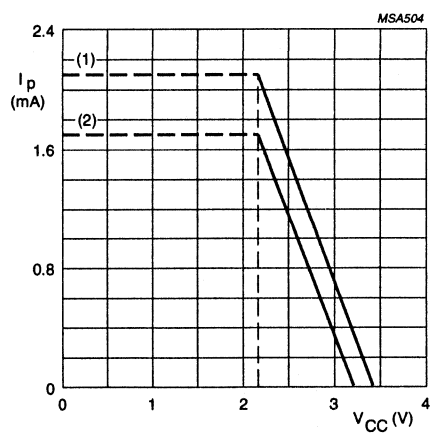


Fig.8 Supply arrangement.



(1) I_p = 2.1 mA.
(2) I_p = 1.7 mA.

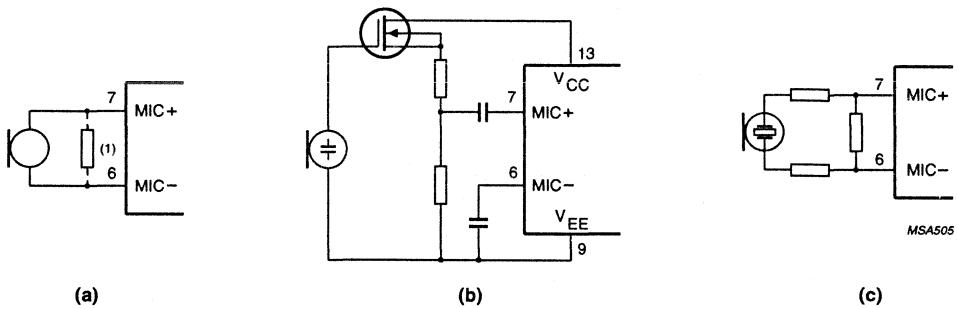
Fig.9 Typical current I_p available from V_{CC} for peripheral circuitry with V_{CC} > 2.2 V; I_{line} = 15 mA at V_{LN} = 4 V; R1 = 620 Ω; R9 = 20 Ω.

Notes to Fig.9

Curve (1) is valid when the receiving amplifier is not driven or when MUTE = HIGH (TEA1062), $\overline{\text{MUTE}}$ = LOW (TEA1062A).

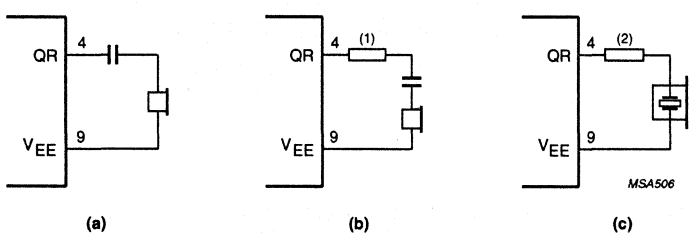
Curve (2) is valid when MUTE = LOW (TEA1062), $\overline{\text{MUTE}}$ = HIGH (TEA1062A) and the receiving amplifier is driven; $V_{o(RMS)}$ = 150 mV, R_L 150 Ω.

The supply possibilities can be increased by setting the voltage drop over the circuit V_{LN} to a higher value by resistor R_{VA} connected between REG and SLPE.



(1) Resistor may be connected to reduce the terminating impedance.

Fig.10 Alternative microphone arrangements (a) magnetic or dynamic microphone (b) electret microphone (c) piezo-electric microphone.



(1) Resistor may be connected to prevent distortion (inductive load).
(2) Resistor is required to increase the phase margin (capacitive load).

Fig.11 Alternative receiver arrangements (a) dynamic earpiece (b) magnetic earpiece (c) piezo-electric earpiece.

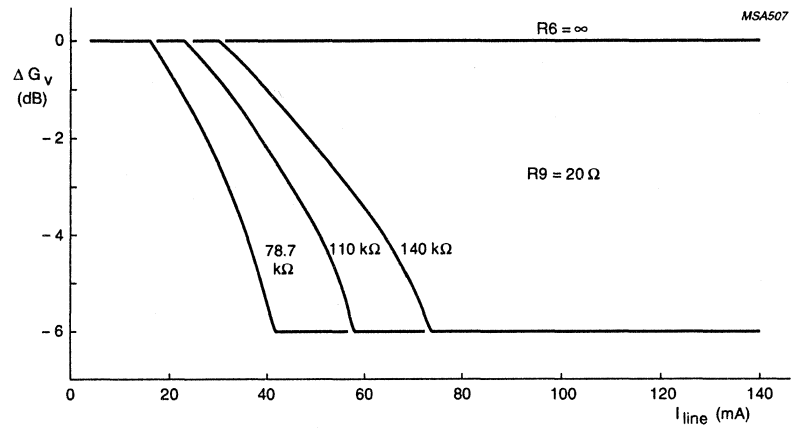
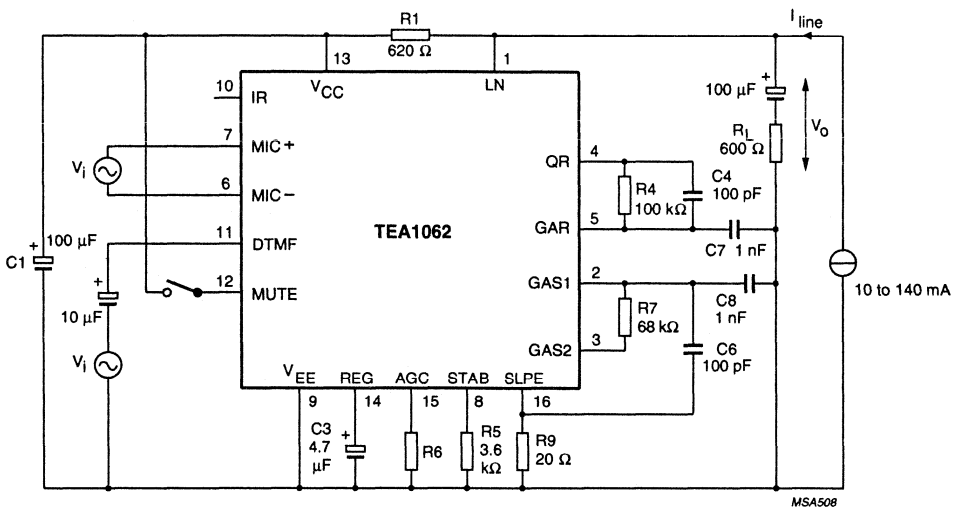


Fig.12 Variation of gain as a function of line current with R6 as a parameter.

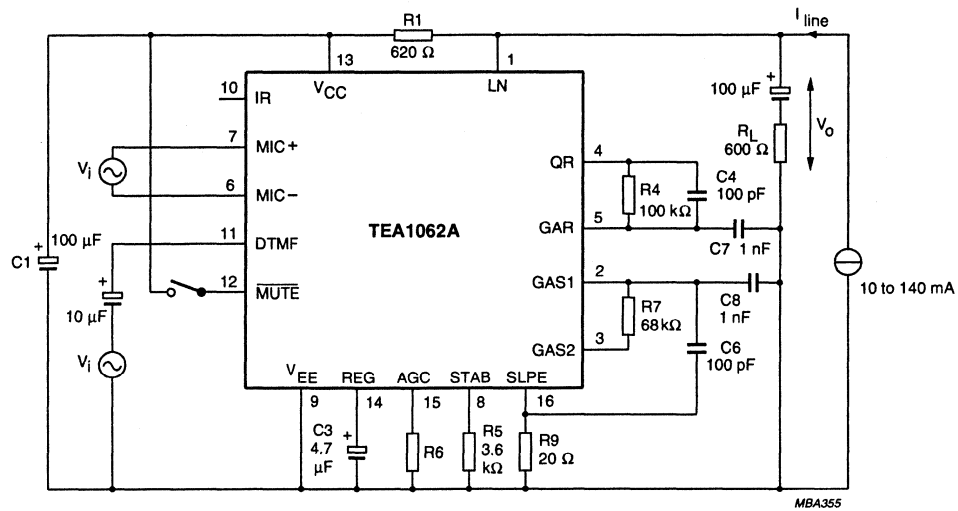
Table 1 Values of resistor R6 for optimum line-loss compensation at various values of exchange supply voltage (V_{exch}) and exchange feeding bridge resistance (R_{exch}); R9 = 20 Ω.

		R_{exch} (Ω)			
		400	600	800	1000
		R6 (kΩ)			
V_{exch} (V)	36	100	78.7	X	X
	48	140	110	93.1	82
	60	X	X	120	102



For measuring gain from MIC+ and MIC– the MUTE input should be LOW or open-circuit.
For measuring the DTMF input, the MUTE input should be HIGH.
Inputs not being tested should be open-circuit.

Fig.13 Test circuit for defining TEA1062 voltage gain of MIC+, MIC– and DTMF inputs; voltage gain is defined as $G_v = 20 \log |V_o/V_i|$.



For measuring gain from MIC+ and MIC– the $\overline{\text{MUTE}}$ input should be HIGH.
For measuring the DTMF input, the $\overline{\text{MUTE}}$ input should be LOW or open-circuit.
Inputs not being tested should be open-circuit.

Fig.14 Test circuit for defining TEA1062A voltage gain of MIC+, MIC– and DTMF inputs; voltage gain is defined as $G_v = 20 \log |V_o/V_i|$.

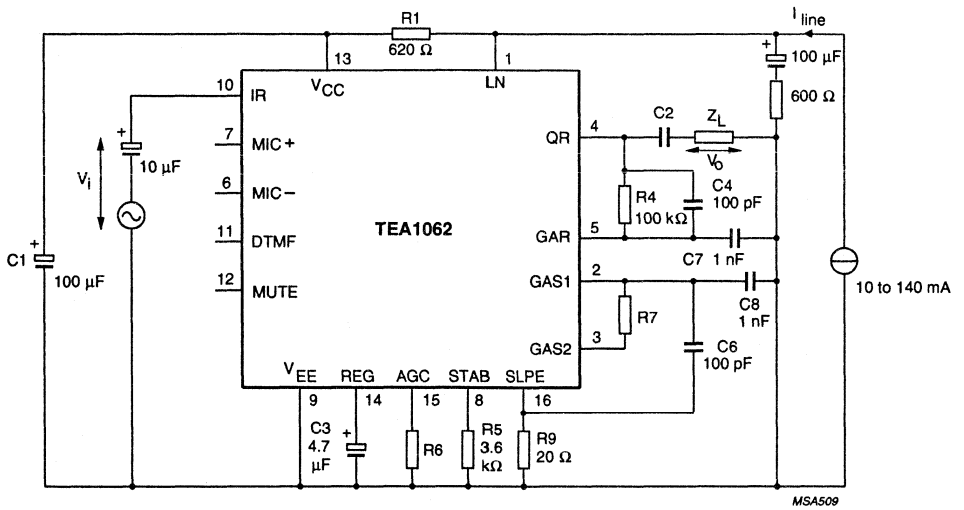


Fig.15 Test circuit for defining TEA1062 voltage gain of the receiving amplifier; voltage gain is defined as $G_v = 20 \log |V_o/V_i|$.

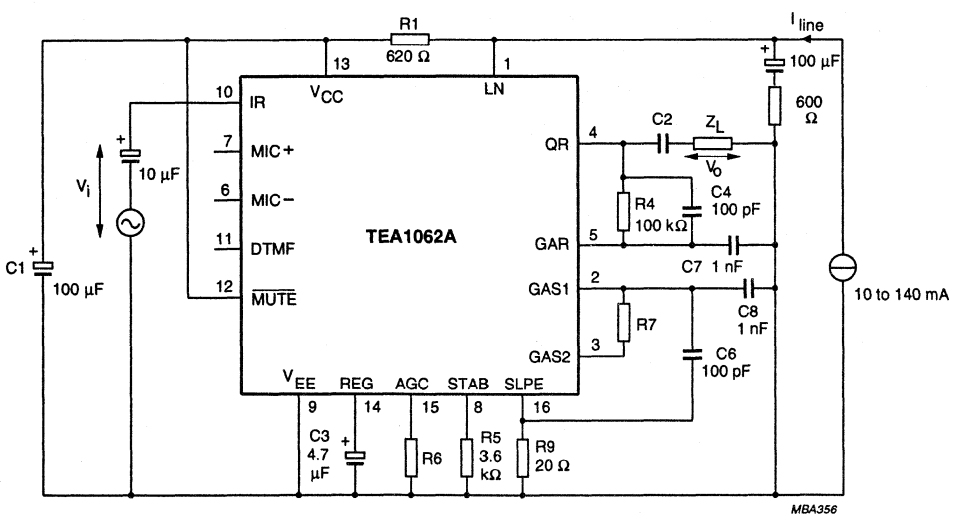
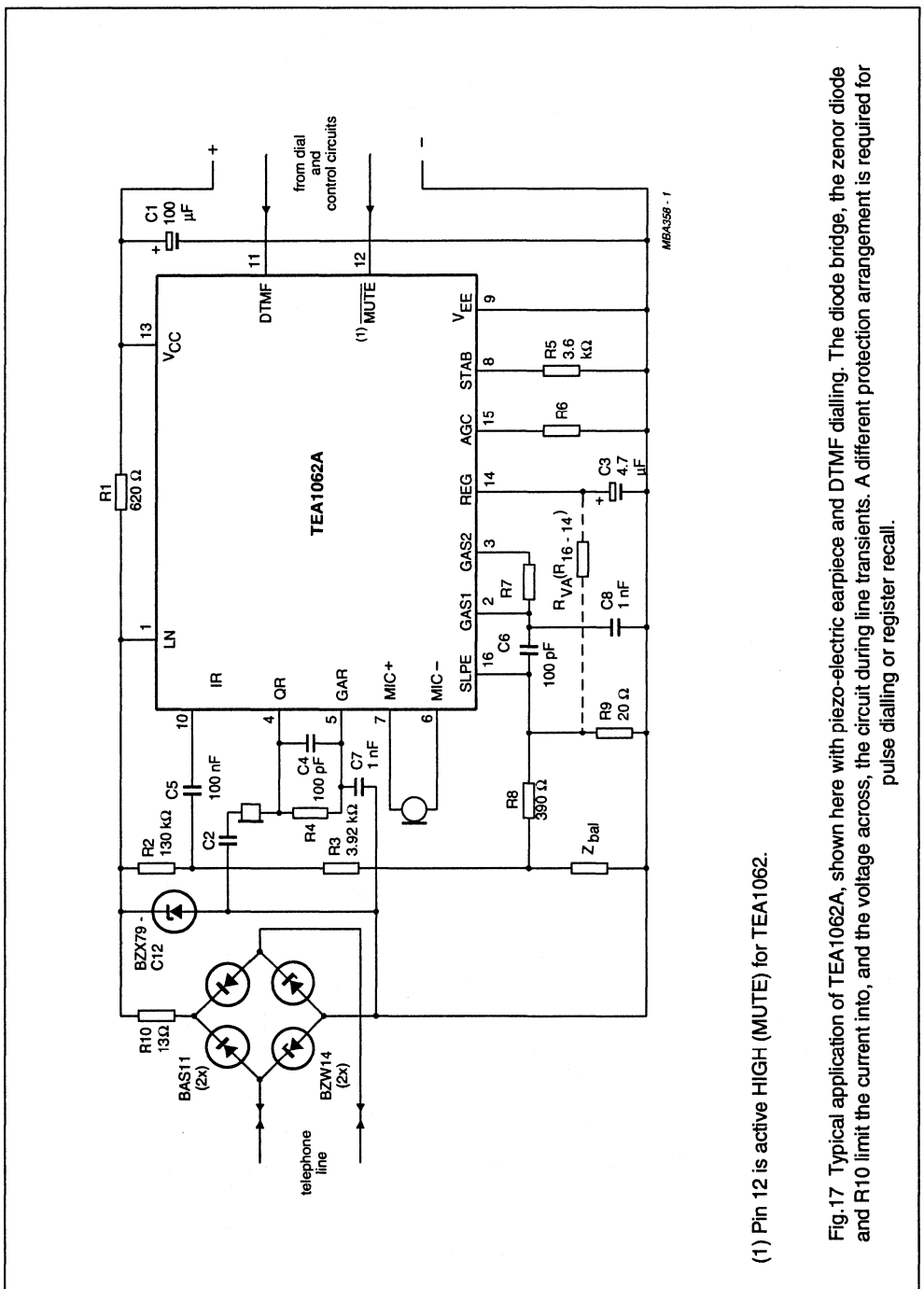


Fig.16 Test circuit for defining TEA1062A voltage gain of the receiving amplifier; voltage gain is defined as $G_v = 20 \log |V_o/V_i|$.

APPLICATION INFORMATION

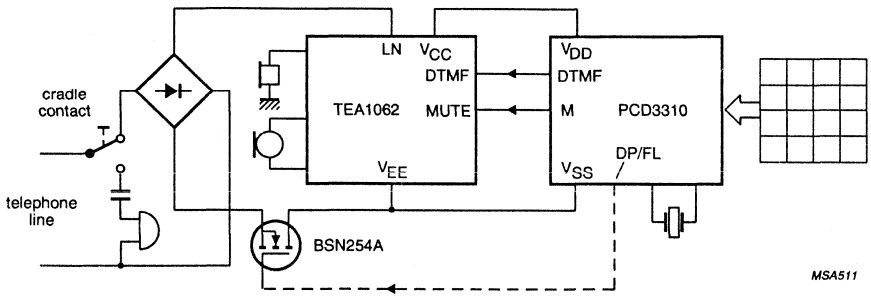
Further information can be found in Application note ETT/AN 89008.



(1) Pin 12 is active HIGH (MUTE) for TEA1062.

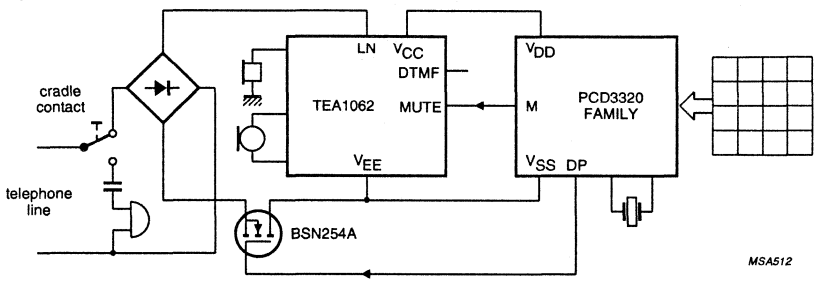
Fig.17 Typical application of TEA1062A, shown here with piezo-electric earpiece and DTMF dialling. The diode bridge, the zenor diode and R10 limit the current into, and the voltage across, the circuit during line transients. A different protection arrangement is required for pulse dialling or register recall.

Note to Fig.17.
The DC line voltage can be set to a higher value by the resistor R_{VA} (REG to SLPE).



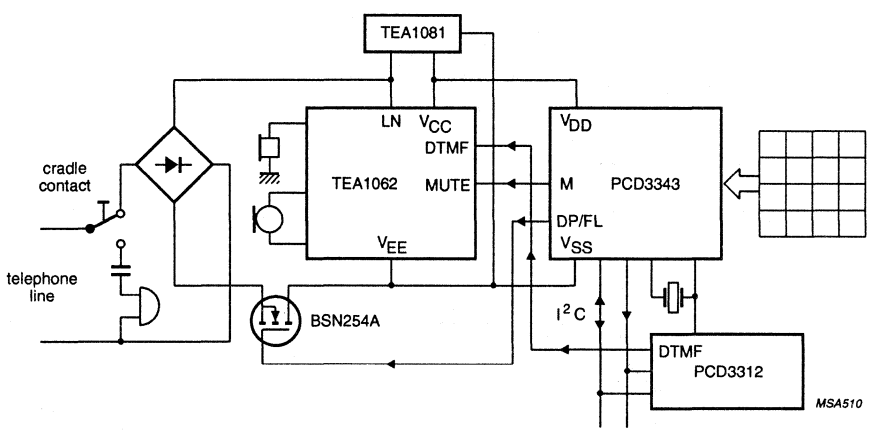
(a)

(a) DTMF pulse set with CMOS bilingual dialling circuit PCD3310. The dashed lines show an optional flash (register recall by timed loop break).



(b)

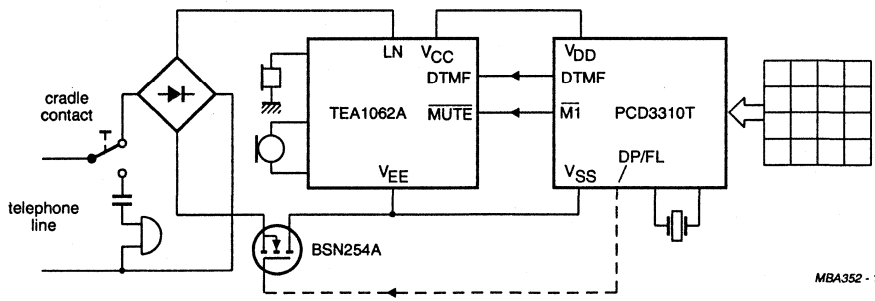
(b) Pulse dial set with one of the PCD3320 family of CMOS interrupted current-loop dialling circuits.



(c)

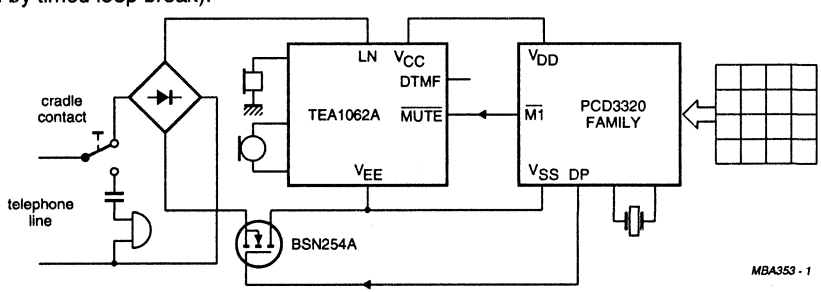
(c) Dual standard (pulse and DTMF) feature phone with the PCD3343 CMOS controller and the PCD3312 CMOS DTMF generator with I²C-bus. Supply is provided by the TEA1081 supply circuit.

Fig.18 Typical simplified applications of the TEA1062.



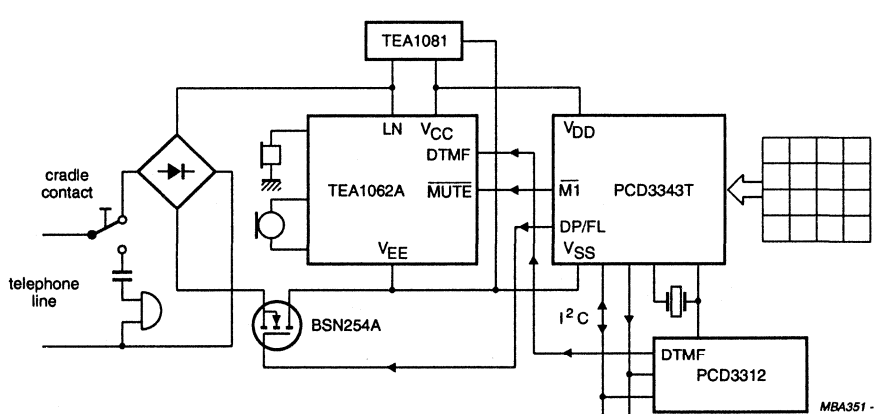
(a)

(a) DTMF pulse set with CMOS bilingual dialling circuit PCD3310T. The dashed lines show an optional flash (register recall by timed loop break).



(b)

(b) Pulse dial set with one of the PCD3320 family of CMOS interrupted current-loop dialling circuits.



(c)

(c) Dual standard (pulse and DTMF) feature phone with the PCD3343T CMOS controller and the PCD3312 CMOS DTMF generator with I²C-bus. Supply is provided by the TEA1081 supply circuit.

Fig.19 Typical simplified applications of the TEA1062A.

LOW VOLTAGE VERSATILE TELEPHONE TRANSMISSION CIRCUIT WITH DIALLER INTERFACE AND TRANSMIT LEVEL DYNAMIC LIMITING

GENERAL DESCRIPTION

The TEA1064A is a bipolar integrated circuit that performs all the speech and line interface functions required in fully electronic telephone sets. It performs electronic switching between dialling and speech and has a powerful DC supply for peripheral circuits. The IC operates at line voltages down to 1.8 V DC (with reduced performance) to facilitate the use of more telephone sets connected in parallel. The transmit signal on the line is dynamically limited (speech-controlled) to prevent distortion at high transmit levels of both the sending signal and the sidetone.

Features

- Low DC line voltage; operates down to 1.8 V (excluding polarity guard)
- Voltage regulator with low voltage drop and adjustable static resistance
- DC line voltage adjustment facility
- Provides a supply for external circuits in two options:
  unregulated supply, regulated line voltage;
  stabilized supply, line voltage varies with supply current
- Dynamic limiting (speech-controlled) in transmit direction prevents distortion of line signal and sidetone
- Symmetrical high-impedance inputs (64 kΩ) for dynamic, magnetic or piezo-electric microphones
- Asymmetrical high-impedance input (32 kΩ) for electret microphones
- DTMF signal input
- Confidence tone in the earpiece during DTMF dialling
- Mute input for disabling speech during pulse or DTMF dialling
- Power-down input for improved performance during pulse dial or register recall (flash)
- Receiving amplifier for magnetic, dynamic or piezo-electric earpieces
- Large amplification setting ranges on microphone and earpiece amplifiers
- Line loss compensation (line current dependent) for microphone and earpiece amplifiers (not used for DTMF amplifier)
- Gain control curve adaptable to exchange supply
- Automatic disabling of the DTMF amplifier in extremely-low voltage conditions
- Microphone MUTE function available with switch

PACKAGE OUTLINES

TEA1064A :20-lead DIL; plastic (SOT146).
TEA1064AT: 20-lead mini-pack; plastic (SO20; SOT163A).

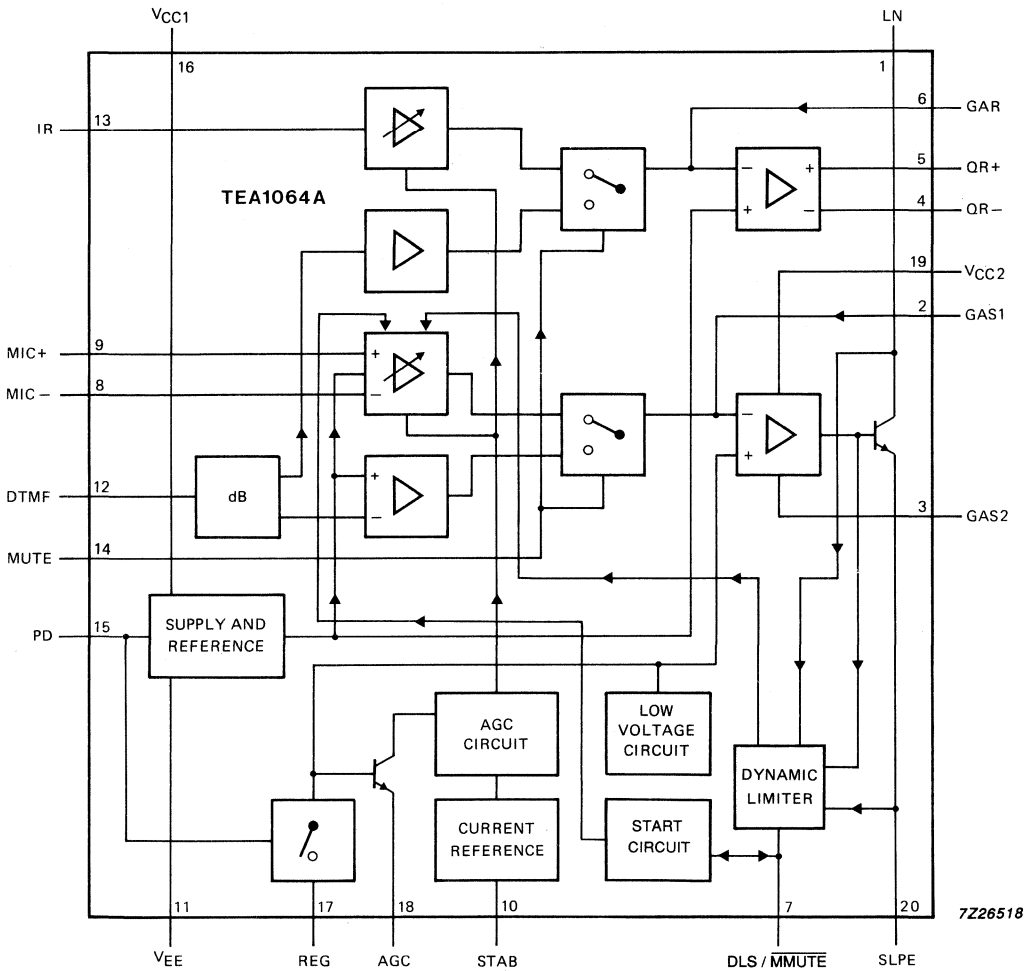


Fig. 1 Block diagram.

DEVELOPMENT DATA

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Operating ambient temperature range		T_{amb}	−25	–	+ 75	°C
Line current operating range:						
normal operation		I_{line}	11	–	140*	mA
with reduced performance		I_{line}	2	–	11	mA
Internal supply current:						
power-down input LOW	V_{CC1} = 2.8 V	I_{CC1}	–	1.3	1.6	mA
power-down input HIGH	V_{CC1} = 2.8 V	I_{CC1}	–	60	82	μA
Voltage gain range:						
microphone amplifier		G_v	44	–	52	dB
receiving amplifier		G_v	20	–	45	dB
Line loss compensation:						
gain control range		G_v	5.7	6.1	6.5	dB
exchange supply voltage range		V_{exch}	36	–	60	V
exchange feeding bridge resistance range		R_{exch}	400	–	1000	Ω
Maximum output voltage swing on LN (peak-to-peak value)	R15 + R16 = 448 Ω I_{line} = 15 mA					
	I_p = 2 mA	$V_{LN(p-p)}$	3.7	3.95	4.2	V
	I_p = 4 mA	$V_{LN(p-p)}$	3.0	3.25	3.5	V
Regulated line voltage application						
	R15 = 0 Ω; R16 = 392 Ω					
Supply for peripherals	I_{line} = 15 mA					
	I_p = 1.4 mA	V_p	2.5	–	–	V
	I_p = 2.7 mA; $R_{REG-SLPE}$ = 20 kΩ	V_p	2.9	–	–	V
DC line voltage	I_{line} = 15 mA					
	without $R_{REG-SLPE}$	V_{LN}	–	3.57	–	V
	$R_{REG-SLPE}$ = 20 kΩ	V_{LN}	–	4.57	–	V
Stabilized supply voltage application						
	R15 = 392 Ω; R16 = 56 Ω					
Supply for peripherals	I_{line} = 15 mA					
	I_p = 0 to 4 mA	$V_{CC2-SLPE}$	3.05	3.3	3.55	V
DC line voltage	I_{line} = 15 mA					
	I_p = 2 mA	V_{LN}	4.2	4.4	4.8	V
	I_p = 4 mA	V_{LN}	4.9	5.1	5.5	V

* For TEA1064AT the maximum line current depends on the heat dissipating qualities of the mounted device.

PINNING

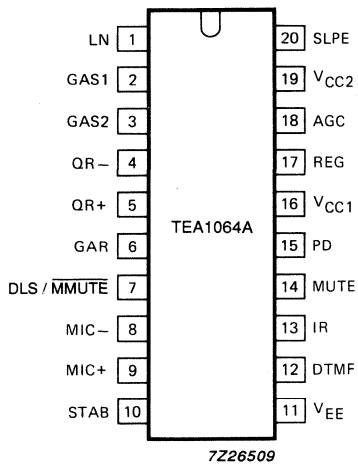


Fig. 2 Pinning diagram.

1	LN	positive line terminal
2	GAS1	gain adjustment; transmitting amplifier
3	GAS2	gain adjustment; transmitting amplifier
4	QR−	inverting output, receiving amplifier
5	QR+	non-inverting output, receiving amplifier
6	GAR	gain adjustment; receiving amplifier
7	DLS/$\overline{\text{MMUTE}}$	decoupling for transmit amplifier dynamic and microphone MUTE input
8	MIC−	inverting microphone input
9	MIC+	non-inverting microphone input
10	STAB	current stabilizer
11	V_{EE}	negative line terminal
12	DTMF	dual-tone multi-frequency input
13	IR	receiving amplifier input
14	MUTE	mute input
15	PD	power-down input
16	V_{CC1}	internal supply decoupling
17	REG	voltage regulator decoupling
18	AGC	automatic gain control input
19	V_{CC2}	reference voltage with respect to SLPE
20	SLPE	slope adjustment for DC curve/reference for peripheral circuits.

FUNCTIONAL DESCRIPTION

Supplies V_{CC1}, V_{CC2}, LN, SLPE, REG and STAB (Fig. 3)

Power for the TEA1064A and its peripheral circuits is usually obtained from the telephone line. The IC develops its own supply voltage at V_{CC1} and regulates its voltage drop. The internal supply requires a decoupling capacitor between V_{CC1} and V_{EE}. The internal current stabilizer is set by a 3.6 kΩ resistor between STAB and V_{EE}.

The DC current flowing into the set is determined by the exchange supply voltage V_{exch}, the feeding bridge resistance R_{exch}, the subscriber line DC resistance R_{line} and the DC voltage (including polarity guard) on the subscriber set (see Fig. 3).

The internal voltage regulator generates a temperature-compensated reference voltage that is available between V_{CC2} and SLPE [$V_{ref} = V_{CC2\text{-}SLPE} = 3.3$ V (typ.)]. This internal voltage regulator requires decoupling by a capacitor between REG and V_{EE} (C3).

The reference voltage can be used to:

- regulate directly the line voltage (stabilized $V_{LN\text{-}SLPE} = V_{CC2\text{-}SLPE}$)*;
- to stabilize the supply voltage for peripherals.

Regulated line voltage

In this application the V_{CC2} pin is connected to the LN pin as shown in Fig. 3. This configuration gives a stabilized voltage across pins LN and SLPE which, applied via the low-pass filter R16, C15, provides a supply to the peripherals that is independent of the line current and depends only on the peripheral supply current.

The value of R16 and the level of the DC voltage $V_{LN\text{-}SLPE}$ determine the supply capabilities. In the basic application R16 = 392 Ω and C15 = 220 μF. The worst-case peripheral supply current as a function of supply voltage is shown in Fig. 4. To increase the supply capabilities, the DC voltage $V_{LN\text{-}SLPE}$ can be increased by using $R_{VA(REG\text{-}SLPE)}$ or by decreasing the value of R16.

* The TEA1064A application with regulated line voltage is the same as is used for TEA1060/TEA1061, TEA1067 and TEA1068 integrated circuits.

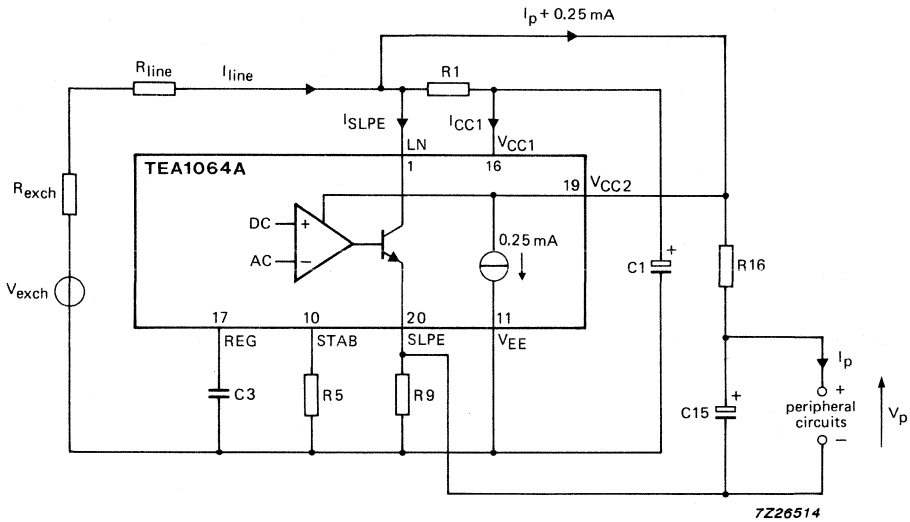


Fig. 3 Application with regulated line voltage (stabilized $V_{LN-SLPE}$). The voltage $V_{LN-SLPE}$ is fixed to V_{ref} = 3.3 ± 0.25 V. Resistor R16 together with the line current determine the supply capabilities and the maximum output swing on the line (no loop damping is necessary). The line voltage V_{LN} = V_{ref} + ([I_{line} - 1.55 mA] x R9).

DEVELOPMENT DATA

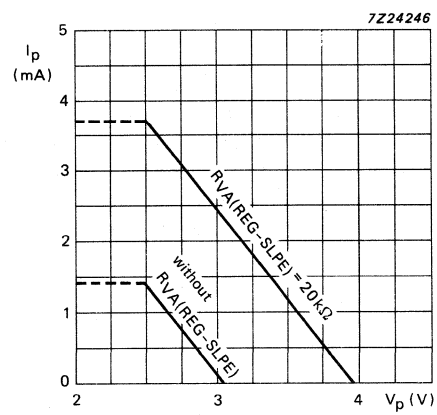


Fig. 4 Minimum supply current for peripherals (I_p) as a function of the peripheral supply voltage (V_p): I_{line} = 15 mA; R16 = 392 Ω; R15 = 0 Ω; valid for MUTE = 0 and 1. Line current has very little influence.

FUNCTIONAL DESCRIPTION (continued)

Regulated line voltage (continued)

The maximum AC output swing on the line at low line currents is influenced by R16 (limited by current) and the maximum output swing on the line at high line currents is influenced by the DC voltage $V_{LN-SLPE}$ (limited by voltage). In both these situations, the internal dynamic limiter in the sending channel prevents distortion when the microphone input is overdriven. The maximum AC output swing on LN is shown in Fig. 5; practical values for R16 are from 200 to 600 Ω and this influences both the maximum output swing at low line currents and the supply capabilities.

The SLPE pin is the ground reference for peripheral circuits, therefore inputs MUTE, PD and DTMF are also referenced to SLPE.

Active microphones can be supplied between V_{CC1} and V_{EE}. Low-power circuits that provide only MUTE and/or PD inputs to the TEA1064A also can be powered from V_{CC1}. However V_{CC1} cannot be used for circuits that provide DTMF signals to the TEA1064A because V_{CC1} is referred to ground.

If the line current I_{line} exceeds I_{CC1} + 0.25 mA, the voltage converter shunts the excess current to SLPE via LN; where $I_{CC1} \approx 1.3$ mA, the value required by the IC for normal operation.

The DC line voltage on LN is:

$$V_{LN} = V_{LN-SLPE} + (I_{SLPE} \times R9)$$

$$V_{LN} = V_{ref} + ([I_{line} - I_{CC1} - 0.25 \times 10^{-3} A] \times R9)$$

in which

V_{ref} = 3.3 V ± 0.25 V is the internal reference voltage between V_{CC2} and SLPE; its value can be adjusted by external resistor R_{VA}

R9 = external resistor between SLPE and V_{EE} (20 Ω in basic application).

With R9 = 20 Ω, this results in:

V_{LN} = 3.57 ± 0.25 V at I_{line} = 15 mA

V_{LN} = 4.17 ± 0.3 V at I_{line} = 15 mA, $R_{VA(REG-SLPE)}$ = 33 kΩ

V_{LN} = 4.57 ± 0.35 V at I_{line} = 15 mA, $R_{VA(REG-SLPE)}$ = 20 kΩ

The preferred value for R9 is 20 Ω. Changing R9 influences microphone gain, DTMF gain, the gain control characteristics, sidetone, and the DC characteristics (especially the low voltage characteristics).

In normal conditions, $I_{SLPE} >> (I_{CC1} + 0.25$ mA) and the static behaviour is equivalent to a voltage regulator diode with an internal resistance of R9. In the audio frequency range the dynamic impedance is determined mainly by R1. The equivalent impedance of the circuit in the audio frequency range is shown in Fig. 6.

The internal reference voltage $V_{CC2-SLPE}$ can be increased by external resistor $R_{VA(REG-SLPE)}$ connected between REG and SLPE. The supply voltage $V_{CC2-SLPE}$ is shown as a function of $R_{VA(REG-SLPE)}$ in Fig. 7. Changing the reference voltage influences the output swing of both sending and receiving amplifiers.

At line currents below 8 mA (typ.), the DC voltage dropped across the circuit is adjusted to a lower level automatically (approximately 1.8 V at 2 mA). This gives the possibility of operating more telephone sets in parallel with DC line voltages (excluding polarity guard) down to an absolute minimum of 1.8 V. At line currents below 8 mA (typ.), the circuit has limited sending and receiving levels.

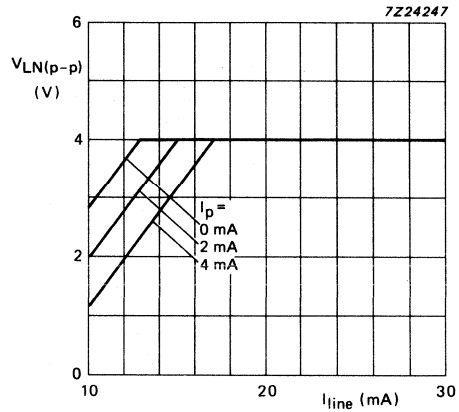


Fig. 5 Maximum AC output swing on the line as a function of line current with peripheral supply current as a parameter: R15 = 0 Ω; R16 = 392 Ω.

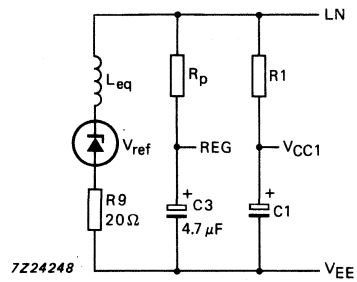


Fig. 6 Equivalent impedance between LN and V_{EE} in the application with stabilized $V_{LN-SLPE}$:
R15 = 0 Ω
L_{eq} = C3 x R9 x R_p
R_p = 15 kΩ

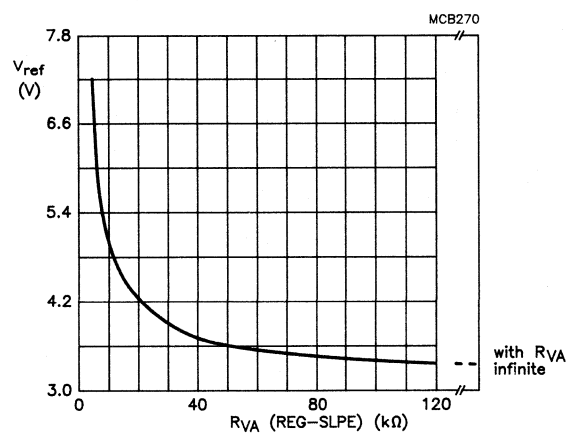


Fig. 7 Internal reference voltage $V_{CC2-SLPE}$ as a function of resistor $R_{VA(REG-SLPE)}$ for line currents between 11 and 140 mA.

In the stabilized supply application:

$$V_{LN} = V_{CC2-SLPE} + ([I_p + 0.25 \times 10^{-3}\,A] \times R15) + ([I_{line} - 1.55 \times 10^{-3}\,A] \times R9)$$

In the unregulated supply application (R15 = 0 Ω):

$$V_{LN} = V_{CC2-SLPE} + ([I_{line} - 1.55 \times 10^{-3}\,A] \times R9)$$

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

Stabilized peripheral supply voltage

The configuration shown in Fig. 8 provides a stabilized voltage across pins V_{CC2} and SPLE for peripheral circuits (such as dialling and control circuits); the DC voltage V_{LN} now varies with the peripheral supply current.

The $V_{CC2\text{-}SLPE}$ supply must be decoupled by capacitor C15. For stable loop operation, resistor R16 ($\approx 50\ \Omega$) is connected between V_{CC2} and SLPE in series with C15. The voltage regulator control loop is completed by resistor R15 between LN and V_{CC2}.

For sets with an impedance of 600 Ω, practical values are: R15 = 200 to 600 Ω; C15 = 220 μF; C3 = 470 nF. The ratio $R15/R16 \leqslant 8$ is for stable loop operation with sufficient phase margin, and $R15/R16 \geqslant 6$ is for satisfactory set impedance in the audio frequency range.

For sets with complex impedance, the value of C3 and the ratio R15/R16 are different (further information is given in the TEA1064A Application Report*).

The peripheral supply capability depends mainly on the available line current, the required AC output swing on the line, the maximum permitted DC voltage on the line and the values of external components (especially R15). With R15 = 392 Ω and R16 = 56 Ω (basic application) the maximum possible AC output swing on the line as a function of line current is as shown in Fig. 9, the curve parameter is the peripheral supply current (I_p). Different values for R15 (from 200 to 600 Ω) maintaining $6 < R15/R16 < 8$ give different results (these are described in the TEA1064A Application Report*).

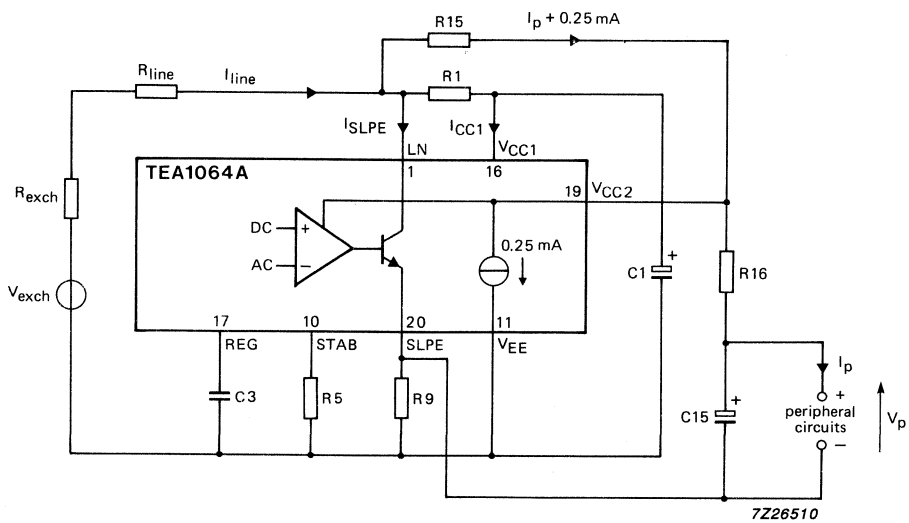


Fig. 8 Application with stabilized supply voltage for peripheral circuits: R15 = 392 Ω; R16 = 56 Ω.

* Supplied on request.

The DC line voltage on LN is

$$V_{LN} = V_{LN\text{-}SLPE} + (I_{SLPE} \times R9).$$

Therefore

$$V_{LN} = V_{ref} + ([I_p + 0.25 \times 10^{-3}\,A] \times R15) + ([I_{line} - I_{CC1} - 0.25 \times 10^{-3}\,A] \times R9)$$

in which:

V_{ref} is the internal reference voltage between V_{CC2} and SLPE (the value of V_{ref} can be adjusted by an external resistor, R_{VA}). V_{ref} = 3.3 V (typ.) without R_{VA}

I_p is the supply current used by peripheral circuits

R15 is an external resistor between LN and V_{CC2} (392 Ω in the basic application)

R9 is an external resistor between SLPE and V_{EE} (20 Ω in the basic application)

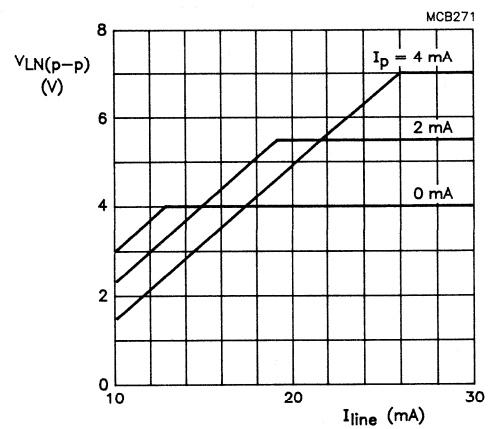


Fig. 9 Maximum output swing on line as a function of line current with the peripheral supply current as a parameter; R15 = 392 Ω; R16 = 56 Ω. As different values of R15 and R16 are allowed, different curves would then apply.

The DC voltage $V_{LN\text{-}SLPE}$ as a function of I_p with R15 as a parameter is shown in Fig. 10. In the audio frequency range, the dynamic impedance is determined mainly by R1. The equivalent impedance in the audio range of the circuit (Fig. 8) is shown in Fig. 11.

FUNCTIONAL DESCRIPTION (continued)

Stabilized peripheral supply voltage (continued)

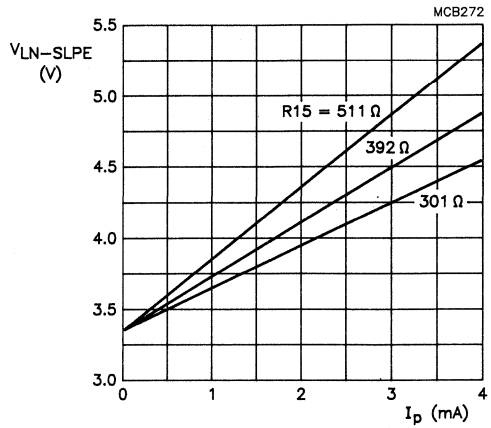
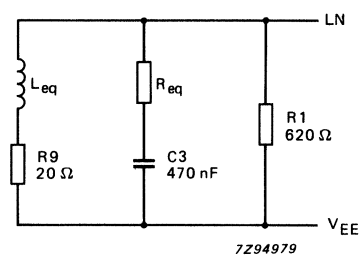


Fig. 10 Curves showing the typical voltage drop between LN and SLPE as a function of the supply current for peripherals with R15 as a parameter: $V_{CC2-SLPE}$ = 3.3 V (R_{VA} not connected). $V_{CC2-SLPE}$ can be adjusted between approximately 3.3 and 4.3 V by changing the value of R_{VA}, this results in a parallel-shift of the curves.
The total voltage drop $V_{LN} \approx V_{LN-SLPE} + ([I_{line} - 1.55\ mA] \times R9)$.



$$R_{eq} = R_p \left(\frac{R15}{R16} + 1\right)$$

$$L_{eq} = C3 \times R9 \times R_{eq}$$

with R_p = 15 kΩ

Fig. 11 Equivalent impedance between LN and V_{EE} at f > 300 Hz in the application with stabilized supply voltage for peripheral circuits.

Microphone inputs MIC+ and MIC– and gain pins GAS1 and GAS2

The TEA1064A has symmetrical microphone inputs, its input impedance is 64 kΩ (2 x 32 kΩ) and its voltage amplification is typ. 52 dB with R7 = 68 kΩ. Either dynamic, magnetic or piezo-electric microphones can be used, or an electret microphone with a built-in FET buffer. Arrangements for the microphone types are shown in Fig. 12.

The gain of the microphone amplifier is proportional to external resistor R7 connected between GAS1 and GAS2 and with this it can be adjusted between 44 dB and 52 dB to suit the sensitivity of the transducer.

An external 100 pF capacitor (C6) is required between GAS1 and SLPE to ensure stability. A larger value of C6 may be chosen to obtain a first-order low-pass filter with a cut-off frequency corresponding to the time constant R7 x C6.

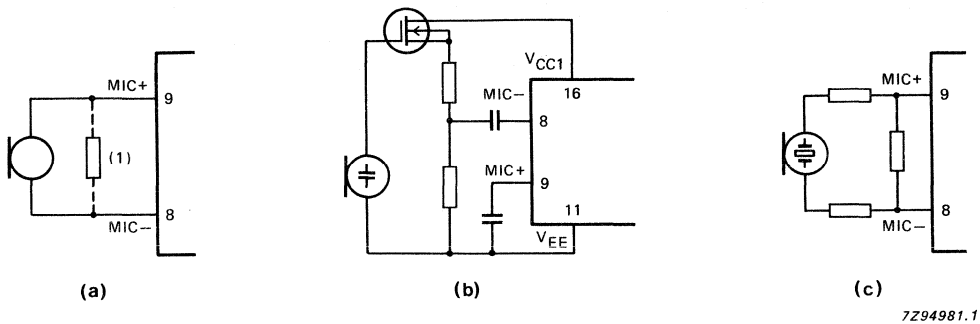


Fig. 12 Microphone arrangements: a) magnetic or dynamic microphone, the resistor (1) may be connected to reduce the terminating impedance, or for sensitive types a resistive attenuator can be used to prevent overloading the microphone inputs; b) electret microphone; c) piezo-electric microphone.

Dynamic limiter (microphone) pin DLS/$\overline{\text{MMUTE}}$

A low level at the DLS/$\overline{\text{MMUTE}}$ pin inhibits the microphone inputs MIC+ and MIC– but has no influence on the receiving and DTMF amplifiers.
Removing the low level at the DLS/$\overline{\text{MMUTE}}$ pin provides the normal function of the microphone amplifier after a short time determined by the capacitor connected to DLS/$\overline{\text{MMUTE}}$ pin. The microphone mute function can be realised by a simple switch as shown in Fig.13.

To prevent distortion of the transmitted signal, the gain of the sending amplifier is reduced rapidly when peaks of the signal on the line exceed an internally-determined threshold. The time in which gain reduction is effected (attack time) is very short. The circuit stays in the gain-reduced condition until the peaks of the sending signal remain below the threshold level. The sending gain then returns to normal after a time determined by the capacitor connected to DLS/$\overline{\text{MMUTE}}$ (release time).

The internal threshold adapts automatically to the DC voltage setting of the circuit (voltage $V_{LN-SLPE}$). This means that the maximum output swing on the line will be higher if the DC voltage dropped across the circuit is increased.

Fig. 14 shows the maximum possible output swing on the line as a function of the DC voltage drop ($V_{LN-SLPE}$) with $I_{line} - I_p$ as a parameter.

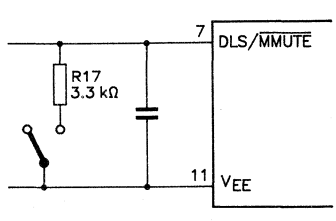


Fig. 13 Microphone-mute function.

FUNCTIONAL DESCRIPTION (continued)

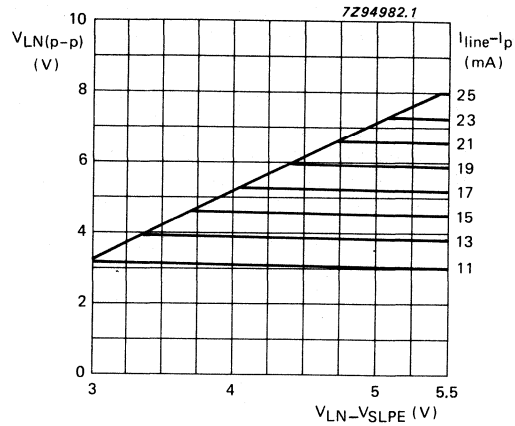


Fig. 14 Maximum output swing on line as a function of the DC voltage drop $V_{LN-SLPE}$ with $I_{line} - I_p$ as a parameter: R15 = 392 Ω; R16 = 56 Ω; or R15 = 0 Ω and R16 = 392 + 56 = 448 Ω.

The internal threshold level is lowered automatically if the DC current in the transmit output stage is insufficient. This prevents distortion of the sending signal in applications using parallel-connected telephones or telephones operating over long lines, for example.

Dynamic limiting also considerably improves sidetone performance in over-drive conditions (less distortion; limited sidetone level).

Receiving amplifier IR, QR+, QR− and GAR

The receiving amplifier has one input IR and two complementary outputs, QR+ (non-inverting) and QR− (inverting). These outputs may be used for single-ended or differential drive, depending on the type and sensitivity of the earpiece used (see Fig. 15). Gain from IR to QR+ is typically 31 dB with R4 = 100 kΩ, sufficient for low-impedance magnetic or dynamic earpieces which are suitable for single-ended drive. By using both outputs (differential drive) the gain is increased by 6 dB. Differential drive can be used when the earpiece impedance exceeds 450 Ω as with high-impedance dynamic, magnetic or piezo-electric earpieces.

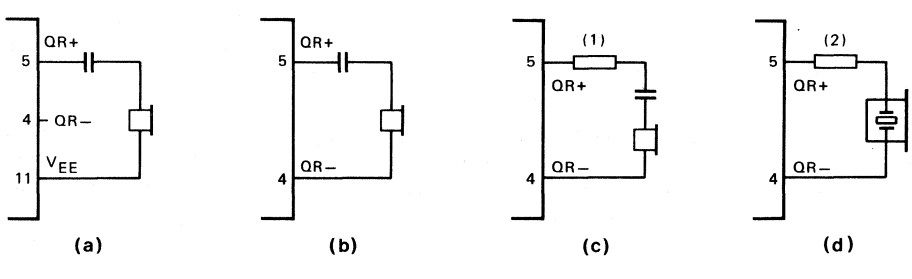


Fig. 15 Alternative receiver arrangements: a) dynamic earpiece with an impedance less than 450 Ω; b) dynamic earpiece with an impedance more than 450 Ω; c) magnetic earpiece with an impedance more than 450 Ω, resistor (1) may be connected to prevent distortion (inductive load); d) piezo-electric earpiece, resistor (2) is required to increase the phase margin (stability with capacitive load).

The output voltage of the receiving amplifier is specified for continuous-wave drive. Fig. 16 shows the maximum output swing of the receiving amplifier as a function of the DC voltage drop (V_{LN}). The maximum output voltage will be higher under speech conditions, where the ratio of the peak to the RMS value is higher.

The gain of the receiving amplifier can be adjusted to suit the sensitivity of the transducer used. The adjustment range is between 20 dB and 39 dB with single-ended drive and between 26 dB and 45 dB with differential drive. The gain is proportional to the external resistor R4 connected between GAR and QR+. The overall gain between LN and QR+ can be found by subtracting the attenuation of the anti-sidetone network (32 dB) from the amplifier gain.

Two external capacitors (C4 = 100 pF and C7 = 10 x C4 = 1 nF) ensure stability. A larger value may be chosen to obtain a first-order low-pass filter. The cut-off frequency corresponds with the time constant R4 x C4. The relationship C7 = 10 x C4 must be maintained.

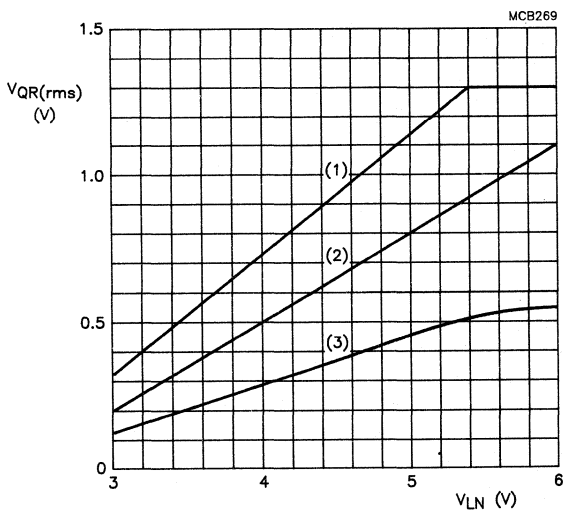


Fig. 16 Maximum output swing of the receiving amplifier as a function of DC voltage drop V_{LN} with the load at the receiver output as parameter: valid for both supply options; THD = 2%; I_{line} = 15 mA. Curve (1) is for a differential load of 47 nF (series resistance = 100 Ω); f = 3400 Hz. Curve (2) is for a differential load of 450 Ω; f = 1 kHz. Curve (3) is for a single-ended load of 150 Ω; f = 1 kHz.

DEVELOPMENT DATA

Automatic gain control input AGC

Automatic compensation of line loss is obtained by connecting a resistor (R6) between AGC and V_{EE}. This automatic gain control varies the gain of the microphone amplifier and receiving amplifier in accordance with the DC line current. The control range is 6.1 dB; this corresponds to a 5 km line of 0.5 mm diameter copper twisted-pair cable (DC resistance = 176 Ω/km, average attenuation = 1.2 dB/km). The DTMF gain is not affected by this feature.

The value of R6 must be chosen with reference to the exchange supply voltage and its feeding bridge resistance (see Fig. 17 and Table 1). Different values of R6 give the same line current ratios at the start and the end of the control range. If automatic line-loss compensation is not required the AGC pin can be left open, the amplifiers then give their maximum gain.

FUNCTIONAL DESCRIPTION (continued)

Automatic gain control input AGC (continued)

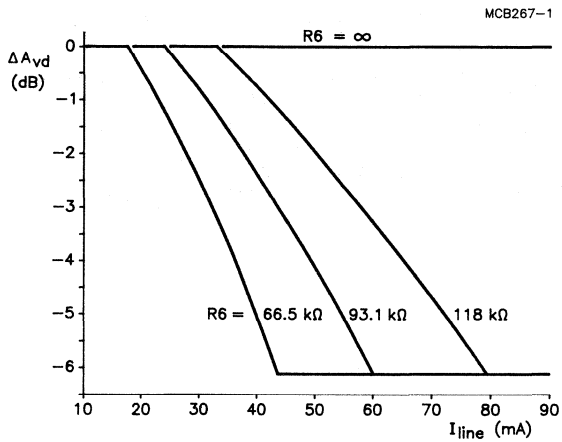


Fig. 17 Variation of gain as a function of line current with R6 as a parameter; R9 = 20 Ω.

Table 1 Values of R6 giving optimum line-loss compensation at various values of exchange supply voltage (V_{exch}) and exchange feeding bridge resistance (R_{exch}); R9 = 20 Ω.

		R_{exch} (Ω)			
		400	600	800	1000
		R6 (kΩ)			
V_{exch} (V)	36	84.5	66.5	X	X
	48	118	93.1	77.8	66.5
	60	X	X	97.6	84.5

MUTE input (see notes 1 and 2)

MUTE = HIGH enables the DTMF input and inhibits the microphone and receiving amplifier inputs.

MUTE = LOW or open-circuit disables the DTMF input and enables the microphone and receiving amplifier inputs.

Switching MUTE gives negligible clicks at the telephone outputs and on the line.

Dual-tone multi-frequency input DTMF (see note 1)

When the DTMF input is enabled, dialling tones may be sent on to the line. The voltage gain between DTMF-SLPE and LN-V_{EE} is typ. 26 dB less than the gain of the microphone amplifier and varies with R7 in the same way as the gain of the microphone amplifier. This means that the tone level at the DTMF input has to be adjusted after setting the gain of the microphone amplifier.
With R7 = 68 kΩ the gain is typically 26 dB.

The signalling tones can be heard in the earpiece at a low level (confidence tone).

Power-down input PD (see notes 1 and 2)

During pulse dialling or register recall (timed loop break) the telephone line is interrupted; as a consequence it provides no supply for the transmission circuit connected to V_{CC1} or for the peripherals between V_{CC2} and SLPE.
These supply gaps are bridged by the charges in the capacitors C1 and C15. The requirements on these capacitors are eased by applying a HIGH level to the PD input during the time of the loop break. This reduces the internal supply current I_{CC1} from (typ.) 1.3 mA to (typ.) 60 μA and switches off the voltage regulator to prevent discharge via LN and V_{CC2}.

A HIGH level at PD also internally disconnects the capacitor at REG so that the voltage stabilizer has no switch-on delay after line interruptions. This minimizes the contribution of the IC to the current waveform during pulse dialling or register recall.

When the power-down facility is not required, the PD pin can be left open-circuit or connected to SLPE.

DEVELOPMENT DATA

Side-tone suppression

Suppression of the transmitted signal in the earpiece is obtained by the anti-sidetone network comprising $R1//Z_{line}$, R2, R3, R8, R9 and Z_{bal} (see Fig. 18). Maximum compensation is obtained when the following conditions are fulfilled:

$$\text{a)}\quad R9 \times R2 = R1 \times (R3 + [R8//Z_{bal}])$$

$$\text{b)}\quad (Z_{bal}/[Z_{bal} + R8]) = (Z_{line}/[Z_{line} + R1])$$

If fixed values are chosen for R1, R2, R3 and R9, then condition a) is always fulfilled provided $|R8//Z_{bal}| << R3$.

To obtain optimum sidetone suppression, condition b) has to be fulfilled, resulting in:

$$Z_{bal} = (R8/R1) \times Z_{line} = k \times Z_{line}$$

where k is a scale factor; k = (R8/R1).

The scale factor k (value of R8) is chosen to meet the following criteria:

- compatibility with a standard capacitor from the E6 or E12 range for Z_{bal};
- $|Z_{bal}//R8| << R3$ to fulfill condition a) and thus ensure correct anti-sidetone bridge operation;
- $|Z_{bal} + R8| >> R9$ to avoid influencing the transmit gain.

In practice Z_{line} varies considerably with the line length and line type. Therefore the value chosen for Z_{bal} should be for an average line length giving satisfactory sidetone suppression with short and long lines. The suppression also depends on the accuracy of the match between Z_{bal} and the impedance of the average line.

Example

The line impedance for which optimum suppression is to be obtained can be represented by 210 Ω + (1265 Ω // 140 nF). This represents a 5 km line of 0.5 mm diameter copper twisted-pair cable matched with 600 Ω (176 Ω/km; 38 nF/km).

With k = 0.64 this results in: R8 = 390 Ω; Z_{bal} = 130 Ω + (820 Ω // 220 nF).

Side-tone suppression (continued)

The anti-sidetone network for the TEA1060 family shown in Fig. 18 attenuates the signal received from the line by 32 dB before it enters the receiving amplifier. The attenuation is almost constant over the whole audio-frequency range.

Alternatively a conventional Wheatstone bridge can be used as an anti-sidetone circuit (Fig. 19). Both bridge types can be used with either resistive or complex set impedances. (More information on the balancing of anti-sidetone bridges can be obtained in our publication 'Versatile speech transmission ICs for electronic telephone sets', order number 9398 341 10011.)

Notes

1. The reference used for the MUTE, DTMF and PD inputs is SLPE.
2. A LOW level for any of these pins is defined by connection to SLPE, a HIGH level is defined as a voltage greater than V_{SLPE} + 1.5 V and smaller than V_{CC1} + 0.4 V.

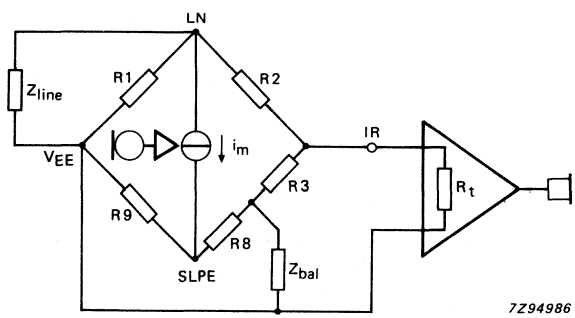


Fig. 18 Equivalent circuit of TEA1060 family anti-side-tone bridge.

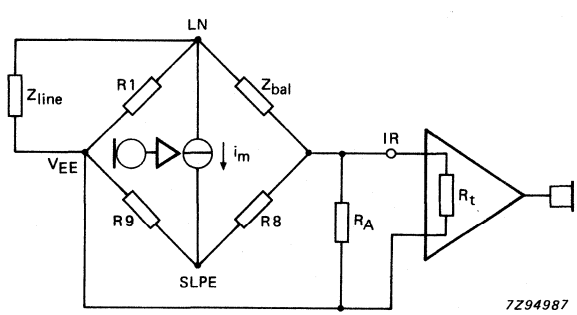


Fig. 19 Equivalent circuit of an anti-sidetone network in the Wheatstone bridge configuration.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Positive line voltage continuous		V_{LN}	–	12	V
Repetitive line voltage during switch-on line interruption		V_{LN}	–	13.2	V
Repetitive peak line voltage one 1 ms pulse per 5 s	R9 = 20 Ω; R10 = 13 Ω (Fig. 24)	V_{LN}	–	28	V
Line current TEA1064A (1)	R9 = 20 Ω	I_{LN}	–	140	mA
Line current TEA1064AT (1)	R9 = 20 Ω	I_{LN}	–	140	mA
Input voltage on pins other than LN and V_{CC2}		V_i	$V_{EE}-0.7$	$V_{CC1}+0.7$	V
Total power dissipation (2)	R9 = 20 Ω				
TEA1064A		P_{tot}	–	714	mW
TEA1064AT		P_{tot}	–	555	mW
Storage temperature range		T_{stg}	−40	+ 125	°C
Operating ambient temperature range		T_{amb}	−25	+ 75	°C
Junction temperature		T_j	–	+ 125	°C

(1) Mostly dependent on the maximum required T_{amb} and on the voltage between LN and SLPE. See Figs 20 and 21 to determine the current as a function of the required voltage and the temperature.

(2) Calculated for the maximum ambient temperature specified T_{amb} = 75 °C and a maximum junction temperature of 125 °C.

THERMAL RESISTANCE

From junction to ambient in free air

TEA1064A	$R_{th\ j\text{-}a}$	=	70 K/W
TEA1064AT mounted on glass epoxy board 41 x 19 x 1.5 mm	$R_{th\ j\text{-}a}$	=	90 K/W

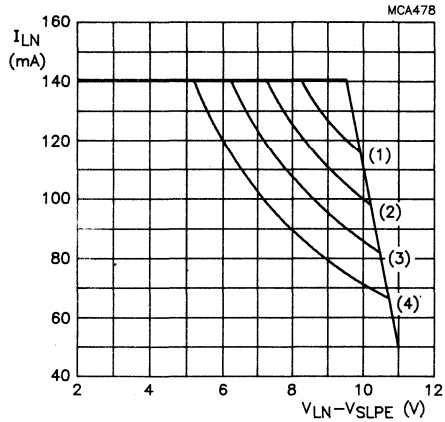


Fig. 20 TEA1064A safe operating area.

	T_{amb}	P_{tot}
(1)	45 °C	1143 mW
(2)	55 °C	1000 mW
(3)	65 °C	857 mW
(4)	75 °C	714 mW

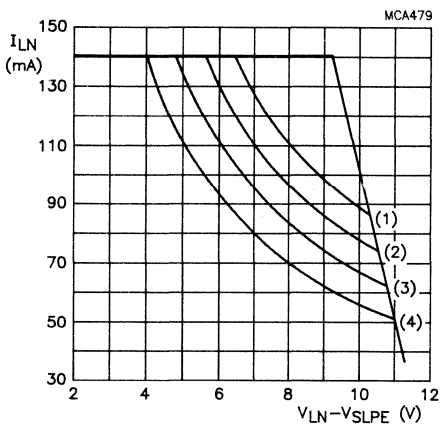


Fig. 21 TEA1064AT safe operating area.

	T_{amb}	P_{tot}
(1)	45 °C	888 mW
(2)	55 °C	777 mW
(3)	65 °C	666 mW
(4)	75 °C	555 mW

DEVELOPMENT DATA

CHARACTERISTICS

I_{line} = 11 to 140 mA; V_{EE} = 0 V; f = 800 Hz; T_{amb} = 25 °C; R_L = 600 Ω; tested in the circuit of Fig. 22 or 23); unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies LN, V_{CC1}, V_{CC2} (pins 1, 16, 19)						
Reference DC voltage between V_{CC2} and SLPE	I_{line} = 15 mA I_p = 0; 4 mA					
R_{VA} not connected		$V_{CC2-SLPE}$	3.05	3.3	3.55	V
Variation with temperature	I_{line} = 15 mA	$\frac{V_{CC2-SLPE}}{\Delta T}$	−3.0	−1.0	1.0	mV/K
Variation with line current referred to 15 mA	I_{line} = 100 mA	$\Delta V_{CC2-SLPE}$	–	60	–	mV
With R_{VA} connected between REG and SLPE	R_{VA} = 33 kΩ	$V_{CC2-SLPE}$	3.6	3.8	4.2	V
	R_{VA} = 20 kΩ	$V_{CC2-SLPE}$	3.95	4.2	4.65	V
DC line voltage:						
voltage drop between LN and V_{EE}	MIC−, MIC+ inputs open; R15 = 392 Ω; without R_{VA}					
at I_{line} = 15 mA	I_p = 0 mA	V_{LN}	3.4	3.6	4.0	V
	I_p = 2 mA	V_{LN}	4.2	4.4	4.8	V
	I_p = 4 mA	V_{LN}	4.9	5.1	5.5	V
at I_{line} = 100 mA	I_p = 2 mA	V_{LN}	–	6.1	7.0	V
at I_{line} = 140 mA	I_p = 2 mA	V_{LN}	–	7.0	7.8	V
Voltage drop under low current conditions	I_p = 0 mA					
	I_{line} = 2 mA	V_{LN}	–	1.8	–	V
	I_{line} = 4 mA	V_{LN}	*	2.2	*	V
	I_{line} = 7 mA	V_{LN}	*	3.2	*	V
	I_{line} = 11 mA	V_{LN}	*	3.5	*	V
Internal supply current I_{CC1}:						
current into pin V_{CC1}	V_{CC1} = 2.8 V					
	PD = LOW	I_{CC1}	–	1.3	1.6	mA
	PD = HIGH	I_{CC1}	–	60	82	μA
Microphone inputs MIC−, MIC+ (pins 8, 9)						
Input impedance:						
differential		Z_i	51	64	77	kΩ
single-ended		Z_i	25.5	32.0	38.5	kΩ

* Value to be fixed.

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Common mode rejection ratio		CMRR	–	82	–	dB
Voltage gain (see Fig. 22)	I_{line} = 15 mA; R7 = 68 kΩ	G_v	51	52	53	dB
Variation of G_v with frequency, referred to 0.8 kHz	f = 300 and 3400 Hz	$\Delta G_v/\Delta f$	−0.5	± 0.1	+ 0.5	dB
Variation of G_v with temperature, referred to 25 °C	without R6; I_{line} = 50 mA; T_{amb} = −25 to + 75 °C	$\Delta G_v/\Delta T$	–	± 0.2	–	dB
DTMF input (pin 12)						
Input impedance		Z_i	16.8	20.7	24.6	kΩ
Voltage gain (see Fig. 22)	I_{line} = 15 mA; R7 = 68 kΩ	G_v	25	26	27	dB
Variation of G_v with frequency, referred to 0.8 kHz	f = 300 and 3400 Hz	$\Delta G_v/\Delta f$	−0.5	± 0.1	+ 0.5	dB
	f = 697 and 1633 Hz	$\Delta G_v/\Delta f$	−0.2	± 0.05	+ 0.2	dB
Variation of G_v with temperature, referred to 25 °C	I_{line} = 50 mA; T_{amb} = −25 to + 75 °C	$\Delta G_v/\Delta T$	–	± 0.2	0.5	dB
Gain adjustment inputs GAS1, GAS2 (pins 2, 3)						
Transmitting amplifier, gain adjustment range		ΔG_v	−8	–	+ 0	dB
Sending amplifier output LN (pin 1)						
Dynamic limiter						
Output voltage swing (peak-to-peak value)	I_{line} = 15 mA; R7 = 68 kΩ; I_p = 0 mA; $V_{i(rms)}$ = 3.6 mV	$V_{LN(p-p)}$	3.6	4.0	4.5	V
Total harmonic distortion	V_i = 3.6 mV + 10 dB	THD	–	1.5	2.0	%
	V_i = 3.6 mV + 15 dB	THD	–	2.8	10.0	%
Output voltage swing (peak-to-peak value)	V_i = 3.6 mV + 10 dB					
	I_p = 2 mA	$V_{LN(p-p)}$	3.7	3.95	4.2	V
	I_p = 4 mA	$V_{LN(p-p)}$	3.0	3.25	3.5	V
	I_p = 0 mA; I_{line} = 7 mA	$V_{LN(p-p)}$	–	2	–	V
	I_p = 0 mA; I_{line} = 4 mA	$V_{LN(p-p)}$	–	1	–	V

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
LN output (continued)						
Dynamic behaviour of limiter	C16 = 470 nF					
attack time, V_{mic} jumps from 2 mV to 40 mV		t_{att}	–	1.5	5.0	ms
release time, V_{mic} jumps from 40 mV to 2 mV		t_{rel}	50	150	–	ms
Noise output voltage (RMS value)	I_{line} = 15 mA; R7 = 68 kΩ; 200 Ω between MIC– and MIC+; psophometrically weighted (P53 curve)	$V_{no(rms)}$	–	–72	–	dBmp
Receiving amplifier input IR (pin 13)						
Input impedance		Z_i	17	21	25	kΩ
Receiving amplifier outputs QR– QR+ (pins 4, 5)						
Output impedance	single-ended	Z_o	–	4	–	Ω
Voltage gain	Fig. 23; I_{line} = 15 mA; R4 = 100 kΩ					
single-ended; R_T = 300 Ω		G_v	30	31	32	dB
differential; R_T = 600 Ω		G_v	36	37	38	dB
Variation with frequency, referred to 0.8 kHz	f = 300 and 3400 Hz	$\Delta G_v/\Delta f$	–0.5	–0.2	0	dB
Variation with temperature, referred to 25 °C	without R6; I_{line} = 50 mA; T_{amb} = –25 to +75 °C	$\Delta G_v/\Delta T$	–	± 0.2	–	dB
Output voltage (RMS value)	THD = 2%; sinewave drive; R4 = 100 kΩ; I_{line} = 15 mA					
single-ended; R_T = 150 Ω	I_p = 0 mA	$V_{o(rms)}$	*	0.22	–	V
	I_p = 2 mA	$V_{o(rms)}$	*	0.35	–	V
differential; R_T = 450 Ω	I_p = 0 mA	$V_{o(rms)}$	*	0.39	–	V
	I_p = 2 mA	$V_{o(rms)}$	*	0.64	–	V
differential; C_T = 47 nF; (100 Ω series resistor); f = 3400 Hz	I_p = 0 mA	$V_{o(rms)}$	*	0.57	–	V
	I_p = 2 mA	$V_{o(rms)}$	*	0.9	–	V

* Value to be fixed.

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Output voltage (RMS value)	I_p = 0 mA; THD = 10%; sinewave drive; R4 = 100 kΩ; single-ended; R_T = 150 Ω;					
	I_{line} = 4 mA	$V_{o(rms)}$	–	25	–	mV
	I_{line} = 7 mA	$V_{o(rms)}$	–	160	–	mV
Noise output voltage (RMS value)	I_{line} = 15 mA; R4 = 100 kΩ; psophometrically weighted (P53 curve); pin IR open					
	single-ended; R_T = 300 Ω	$V_{no(rms)}$	–	45	–	μV
	differential; R_T = 600 Ω	$V_{no(rms)}$	–	90	–	μV
Noise output voltage (RMS value)	in circuit of Fig. 23; S1 in position 2; 200 Ω between MIC+ and MIC−; single-ended; R_T = 300 Ω					
	R7 = 68 kΩ	$V_{no(rms)}$	–	100	–	μV
	R7 = 24.9 kΩ	$V_{no(rms)}$	–	65	–	μV
Gain adjustment input GAR (pin 6)						
Receiving amplifier, gain adjustment range		ΔG_v	−11	–	+8	dB
MUTE INPUT (pin 14)						
Input voltage HIGH		V_{IH}	1.5 + V_{SLPE}	–	V_{CC1} + 0.4	V
Input voltage LOW		V_{IL}	0	–	0.3 + V_{SLPE}	V
Input current		I_{mute}	–	11	20	μA
Change of microphone amplifier gain at mute-ON	MUTE = HIGH	$-\Delta G_v$	–	100	–	dB
Voltage gain from input DTMF-SLPE to QR+ output with mute-ON	MUTE = HIGH; single-ended load; R_L = 300 Ω	G_v	–	−18	–	dB

parameter	conditions	symbol	min.	typ.	max.	unit
Power-down input PD (pin 15)						
Input voltage HIGH		V_{IH}	1.5 + V_{SLPE}	–	V_{CC1} + 0.4	V
Input voltage LOW		V_{IL}	0	–	0.3 + V_{SLPE}	V
Input current		I_{PD}	–	5	10	μA
Automatic gain control input AGC (pin 18)						
Controlling the gain from IR (pin 13) to QR+, QR– (pins 4, 5) and the gain from MIC+, MIC– (pins 8, 9) to LN (pin 1)	R6 = 93.1 kΩ (between pins 18 and 11)					
gain control range with respect to I_{line} = 15 mA	I_{line} = 75 mA	$-G_v$	5.7	6.1	6.5	dB
Highest line current for maximum gain		I_{line}	–	24	–	mA
Lowest line current for minimum gain		I_{line}	–	61	–	mA
Change of gain between I_{line} = 15 and 35 mA		$-\Delta G_v$	0.9	1.4	1.9	dB
Microphone mute input DLS/$\overline{\text{MMUTE}}$ (pin 7)						
Input voltage low		V_{IL}	V_{EE}	–	V_{EE} + 0.3	V
Input current at low input voltage		I_{IL}	–85	–60	–35	μA
Release time after a low level on pin 7	C16 = 470 nF	t_{rel}	–	30	–	ms
Change of microphone amplifier gain at low input voltage on pin 7		$-\Delta G_v$	–	100	–	dB

DEVELOPMENT DATA

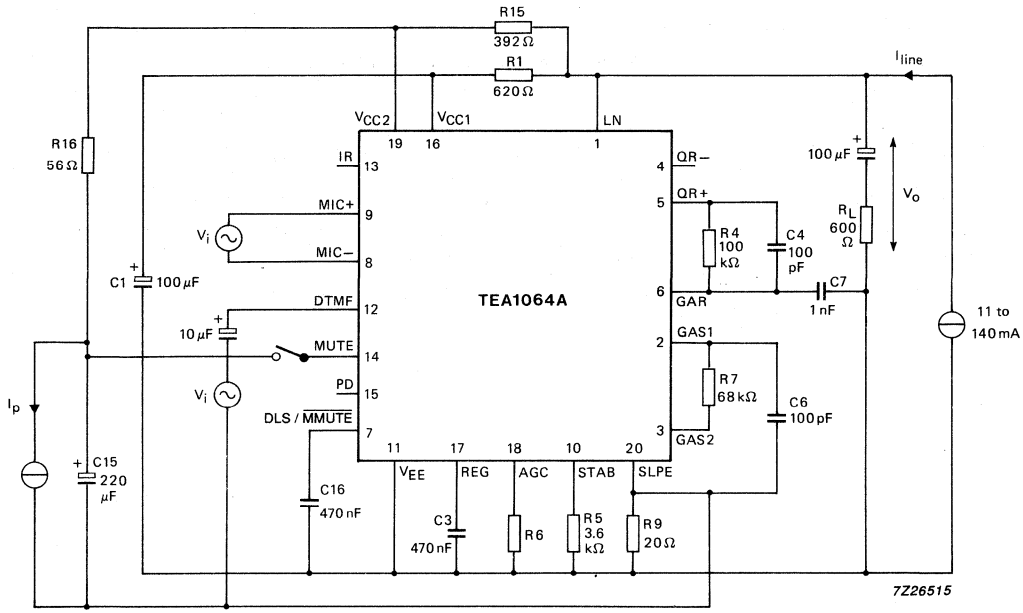


Fig. 22 Test circuit for defining voltage gain of MIC−, MIC+ and DTMF inputs; voltage gain (G_V) is defined as 20 log$|V_o/V_i|$. For measuring the gain from MIC+ and MIC− the MUTE input should be LOW or open-circuit; for measuring the DTMF input, the MUTE input should be HIGH. Inputs not being tested should be open-circuit.

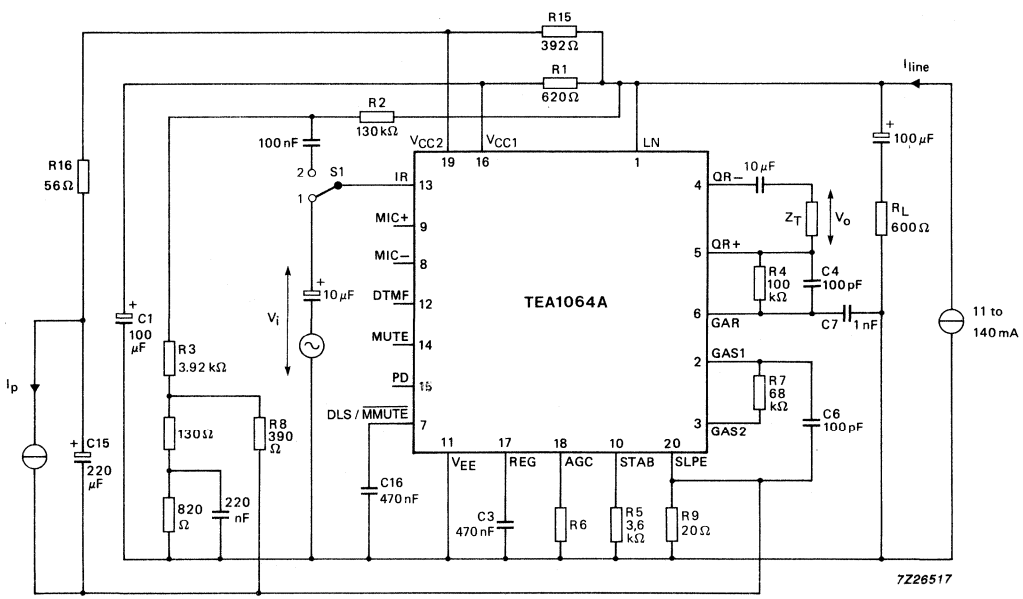


Fig. 23 Test circuit for defining voltage gain of the receiving amplifier, voltage gain (G_V) is defined as 20 log$|V_o/V_i|$ (with S1 in position 1).

APPLICATION INFORMATION

The basic application circuit is shown in Fig. 24 and some typical applications are shown in Figs 25, 26 and 27.

In the basic application, the circuit provides two possibilities for supplies to peripheral circuits:

- regulated line voltage V_{LN} (stabilized $V_{LN\text{-}SLPE}$) and unregulated supply voltage for peripheral circuits, the supply voltage is dependent only on the peripheral supply current. This application is the same as that used for TEA1060/TEA1061, TEA1067 and TEA1068;
- stabilized supply voltage for peripherals ($V_{CC2\text{-}SLPE}$), the DC line voltage depends on the current flowing to the peripheral circuits.

APPLICATION INFORMATION (continued)

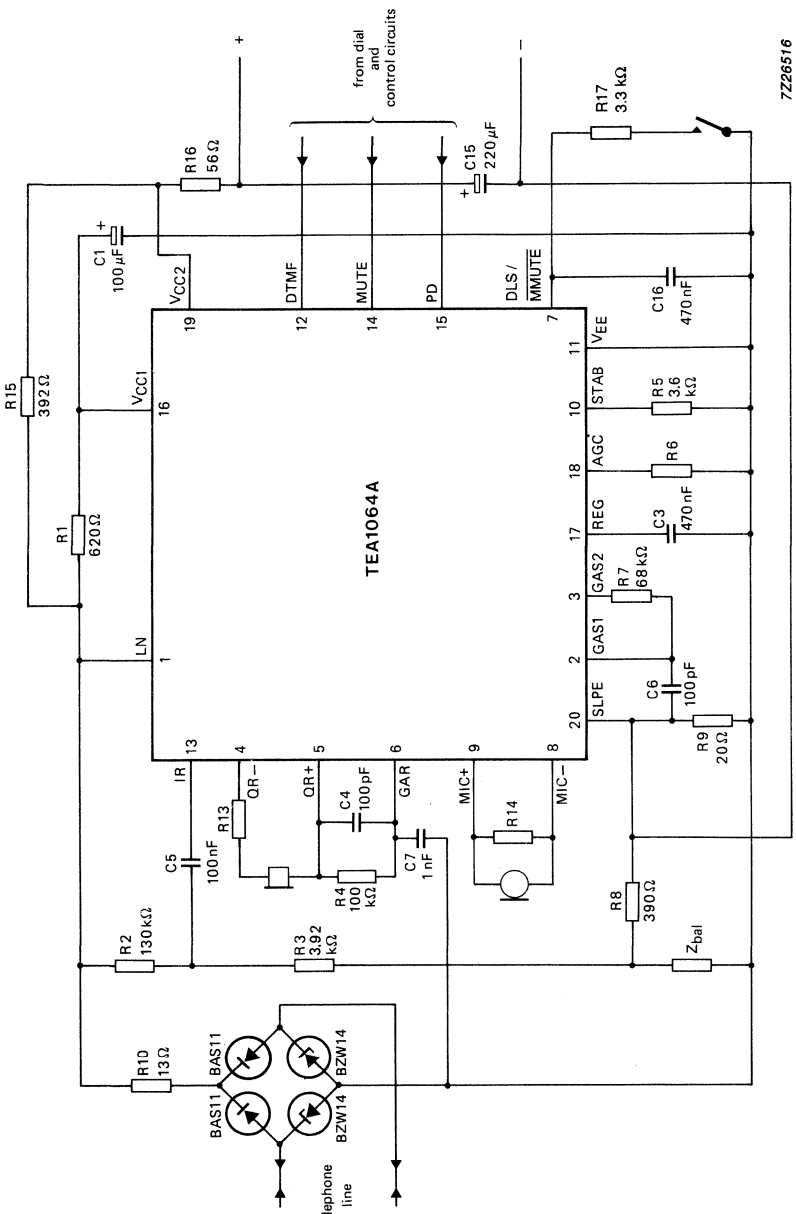


Fig. 24 Basic application of the TEA1064A with stabilized supply for peripherals, shown here with a piezo-electric earpiece and DTMF dialling. The diode bridge and R10 limit the current into, and the voltage across, the circuit during line transients. A different protection arrangement is required for pulse dialling or register recall.

For the basic application giving regulated line voltage the above circuit is changed as follows:

- R15 must be short-circuited;
- the value of R16 is changed to 392 Ω;
- the value of C3 is changed to 4.7 μF.

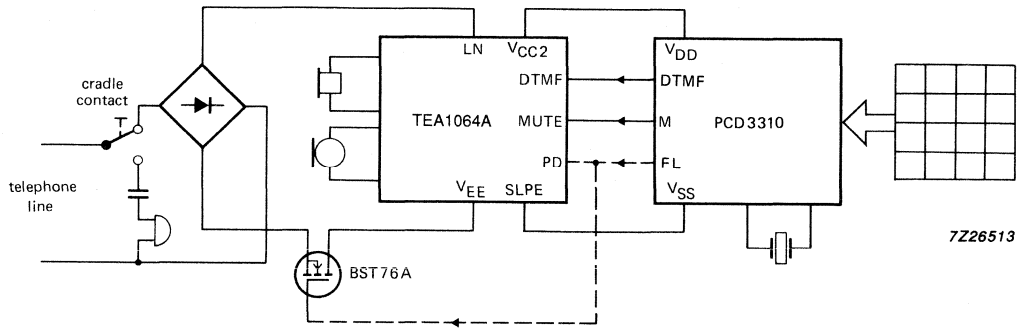


Fig. 25 Typical DTMF-pulse set application circuit (simplified) showing the TEA1064A with the CMOS bilingual dialling circuit PCD3310; the broken line indicates optional flash (register recall by timed loop break).

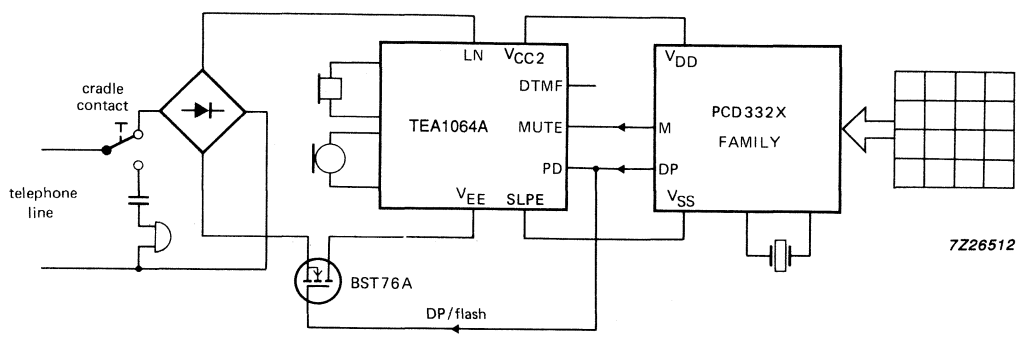


Fig. 26 Typical pulse dial set application circuit (simplified) showing the TEA1064A with one of the PCD332X family of CMOS interrupted current-loop dialling circuits.

APPLICATION INFORMATION (continued)

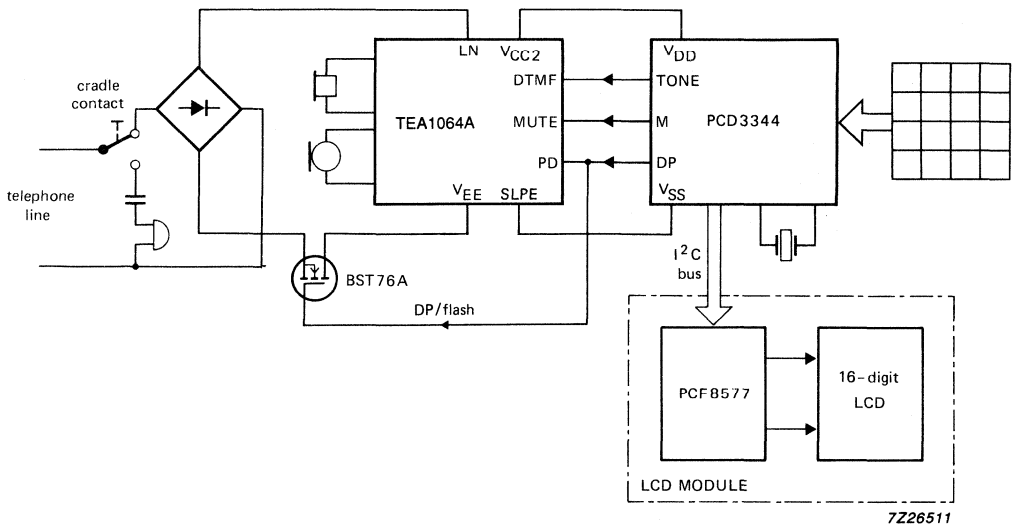


Fig. 27 Typical dual-standard (pulse and DTMF) feature phone application circuit (simplified) showing the TEA1064A and the PCD3344 CMOS telephone microcontroller with on-chip DTMF generator plus I^2C-bus.

Low voltage versatile telephone transmission circuit with dialler interface and transmit level dynamic limiting

TEA1064B

FEATURES

- Low DC line voltage; operates down to 1.8 V (excluding polarity guard)
- Voltage regulator with low voltage drop and adjustable static resistance
- DC line voltage adjustment facility
- Provides a supply for external circuits
- Dynamic limiting (speech-controlled) in transmit direction prevents distortion of line signal and sidetone
- Symmetrical high-impedance inputs (64 kΩ) for dynamic, magnetic or piezo-electric microphones
- Asymmetrical high-impedance input (32 kΩ) for electret microphones
- DTMF signal input
- Confidence tone in the earpiece during DTMF dialling
- Mute input for disabling speech during pulse or DTMF dialling
- Power-down input for improved performance during pulse dial or register recall (flash)
- Receiving amplifier for dynamic, magnetic or piezo-electric earpieces
- Large amplification setting ranges on microphone and earpiece amplifiers
- Line loss compensation (line current dependent) for microphone and earpiece amplifiers (not used for DTMF amplifier)
- Gain control curve adaptable to exchange supply
- Automatic disabling of the DTMF amplifier in extremely-low voltage conditions
- Microphone MUTE function available with switch
- MUTE, POWER-DOWN and DTMF input reference (pin V_{EE2}) can be connected either to V_{EE1} or SLPE.

GENERAL DESCRIPTION

The TEA1064B is a bipolar integrated circuit that performs all the speech and line interface functions required in fully electronic telephone sets. It performs electronic switching between dialling and speech. The IC operates at line voltages down to 1.8 V DC (with reduced performance) to facilitate the use of more telephone sets connected in parallel. The transmit signal on the line is dynamically limited (speech-controlled) to prevent distortion at high transmit levels of both the sending signal and the sidetone.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA1064B	20	DIL	plastic	SOT146
TEA1064BT	20	mini-pack	plastic	SO20; SOT163A

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{line}	line current operating range					
	normal operation	note 1	11	–	140	mA
	with reduced performance		2	–	11	mA
I_{CC}	internal supply current	V_{CC} = 2.8 V				
	power-down input LOW		–	1.3	1.6	mA
	power-down input HIGH		–	60	82	µA
G_v	voltage gain range					
	microphone amplifier		44	–	52	dB
	receiving amplifier		20	–	45	dB
	line loss compensation ranges					
G_v	gain control		5.7	6.1	6.5	dB
V_{exch}	exchange supply voltage		36	–	60	V
R_{exch}	exchange feeding bridge resistance		400	–	1000	Ω
$V_{LN(p-p)}$	maximum output voltage swing on LN (peak-to-peak value)	R16 = 392 Ω; I_{line} = 15 mA				
		I_p = 1.4 mA	3.55	3.80	4.05	V
		I_p = 2.7 mA	3.25	3.50	3.75	V
V_p	supply for peripherals	I_{line} = 15 mA				
		I_p = 1.4 mA	2.5	2.7	–	V
		I_p = 2.7 mA; $R_{REG-SLPE}$ = 20 kΩ	2.9	3.1	–	V
V_{LN}	DC line voltage	I_{line} = 15 mA				
		without $R_{REG-SLPE}$	3.25	3.5	3.75	V
		$R_{REG-SLPE}$ = 20 kΩ	4.05	4.4	4.75	V
T_{amb}	operating ambient temperature range		–25	–	+75	°C

Note

1. For the TEA1064BT the maximum line current depends on the heat dissipating qualities of the mounted device.

Low voltage versatile telephone transmission circuit with dialler interface and transmit level dynamic limiting

TEA1064B

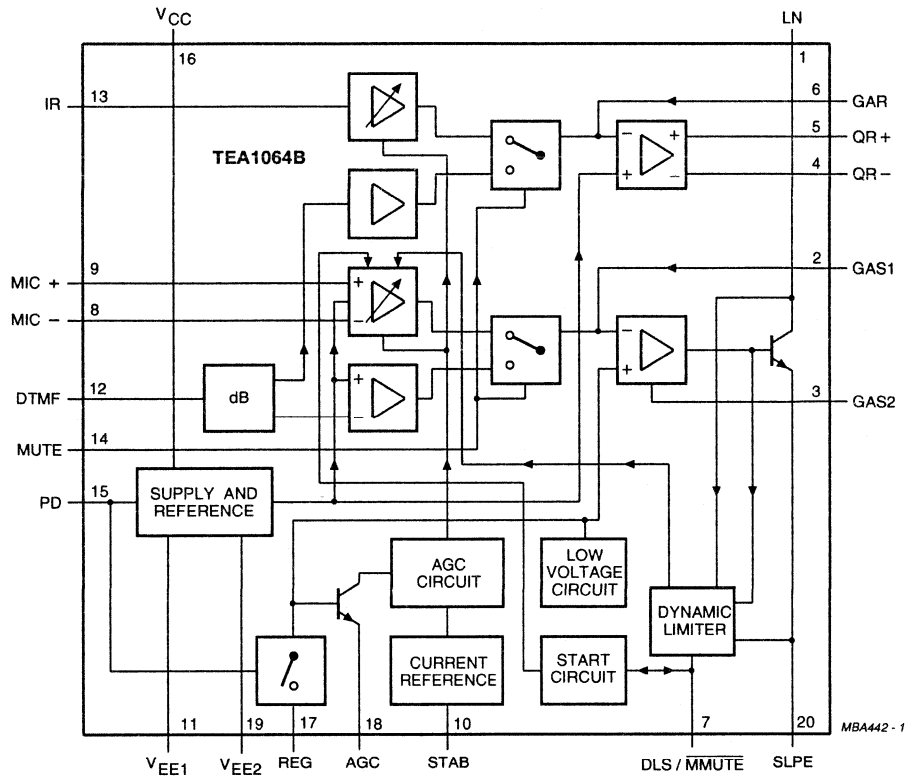


Fig.1 Block diagram.

Low voltage versatile telephone transmission circuit with dialler interface and transmit level dynamic limiting

TEA1064B

PINNING

SYMBOL	PIN	DESCRIPTION
LN	1	positive line terminal
GAS1	2	gain adjustment; transmitting amplifier
GAS2	3	gain adjustment; transmitting amplifier
QR–	4	inverting output; receiving amplifier
QR+	5	non-inverting output; receiving amplifier
GAR	6	gain adjustment; receiving amplifier
DLS/$\overline{\text{MMUTE}}$	7	decoupling for transmit amplifier dynamic and microphone MUTE input
MIC–	8	inverting microphone input
MIC+	9	non-inverting microphone input
STAB	10	current stabilizer
V_{EE1}	11	negative line terminal
DTMF	12	dual-tone multi-frequency input
IR	13	receiving amplifier input
MUTE	14	mute input
PD	15	power-down input
V_{CC}	16	internal supply decoupling
REG	17	voltage regulator decoupling
AGC	18	automatic gain control input
V_{EE2}	19	reference for POWER-DOWN (PD), MUTE and DTMF
SLPE	20	slope adjustment for DC curve/reference for peripheral circuits

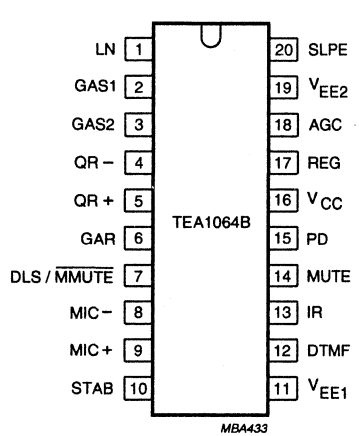


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Supplies V_{CC}, V_{EE2}, LN, SLPE, REG and STAB (Figs 3 and 5)

Power for the TEA1064B and its peripheral circuits is usually obtained from the telephone line. The IC develops its own supply voltage at V_{CC} and regulates its voltage drop. The internal supply requires a decoupling capacitor between V_{CC} and V_{EE1}. The internal current stabilizer is set by a 3.6 kΩ resistor between STAB and V_{EE1}.

The DC current flowing into the set is determined by the exchange supply voltage V_{exch}, the feeding bridge resistance R_{exch}, the subscriber line DC resistance R_{line} and the DC voltage (including polarity guard) on the subscriber set (see Fig.3).

The internal voltage regulator generates a temperature-compensated reference voltage that is available between LN and SLPE ($V_{ref} = V_{LN-SLPE}$ = 3.23 V typ.). This internal voltage regulator requires decoupling by a capacitor between REG and V_{EE1} (C3).

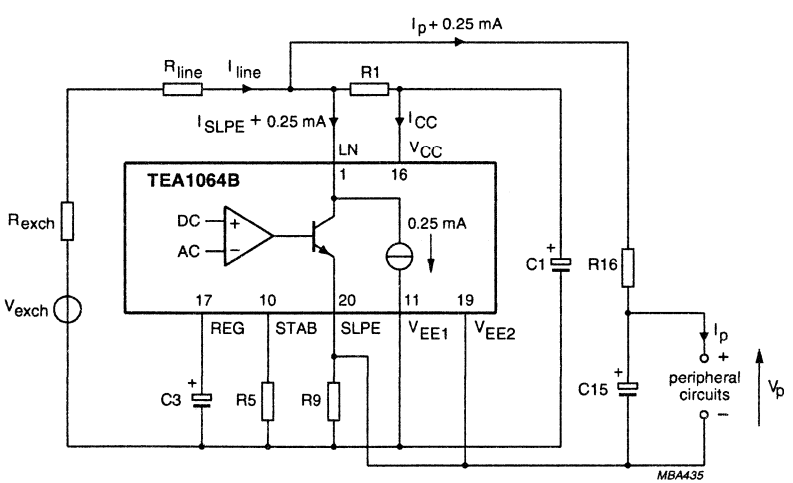
The configuration shown in Fig.3, gives a stabilized voltage across pins LN and SLPE which, applied via the low-pass filter R16, C15, provides a supply to the peripherals that is indendent of the line current and depends only on the peripheral supply current.

The value of R16 and the level of the DC voltage $V_{LN-SLPE}$ determine the supply capabilities. In the basic application R16 = 392 Ω and C15 = 220 µF. The worst-case peripheral supply current as a function of supply voltage is shown in Fig.4.

To increase the supply capabilities, the value of R16 can be decreased or the DC voltage $V_{LN-SLPE}$ can be increased by using $R_{VA(REG-SLPE)}$.

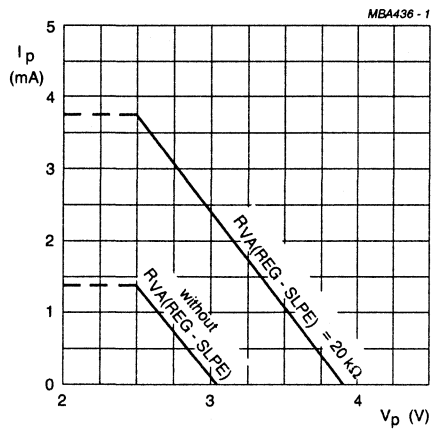
Note

The TEA1064B application is the same as is used for TEA1060/TEA1061, TEA1067 and TEA1068 integrated circuits.



The voltage $V_{LN-SLPE}$ is fixed to V_{ref} = 3.323 ±0.25 V.
Resistor R16 together with the line current determine the supply capabilities and the maximum output swing on the line (no loop damping is necessary).
The line voltage $V_{LN} = V_{ref} + (\{I_{line} - 1.55\ mA\} \times R9)$.

Fig.3 Supply arrangement with reference to SLPE.



I_{line} = 15 mA; R16 = 392 Ω; valid for MUTE = 0 and 1.
Line current has very little influence.

Fig.4 Maximum supply current with respect to Fig.3 for peripherals (I_p) as a function of the peripheral supply voltage (V_p).

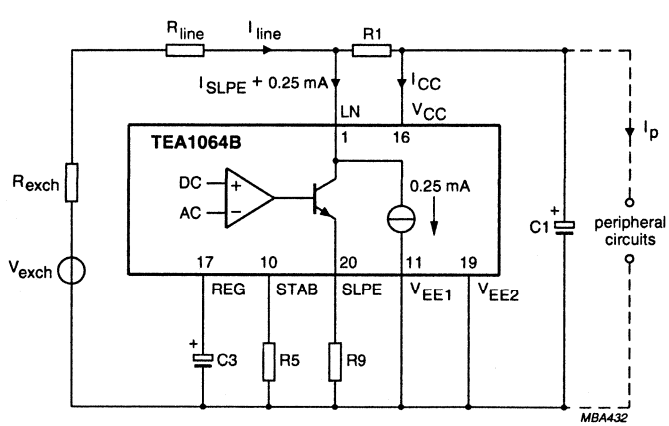
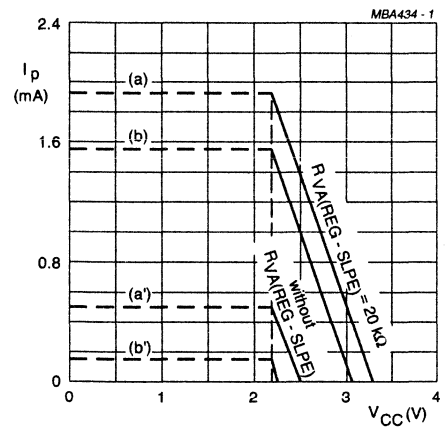


Fig.5 Supply arrangement with reference to V_{EE1}.



(a) I_p = 1.94 mA
(b) I_p = 1.54 mA
(a') I_p = 0.54 mA
(b') I_p = 0.16 mA
I_{line} = 15 mA
R1 = 620 Ω and R9 = 20 Ω
Curve (a) and (a') are valid when the receiving amplifier is not driven or when MUTE = HIGH.
Curve (b) and (b') are valid when the receiving amplifier is driven and when MUTE = LOW.
$V_{o(RMS)}$ = 150 mV, R_T = 150 Ω.

Fig.6 Maximum current I_p with respect to Fig.5 available from V_{CC} for peripheral circuitry with V_{CC} > 2.2 V.

The maximum AC output swing on the line at low currents is influenced by R16 (limited by current) and the maximum output swing on the line at high currents is influenced by DC voltage $V_{LN-SLPE}$ (limited by voltage). In both these situations, the internal dynamic limiter in the sending channel prevents distortion when the microphone is overdriven. The maximum AC output swing on LN is shown in Fig.7; practical values for R16 are from 200 Ω to 600 Ω and this influences both maximum output swing at low line currents and the supply capabilities.

When the SLPE pin is the reference for peripheral circuits, inputs MUTE, PD and DTMF must be referenced to SLPE. This is achieved by connecting pin V_{EE2} to pin SLPE; V_{EE2} being the reference of MUTE, PD and DTMF input stages.

Active microphones can be supplied between V_{CC} and V_{EE1} as shown in Fig.5. Low power circuits that provide MUTE, PD and DTMF inputs to the TEA1064B can also be powered from V_{CC} (see Fig.6 for the supply capability of V_{CC}). MUTE, PD and DTMF are then referenced to V_{EE1} and the pin V_{EE2} must therefore be connected to V_{EE1}.
If the line current I_{line} exceeds I_{CC} + 0.25 mA, the voltage converter shunts the excess current to SLPE via LN; where $I_{CC} \approx$ 1.3 mA, the value required by the IC for normal operation.

The DC line voltage on LN is:

- $V_{LN} = V_{LN\text{-}SLPE} + (I_{SLPE} \times R9)$
- $V_{LN} = V_{ref} + (\{I_{line} - I_{CC} - 0.25 \times 10^{-3}\ A\} \times R9)$

in which:

- V_{ref} = 3.23 V ± 0.25 V is the internal reference voltage between LN and SLPE; its value can be adjusted by external resistor R_{VA}.
- R9 = external resistor between SLPE and V_{EE1} (20 Ω in basic operation).

With R9 = 20 Ω, this results in:

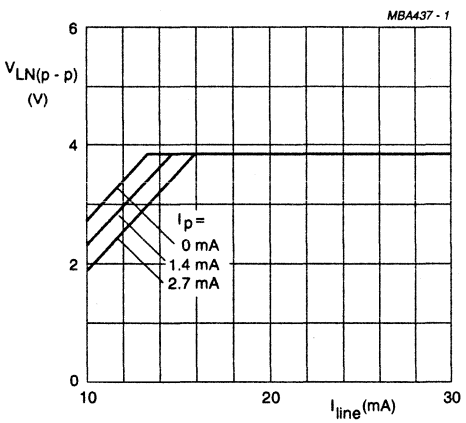
- V_{LN} = 3.3 ± 0.25 V at I_{line} = 15 mA
- V_{LN} = 4.1 ± 0.3 V at I_{line} = 15 mA, $R_{VA(REG\text{-}SLPE)}$ = 33 kΩ
- V_{LN} = 4.4 ± 0.35 V at I_{line} = 15 mA, $R_{VA(REG\text{-}SLPE)}$ = 20 kΩ

The preferred value for R9 is 20 Ω. Changing R9 influences microphone gain, DTMF gain, the gain control characteristics, sidetone and the DC characteristics (especially the low voltage characteristics).

In normal conditions, $I_{SLPE} >> (I_{CC}$ + 0.25 mA) and the static behaviour is equivalent to a voltage regulator diode with an internal resistance of R9. In the audio frequency range the dynamic impedance is determined mainly by R1. The equivalent impedance of the circuit in audio frequency range is shown in Fig.8.

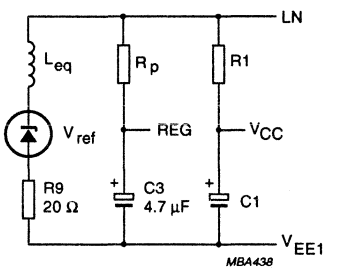
The internal reference voltage $V_{LN\text{-}SLPE}$ can be increased by external resistor $R_{VA(REG\text{-}SLPE)}$ connected between REG and SLPE. The voltage $V_{LN\text{-}SLPE}$ is shown as a function of $R_{VA(REG\text{-}SLPE)}$ in Fig.9. Changing the reference voltage influences the output swing of both sending and receiving amplifiers.

At line currents below 8 mA (typ.), the DC voltage dropped across the circuit is adjusted to a lower level automatically (approximately 1.8 V at 2 mA). This gives the possibility of operating more telephone sets in parallel with DC line voltages (excluding polarity guard) down to an absolute minimum of 1.8 V. At line currents below 8 mA (typ.), the circuit has limited sending and receiving levels.



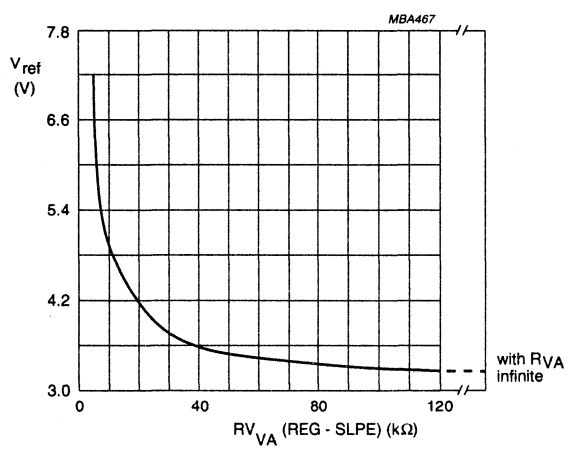
R16 = 392 Ω; I_p with respect to Fig.3.

Fig.7 Typical AC output swing at total harmonic distortion (THD) = 2% on the line as a function of line current with peripheral supply current as a parameter.



$L_{eq} = C3 \times R9 \times R_p$
R_p = 15 kΩ

Fig.8 Equivalent impedance between LN and V_{EE}.



$V_{LN} = V_{LN-SLPE} + (\{I_{line} - 1.55 \times 10^{-3}\ A\} \times R9)$.

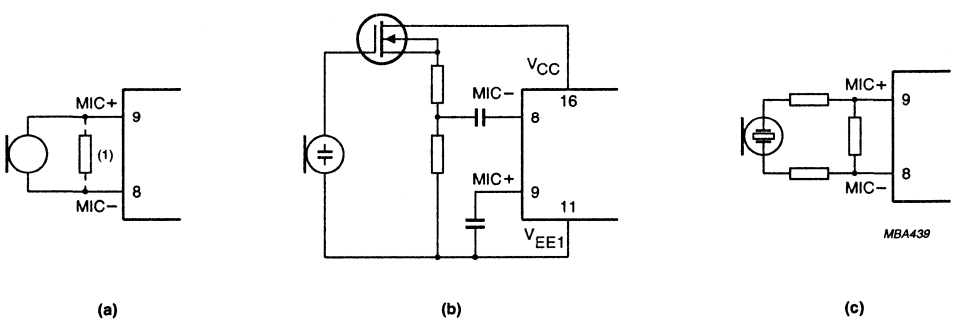
Fig.9 Internal reference voltage $V_{LN-SLPE}$ as a function of resistor $R_{VA(REG-SLPE)}$ for line currents between 11 mA and 140 mA.

Microphone inputs MIC+ and MIC– and gain pins GAS1 and GAS2

The TEA1064B has symmetrical microphone inputs, its input impedance is 64 kΩ (2 x 32 kΩ) and its voltage amplification is typicallly 52 dB with R7 = 68 kΩ. Either dynamic, magnetic or piezo-electric microphones can be used, or an electret microphone with a built-in FET buffer. Arrangements for the microphone types are shown in Fig.10.

The gain of the microphone amplifier is proportional to external resistor R7 connected between GAS1 and GAS2 and with this it can be adjusted between 44 dB and 52 dB to suit the sensitivity of the transducer.

An external 100 pF capacitor (C6) is required between GAS1 and SLPE to ensure stability. A larger value of C6 may be chosen to obtain a first-order low-pass filter with a cut-off frequency corresponding to the time constant R7 x C6.



Resistor (1) may be connected to reduce the terminating impedance, or for sensitive types a resistive attenuator can be used to prevent overloading the microphone inputs.

Fig.10 Microphone arrangements (a) magnetic or dynamic microphone (b) electret microphone (c) piezo-electric microphone currents.

Dynamic limiter (microphone) pin DLS/$\overline{\text{MMUTE}}$

A low level at the DLS/$\overline{\text{MMUTE}}$ pin inhibits the microphone inputs MIC+ and MIC– but has no influence on the receiving and DTMF amplifiers.
Removing the low level at the DLS/$\overline{\text{MMUTE}}$ pin provides the normal function of the microphone amplifier after a short time determined by the capacitor connected to DLS/$\overline{\text{MMUTE}}$ pin. The microphone mute function can be realised by a simple switch as shown in Fig.11.

To prevent distortion of the transmitted signal, the gain of the sending amplifier is reduced rapidly when peaks of the signal on the line exceed an internally-determined threshold. The time in which gain reduction is effected (attack time) is very short. The circuit stays in the gain-reduced condition until the peaks of the sending signal remain below the threshold level. The sending gain then returns to normal after a a time determined by the capacitor connected to DLS/$\overline{\text{MMUTE}}$ (release time).

The internal threshold adapts automatically to the DC voltage setting of the circuit ($V_{LN\text{-}SLPE}$). This means that the maximum output swing on the line will be higher if the DC voltage dropped across the circuit is increased. Fig.12 shows the maximum possible output swing on the line as a function of the DC voltage drop ($V_{LN\text{-}SLPE}$) with I_{line} -I_p as a parameter.

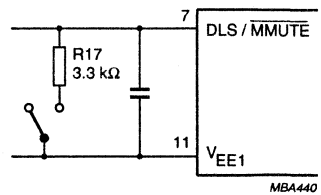
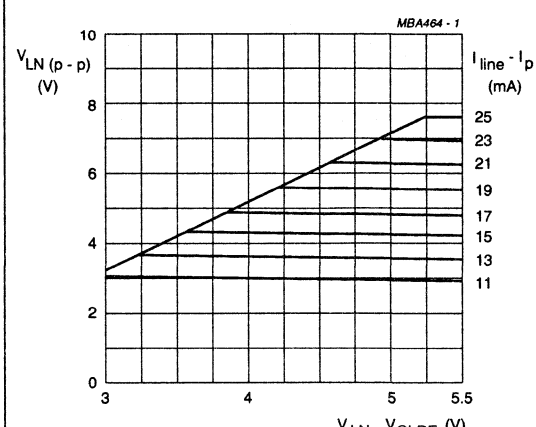


Fig.11 Microphone-mute function.

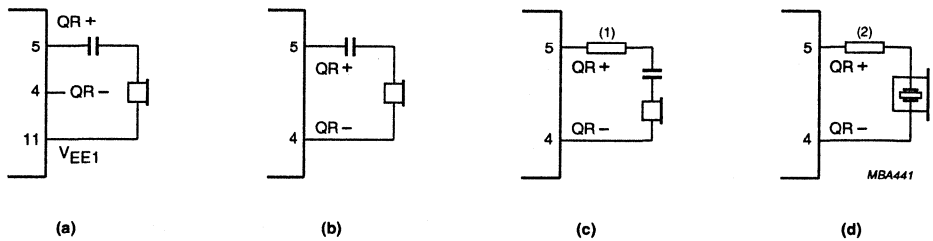
The internal threshold level is lowered automatically if the DC current in the transmit output stage is insufficient. This prevents distortion of the sending signal in applications using parallel-connected telephones or telephones operating over long lines, for example.

Dynamic limiting also considerably improves sidetone performance in over-drive conditions (less distortion; limited sidetone level).



R16 = 392 Ω.

Fig.12 Typical output swing on line as a function of the DC voltage drop $V_{LN\text{-}SLPE}$ with I_{line} - I_p as a parameter.

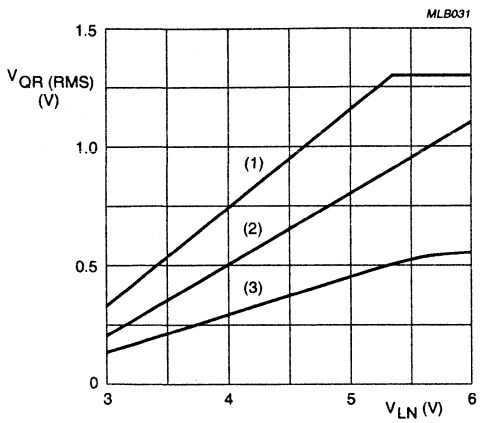


Resistor (1) may be connected to prevent distortion (inductive load).
Resistor (2) is required to increase the phase margin (stability with capacitive load).

Fig.13 Alternative receiver arrangements (a) dynamic earpiece with an impedance less than 450 Ω (b) dynamic earpiece with an impedance more than 450 Ω (c) magnetic earpiece with an impedance more than 450 Ω (d) piezo-electric earpiece.

Receiving amplifier IR, QR+, QR− and GAR

The receiving amplifier has one input IR and two complimentary outputs, QR+ (non-inverting) and QR− (inverting). These outputs may be used for single-ended or differential drive, depending on the type and sensitivity of the earpiece used (see Fig.13). Gain from IR to QR+ is typically 31 dB with R4 = 100 kΩ, sufficient for low-impedance magnetic or dynamic earpieces which are suitable for single-ended drive. By using both outputs (differential drive) the gain is increased by 6 dB. Differential drive can be used when the earpiece impedance exceeds 450 Ω as with high-impedance dynamic, magnetic or piezo-electric earpieces.



Valid for both options; THD = 2%, I_{line} = 15 mA.
Curve (1) is for a differential load of 47 nF (series resistance = 100 Ω; f = 3400 Hz.
Curve (2) is for a differential load of 450 Ω; f = 1 kHz.
Curve (3) is for a single-ended load of 150 Ω; f = 1 kHz.

Fig.14 Typical output swing of the receiving amplifier as a function of DC voltage drop V_{LN} with the load at the receiver output as parameter.

The output voltage of the receiving amplifier is specified for continuous-wave drive. Fig.14 shows the maximum output swing of the receiving amplifier as a function of the DC voltage drop (V_{LN}). The maximum output voltage will be higher under speech conditions, where the ratio of the peak to the RMS value is higher.

The gain of the receiving amplifier can be adjusted to suit the sensitivity of the transducer used. The adjustment range is between 20 dB and 39 dB with single-ended drive and between 26 dB and 45 dB with differential drive. The gain is proportional to the external resistor R4 connected between GAR and QR+. The overall gain between LN and QR+ can be found by subtracting the attenuation of the anti-sidetone network (32 dB) from the amplifier gain.

Two external capacitors (C4 = 100 pF and C7 = 10 x C4 = 1 nF) ensure stability. A larger value may be chosen to obtain a first-order low-pass filter. The cut-off frequency corresponds with time constant R4 x C4. The relationship C7 = 10 x C4 must be maintained.

Automatic gain control input AGC

Automatic compensation of line loss is obtained by connecting a resistor (R6) between AGC and V_{EE1}. This automatic gain control varies the gain of the microphone amplifier and receiving amplifier in accordance with the DC line current. The control range is 6.1 dB; this corresponds to a 5 km line of 0.5 dB diameter copper twisted-pair cable (DC resistance = 176 Ω/km, average attenuation = 1.2 dB/km). The DTMF gain is not affected by this feature.

The value of R6 must be chosen with reference to the exchange supply voltage and its feeding bridge resistance (see Fig.15 and Table 1). Different values of R6 give the same line current ratios at the start and the end of the control range. If automatic line-loss compensation is not required the AGC pin can be left open-circuit, the amplifiers then provide their maximum gain.

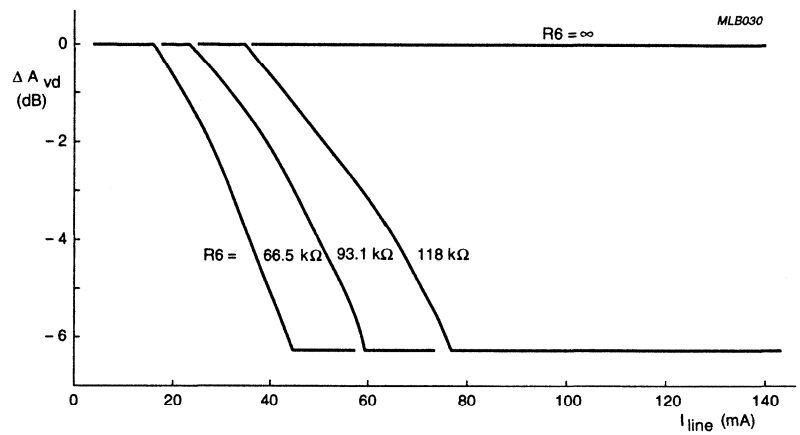


Fig.15 Variation of gain as a function of line current with R6 as a parameter; R9 = 20 Ω.

Table 1 Values of R6 giving optimum line-loss compensation at various values of exchange supply voltage (V_{exch}) and exchange feeding bridge resistance (R_{exch}); R9 = 20 Ω

		R_{exch} (Ω)			
		400	600	800	1000
		R6 (kΩ)			
V_{exch} (V)	35	84.5	66.5	x	x
	48	118	93.1	77.8	66.5
	60	x	x	97.6	84.5

V_{EE2} input

V_{EE2} is the reference for MUTE, POWER-DOWN and DTMF inputs. These signals are referenced to V_{EE1} when generated by peripherals powered between V_{CC} and V_{EE1}, but they can also be referenced to SLPE when peripherals are powered as shown in Fig.3. In the first instance (reference to V_{EE1}), V_{EE2} has to be connected to V_{EE1}. In the second instance (reference to SLPE), V_{EE2} has to be connected to SLPE.

MUTE input (see notes 1 and 2)

MUTE = HIGH enables the DTMF input and inhibits the microphone and receiving amplifier inputs.

MUTE = LOW or open-circuit disables the DTMF input and enables the microphone and receiving amplifier inputs.

Switching MUTE gives negligible clicks at the telephone outputs and on the line.

Dual-tone multi-frequency input DTMF (see note 1)

When the DTMF input is enabled, dialling tones may be sent on the line. The voltage gain between DTMF-V_{EE2} and LN-V_{EE1} is typically 26.5 dB less than the gain of the microphone amplifier and varies with R7 in the same way as the gain of the microphone amplifier. This means that the tone level at the DTMF input has to be adjusted after setting the gain of the microphone amplifier.
With R7 = 68 kΩ the gain is typically 25.5 dB.

The signalling tones can be heard in the earpiece at a low level (confidence tone).

Power-down input PD (see notes 1 and 2)

During pulse dialling or register recall (timed loop break) the telephone line is interrupted; as a consequence it provides no supply for the transmission circuit connected to V_{CC} or for the peripherals between V_{LN} and SLPE. These supply gaps are bridged by the charges in the capacitors C1 and C15. The requirements on these capacitors are eased by an applied HIGH level to the PD input during the time of the loop break. This reduces the internal supply current I_{CC1} from 1.3 mA (typ.) to 60 μA (typ.) and switches off the voltage regulator to prevent discharge via LN to V_{CC2}.

A HIGH level at PD also internally disconnects the capacitor at REG so that the voltage stabilizer has no switch-on delay after line interruptions. This minimizes the contribution of the IC to the current waveform during pulse dialling or register recall.

When the power-down facility is not required, the PD pin can be left open-circuit or connected to V_{EE2}.

Sidetone suppression

Suppression of the transmitted signal in the earpiece is obtained by the anti-sidetone network comprising R1//Z_{line}, R2, R3, R8, R9 and Z_{bal} (see Fig.16). Maximum compensation is obtained when the following conditions are fulfilled:

(a) $R9 \times R2 = R1 \times (R3 + \{R8//Z_{bal}\})$

(b) $(Z_{bal}/\{Z_{bal} + R8\}) = (Z_{line}/\{Z_{line} + R1\})$

If fixed values are chosen for R1, R2, R3 and R9, then condition (a) is always fulfilled provided $|R8//Z_{bal}| \ll R3$

To obtain optimum sidetone suppression, condition (b) has to be fulfilled, resulting in:

$$Z_{bal} = (R8/R1) \times Z_{line} = k \times Z_{line}$$

Where k is a scale factor; k = (R8/R1).

The scale factor k (value of R8) is chosen to meet the following criteria:

- compatibility with a standard capacitor from the E6 or E12 range for Z_{bal}
- $|Z_{bal}//R8| \ll R3$ to fulfill condition (a) and thus ensure correct anti-sidetone bridge operation
- $|Z_{bal} + R8| \gg R9$ to avoid influencing the transmit gain

In practise Z_{line} varies considerably with the line length and line type. Therefore the value chosen for Z_{bal} should be for an average line length giving satisfactory sidetone suppression with short and long lines. The suppression also depends on the accuracy of the match between Z_{bal} and the impedance of the average line.

EXAMPLE

The line impedance for which optimum suppression is to be obtained can be represented by 210 Ω + (1265 Ω//140 nF). This represents a 5 km line of 0.5 mm diameter copper twisted-pair cable matched with 600 Ω (176 Ω/km; 38 nF/km).

With k = 0.64 this results in : R8 = 390 Ω; Z_{bal} = 130 Ω + (820 Ω//220 nF).

The anti-sidetone network for the TEA1060 family shown in Fig.16 attenuates the signal received from the line by 32 dB before it enters the receiving amplifier. The attenuation is almost constant over the whole audio-frequency range.

Alternatively a conventional Wheatstone bridge can be used as an anti-sidetone circuit (see Fig.17). Both bridge types can be used with either resistive or complex set impedances. (More information on the balancing of anti-sidetone bridges can be obtained in our publication 'Versatile speech transmission ICs for electronic telephone sets', order number 9398 341 10011).

Notes

1. The reference level used for the MUTE, DTMF and PD inputs is V_{EE2}.
2. A LOW level for any of these pins is defined by connection to V_{EE2}, a HIGH level is defined as a voltage greater than V_{EE2} + 1.5 V and smaller than V_{CC} + 0.4 V.

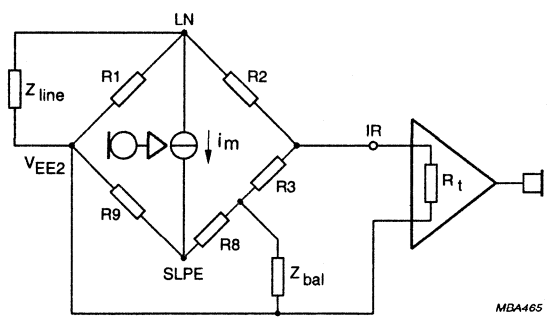


Fig.16 Equivalent circuit of TEA1060 family anti-sidetone bridge.

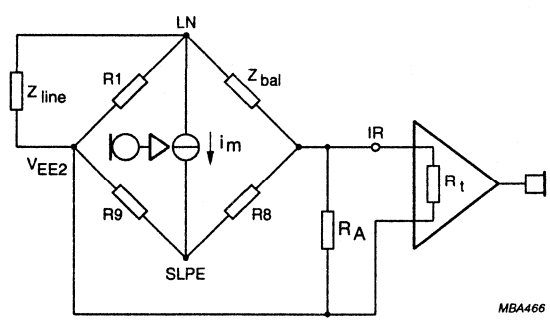


Fig.17 Equivalent circuit of an anti-sidetone network in the Wheatstone bridge configuration.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{LN}	positive line voltage continuous		–	12	V
V_{LN}	repetitive line voltage during switch-on line interruption		–	13.2	V
V_{LN}	repetitive peak line voltage one 1 ms pulse per 5 s	R9 = 20 Ω; R10 = 13 Ω; see Fig.22	–	28	V
I_{LN}	line current	R9 = 20 Ω			
	TEA1064B	note 1	–	140	mA
	TEA1064BT	note 1	–	140	mA
V_i	input voltage on pins other than LN		V_{EE1}–0.7	V_{CC}+0.7	V
P_{tot}	total power dissipation	R9 = 20 Ω; note 2			
	TEA1064B		–	717	mW
	TEA1064BT		–	555	mW
T_{amb}	operating ambient temperature		–25	+75	°C
T_{stg}	storage temperature		–40	+125	°C
T_j	junction temperature		–	+125	°C

Notes

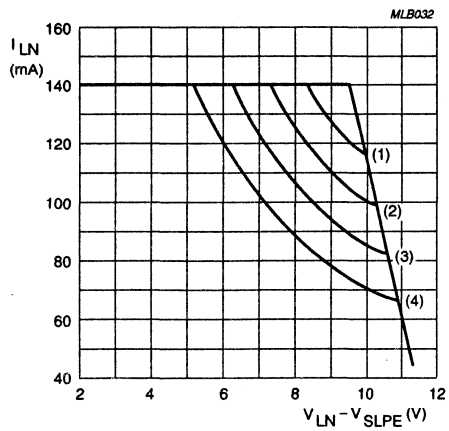
1. Mostly dependent on the maximum required T_{amb} and on the voltage between LN and SLPE. See Figs18 and 19 to determine the current as a function of the required voltage and the temperature.
2. Calculated for the maximum ambient temperature specified T_{amb} = 75 °C and a maximum junction temperature of 125 °C.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	SOT146	70 K/W
	SOT163A (note 1)	90 K/W

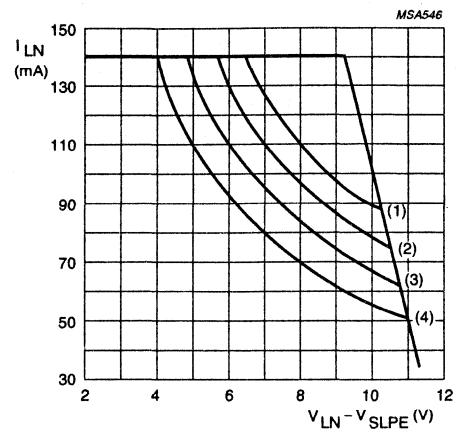
Note

1. Mounted on glass epoxy board 41 x 19 x 1.5 mm.



(1) T_{amb} = 45 °C; P_{tot} = 1143 mW.
(2) T_{amb} = 55 °C; P_{tot} = 1000 mW.
(3) T_{amb} = 65 °C; P_{tot} = 857 mW.
(4) T_{amb} = 75 °C; P_{tot} = 714 mW.

Fig.18 TEA1064B safe operating area.



(1) T_{amb} = 45 °C; P_{tot} = 888 mW.
(2) T_{amb} = 55 °C; P_{tot} = 777 mW.
(3) T_{amb} = 65 °C; P_{tot} = 666 mW.
(4) T_{amb} = 75 °C; P_{tot} = 555 mW.

Fig.19 TEA1064BT safe operating area.

CHARACTERISTICS

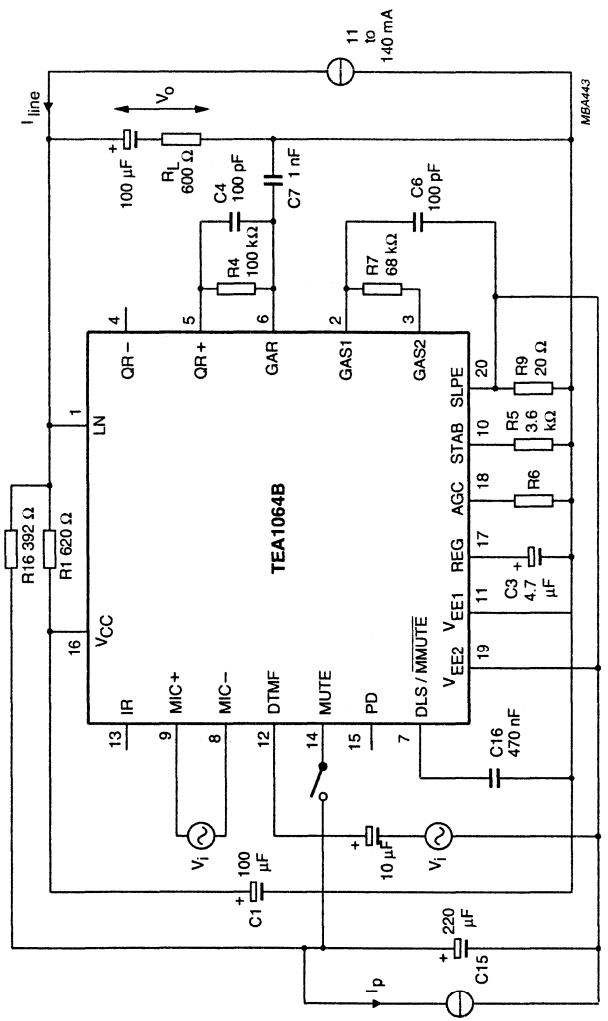
I_{line} = 11 to 140 mA; V_{EE1} = 0 V; f = 800 Hz; T_{amb} = 25 °C; R_L = 600 Ω; tested in the circuits of Fig.20 or Fig.21; V_{EE2} connected to SLPE; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies LN and V_{CC} (pins 1 and 16)						
V_{LN}	DC line voltage: voltage drop between LN and V_{EE1}	MIC–, MIC+ inputs open-circuit; without R_{VA}				
		I_{line} = 2 mA	–	1.8	–	V
		I_{line} = 4 mA	–	2.2	–	V
		I_{line} = 7 mA	–	3.2	–	V
		I_{line} = 11 mA	–	3.4	–	V
		I_{line} = 15 mA	3.25	3.5	3.75	V
		I_{line} = 100 mA	–	5.25	6.05	V
		I_{line} = 140 mA	–	6.1	7.0	V
$\Delta V_{LN}/\Delta T$	variation with temperature	I_{line} = 15 mA	–3	–1	+1	mV/K
V_{LN}	voltage drop over circuit with R_{VA} connected between REG and SLPE					
		R_{VA} = 33 kΩ	3.8	4.1	4.4	V
		R_{VA} = 20 kΩ	4.05	4.4	4.75	V
I_{CC}	internal supply current into pin 16	V_{CC} = 2.8 V				
		PD = LOW	–	1.3	1.6	mA
		PD = HIGH	–	60	82	μA
V_{CC}	supply voltage available for peripheral circuitry V_{EE2} connected to V_{EE1}	I_{line} = 15 mA; MUTE = HIGH; see Fig.5				
		I_p = 0.54 mA	2.2	2.4	–	V
		I_p = 0 mA	2.5	2.7	–	V
V_p	supply voltage available for peripheral circuitry	I_{line} = 15 mA				
		I_p = 1.4 mA	2.5	2.7	–	V
		I_p = 2.7 mA; $R_{REG-SLPE}$ = 20 kΩ	2.9	3.1	–	V
Microphone inputs MIC– and MIC+ (pins 8 and 9)						
Z_I	input impedance					
	differential		51	64	77	kΩ
	single-ended		25.5	32.0	38.5	kΩ
CMRR	common mode rejection ratio		–	82	–	dB
G_v	voltage gain (see Fig.20)	I_{line} = 15 mA; R7 = 68 kΩ	51	52	53	dB
$\Delta G_v/\Delta f$	variation of G_v with frequency referred to 0.8 kHz	f = 300 and 3400 Hz	–0.5	±0.1	+0.5	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\Delta G_v/\Delta T$	variation of G_v with temperature referred to 25 °C	without R6; I_{line} = 50 mA; T_{amb} = −25 to +75 °C	–	±0.2	–	dB
DTMF input (pin 12)						
Z_i	input impedance		16.8	20.7	24.6	kΩ
G_v	voltage gain (see Fig.20)	I_{line} = 15 mA; R7 = 68 kΩ	24.5	25.5	26.5	dB
$\Delta G_v/\Delta f$	variation of G_v with frequency referred to 0.8 kHz					
		f = 300 and 3400 Hz	−0.5	±0.01	+0.5	dB
		f = 697 and 1633 Hz	−0.2	±0.05	+0.2	dB
$\Delta G_v/\Delta T$	variation of G_v with temperature referred to 25 °C	I_{line} = 50 mA; T_{amb} = −25 to +75 °C	–	±0.2	0.5	dB
Gain adjustment inputs GAS1 and GAS2 (pins 2 and 3)						
ΔG_v	transmitting amplifier gain adjustment range		−8	–	+0	dB
Sending amplifier output LN (pin 1)						
DYNAMIC LIMITER						
$V_{LN(p-p)}$	output voltage swing (peak-to-peak value)	I_{line} = 15 mA; R7 = 68 kΩ; $V_{i(RMS)}$ = 3.6 mV	3.4	3.8	4.2	V
THD	total harmonic distortion					
		V_i = 3.6 mV +10 dB	–	1.5	–	%
		V_i = 3.6 mV +15 dB	–	2.8	–	%
$V_{LN(p-p)}$	output voltage swing (peak-to-peak value)	V_i = 3.6 mV +10 dB				
		I_p = 1.4 mA	3.55	3.8	4.05	V
		I_p = 2.7 mA	3.25	3.5	3.75	V
		I_p = 0 mA; I_{line} = 7 mA	–	1.8	–	V
		I_p = 0 mA; I_{line} = 4 mA	–	0.9	–	V
	dynamic behaviour of limiter	C16 = 470 nF				
t_{att}	attack time V_{mic} jumps from 2 mV to 40 mV		–	1.5	5.0	ms
t_{rel}	release time V_{mic} jumps from 40 mV to 2 mV		50	150	–	ms
$V_{no(RMS)}$	noise output voltage (RMS value)	I_{line} = 15 mA; R7 = 68 kΩ; 200 Ω between MIC− and MIC+; psophometrically weighted (P53 curve)	–	−72	–	dBmp

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Receiving amplifier input IR (pin 13)						
Z_i	input impedance		17	21	25	kΩ
Receiving amplifier outputs QR– and QR+ (pins 4 and 5)						
Z_o	output impedance	single-ended	–	4	–	Ω
G_v	voltage gain (see Fig.21)	I_{line} = 15 mA; R4 = 100 kΩ				
	single-ended	R_T = 300 Ω	30	31	32	dB
	differential	R_T = 600 Ω	36	37	38	dB
$\Delta G_v/\Delta f$	variation of G_v with frequency referred to 0.8 kHz	f = 300 and 3400 Hz	–0.5	–0.2	0	dB
$\Delta G_v/\Delta T$	variation of G_v with temperature referred to 25 °C	without R6; I_{line} = 50 mA; T_{amb} = –25 to +75 °C	–	±0.2	–	dB
$V_{o(RMS)}$	output voltage (RMS value)	TDA = 2%; sinewave drive; R4 = 100 kΩ; I_{line} = 15 mA				
	single-ended	R_T = 150 Ω	–	0.2	–	V
	differential	R_T = 450 Ω	–	0.37	–	V
	differential	C_T = 47 nF; R_s = 100 Ω; f = 3400 Hz	–	0.52	–	V
$V_{o(RMS)}$	output voltage (RMS value)	I_p = 0 mA; TDA = 10%; sinewave drive; R4 = 100 kΩ; R_T = 150 Ω				
		I_{line} = 4 mA	–	20	–	mV
		I_{line} = 7 mA	–	160	–	mV
$V_{no(RMS)}$	noise output voltage (RMS value)	I_{line} = 15 mA; R4 = 100 kΩ; psophometrically weighted (P53 curve); pin IR open-circuit				
	single-ended	R_T = 300 Ω	–	45	–	μV
	differential	R_T = 600 Ω	–	90	–	μV
$V_{no(RMS)}$	noise output voltage (RMS value)	see Fig.21; S1 in position 2; 200 Ω between MIC– and MIC+; single-ended; R_T = 300 Ω				
		R7 = 68 kΩ	–	100	–	μV
		R7 = 24.9 kΩ	–	65	–	μV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Gain adjustment input GAR (pin 6)						
ΔG_v	receiving amplifier gain adjustment range		−11	–	+8	dB
MUTE input (pin 14)						
V_{IH}	HIGH level input voltage		1.5 +V_{EE2}	–	V_{CC} +0.4	V
V_{IL}	LOW level input voltage		0	–	0.3 +V_{EE2}	V
I_{mute}	input current		–	11	20	μA
ΔG_v	change of microphone amplifier gain at mute on	MUTE = HIGH	–	−100	–	dB
G_v	voltage gain from input DTMF-SLPE to QR+ output with mute on	MUTE = HIGH; single-ended load; R_L = 300 Ω	–	−18	–	dB
Power-down input PD (pin 15)						
V_{IH}	HIGH level input voltage		1.5 +V_{EE2}	–	V_{CC1} +0.4	V
V_{IL}	LOW level input voltage		0	–	0.3 +V_{EE2}	V
I_{PD}	input current		–	5	10	μA
Automatic gain control input AGC (pin 18)						
	controlling the gain from IR (pin13) to QR+, QR− (pins 4, 5) and the gain from MIC+, MIC− (pins 8, 9) to LN (pin 1)	R6 = 93.1 kΩ (between pins 18 and 11)				
G_v	gain control range with respect to I_{line} = 15 mA	I_{line} = 75 mA	−5.7	−6.1	−6.5	dB
I_{line}	highest line current for maximum gain		–	24	–	mA
I_{line}	lowest line current for minimum gain		–	61	–	mA
ΔG_v	change of gain between I_{line} = 15 and 35 mA		−0.9	−1.4	−1.9	dB
Microphone mute input DLS/$\overline{\text{MMUTE}}$ (pin 7)						
V_{IL}	LOW level input voltage		V_{EE1}	–	V_{EE1} +0.3	V
I_{IL}	input current at LOW level input voltage		−85	−60	−35	μA
t_{rel}	release time after a LOW level on pin 7	C16 = 470 nF	–	30	–	ms
ΔG_v	change of microphone amplifier gain at LOW level input voltage on pin 7		–	−100	–	dB



For measuring gain from MIC+ amd MIC− the MUTE input should be LOW or open-circuit.
For measuring the DTMF input, the MUTE input should be HIGH.
Inputs not being tested should be open-circuit.

Fig.20 Test circuit for defining voltage gain of MIC−, MIC+ and DTMF inputs; voltage gain (G_v) is defined as $20\log|V_o/V_i|$.

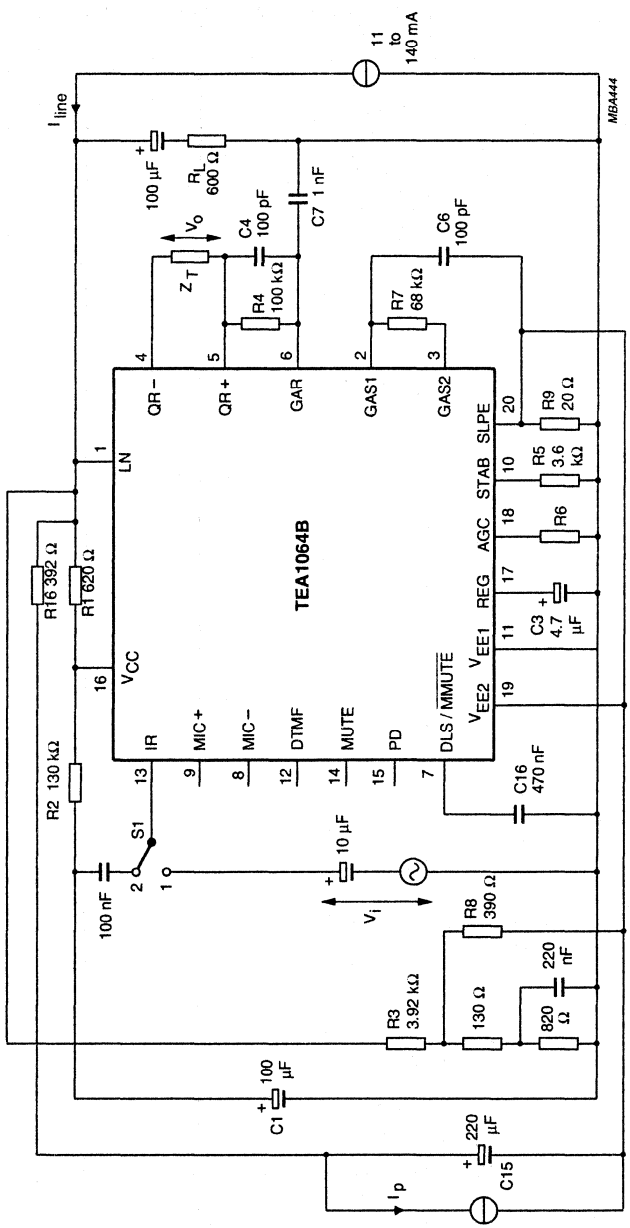
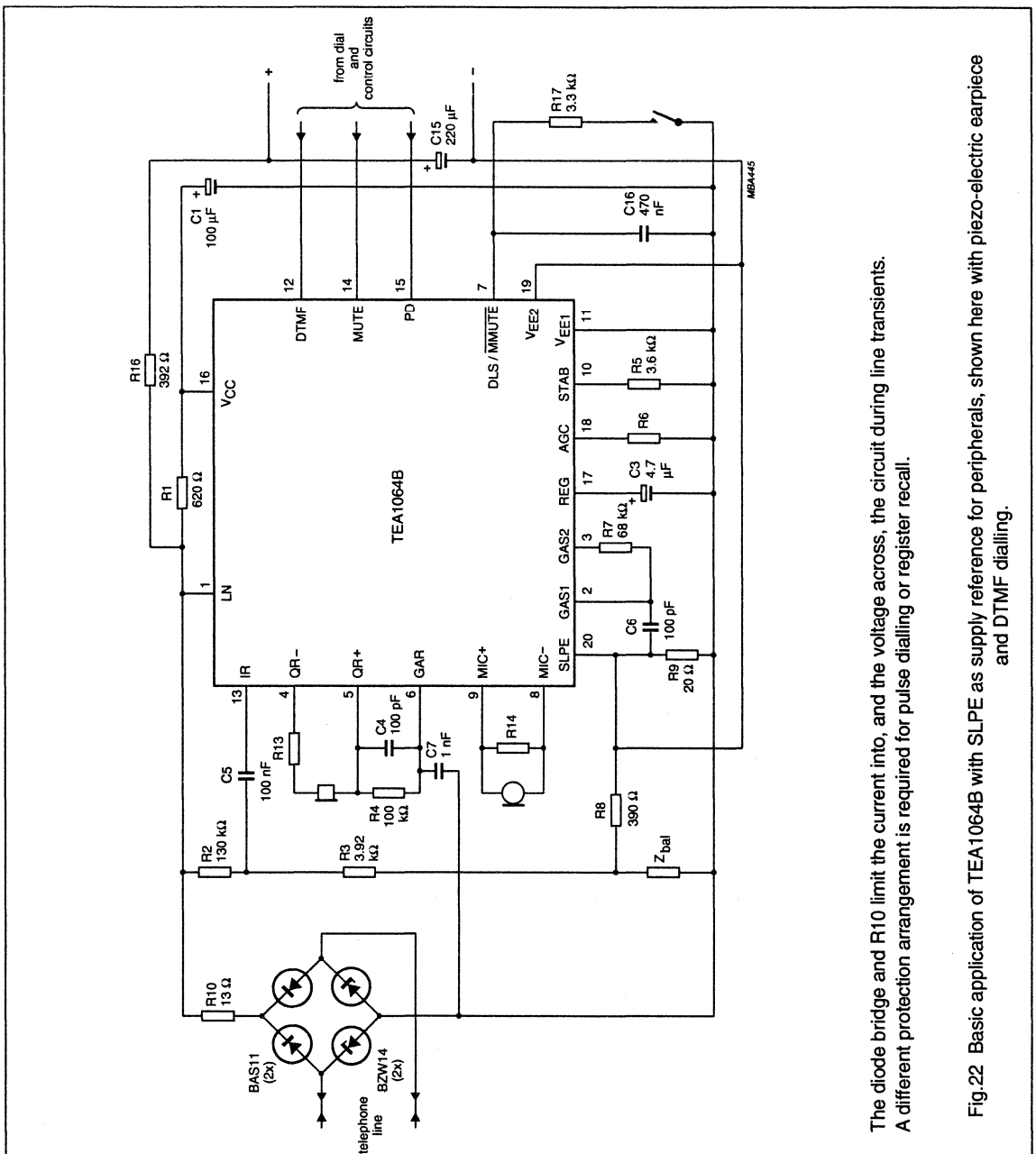


Fig.21 Test circuit for defining voltage gain of the receiving amplifier; voltage gain (G_v) is defined as $20\log|V_o/V_i|$ (with S1 in position 1).

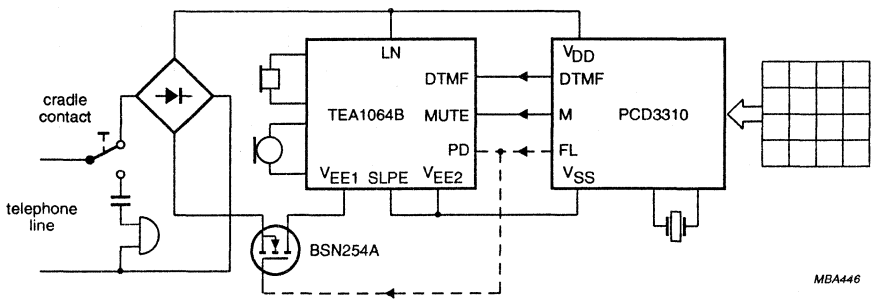
APPLICATION INFORMATION

The basic application circuit is shown in Fig.22 and some typical application are shown in Fig.23, Fig.24 and Fig.25.



The diode bridge and R10 limit the current into, and the voltage across, the circuit during line transients.
A different protection arrangement is required for pulse dialling or register recall.

Fig.22 Basic application of TEA1064B with SLPE as supply reference for peripherals, shown here with piezo-electric earpiece and DTMF dialling.



The broken line indicates optional flash (register recall by timed loop break).

Fig.23 Typical DTMF-pulse set application circuit (simplified) showing the TEA1064B with the CMOS bilingual dialling circuit PCD3310.

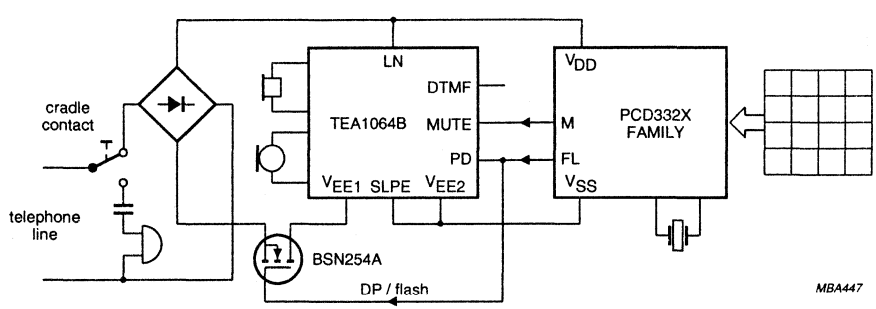


Fig.24 Typical pulse dial set application circuit (simplified) showing the TEA1064B with one of the PCD331X family of CMOS interrupted current-loop dialling circuits.

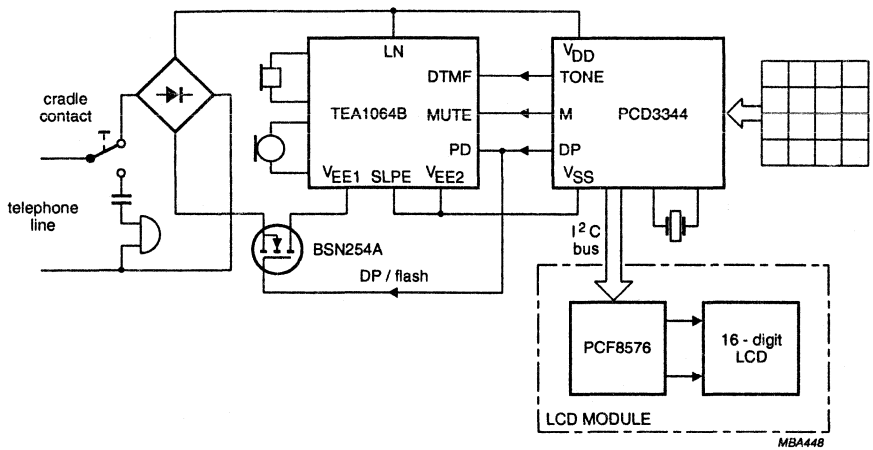


Fig.25 Typical dual-standard (pulse and DTMF) feature phone application circuit (simplified) showing the TEA1064B and the PCD3344 CMOS telephone microcontroller with on-chip DTMF generator plus I²C-bus.

Philips Semiconductors

Data sheet	
status	Objective specification
date of issue	June 1991

TEA1065

Versatile telephone transmission circuit with dialler interface

FEATURES

- Current and voltage regulator mode with adjustable static resistances
- Provides supply for external circuitry
- Symmetrical high-impedance inputs for piezoelectric microphone
- Asymmetrical high-impedance input for electret microphone
- DTMF signal input with confidence tone
- Mute input for pulse or DTMF dialling
- Power-down input for pulse dial or register recall
- Digital pulse input to drive an external switch transistor
- Receiving amplifier for magnetic, dynamic or piezoelectric earpieces
- Large gain setting range on microphone and earpiece amplifiers
- Line loss compensation facility, line current dependent (on microphone and earpiece amplifiers)
- Adjustable gain control
- DC line voltage adjustment facility

GENERAL DESCRIPTION

The TEA1065 is a bipolar integrated circuit which performs all speech and line interface functions that are required in fully electronic telephone sets with adjustable DC mask. The circuit performs electronic switching between dialling and speech internally.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA1065	24	DIL	plastic	SOT101L
TEA1065T	24	SO24	plastic	SOT137A

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{LN}	line voltage	I_{line} = 15 mA	4.25	4.45	4.65	V
I_{line}	normal operation line current range		10	-	150	mA
I_{CC}	internal supply consumption power-down input LOW power-down input HIGH		 - -	 1.14 73	 1.5 105	 mA µA
V_{CC}	supply voltage for peripherals	I_{line} = 15 mA; MUTE input HIGH I_P = 1.2 mA I_P = 1.55 mA	 2.7 2.5	 - -	 - -	 V V
G_V	voltage gain range microphone amplifier earpiece amplifier		 30 20	 - -	 46 45	 dB dB
ΔG_V	line loss compensation gain control range		–5.5	–5.9	–6.3	dB
T_{amb}	operating ambient temperature range		–25	-	+75	°C

Versatile telephone transmission circuit with dialler interface

TEA1065

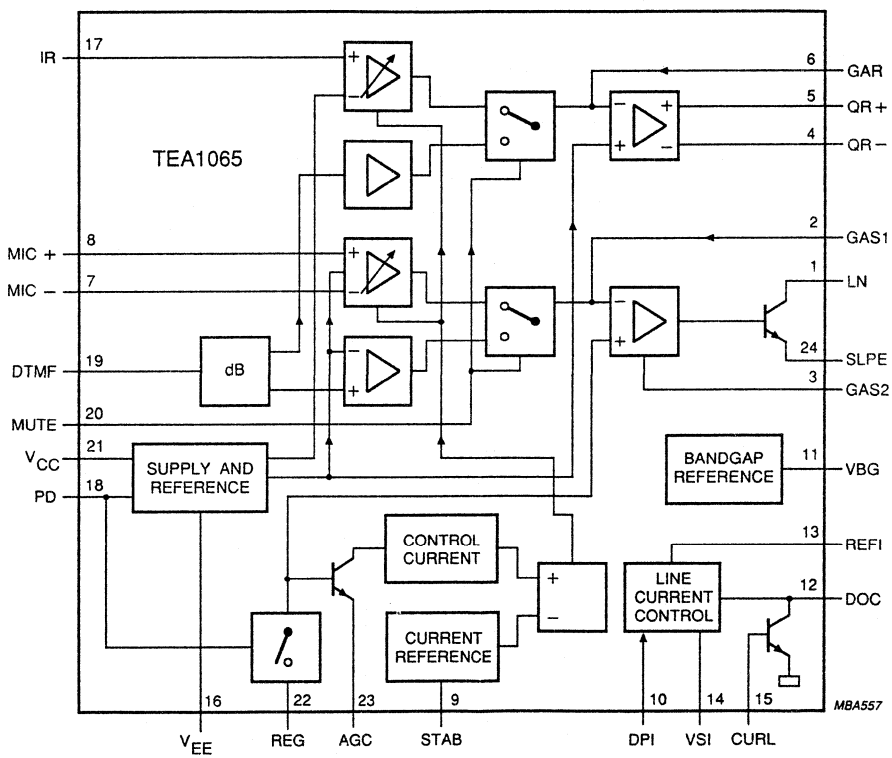


Fig.1 Block diagram.

Versatile telephone transmission circuit with dialler interface

TEA1065

PINNING

SYMBOL	PIN	DESCRIPTION
LN	1	positive line terminal
GAS1	2	gain adjustment; sending amplifier
GAS2	3	gain adjustment; sending amplifier
QR–	4	inverting output; receiving amplifier
QR+	5	non-inverting output; receiving amplifier
GAR	6	gain adjustment; receiving amplifier
MIC–	7	inverting microphone input
MIC+	8	non-inverting microphone input
STAB	9	current stabilizer
DPI	10	digital pulse input
VBG	11	bandgap output reference
DOC	12	drive current output
REFI	13	reference voltage input
VSI	14	voltage sense input
CURL	15	current limitation input
V_{EE}	16	negative line terminal
IR	17	receiving amplifier input
PD	18	power-down input
DTMF	19	dual-tone multifrequency input
MUTE	20	MUTE input
V_{CC}	21	positive supply decoupling
REG	22	voltage regulator decoupling
AGC	23	automatic gain control input
SLPE	24	slope (DC resistance) adjustment

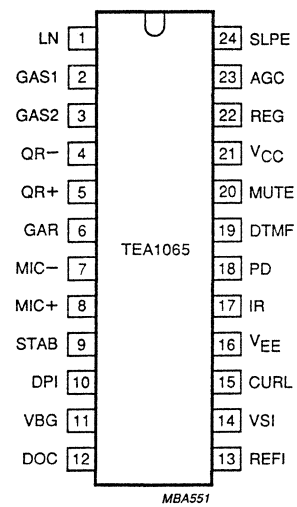


Fig.2 Pinning diagram.

FUNCTIONAL DESCRIPTION

Supply: V_{CC}, LN, SLPE, REG and STAB

The circuit and its peripherals are usually supplied from the telephone line. The circuit develops its own supply voltage at V_{CC} (pin 21) and regulates its voltage drop between LN and SLPE (pins 1 and 24). The internal supply requires a decoupling capacitor between V_{CC} and V_{EE} (pin 16); the internal voltage regulator has to be decoupled by a capacitor from REG (pin 22) to V_{EE}. The internal current stabilizer is set by a 3.6 kΩ resistor connected between STAB (pin 9) and V_{EE}.
The TEA1065 can be set either in a DC voltage regulator mode or in a DC current regulator mode. The DC mask can be selected by connecting the appropriate external components to the dedicated pins (VSI, REFI, DOC, VBG).
When the DC current regulator mode is not required it can be cancelled by connecting pin VSI to V_{EE}; pins REFI, VBG and DOC are left open-circuit.

Voltage regulator mode

The voltage regulator mode is achieved when the line current is less than the current I_{knee} as illustrated in Fig.3. With R13 = R14 = 30 kΩ, the current I_{knee} = 30 mA (I_P = 0 mA).

This line current value will be reached when the voltage on pin VSI (almost equal to the voltage on pin SLPE) exceeds the voltage on pin REFI (equal to the voltage on pin VBG divided by the resistor tap R13, R14). For other values of R13 and R14, the I_{knee} current is given by the following formula:

$$I_{knee} = I_{CC} + I_P + (VBG/R9) \times \{R14/(R14 + R13)\} - (R15/R9) \times I_{O(VSI)}$$

I_{CC} is the current required by the circuit itself (typ. 1.14 mA).
I_P is the current required by the peripheral circuits connected between V_{CC} and V_{EE}. $I_{O(VSI)}$ is the output current from pin VSI (typ. 2.5 μA).

The DC slope of the V_{line}/I_{line} curve is, in this mode, determined by R9(R9 = R9a + R9b) in series with the r_{ds} of the external line current control transistor (see Fig.4; $r_{ds} = \partial V_{GS}/\partial I_D$ at $V_{GS} = V_{DS}$).

Current regulator mode

The current regulator mode is achieved when the line current is greater than I_{knee}. In this mode, the slope of the V_{line}/I_{line} curve is approximately 1300 Ω with R9 = 20 Ω, R16 = 1 MΩ, R13 = R14 = 30 kΩ. For other values of these resistances, the slope value can be approximated by the following formula:
R9 x {1 + R16 x (1/R13 + 1/R14)}

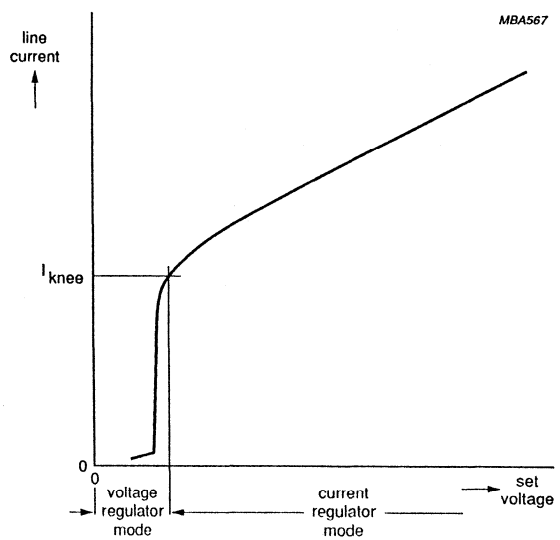


Fig.3 Voltage and current regulator mode.

Versatile telephone transmission circuit with dialler interface

TEA1065

The DC current flowing into the set is determined by the exchange supply voltage (V_{exch}), the DC resistance of the subscriber line (R_{line}) and the DC voltage on the subscriber set (see Fig.4).
If the line current exceeds I_{CC} +0.3 mA, required by the circuit itself ($I_{CC} \approx 1.14$ mA), plus the current I_p required by the peripheral circuits connected to V_{CC} then the voltage regulator will divert the excess current via LN.

$V_{LN} = V_{ref} + I_{SLPE} \times R9 = V_{ref} + (I_{line} - I_{CC} - 0.3 \times 10^{-3} - I_p) \times R9$

where: V_{ref} is an internally generated temperature compensated reference voltage of 4.18 V and R9 is an external resistor connected between SLPE and V_{EE}.

The preferred value of R9 is 20 Ω. Changing R9 will influence the microphone gain, gain control characteristics, sidetone and the maximum output swing on LN. In this instance, the voltage on the line (excluding the diode rectifier bridge; see Fig.4) is:

$V_{line} = V_{LN} + V_{GS} + R16 \times I_{DOC}$

where: V_{GS} is the voltage drop between the gate and source terminal of the external line current control transistor and I_{DOC} is the current sunk by pin DOC ($I_{DOC} = 0$ in the voltage regulator mode and increases with I_{line} in the current regulator mode).
Under normal conditions $I_{SLPE} >> I_{CC} + 0.3$ mA + I_p and for the voltage regulator mode ($I_{line} < I_{knee}$), the static behavior of the circuit is equal to a 4.18 V voltage regulator diode with an internal resistance of R9 in series with the V_{GSon} of the external line current control transistor. For the current regulator mode ($I_{line} > I_{knee}$), the static behaviour of the circuit is equal to a 4.18 V voltage regulator diode with an internal resistance of R9 in series with the V_{GSon} of the external line current control transistor and also in series with a DC voltage source R16 x I_{DOC} (the preferred value of R16 is 1 MΩ at this value the current I_{DOC} is negligible compared to I_{line}).

In the audio frequency range the dynamic impedance between LN and V_{EE} is equal to R1 (see Fig.8). The internal reference voltage V_{ref} can be adjusted by means of an external resistor R_{VA}. This resistor, connected between LN and REG, will decrease the internal reference voltage. When R_{VA} is connected between REG and SLPE the internal reference voltage will increase.
The maximum allowed line current is given in Figs 5 and 6, where the current is shown as a function of the required reference voltage, ambient temperature and applied package.

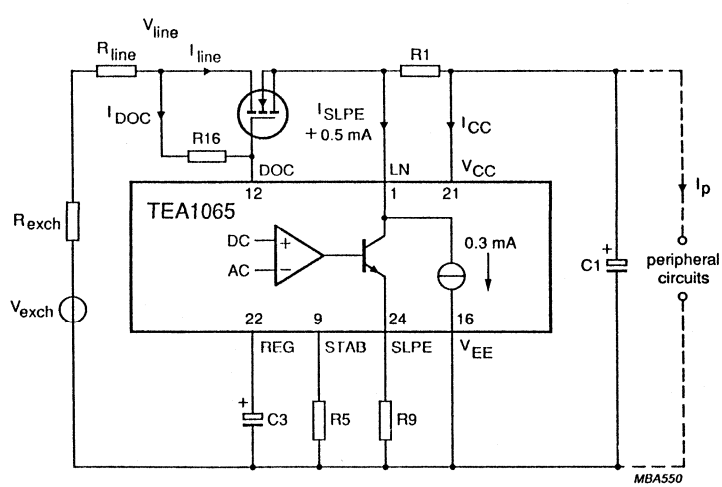
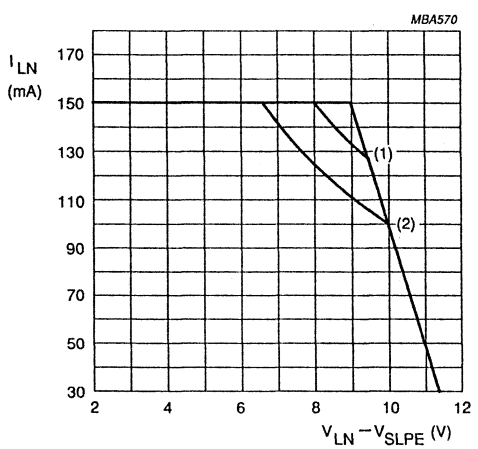


Fig.4 Supply arrangement.

Versatile telephone transmission circuit with dialler interface

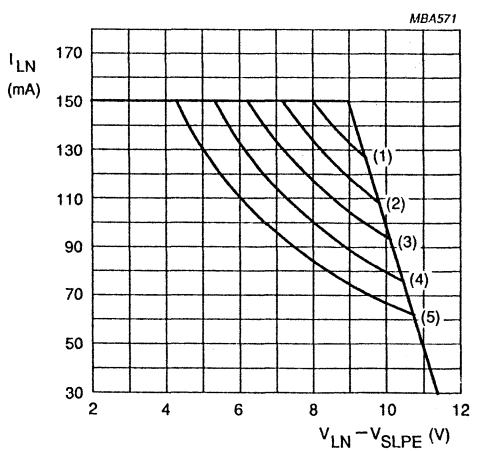
TEA1065

The current I_p, available from V_{CC} for supplying peripheral circuits, depends on the external components and on the line current. Fig.7 shows this current for $V_{CC} > 2.2$ V and for $V_{CC} > 3$ V, where 3 V is the minimum supply voltage for most CMOS circuits including a diode voltage drop for a back-up diode. If MUTE is LOW the available current is further reduced when the receiving amplifier is driven (earpiece amplifier supplied from V_{CC}).



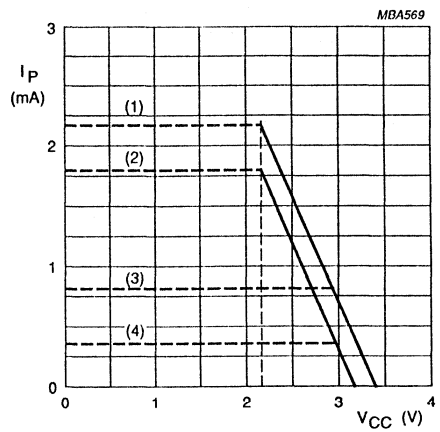
T_{amb}	P_{tot}
(1) 65 °C	1.2 W
(2) 75 °C	1.0 W

Fig.5 TEA1065 safe operating area.



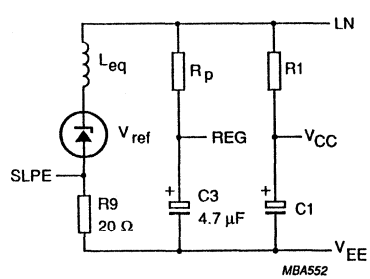
T_{amb}	P_{tot}
(1) 35 °C	1.2 W
(2) 45 °C	1.07 W
(3) 55 °C	0.93 W
(4) 65 °C	0.8 W
(5) 75 °C	0.67 W

Fig.6 TEA1065T safe operating area.



I_{line} = 15 mA at V_{LN} = 4.45 V
R1 = 620 Ω
R9 = 20 Ω

Fig.7 Maximum current I_p available from V_{CC} for external (peripheral) circuitry with V_{CC} > 2.2 V and V_{CC} > 3 V. Curve (1) and (3) are valid when the receiving amplifier is not driven or when MUTE = HIGH, curves (2) and (4) are valid when MUTE = LOW and the receiving amplifier is driven, $V_{o(rms)}$ = 150 mV, R_L = 150 Ω (asymmetrical). (1) = 2.2 mA; (2) = 1.77 mA; (3) = 0.78 mA and (4) = 0.36 mA.



L_{eq} = C3 x R9 x R_p
R_p = 17.5 kΩ

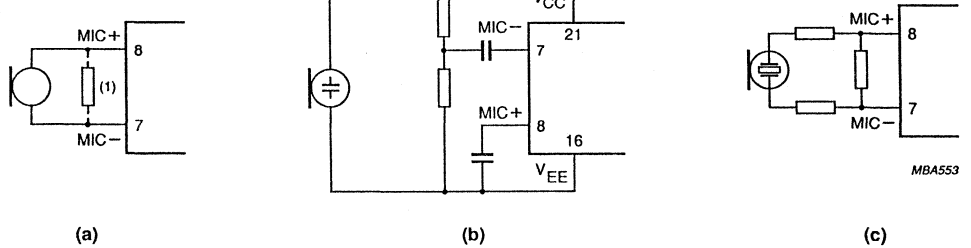
Fig.8 Equivalent circuit impedance between LN and V_{EE}.

Microphone inputs MIC+ and MIC– and gain adjustment connections GAS1 and GAS2

The TEA1065 has symmetrical microphone inputs, its input impedance is 40.8 kΩ (2 x 20.4 kΩ) and its voltage gain is typ. 38 dB with R7 = 68 kΩ. Either dynamic, magnetic or piezoelectric microphones can be used, or an electret microphone with a built-in FET buffer. Arrangements for the microphones types are illustrated in Fig.9.

The gain of the microphone amplifier is proportional to external resistor R7, connected between GAS1 and GAS2, which can be adjusted between 30 dB and 46 dB to suit the sensitivity of the transducer.

An external 100 pF capacitor (C6) is required between GAS1 and SLPE to ensure stability. A larger value of C6 may be chosen to obtain a first-order low-pass filter. The "cut-off" frequency corresponds with the time constant R7 x C6.



(a) magnetic or dynamic microphone, the resistor (1) may be connected to reduce the terminating impedance, or for sensitive types a resistive attenuator can be used to prevent overloading the microphone inputs;

(b) electret microphone;

(c) piezoelectric microphone.

Fig.9 Microphone arrangements.

MUTE input

When MUTE = HIGH the DTMF input is enabled and the microphone and receiving amplifier inputs are inhibited. When MUTE = LOW or open-circuit the DTMF input is inhibited and the microphone and receiving amplifier inputs are enabled. Switching the MUTE input will cause negligible clicks at the earpiece outputs and on the line. An electrostatic discharge protection diode is connected between pin MUTE and pin V_{CC} (pins 20 and 21).

Dual-tone multifrequency input DTMF

When the DTMF input is enabled, dialling tones may be sent onto the line. The voltage gain from DTMF to LN is typ. 12.5 dB less than the gain of the microphone amplifier and varies with R7 in the same way as the gain of the microphone amplifier. This means that the tone level at the DTMF input has to be adjusted after setting the gain of the microphone amplifier. When R7 = 68 kΩ the gain is typically 25.5 dB. The signaling tones can be heard in the earpiece at a low level (confidence tone).

Receiving amplifiers: IR, QR+, QR– and GAR

The receiving amplifier has one input IR and two complementary outputs, QR+ (non-inverting) and QR– (inverting). These outputs may be used for single-ended or differential drive, depending on the type and sensitivity of the earpiece used (see Fig.10). Gain from IR to QR+ is typically 31 dB with R4 = 100 kΩ, which is sufficient for low-impedance magnetic or dynamic earpieces which are suitable for single-ended drive. By using both outputs (differential drive) the gain is increased by 6 dB. Differential drive can be used when earpiece impedance exceeds 450 Ω as with high impedance dynamic, magnetic or piezoelectric earpieces.

The output voltage of the receiving amplifier is specified for continuous-wave drive. The maximum output voltage will be higher under speech conditions where the ratio of peak and RMS value is higher.

The gain of the receiving amplifier can be adjusted over a range of −11 dB to +8 dB to suit the sensitivity of the transducer that is used. The gain is proportional to external resistor R4 connected between GAR and QR+.

Two external capacitors, C4 = 100 pF and C7 = 1 nF, are necessary to ensure stability. A larger value of C4 may be chosen to obtain a first-order low-pass filter. The "cut-off" frequency corresponds with the time constant R4 x C4.

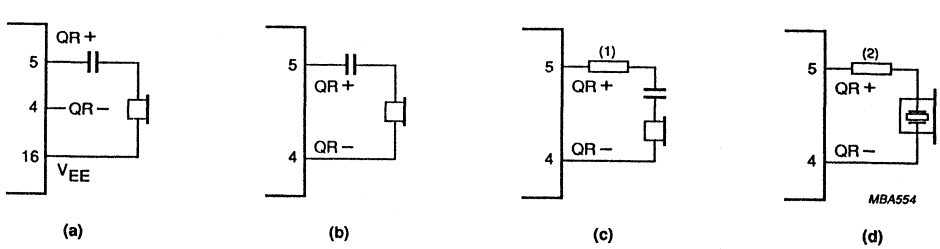


Fig.10 Alternative receiver arrangements: (a) dynamic earpiece with an impedance less than 450 Ω; (b) dynamic earpiece with an impedance more than 450 Ω; (c) magnetic earpiece with an impedance more than 450 Ω, resistor (1) may be connected to prevent distortion (inductive load); (d) piezoelectric earpiece, resistor (2) is required to increase the phase margin (stability with capacitive load).

Automatic gain control

Automatic compensation of line loss is obtained by connecting a resistor (R6) between AGC and V_{EE}. The automatic gain control varies the gain of the microphone amplifier and receiving amplifier in accordance with the DC line current (see Fig.12). The control range is 5.9 dB; this corresponds to a line length of 3.5 km of twisted pair cable (see Fig.11). The DTMF gain is not affected by this feature.

If automatic line loss compensation is not required the AGC pin can be left open-circuit, the amplifiers then give their maximum gain.

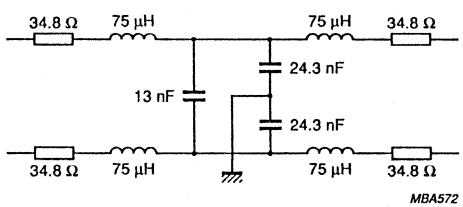


Fig.11 Typical 0.5 km line cell model used for automatic gain control optimization.

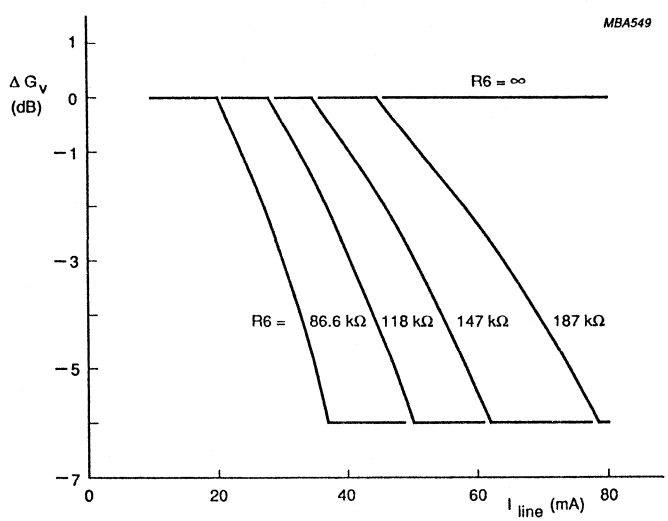


Fig.12 Variation of gain as a function of line current with R6 as a parameter; R9 = 20 Ω.

Power-down input PD

During pulse dialling or register recall (timed-loop-break) the telephone line is interrupted, consequently it provides no supply for the transmission circuit and the peripherals connected to V_{CC}. These gaps have to be bridged by the charge in the smoothing capacitor C1. The requirement on this capacitor is relaxed by applying a HIGH level to the PD input during the loop-break. This reduces the internal supply current from typ. 1.14 mA to 73 μA.

A HIGH level at PD also disconnects the capacitor at REG which results in the voltage stabilizer having no switch-on delay after line interruptions. This results in no contribution of the IC to the current waveform during pulse dialling or register recall. When this facility is not required PD may be left open-circuit or connected to V_{EE}. An electrostatic discharge protection diode is connected between pin PD and V_{CC}.

Digital pulse input DPI

A HIGH level at DPI creates a current which flows from pin DOC to V_{EE} in order to interrupt the line current by the external line current control transistor (see Fig.18; MOSFET BUK554). A LOW level (or pin left open-circuit) disables this current to provide the normal DC regulation (voltage or current). A simple application without regulation of current in pulse dialling mode is given in Fig.18.

When DPI is activated (HIGH level), the external line current control transistor is switched off resulting in no current in the TEA1065. The voltage on pin SLPE becomes zero and capacitor C15 discharges cancelling the current regulation when DPI becomes inactive (LOW level).

To provide a constant regulation (in speech mode and pulse mode), an external transistor is required to keep C15 charged during DPI active (see Fig.19 in which the Field Effect Transistor BSJ177 is directly driven by the DPI signal).
An electrostatic discharge protection diode is connected between pin DPI and pin V_{CC}.

Voltage sense input and reference voltage input VSI and REFI

The voltage on pin VSI represents the DC voltage of pin SLPE. The RC filter (R15 x C15) is also intended to disable the DC regulation when C15 is shunted or not yet charged (especially directly after hook-off). The time constant R15 x C15 determines approximatively the time when no regulation (except CURL pin limitation) is activated.
The voltage applied on pin REFI represents a fraction of the bandgap reference voltage given by pin VBG (resistor tap R13 and R14) in order to determine I_{knee}.

Drive current output DOC

Pin DOC drives the external line current control transistor in order to achieve line interruption during pulse dialling (or register recall) and also the DC slope when $I_{line} > I_{knee}$. The current sunk by pin DOC is determined by the voltage on pin VSI in comparison with the voltage on pin VBG divided by the resistor tap R13 and R14.
When pin DPI is activated, pin DOC changes to a low voltage (by trying to sink typ. 900 μA to V_{EE}) to switch off the external line current control transistor.

Bandgap reference output VBG

This output provides a voltage reference to set the knee line current with the following formula:

$$I_{knee} = I_{CC} + I_P + (VBG/R9) \times \{R14/(R14 + R13)\} \quad (R15/R9) \times 2.5 \times 10^{-6}$$

In order to improve stability, a capacitive load is not allowed on this output.

Current limit input CURL

This input is applied to the base of an internal NPN transistor which has its collector connected to pin DOC and its emitter to V_{EE} (see Fig.13). The transistor limits the line current just after hook-off or during line transients to a value given by the following formula:

$$I_{hook\text{-}off} = I(R1) + V_{BE}/R9b$$

V_{BE} is the base-emitter voltage of the transistor (typ. 700 mV at 25 °C).
I(R1) is the current flowing through R1 to charge C1 just after hook-off.

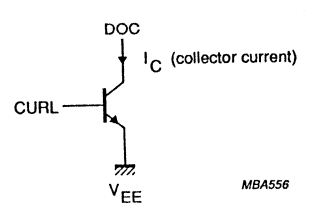


Fig.13 Internal current limiting transistor.

The maximum hook-off current then becomes:

$I_{hook\text{-}off} = V_Z/R1 + V_{BE} \times (R9a + R9b + R1)/(R1 \times R9b)$

where V_Z is the Zener voltage of diode D5 (see Fig.18).

Side-tone suppression

Suppression of the transmitted signal in the earpiece is obtained by the anti-sidetone network comprising $R1//Z_{line}$, R2, R3, R9 and Z_{bal} (see Fig.18). Maximum compensation is obtained when the following conditions are fulfilled:

a) $R9 \times R2 = R1 \times (R3 + R8)$

b) $k = R3 \times (R8 + R9)/(R2 \times R9)$

c) $Z_{bal} = k \times Z_{line}$

The scale factor k is chosen to meet the compatibility with a standard capacitor from the E6 or E12 range for Z_{bal}.

In practice Z_{line} varies considerably with the line length and line type. Therefore, the value chosen for Z_{bal} should be for an average line length giving satisfactory sidetone suppression with long and short times. The suppression also depends on the accuracy of the match between Z_{bal} and the impedance of the average line.

Example

With k = 1, R1 = 619 Ω, R9 = 20 Ω and an average line impedance represented by 270 Ω + (120 nF // 1100 Ω), the calculation results in:

- R2 = 130 kΩ
- R3 = 3650 Ω
- R8 = 715 Ω

The anti-sidetone network for the TEA1060 family, shown in Fig.15, attenuates the signal received from the line by 32 dB before it enters the receiving amplifier. The attenuation is almost constant over the whole audio-frequency range.

Note

More information on the balancing of the anti-sidetone bridges can be obtained in our publication 'Versatile speech transmission ICs for electronic telephone sets', order number 9398 341 10011.

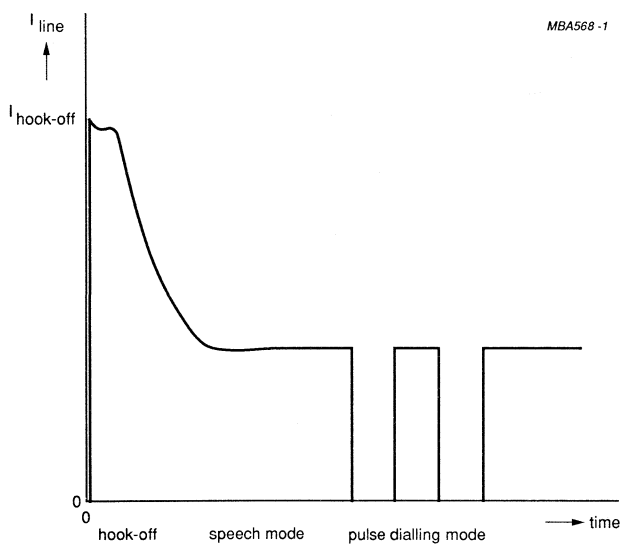


Fig.14 Example of line current shape in pulse dialling mode (see also Fig.18).

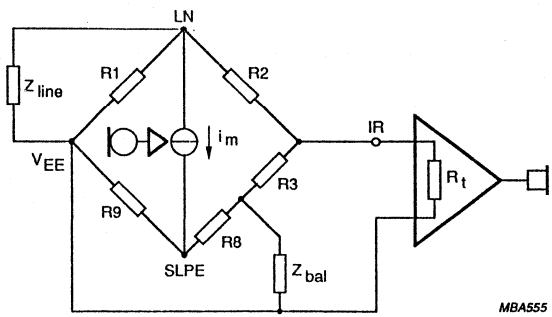


Fig.15 Equivalent circuit of TEA1060 family anti-sidetone bridge.

LIMITING VALUES

In accordance with the absolute maximum system (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{LN}	positive line voltage continuous		-	12	V
V_{DOC}	positive DOC voltage continuous		-	12	V
V_{LN}	repetitive line voltage during switch-on or line interruption		-	13.2	V
I_{LN}	line current (see also Fig.5 and 6)		-	150	mA
V_I	input voltage on pins other than LN, DOC, VSI, REFI and CURL		V_{EE}-0.7	V_{CC}+0.7	V
P_{tot}	total power dissipation	see Figs 5 and 6			
T_{stg}	storage temperature range		–40	+125	°C
T_{amb}	operating ambient temperature range		–25	+75	°C
T_j	junction temperature		-	+125	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient in free air	-	50	K/W
$R_{th\ j\text{-}a}$	from junction to ambient in free air	-	75	K/W

TEA1065T is mounted on glassy epoxy board 28.5 x 19.1 x 1.5 mm

HANDLING

Every pin withstands the ESD test in accordance with MIL-STD-883C class 2, method 3015 (HBM 1500 Ω, 100 pF, 3 positive pulses and 3 negative pulses on each pin as a function of pin V_{EE}.

CHARACTERISTICS

I_{LN} = 10 to 150 mA; V_{EE} = 0 V; f = 800 Hz; T_{amb} = 25 °C; R9 = 20 Ω; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply LN and V_{CC} (pins 1 and 21)						
V_{LN}	voltage drop over circuit	I_{line} = 5 mA	3.95	4.25	4.55	V
		I_{line} = 15 mA	4.25	4.45	4.65	V
		I_{line} = 100 mA	5.4	6.1	6.7	V
		I_{line} = 140 mA	-	-	7.5	V
$\Delta V_{LN}/\Delta T$	variation with temperature	I_{line} = 15 mA	−3	−1	+1	mV/K
V_{LN}	voltage drop over circuit	I_{line} = 15 mA				
		$R_{VA} = R_{1\text{-}22}$ = 68 kΩ	3.6	3.9	4.15	V
		$R_{VA} = R_{22\text{-}24}$ = 39 kΩ	4.7	5.0	5.3	V
I_{CC}	supply current	PD = LOW; V_{CC} = 2.8 V	-	1.14	1.5	mA
		PD = HIGH; V_{CC} = 2.8 V	-	73	105	µA
Microphone inputs MIC+ and MIC− (pins 8 and 7)						
$\|Z_I\|$	input impedance		18.5	20.4	24.3	kΩ
G_v	voltage gain	I_{line} = 15 mA; R7 = 68 kΩ	37	38	39	dB
$\Delta G_v/\Delta f$	variation with frequency referred to 800 Hz	I_{line} = 15 mA; f = 300 to 3400 Hz	−0.5	±0.2	+0.5	dB
$\Delta G_v/\Delta T$	variation with temperature referred to 25 °C	I_{line} = 50 mA; T_{amb} = −25 to 75 °C; without R6	-	±0.5	-	dB
Dual-tone multi-frequency input DTMF (pin 19)						
$\|Z_I\|$	input impedance		16.8	20.7	24.6	kΩ
G_v	voltage gain	I_{line} = 15 mA; R7 = 68 kΩ	24.5	25.5	26.5	dB
$\Delta G_v/\Delta f$	variation with frequency referred to 800 Hz	I_{line} = 15 mA f = 300 to 3400 Hz	−0.5	±0.2	+0.5	dB
$\Delta G_v/\Delta T$	variation with temperature referred to 25 °C	I_{line} = 50 mA; T_{amb} = −25 to +75 °C	-	±0.5	-	dB
Gain adjustment GAS1 and GAS2 (pin 2 and 3)						
ΔG_v	gain variation with R7 connected between pins 2 and 3; transmitting amplifier		−8	-	+8	dB
Transmitting amplifier output LN (pin 1)						
$V_{LN(rms)}$	output voltage (RMS value)	I_{line} = 15 mA				
		d_{tot} = 2%	1.9	2.3	-	V
		d_{tot} = 10%	-	2.6	-	V
$V_{no(rms)}$	noise output voltage (RMS value)	I_{line} = 15 mA; R7 = 68 kΩ; pin 7 and 8 open-circuit psophometrically weighted (P53 curve); control transistor included (MOS BUK554 type see Fig.18)	-	−68	-	dBmp
Receiving amplifier input IR (pin 17)						
Z_I	input impedance		17	21	25	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Receiving amplifier outputs QR+ and QR– (pin 5 and 4)						
Z_O	output impedance		-	4	-	Ω
G_v	voltage gain	I_{line} = 15 mA; R4 = 100 kΩ				
		single-ended; RT = 300 Ω	30	31	32	dB
		differential; RT = 600 Ω	36	37	38	dB
$\Delta G_v/\Delta f$	variation with frequency referred to 800 Hz	f = 300 to 3400 Hz	–0.5	±0.2	+0.5	dB
$\Delta G_v/\Delta T$	variation with temperature referred to 25 °C	without R6; I_{line} = 50 mA; T_{amb} = –25 to +75 °C	-	±0.2	-	dB
$V_{O(rms)}$	output voltage (RMS value)	I_{line} = 15 mA; THD = 2 %; sinewave drive; R4 = 100 kΩ				
		single-ended; RT = 150 Ω	0.3	0.38	-	V
		differential; RT = 450 Ω	0.56	0.72	-	V
		differential; CT = 60 nF; (1500 Ω series resistor); f = 3400 Hz	0.87	1.07	-	V
		I_{line} = 30 mA; differential; CT = 60 nF; (1500 Ω series resistor); f = 3400 Hz	1.02	1.22	-	V
$V_{O(rms)}$	noise output voltage (RMS value)	I_{line} = 15 mA; R4 = 100 kΩ				
		single-ended; RT = 300 Ω	-	50	-	μV
		differential; RT = 600 Ω	-	100	-	μV
Gain adjustment GAR (pin 6)						
ΔG_v	receiving amplifier, gain adjustment range		–11	-	+8	dB
Mute input MUTE (pin 20)						
V_{IH}	input voltage HIGH		1.5	-	V_{CC}	V
V_{IL}	input voltage LOW		-	-	0.3	V
I_{MUTE}	input current		-	8	15	μA
ΔG_v	change of microphone amplifier gain	MUTE = HIGH	-	–70	-	dB
G_v	voltage gain from DTMF input to QR+ or QR–	MUTE = HIGH; R4 = 100 kΩ single-ended; RT = 300 Ω	–21	–19	–17	dB
Power-down input PD (pin 18)						
V_{IH}	input voltage HIGH		1.5	-	V_{CC}	V
V_{IL}	input voltage LOW		-	-	0.3	V
I_{PD}	input current		-	2.5	5.0	μA
Automatic gain control input AGC (pin 23)						
ΔG_v	controlling the gain from IR to QR+, QR– and the gain from MIC+, MIC– to LN; gain control range with respect to I_{line} = 15 mA	R6 = 118 kΩ	–5.5	–5.9	–6.3	dB
I_{line}	highest line current for maximum gain		-	28	-	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{line}	lowest line current for minimum gain		-	50	-	mA
ΔG_v	change of gain between I_{line} = 15 and 35.5 mA		*	-1.5	*	dB
Current limiting input CURL (pin 15)						
V_{BE}	base-emitter voltage drop of internal transistor	see Fig.13; I_C = 50 µA = I_{DOC}	-	0.7	-	V
H_{FE}	current gain of internal transistor	see Fig.13; I_C = 50 µA = I_{DOC}	60	120	-	
$I_{C(max)}$	maximum collector current of internal transistor	see Fig.13	-	-	2	mA
Bandgap reference voltage output VBG (pin 12)						
V_{BG}	reference voltage		*	1.22	*	V
I_{BG}	output drive capability	note 1	–100	-	+50	µA
Z_O	output impedance		-	12	-	Ω
Voltage sense input VSI (pin 14)						
I_O	output current	pin VSI connected to V_{EE}	-	-2.5	-	µA
Reference input REFI (pin 13)						
I_O	output current		-	-	2.0	mA
Drive current output DOC (pin 11)						
I_O	output current	REFI connected to V_{EE}; VSI not connected; DPI = LOW	120	300	-	µA
		REFI not connected; VSI connected to V_{EE}; DPI = HIGH	200	900	-	µA
Digital pulse input DPI (pin 10)						
V_{IH}	input voltage HIGH		1.5	-	V_{CC}	V
V_{IL}	input voltage LOW		-	-	0.3	V
I_{DPI}	input current		-	2.5	5	µA

Note to the characteristics

1. No capacitive load on the V_{BG} output. Positive current is defined as conventional current flow into a device. Negative current is defined as conventional current flow out of a device.

Versatile telephone transmission circuit with dialler interface

TEA1065

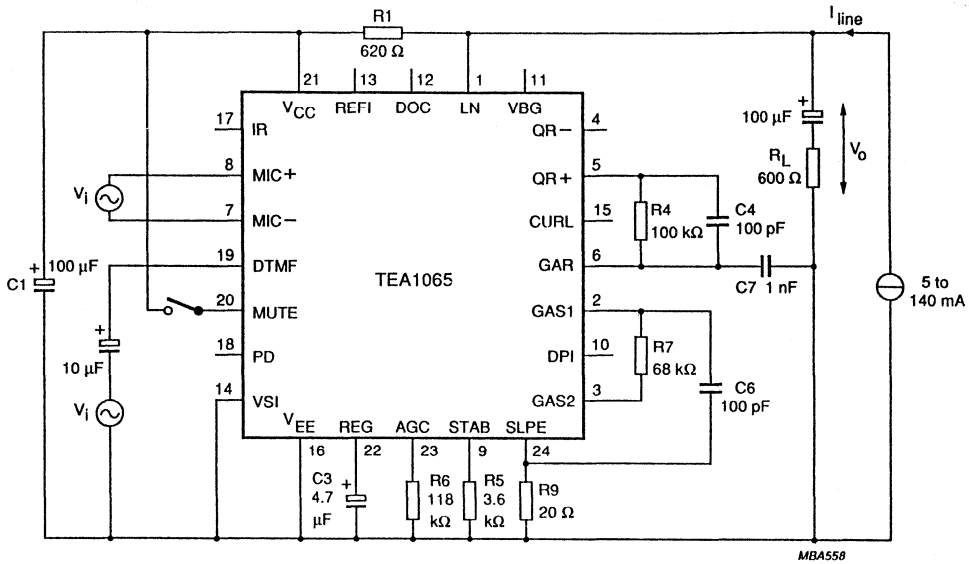


Fig.16 Test circuit for defining voltage gain of MIC+, MIC− and DTMF inputs. Voltage gain is defined as $G_v = 20 \text{ Log} |V_o/V_i|$. For measuring the gain from MIC+ and MIC− the MUTE input should be LOW or open-circuit, for measuring the DTMF input MUTE should be HIGH. Inputs not under test should be open-circuit except VSI that should be connected to V_{EE}.

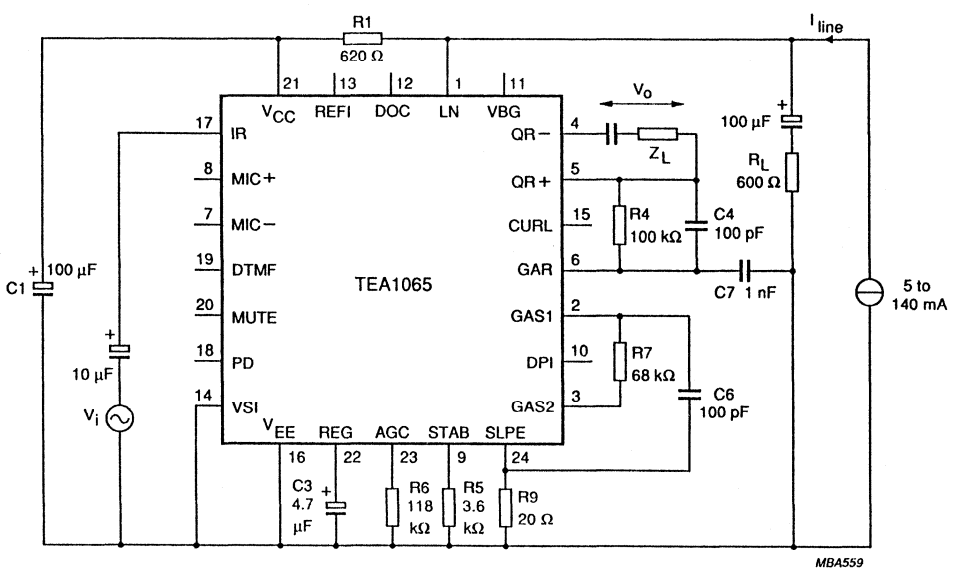


Fig.17 Test circuit for defining voltage gain of the receiving amplifier. Voltage gain is defined as $G_v = 20 \text{ Log} |V_o/V_i|$.

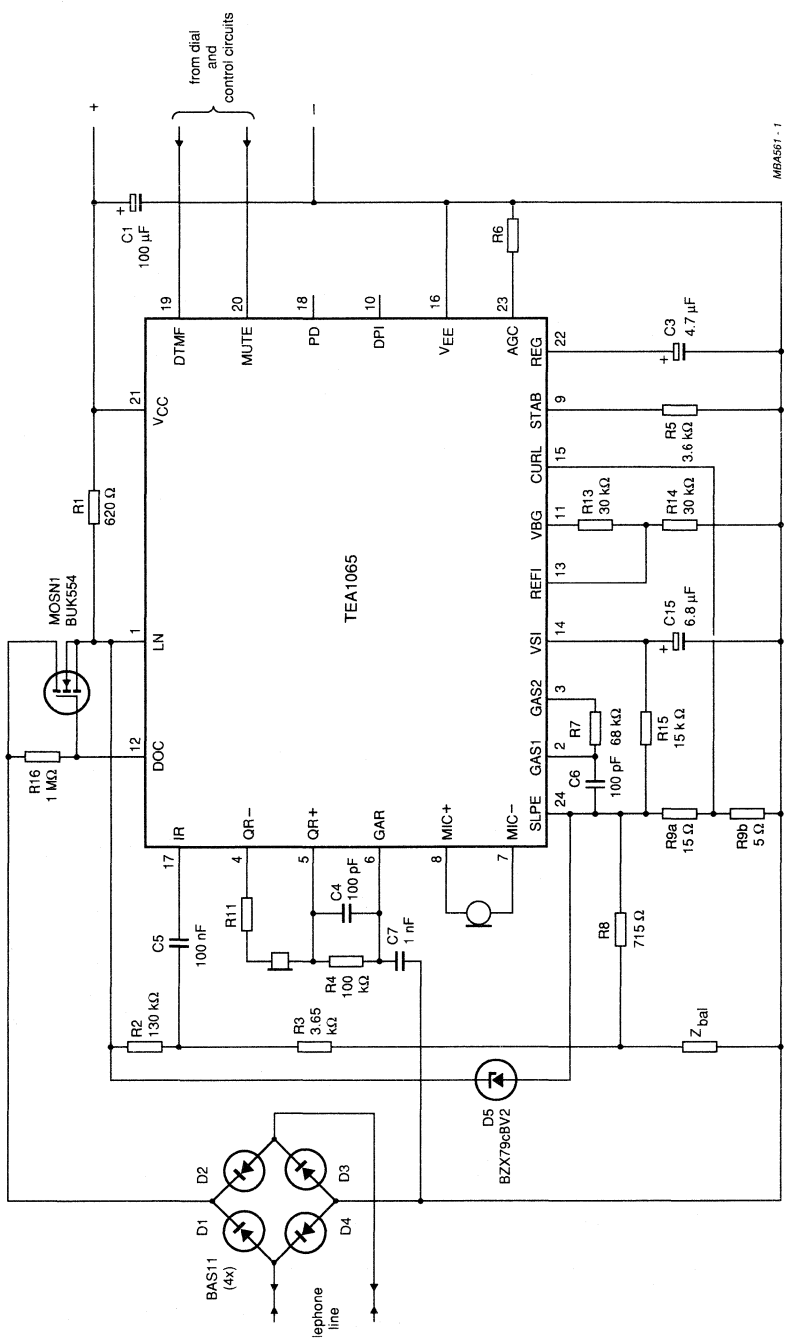


Fig.18 Typical application of the TEA1065, with a piezoelectric earpiece and DTMF dialling.

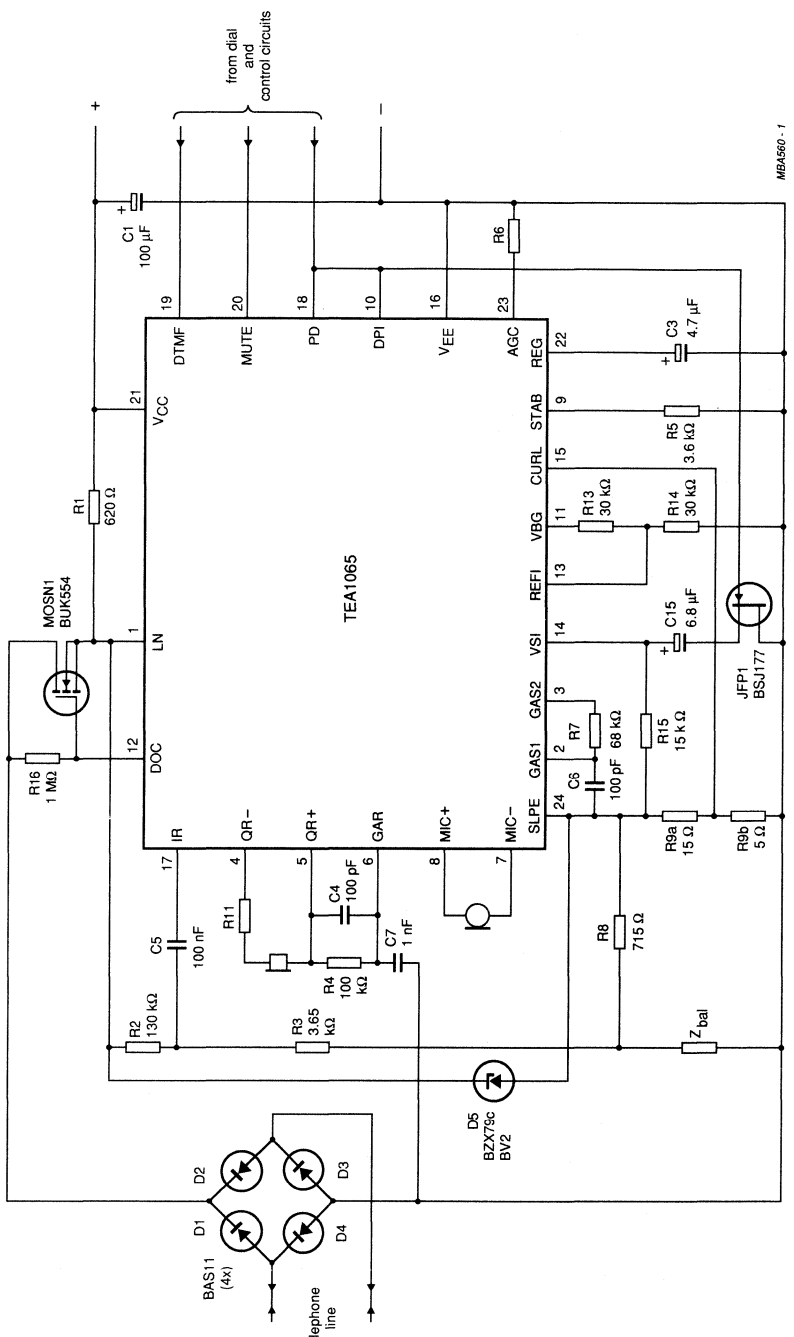


Fig.19 Typical application of the TEA1065, with a piezoelectric earpiece and pulse dialling. DTMF dialling requires a different protection arrangement.

VERSATILE TELEPHONE TRANSMISSION CIRCUIT WITH DIALLER INTERFACE

GENERAL DESCRIPTION

The TEA1066T is a bipolar integrated circuit which performs all speech and line interface functions that are required in fully electronic telephone sets. The circuit performs electronic switching between dialling and speech.

Features

- Voltage regulator with adjustable static resistance
- Provides supply for external circuitry
- Symmetrical low-impedance inputs for dynamic and magnetic microphones
- Symmetrical high-impedance inputs for piezoelectric microphone
- Asymmetrical high-impedance input for electret microphone
- DTMF signal input with confidence tone
- Mute input for pulse or DTMF dialling
- Power down input for pulse dial or register recall
- Receiving amplifier for magnetic, dynamic or piezoelectric earpieces
- Large gain setting range on microphone and earpiece amplifiers
- Line loss compensation facility, line current dependent (microphone and earpiece amplifiers)
- Gain control adaptable to exchange supply
- DC line voltage adjustment facility

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Line voltage	I_{line} = 15 mA	V_{LN}	4.25	4.45	4.65	V
Line current operating range		I_{line}	10	–	100	mA
Internal supply current						
power down input LOW		I_{CC}	–	0.96	1.3	mA
power down input HIGH		I_{CC}	–	55	82	μA
Supply voltage for peripherals	I_{line} = 15 mA; MUTE input HIGH					
	I_p = 1.2 mA	V_{CC}	2.8	3.05	–	V
	I_p = 1.7 mA	V_{CC}	2.5	–	–	V
Voltage gain range for microphone amplifier						
Low impedance inputs (pins 9 and 7)		G_v	44	–	60	dB
High impedance inputs (pins 10 and 8)		G_v	30	–	46	dB
Receiving amplifier		G_v	17	–	39	dB
Line loss compensation						
Gain control range		ΔG_v	5.5	5.9	6.3	dB
Exchange supply voltage range		V_{exch}	24	–	60	V
Exchange feeding bridge resistance range		R_{exch}	400	–	1000	Ω
Operating ambient temperature range		T_{amb}	−25	–	+ 75	°C

PACKAGE OUTLINE

20-lead mini-pack; plastic (SO20; SOT163A).

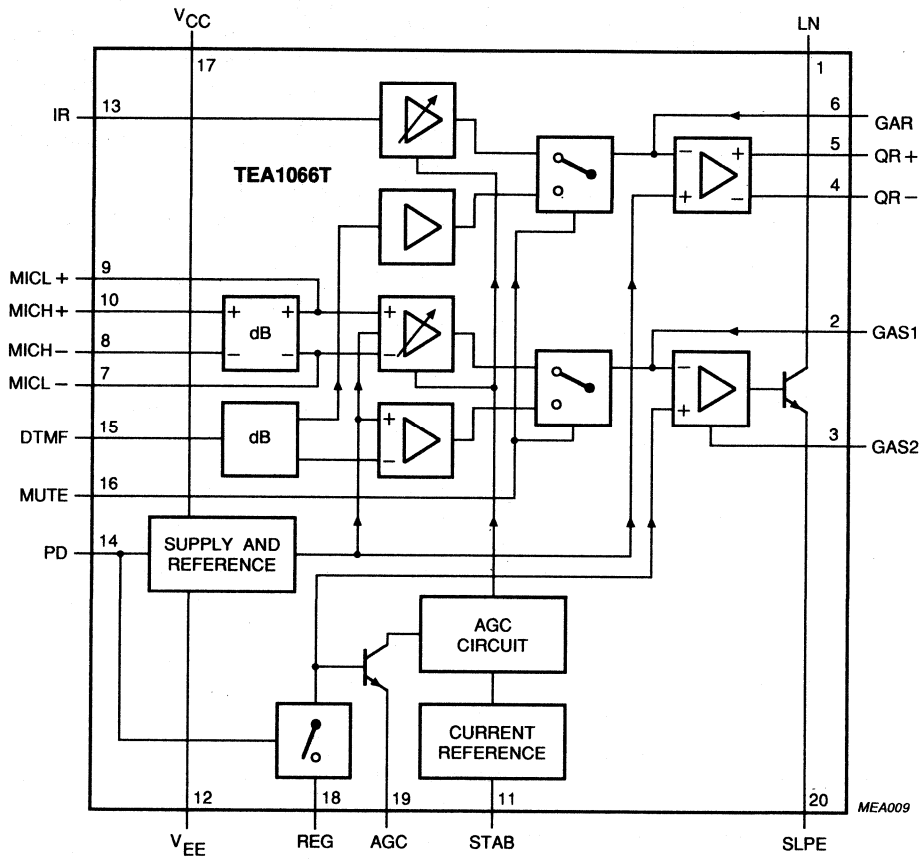


Fig. 1 Block diagram.

The blocks marked "dB" are attenuators.

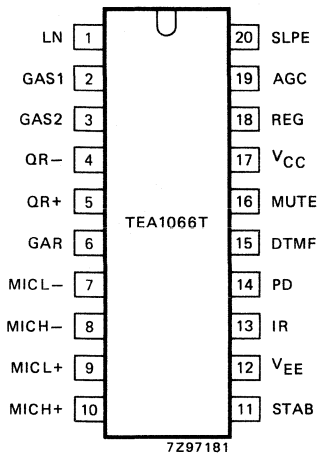


Fig. 2 Pinning diagram.

PINNING

1	LN	positive line terminal
2	GAS1	gain adjustment transmitting amplifier
3	GAS2	gain adjustment transmitting amplifier
4	QR−	inverting output, receiving amplifier
5	QR+	non-inverting output, receiving amplifier
6	GAR	gain adjustment receiving amplifier
7	MICL−	inverting microphone input, low impedance
8	MICH−	inverting microphone input, high impedance
9	MICL+	non-inverting microphone input, low impedance
10	MICH+	non-inverting microphone input, high impedance
11	STAB	current stabilizer
12	V_{EE}	negative line terminal
13	IR	receiving amplifier input
14	PD	power-down input
15	DTMF	dual-tone multi-frequency input
16	MUTE	mute input
17	V_{CC}	positive supply decoupling
18	REG	voltage regulator decoupling
19	AGC	automatic gain control input
20	SLPE	slope (DC resistance) adjustment

FUNCTIONAL DESCRIPTION

Supply: V_{CC}, LN, SLPE, REG and STAB

Power for the TEA1066T and its peripheral circuits is usually obtained from the telephone line. The IC develops its own supply voltage at V_{CC} and regulates its voltage drop. The supply voltage V_{CC} may also be used to supply external peripheral circuits, e.g. dialling and control circuits.

The supply has to be decoupled by connecting a smoothing capacitor between V_{CC} and V_{EE}; the internal voltage regulator has to be decoupled by a capacitor from REG to V_{EE}. An internal current stabilizer is set by a resistor of 3.6 kΩ between STAB and V_{EE}.

The DC current flowing into the set is determined by the exchange supply voltage V_{exch}, the feeding bridge resistance R_{exch}, the DC resistance of the subscriber line R_{line} and the DC voltage on the subscriber set (see Fig. 7).

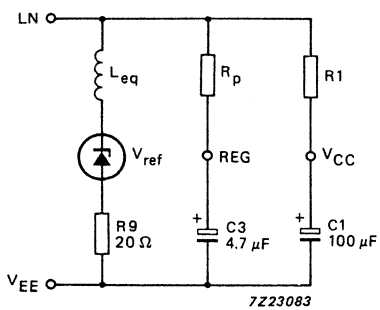
If the line current I_{line} exceeds the current I_{CC} + 0.5 mA required by the circuit itself, about 1 mA, plus the current I_p required by the peripheral circuits connected to V_{CC}, then the voltage regulator diverts the excess current via LN.

The voltage regulator adjusts the average voltage on LN to:
$V_{LN} = V_{ref} + I_{SLPE} \times R9 = V_{ref} + (I_{line} - I_{CC} - 0.5 \times 10^{-3}\text{A} - I_P) \times R9$, where V_{ref} is an internally generated temperature compensated reference voltage of 4,2 V and R9 being an external resistor connected between SLPE and V_{EE}. The preferred value for R9 is 20 Ω. Changing R9 will have influence on microphone gain, DTMF gain, gain control characteristics, side-tone level and maximum output swing on LN.

FUNCTIONAL DESCRIPTION (continued)

Under normal conditions $I_{SLPE} \geqslant I_{CC} + 0.5$ mA + I_P. The static behaviour of the circuit then equals a 4.2 V voltage regulator diode with an internal resistance equal to that of R9. In the audio frequency range the dynamic impedance is largely determined by R1 (see Fig. 3). The internal reference voltage can be adjusted by means of an external resistor R_{VA}. This R_{VA} connected between LN and REG (pins 1 and 18) will decrease the internal reference voltage. R_{VA} connected between REG and SLPE (pins 18 and 20) will increase the internal reference voltage.

Current I_P, available from V_{CC} for supplying peripheral circuits, depends on external components and on the line current. Fig. 8 shows this current for $V_{CC} > 2.2$ V and > 3 V (being the minimum supply voltage for most CMOS circuits including voltage drop for an enable diode). If MUTE is LOW the available current is further reduced when the receiving amplifier is driven.



$R_p = 17.5\ k\Omega$
$L_{eq} = C3 \times R9 \times R_p$

Fig. 3 Equivalent impedance circuit.

Microphone inputs MICL+, MICH+, MICL− and MICH− and amplification adjustment connections GAS1 and GAS2

The TEA1066T has symmetrical microphone inputs. The MICL+ and MICL− inputs are intended for low-sensitivity, low-impedance dynamic or magnetic microphones. Input impedance is 8.2 kΩ (2 x 4.1 kΩ) and its voltage gain is typ. 52 dB. The MICH+ and MICH− inputs are intended for a piezoelectric microphone or an electret microphone with built-in FET source follower. Its input impedance is 40.8 kΩ (2 x 20.4 kΩ) and its voltage gain is typical 38 dB. The arrangements with the microphone types mentioned are shown in Fig. 9.

The gain of the microphone amplifier in both types can be adjusted over a range of ± 8 dB to suit the sensitivity of the transducer used. The gain is proportional to external resistor R7 connected between GAS1 and GAS2.

An external capacitor C6 of 100 pF between GAS1 and SLPE is required to ensure stability. A larger value may be chosen to obtain a first-order low-pass filter. The cut-off frequency corresponds with the time constant R7 x C6.

Mute input MUTE

A HIGH level at MUTE enables the DTMF input and inhibits the microphone inputs and the receiving amplifier; a LOW level or an open circuit does the reverse. Switching the mute input will cause negligible clicks at the earpiece outputs and on the line.

Dual-tone multi-frequency input DTMF

When the DTMF input is enabled, dialling tones may be sent onto the line. The voltage gain from DTMF to LN is typ. 25.5 dB and varies with R7 in the same way as the gain of the microphone amplifier. The signalling tones can be heard in the earpiece at a low level (confidence tone).

Receiving amplifier: IR, QR+, QR− and GAR

The receiving amplifier has one input IR and two complementary outputs, a non-inverting output QR+ and an inverting output QR−. These outputs may be used for single-ended or for differential drive, depending on the sensitivity and type of earpiece used (see Fig. 10). Gain from IR to QR+ is typ. 25 dB. This will be sufficient for low-impedance magnetic or dynamic earpieces; these are suited for single-ended drive. By using both outputs (differential drive) the gain is increased by 6 dB and differential drive becomes possible. This feature can be used in case the earpiece impedance exceeds 450 Ω (high-impedance dynamic, magnetic or piezo-electric earpieces.

The output voltage of the receiving amplifier is specified for continuous-wave drive. The maximum output voltage will be higher under speech conditions, where the ratio of peak and RMS value is higher.

The gain of the receiving amplifier can be adjusted over a range of ± 8 dB to suit the sensitivity of the transducer used. The gain is proportional to external resistor R4 connected from GAR to QR+.

Two external capacitors C4 = 100 pF and C6 = 10 x C4 = 1 nF are necessary to ensure stability. A larger value of C4 may be chosen to obtain a first-order, low-pass filter. The "cut-off" frequency corresponds with the time constant R4 x C4.

Automatic amplification control input AGC

Automatic line loss compensation will be obtained by connecting a resistor R6 from AGC to V_{EE}. This automatic gain control varies the gain of the microphone amplifier and the receiving amplifier in accordance with the DC line current. The control range is 6 dB. This corresponds with a line length of 5 km for a 0.5 mm diameter copper twisted-pair cable with a DC resistance of 176 Ω/km and an average attenuation of 1.2 dB/km.

Resistor R6 should be chosen in accordance with the exchange supply voltage and its feeding bridge resistance (see Fig. 11 and Table 1). Different values of R6 give the same ratio of line currents for begin and end of the control range.

If automatic line loss compensation is not required AGC may be left open. The amplifiers then all give their maximum gain as specified.

Power-down input PD

During pulse dialling or register recall (timed loop break) the telephone line is interrupted, as a consequence it provides no supply for the transmission circuit and the peripherals connected to V_{CC}. These gaps have to be bridged by the charge in the smoothing capacitor C1. The requirements on this capacitor are relaxed by applying a HIGH level to the PD input during the time of the loop break, which reduces the supply current from typ. 1 mA to typ. 55 μA.

A HIGH level at PD further disconnects the capacitor at REG, with the effect that the voltage stabilizer will have no switch-on delay after line interruptions. This results in no contribution of the IC to the current waveform during pulse dialling or register recall.
When this facility is not required PD may be left open.

FUNCTIONAL DESCRIPTION (continued)

Side-tone suppression

Suppression of the transmitted signal in the earpiece is obtained by the anti-side-tone network consisting of $R1//Z_{line}$, R2, R3, R8, R9 and Z_{bal} (see Fig. 14). Maximum compensation is obtained when the following conditions are fulfilled:

a) $R9.R2 = R1(R3 + [R8//Z_{bal}])$

b) $[Z_{bal}/(Z_{bal} + R8)] = [Z_{line}/(Z_{line} + R1)]$

If fixed values are chosen for R1, R2, R3 and R9, then condition a) will always be fulfilled provided that $|R8//Z_{bal}| < R3$.
To obtain optimum side tone suppression, condition b) has to be fulfilled resulting in:

$$Z_{bal} = (R8/R1)\ Z_{line} = k.Z_{line}$$

where k is a scale factor; $k = (R8/R1)$.

Scale factor k (value of R8) must be chosen to meet the following criteria:
- compatibility with a standard capacitor from the E6 or E12 range for Z_{bal}
- $|Z_{bal}//R8| \ll R3$
- $|Z_{bal}+R8| \gg R9$

In practice Z_{line} varies strongly with line length and cable type; consequently an average value has to be chosen for Z_{bal}. The suppression further depends on the accuracy with which Z_{bal}/k equals the average line impedance.

Example

The balanced line impedance $|Z_{bal}|$ at which the optimum suppression is preset can be calculated by: suppose $Z_{line} = 210\ \Omega + (1265\ \Omega/140\ nF)$, representing a 5 km line of 0.5 mm diameter, copper, twisted-pair cable matched to 600 Ω (176 Ω/km; 38 nF/km).
When k = 0.64 then R8 = 390 Ω; $Z_{bal} = 130\ \Omega + (820\ \Omega//220\ nF)$.

The anti-sidetone network for the TEA1060 family shown in Fig. 4 attenuates the signal received from the line by 32 dB before it enters the receiving amplifier. The attenuation is almost constant over the whole audio frequency range. Fig. 5 shows a conventional Wheatstone bridge anti-sidetone circuit that can be used as an alternative. Both bridge types can be used with either resistive or complex set impedances.

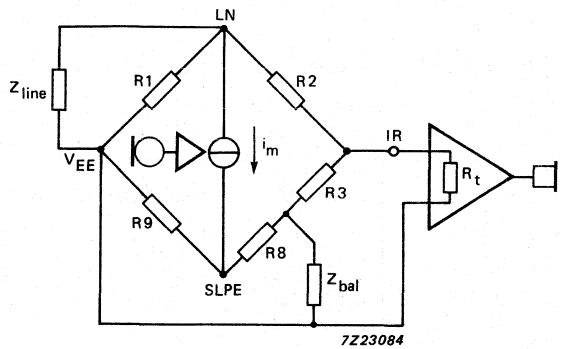


Fig. 4 Equivalent circuit of TEA1060 family anti-sidetone bridge.

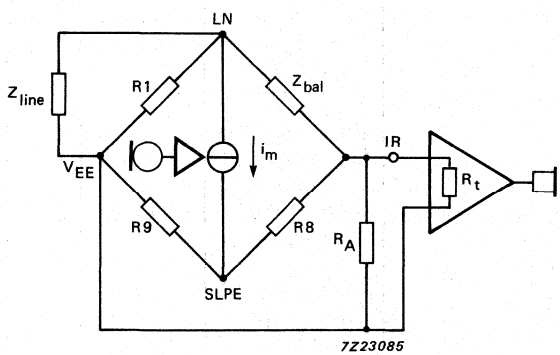


Fig. 5 Equivalent circuit of an anti-sidetone network in a Wheatstone bridge configuration.

FUNCTIONAL DESCRIPTION (continued)

The anti-sidetone network as used in the standard application (Fig. 13) attenuates the signal from the line with 32 dB. The attenuation is nearly flat over the audio-frequency range.
Instead of the above described special TEA1066 bridge, the conventional Wheatstone bridge configuration can be used as an alternative anti-sidetone circuit. Both bridge types can be used with either a resistive set impedance or with a complex set impedance.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Positive line voltage continuous		V_{LN}	–	12	V
Repetitive line voltage during switch-on or line interruption		V_{LN}	–	13.2	V
Repetitive peak line voltage for a 1 ms pulse per 5 s	R9 = 20 Ω; R10 = 13 Ω (Fig. 10)	V_{LN}	–	28	V
Line current (1)	R9 = 20 Ω	I_{line}	–	140	mA
Voltage on all other pins		V_i	–	V_{CC} + 0.7	V
		$-V_i$	–	0.7	V
Total power dissipation (2)	R9 = 20 Ω	P_{tot}	–	555	mW
Storage temperature range		T_{stg}	−40	+ 125	°C
Operating ambient temperature range		T_{amb}	−25	+ 75	°C
Junction temperature		T_j	–	+ 125	°C

Notes to the ratings

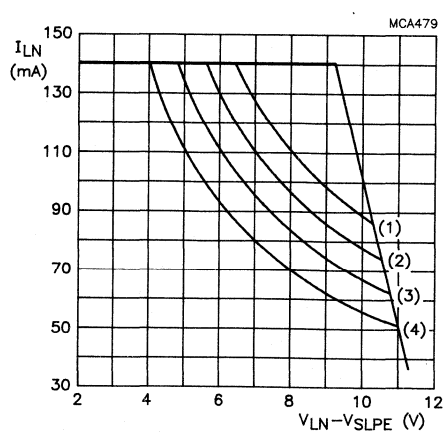
(1) Mostly dependent on the maximum required T_{amb} and the voltage between LN and SLPE (see Fig. 6).

(2) Calculated for the maximum ambient temperature specified T_{amb} = 75 °C and a maximum junction temperature of 125 °C.

THERMAL RESISTANCE

From junction to ambient in free air

TEA1066T mounted on glass epoxy board 41 x 19 x 1.5 mm $R_{th\ j\text{-}a}$ = 90 K/W



	T_{amb}	P_{tot}
(1)	45 °C	888
(2)	55 °C	777
(3)	65 °C	666
(4)	75 °C	555

Fig. 6 Safe operating area.

CHARACTERISTICS

I_{line} = 10 to 100 mA; V_{EE} = 0 V; f = 800 Hz; R9 = 20 Ω; T_{amb} = 25 °C; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply: LN and V_{CC} (pins 1 and 17)						
Voltage drop over circuit	I_{line} = 5 mA	V_{LN}	3.95	4.25	4.55	V
	I_{line} = 15 mA	V_{LN}	4.25	4.45	4.65	V
	I_{line} = 100 mA	V_{LN}	5.40	6.10	6.70	V
	I_{line} = 140 mA	V_{LN}	–	–	7.50	V
Voltage drop variation with temperature	I_{line} = 15 mA	$\Delta V_{LN}/\Delta T$	−4	−2	0	mV/K
Voltage drop over circuit	I_{line} = 15 mA; R_{VA} = R1-18 = 68 kΩ	V_{LN}	3.50	3.80	4.05	V
	R_{VA} = R18-20 = 39 kΩ	V_{LN}	4.70	5.0	5.30	V
Supply current (pin 17)						
PD (pin 14) = LOW	V_{CC} = 2.8 V	I_{CC}	–	0.96	1.3	mA
PD (pin 14) = HIGH	V_{CC} = 2.8 V	I_{CC}	–	55	82	μA
Supply voltage available for peripheral circuits	I_{line} = 15 mA; MUTE = HIGH					
	I_P = 0 mA	V_{CC}	3.5	3.75	–	V
	I_P = 1.2 mA	V_{CC}	2.8	3.05	–	V
Microphone inputs MICL+ and MICL−; MICH+ and MICH−						
Input impedance						
MICL+ (pin 9); MICL− (pin 7)		$\|Z_i\|$	3.3	4.1	4.9	kΩ
MICH+ (pin 10); MICH− (pin 8)		$\|Z_i\|$	16.5	20.4	24.5	kΩ
Common-mode rejection ratio		k_{CMR}	–	82	–	dB
Voltage gain	I_{line} = 15 mA; R7 = 68 kΩ					
MICL+/MICL− to LN		G_v	51	52	53	dB
MICH+/MICH− to LN		G_v	37	38	39	dB
gain variation with frequency at f = 300 Hz and f = 3400 Hz	w.r.t. 800 Hz	ΔG_{vf}	−0.5	±0.2	+ 0.5	dB
gain variation with temperature at T_{amb} = −25 °C and + 75 °C	I_{line} = 50 mA; w.r.t. 800 Hz	ΔG_{vT}	–	±0.2	–	dB

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Dual-tone multi-frequency input DTMF (pin 15)						
Input impedance		$\|Z_i\|$	16.8	20.7	24.6	kΩ
Voltage gain from DTMF to LN	I_{line} = 15 mA; R7 = 68 kΩ	G_v	24.5	25.5	26.5	dB
gain variation with frequency at f = 300 Hz and f = 3400 Hz	w.r.t. 800 Hz	ΔG_{vf}	−0.5	±0.2	+ 0.5	dB
gain variation with temperature at T_{amb} = −25 °C and + 75 °C	I_{line} = 50 mA; w.r.t. 25 °C	ΔG_{vT}	–	±0.2	–	dB
Gain adjustment connections GAS1 and GAS2 (pins 2 and 3)						
Gain variation with R7, transmitting amplifier		ΔG_v	−8	–	+ 8	dB
Transmitting amplifier output LN (pin 1)						
Output voltage	I_{line} = 15 mA; THD = 2%	$V_{LN(rms)}$	1.9	2.3	–	V
	THD = 10%	$V_{LN(rms)}$	–	2.6	–	V
Noise output voltage	I_{line} = 15 mA; R7 = 68 kΩ; microphone inputs open psophometrically weighted (P53 curve)	$V_{no(rms)}$	–	−70	–	dBmp
Receiving amplifier input IR (pin 13)						
Input impedance		$\|Z_i\|$	17	21	25	kΩ
Receiving amplifier outputs QR+ and QR− (pins 5 and 4)						
Output impedance	single-ended	$\|Z_o\|$	–	4	–	Ω
Voltage gain from IR to QR+ or QR−	I_{line} = 15 mA; R4 = 100 kΩ; single-ended R_L = 300 Ω	G_v	24	25	26	dB
	differential R_L = 600 Ω	G_v	30	31	32	dB
Gain variation with frequency at f = 300 Hz and f = 3400 Hz	w.r.t. 800 Hz	ΔG_{vf}	−0.5	±0.2	+ 0.5	dB

parameter	conditions	symbol	min.	typ.	max.	unit
Receiving amplifier outputs QR+ and QR− (continued)						
Gain variation with temperature at T_{amb} = −25 °C and + 75 °C	I_{line} = 50 mA; w.r.t. 25 °C	ΔG_{vT}	–	±0.2	–	dB
Output voltage	I_P = 0 mA; I_{line} = 15 mA; THD = 2%; R4 = 100 kΩ					
sine-wave drive						
single-ended	R_L = 150 Ω	$V_{o(rms)}$	0.30	0.38	–	V
	R_L = 450 Ω	$V_{o(rms)}$	0.4	0.52	–	V
differential	C_L = 47 nF R series = 100 Ω; f = 3400 Hz	$V_{o(rms)}$	0.8	1.0	–	V
Noise output voltage	I_{line} = 15 mA; R4 = 100 kΩ; pin 13 (IR) open psophometrically weighted (P53 curve)					
single-ended	R_L = 300 Ω	$V_{no(rms)}$	–	50	–	μV
differential	R_L = 600 Ω	$V_{no(rms)}$	–	100	–	μV
Gain adjustment GAR (pin 6)						
Gain variation with R4 connected between pin 6 and pin 5 receiving amplifier		ΔG_v	−8	–	+ 8	dB
MUTE input (pin 16)						
Input voltage HIGH		V_{IH}	1.5	–	V_{CC}	V
Input voltage LOW		V_{IL}	–	–	0.3	V
Input current		I_{MUTE}	–	5	10	μA
Reduction of voltage gain from MICL+ (pin 9) and MICL− (pin 7) to LN (pin 1)	MUTE = HIGH	ΔG_v	–	70	–	dB
Voltage gain from DTMF to QR+ or QR−	MUTE = HIGH; R4 = 100 kΩ					
single-ended	R_L = 300 Ω	G_v	−21	−19	−17	dB
Power-down input PD (pin 14)						
Input voltage HIGH		V_{IH}	1.5	–	V_{CC}	V
Input voltage LOW		V_{IL}	–	–	0.3	V
Input current		I_{PD}	–	5	10	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Automatic gain control input AGC (pin 19)						
Gain control range from IR to QR+/QR− and from MIC+/MIC− to LN; R6 = 110 kΩ between AGC and V_{EE}						
Gain control range	I_{line} = 70 mA	$-\Delta G_v$	−5.5	−5.9	−6.3	dB
Highest line current for maximum gain	I_{line}	–	–	23	–	mA
Lowest line current for minimum gain	I_{line}	–	–	61	–	mA
Reduction of gain between I_{line} = 15 mA and I_{line} = 35 mA		$-\Delta G_v$	−1.0	−1.5	−2.0	dB

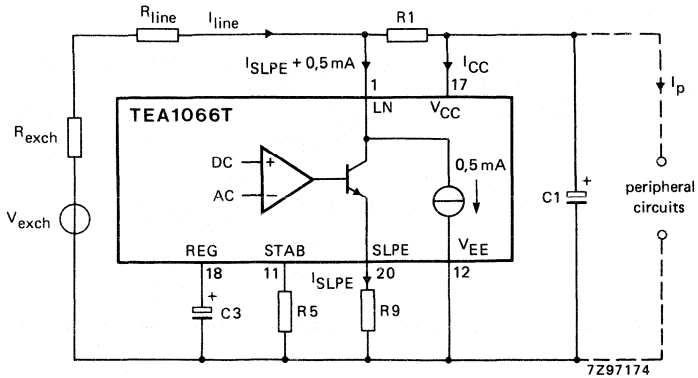


Fig. 7 Supply arrangement.

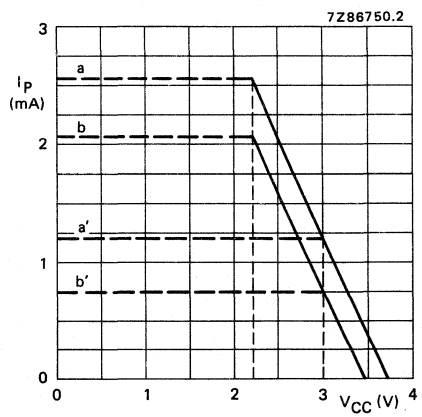


Fig. 8 Typicalmum current Ip available from V_{CC} for external (peripheral) circuitry with $V_{CC} > 2.2$ V and $V_{CC} > 3$ V. Curves (a) and (a') are valid when the receiving amplifier is not driven or when MUTE = HIGH, curves (b) and (b') are valid when MUTE = LOW and the receiving amplifier is driven, $V_{o(rms)} = 150$ mV, $R_L = 150\ \Omega$ (asymmetrical).
$I_{line} = 15$ mA; $V_{LN} = 4.45$ V; R1 = 620 Ω and R9 = 20 Ω.
(a) = 2.55 mA; (b) = 2.1 mA; (a') = 1.2 mA and (b') = 0.75 mA.

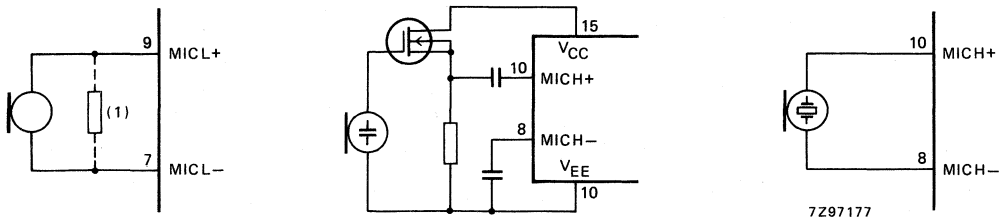


Fig. 9 Alternative microphone arrangements. (a) magnetic or dynamic microphone. The resistor marked (1) may be connected to lower the terminating impedance. (b) electret microphone, (c) piezo-electric microphone.

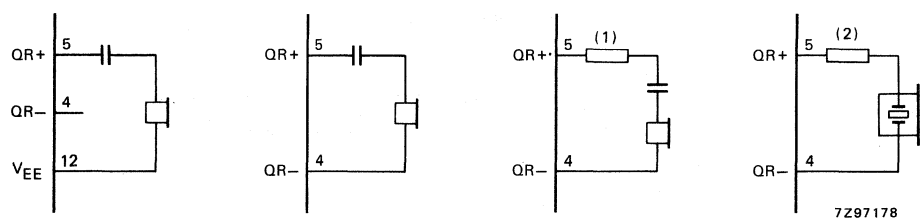


Fig. 10 Alternative receiver arrangements. (a) dynamic earpiece with less than 450 Ω impedance. (b) dynamic earpiece with more than 450 Ω impedance. (c) magnetic earpiece with more than 450 Ω impedance. The resistor marked (1) may be connected to prevent distortion (inductive load). (d) piezoelectric earpiece. The resistor marked (2) is required to increase the phase margin (capacitive load).

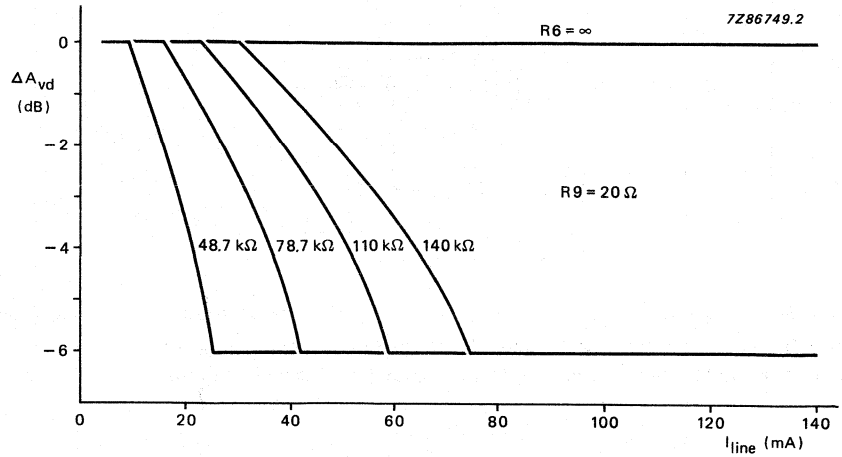


Fig. 11 Variation of gain with line current, with R6 as a parameter.

Table 1 Values of resistor R6 for optimum line loss compensation, for various usual values of exchange supply voltage V_{exch} and exchange feeding bridge resistance R_{exch}; R9 = 20 Ω.

		R_{exch} (Ω)			
		400	600	800	1000
		R6 (kΩ)			
V_{exch} (V)	24	61.9	48.7	X	X
	36	100	78.7	68	60.4
	48	140	110	93.1	82
	60	X	X	120	102

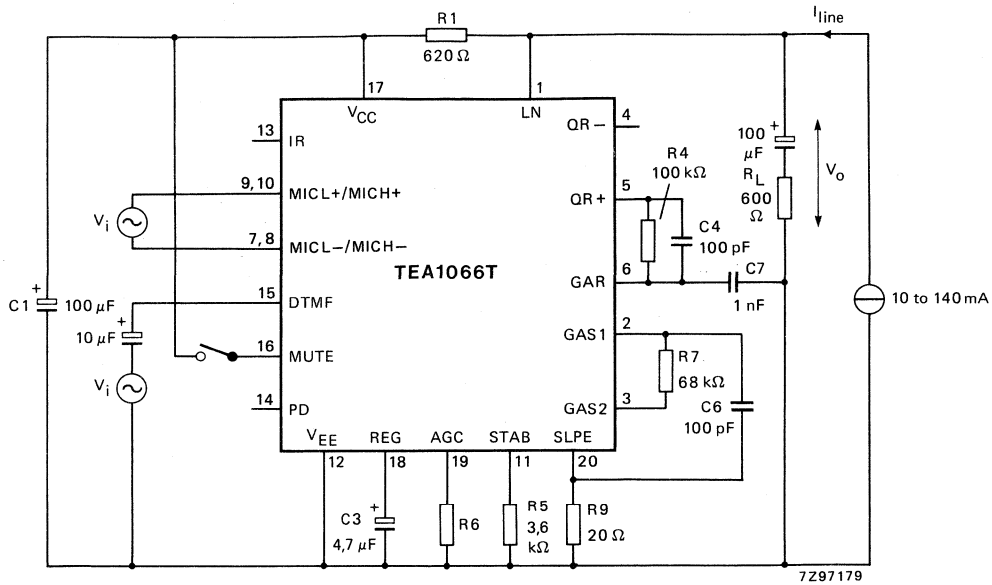


Fig. 12 Test circuit for defining voltage gain of MICL+, MICL−, MICH+ and MICH− DTMF inputs. Voltage gain is defined as: $G_V = 20 \log |V_o/V_i|$. For measuring the gain from MICL+, MICL− or MICH+ and MICH− the MUTE input should be LOW or open, for measuring the DTMF input MUTE should be HIGH. Inputs not under test should be open.

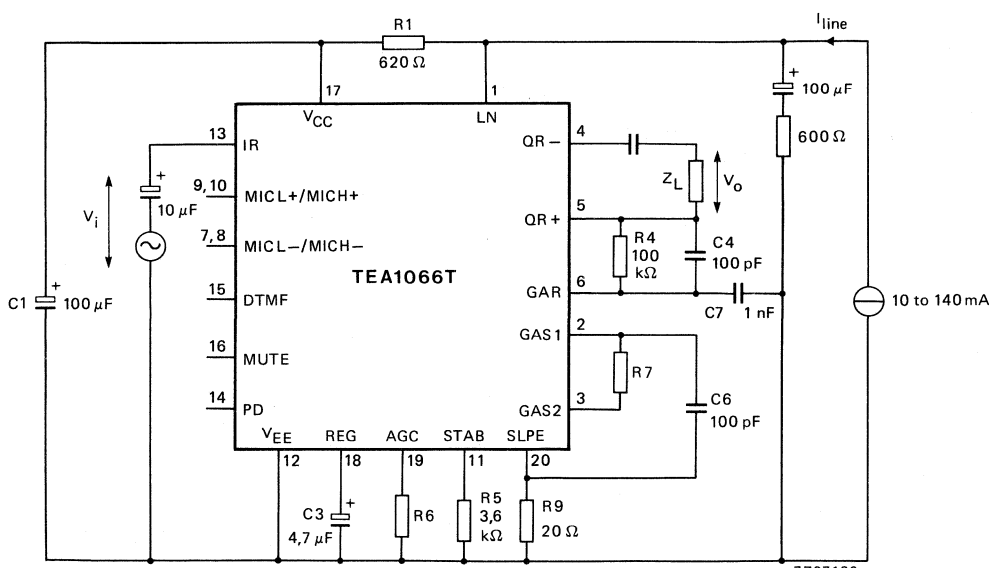


Fig. 13 Test circuit for defining voltage gain of the receiving amplifier. Voltage gain is defined as: $G_V = 20 \log |V_o/V_i|$.

APPLICATION INFORMATION

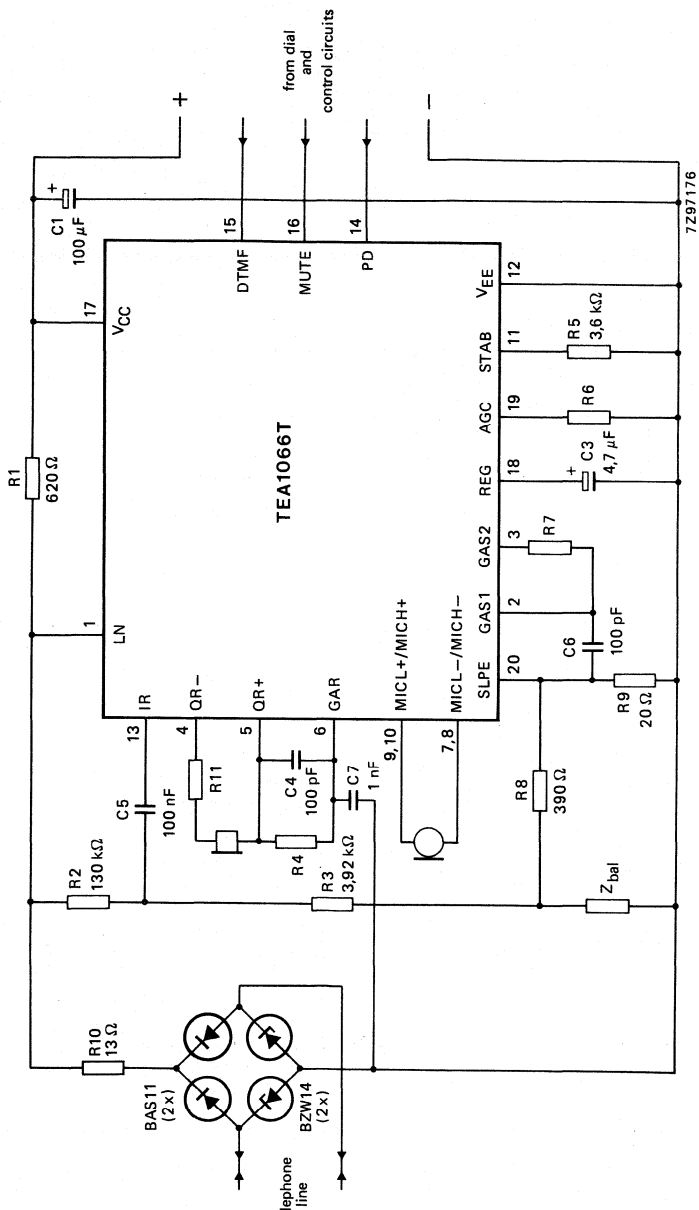
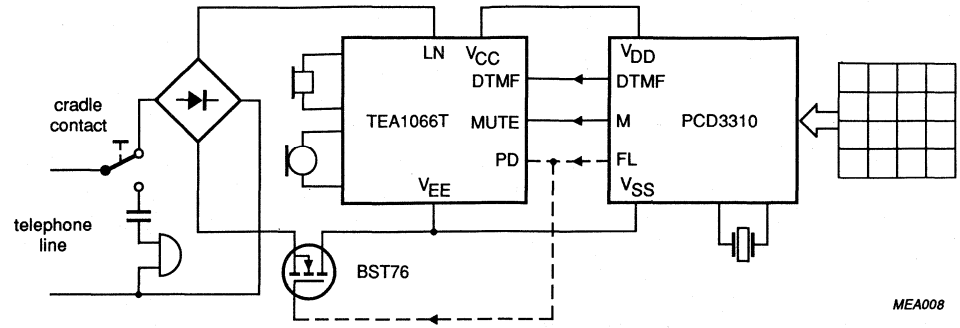
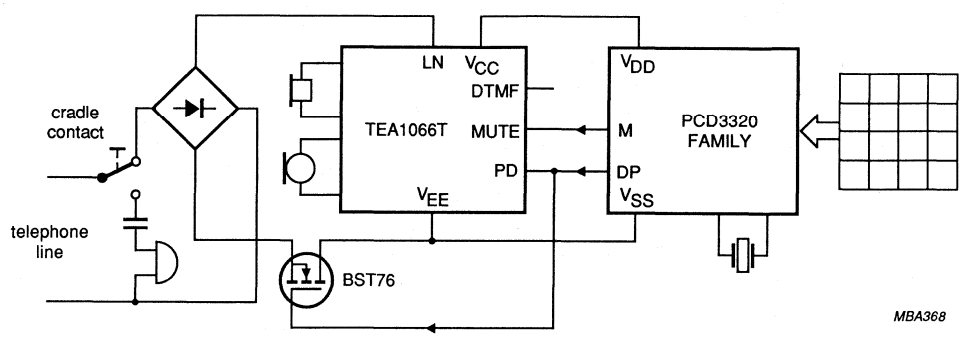


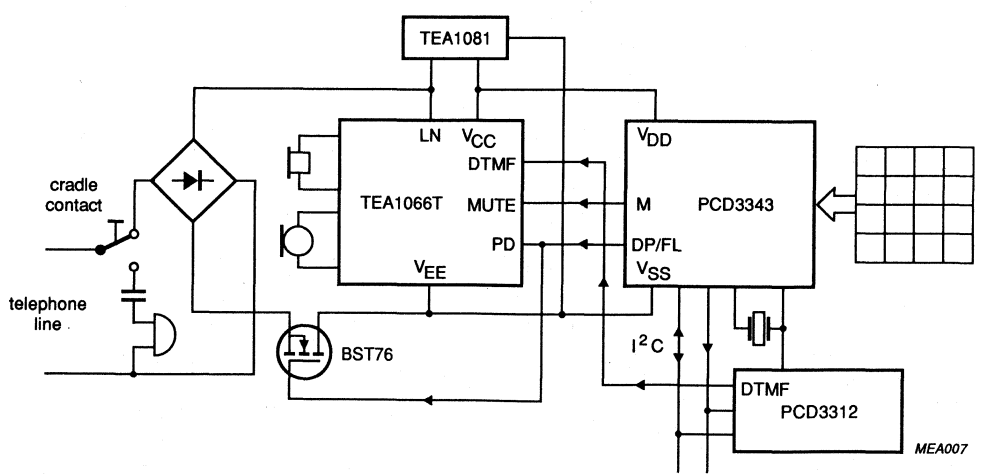
Fig. 14 Typical application of the TEA1066T, shown here with a piezoelectric earpiece and DTMF dialling. The bridge to the left and R10 limit the current into the circuit and the voltage across the circuit during line transients. Pulse dialling or register recall require a different protection arrangement.



(a)



(b)



(c)

Fig.15 Typical applications of the TEA1066T (simplified).

(a) DTMF pulse set with CMOS PCD3310 dialling circuit. The dashed lines show an optional flash (register recall by timed loop break).

(b) Pulse dial set with one of the PCD3320 family of CMOS interrupted current-loop dialling circuits.

(c) Dual-standard (pulse and DTMF) feature phone with the PCD3343 CMOS telephone controller and the PCD3312 CMOS DTMF generator with I^2C-bus. Supply is provided by the TEA1081 supply circuit.

LOW VOLTAGE VERSATILE TELEPHONE TRANSMISSION CIRCUIT WITH DIALLER INTERFACE

GENERAL DESCRIPTION

The TEA1067 is a bipolar integrated circuit performing all speech and line interface functions required in fully electronic telephone sets. It performs electronic switching between dialling and speech. The circuit is able to operate down to a DC line voltage of 1.6 V (with reduced performance) to facilitate the use of more telephone sets in parallel.

Features

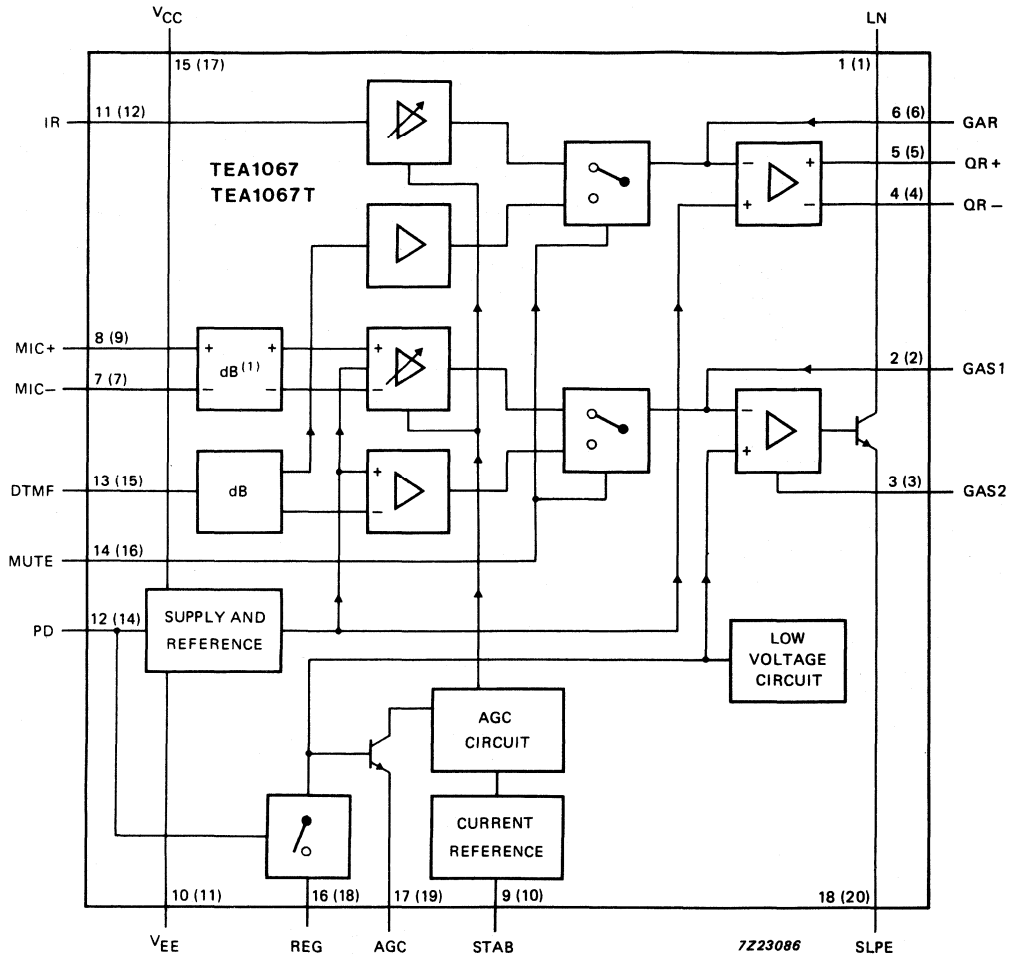
- Low DC line voltage; operates down to 1.6 V (excluding polarity guard)
- Voltage regulator with adjustable static resistance
- Provides supply with limited current for external circuitry
- Symmetrical high-impedance inputs (64 kΩ) for dynamic, magnetic or piezoelectric microphones
- Asymmetrical high-impedance input (32 kΩ) for electret microphone
- DTMF signal input with confidence tone
- Mute input for pulse or DTMF dialling
- Power down input for pulse dial or register recall
- Receiving amplifier for magnetic, dynamic or piezoelectric earpieces
- Large gain setting range on microphone and earpiece amplifiers
- Line current dependent line loss compensation facility for microphone and earpiece amplifiers
- Gain control adaptable to exchange supply
- DC line voltage adjustment capability

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Line voltage	I_{line} = 15 mA	V_{LN}	3.65	3.9	4.15	V
Line current operating range	normal operation					
	TEA1067	I_{line}	11	–	140	mA
	TEA1067T	I_{line}	11	–	140	mA
	with reduced performance	I_{line}	1	–	11	mA
Internal supply current	power down					
	input LOW	I_{CC}	-	1	1.35	mA
	input HIGH	I_{CC}	–	55	82	μA
Supply voltage for peripherals	I_{line} = 15 mA; I_p = 1.4 mA; mute input HIGH	V_{CC}	2.2	2.4	–	V
	I_{line} = 15 mA; I_p = 0.9 mA; mute input HIGH	V_{CC}	2.5	–	–	V
Voltage gain range						
microphone amplifier		G_v	44	–	52	dB
receiving amplifier		G_v	20	–	45	dB
Line loss compensation gain control range		ΔG_v	5.5	5.9	6.3	dB
Exchange supply voltage range		V_{exch}	36	–	60	V
Exchange feeding bridge resistance range		R_{exch}	0.4	–	1	kΩ

PACKAGE OUTLINES

TEA1067: 18-lead DIL; plastic (SOT102).
TEA1067T: 20-lead mini-pack; plastic (SO20; SOT163A).



Figures in parenthesis refer to TEA1067T.

Fig. 1 Block diagram.

PINNING

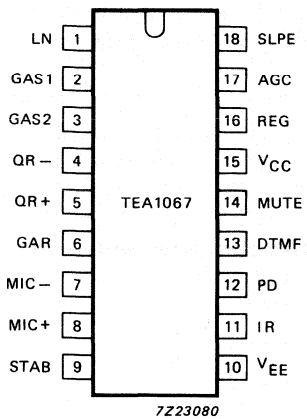


Fig. 2 (a) Pinning diagram for TEA1067 18-lead DIL version.

1	LN	positive line terminal
2	GAS1	gain adjustment; transmitting amplifier
3	GAS2	gain adjustment; transmitting amplifier
4	QR–	inverting output; receiving amplifier
5	QR+	non-inverting output receiving amplifier
6	GAR	gain adjustment; receiving amplifier
7	MIC–	inverting microphone input
8	MIC+	non-inverting microphone input
9	STAB	current stabilizer
10	V_{EE}	negative line terminal
11	IR	receiving amplifier input
12	PD	power-down input
13	DTMF	dual-tone multi-frequency input
14	MUTE	mute input
15	V_{CC}	positive supply decoupling
16	REG	voltage regulator decoupling
17	AGC	automatic gain control input
18	SLPE	slope (DC resistance) adjustment

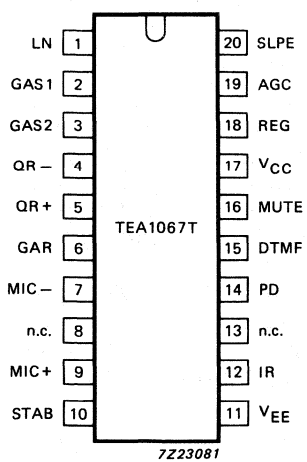


Fig. 2 (b) Pinning diagram for TEA1067T 20-lead mini-pack version.

1	LN	positive line terminal
2	GAS1	gain adjustment; transmitting amplifier
3	GAS2	gain adjustment; transmitting amplifier
4	QR–	inverting output; receiving amplifier
5	QR+	non-inverting output receiving amplifier
6	GAR	gain adjustment, receiving amplifier
7	MIC–	inverting microphone input
8	n.c.	not connected
9	MIC+	non-inverting microphone input
10	STAB	current stabilizer
11	V_{EE}	negative line terminal
12	IR	receiving amplifier input
13	n.c.	not connected
14	PD	power-down input
15	DTMF	dual-tone multi-frequency input
16	MUTE	mute input
17	V_{CC}	positive supply decoupling
18	REG	voltage regulator decoupling
19	AGC	automatic gain control input
20	SLPE	slope (DC resistance) adjustment

FUNCTIONAL DESCRIPTION

Supply: V_{CC}, LN, SLPE, REG and STAB

Power for the TEA1067 and its peripheral circuits is usually obtained from the telephone line. The IC develops its own supply at V_{CC} and regulates its voltage drop. The supply voltage V_{CC} may also be used to supply external circuits e.g. dialling and control circuits.

Decoupling of the supply voltage is performed by a capacitor between V_{CC} and V_{EE} while the internal voltage regulator is decoupled by a capacitor between REG and V_{EE}.

The DC current drawn by the device will vary in accordance with varying values of the exchange voltage (V_{exch}), the feeding bridge resistance, (R_{exch}) and the DC resistance of the telephone line (R_{line}).

The TEA1067 has an internal current stabilizer working at a level determined by a 3.6 kΩ resistor connected between STAB and V_{EE} (see Fig. 6). When the line current (I_{line}) is more than 0.5 mA greater than the sum of the IC supply current (I_{CC}) and the current drawn by the peripheral circuitry connected to V_{CC} (I_p) the excess current is shunted to V_{EE} via LN.
The regulated voltage on the line terminal (V_{LN}) can be calculated as:

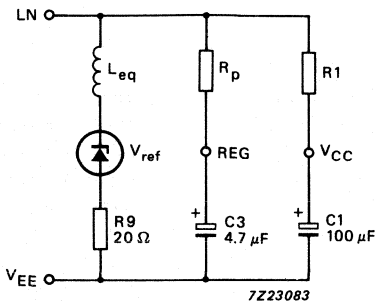
$$V_{LN} = V_{ref} + I_{SLPE} \times R9; \text{ or } V_{LN} = V_{ref} + [(I_{line} - I_{CC} - 0.5 \times 10^{-3}\,A) - I_p] \times R9$$

Where V_{ref} is an internally generated temperature compensated reference voltage of 3.6 V and R9 is an external resistor connected between SLPE and V_{EE}. In normal use the value of R9 would be 20 Ω. Changing the value of R9 will also affect microphone gain, DTMF gain, gain control characteristics, side-tone level and maximum output swing on LN, and the DC characteristics (especially at the lower voltages).

Under normal conditions, when $I_{SLPE} \gg I_{CC} + 0.5\,mA + I_p$, the static behaviour of the circuit is that of a 3.6 V regulator diode with an internal resistance equal to that of R9. In the audio frequency range the dynamic impedance is largely determined by R1. Fig. 3 shows the equivalent impedance of the circuit.

At line currents below 9 mA the internal reference voltage is automatically adjusted to a lower value (typically 1.6 V at 1 mA). This means that the operation of more sets in parallel is possible with DC line voltages (excluding the polarity guard) down to an absolute minimum voltage of 1.6 V. With line currents below 9 mA the circuit has limited sending and receiving levels. The internal reference voltage can be adjusted by means of an external resistor (R_{VA}). This resistor connected between LN and REG will decrease the internal reference voltage, connected between REG and SLPE it will increase the internal reference voltage.

Current (I_p) available from V_{CC} for peripheral circuits depends on the external components used. Fig. 9 shows this current for $V_{CC} > 2.2$ V. If MUTE is LOW when the receiving amplifier is driven the available current is further reduced. Current availability can be increased by connecting the supply IC (TEA1081) in parallel with R1, as shown in Fig. 16 (c), or by increasing the DC line voltage by means of an external resistor (R_{VA}) connected between REG and SLPE.



$R_p = 16.2\ k\Omega$
$L_{eq} = C3 \times R9 \times R_p$

Fig. 3 Equivalent impedance circuit.

Microphone inputs (MIC+ and MIC−) and gain adjustment pins (GAS1 and GAS2)

The TEA1067 has symmetrical microphone inputs. Its input impedance is 64 kΩ (2 x 32 kΩ) and its voltage gain is typically 52 dB (when R7 = 68 kΩ, see Fig. 13). Dynamic, magnetic, piezoelectric or electret (with built-in FET source followers) microphones can be used. Microphone arrangements are shown in Fig. 10.

The gain of the microphone amplifier can be adjusted between 44 dB and 52 dB to suit the sensitivity of the transducer in use. The gain is proportional to the value of R7 which is connected between GAS1 and GAS2. Stability is ensured by the external capacitor C6 which is connected between GAS1 and SLPE. The value of C6 is 100 pF but this may be increased to obtain a first-order low-pass filter. The cut-off frequency corresponds to the time constant R7 x C6.

Mute input (MUTE)

When MUTE is HIGH the DTMF input is enabled and the microphone and receiving amplifier inputs are inhibited. The reverse is true when MUTE is LOW or open-circuit. MUTE switching causes only negligible clicking on the earpiece outputs and line. If the number of parallel sets in use causes a drop in line current to below 6 mA the speech amplifiers remain active independent to the DC level applied to the MUTE input.

Dual-tone multi-frequency input (DTMF)

When the DTMF input is enabled dialling tones may be sent onto the line. The voltage gain from DTMF to LN is typically 25.5 dB (when R7 = 68 kΩ) and varies with R7 in the same way as the microphone gain. The signalling tones can be heard in the earpiece at a low level (confidence tone).

Receiving Amplifier (IR, QR+, QR− and GAR)

The receiving amplifier has one input (IR), one non-inverting complementary output (QR+) and an inverting complementary output (QR−). These outputs may be used for single-ended or differential drive depending on the sensitivity and type of earpiece used (see Fig. 11). IR to QR + gain is typically 31 dB (when R4 = 100 kΩ), this is sufficient for low-impedance magnetic or dynamic microphones which are suited for single-ended drive. Using both outputs for differential drive gives an additional gain of 6 dB. This feature can be used when the earpiece impedance exceeds 450 Ω (high-impedance dynamic or piezoelectric types).

FUNCTIONAL DESCRIPTION (continued)

Receiving Amplifier (IR, QR+, QR− and GAR) (continued)

The receiving amplifier gain can be adjusted between 20 and 39 dB with single-ended drive and between 26 and 45 dB with differential drive, to match the sensitivity of the transducer in use. The gain is set with the value of R4 which is connected between GAR and QR+. Overall receive gain between LN and QR+ is calculated by substracting the anti-sidetone network attenuation (32 dB) from the amplifier gain. Two external capacitors C4 and C7, ensure stability. C4 is normally 100 pF and C7 is 10 x the value of C4. The value of C4 may be increased to obtain a first-order low-pass filter. The cut-off frequency will depend on the time constant R4 x C4.
The output voltage of the receiving amplifier is specified for continuous-wave drive. The maximum output voltage will be higher under speech conditions where the peak to RMS ratio is higher.

Automatic gain control input (AGC)

Automatic line loss compensation is achieved by connecting a resistor (R6) between AGC and V_{EE}. The automatic gain control varies the gain of the microphone amplifier and the receiving amplifier in accordance with the DC line current. The control range is 5.9 dB. This corresponds to a line length of 5 km for a 0.5 mm diameter copper twisted-pair cable with a DC resistance of 176 Ω/km and an average attenuation 1.2 dB/km. Resistor R6 should be chosen in accordance with the exchange supply voltage and its feeding bridge resistance (see Fig. 12 and Table 1). The ratio of start and stop currents of the AGC curve is independent of the value of R6. If no automatic line loss compensation is required the AGC may be left open-circuit. The amplifiers, in this condition, will give their maximum specified gain.

Power-down input (PD)

During pulse dialling or register recall (timed loop break) the telephone line is interrupted. During these interruptions the telephone line provides no power for the transmission circuit or circuits supplied by V_{CC}. The charge held on C1 will bridge these gaps. This bridging is made easier by a HIGH level on the PD input which reduces the typical supply current from 1 mA to 55 μA and switches off the voltage regulator preventing discharge through LN. When PD is HIGH the capacitor at REG is disconnected with the effect that the voltage stabilizer will have no switch-on delay after line interruptions. This minimizes the contribution of the IC to the current waveform during pulse dialling or register recall. When this facility is not required PD may be left open-circuit.

Side-tone suppression

The anti-sidetone network, $R1//Z_{line}$, R2, R3, R9 and Z_{bal}, (see Fig. 4) suppresses transmitted signal in the earpiece. Compensation is maximum when the following conditions are fulfilled:

(a) $R9 \times R2 = R1\ (R3 + [R8//Z_{bal}])$;

(b) $(Z_{bal}/[Z_{bal} + R8]) = (Z_{line}/[Z_{line} + R1])$

If fixed values are chosen for R1, R2, R3, and R9 then condition (a) will always be fulfilled when $|R8//Z_{bal}| \ll R3$. To obtain optimum side-tone suppression condition (b) has to be fulfilled resulting in:

$Z_{bal} = (R8/R1)\ Z_{line} = k.Z_{line}$ where k is a scale factor; $k = (R8/R1)$

The scale factor (k), dependent on the value of R8, is chosen to meet the following criteria:

(a) Compatability with a standard capacitor from the E6 or E12 range for Z_{bal}

(b) $|Z_{bal}//R8| \ll R3$ to fulfill condition (a) and thus ensuring correct anti-sidetone bridge operation

(c) $|Z_{bal} + R8| \gg R9$ to avoid influencing the transmitter gain

In practice Z_{line} varies considerably with the line type and length. The value chosen for Z_{bal} should therefore be for an average line length thus giving optimum setting for short or long lines.

Example

The line balance impedance (Z_{bal}) at which the optimum suppression is present can be calculated by: suppose Z_{line} = 210 Ω + (1265 Ω/140 nF), representing a 5 km line of 0.5 mm diameter, copper, twisted-pair cable matched to 600 Ω (176 Ω/km; 38 nF/km).
When k = 0.64 then R8 = 390 Ω; Z_{bal} = 130 Ω + (820 Ω//220 nF).

The anti-sidetone network for the TEA1060 family shown in Fig. 4 attenuates the signal received from the line by 32 dB before it enters the receiving amplifier. The attenuation is almost constant over the whole audio frequency range. Fig. 5 shows a conventional Wheatstone bridge anti-sidetone circuit that can be used as an alternative. Both bridge types can be used with either resistive or complex set impedances.

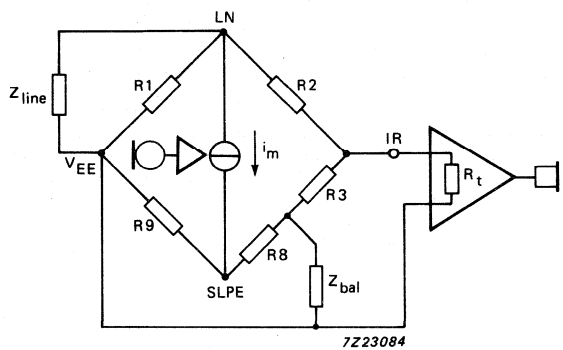


Fig. 4 Equivalent circuit of TEA1060 anti-sidetone bridge.

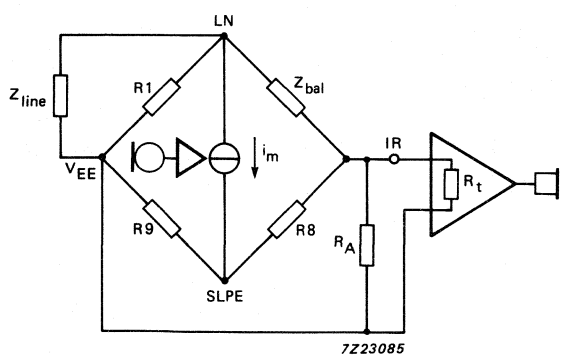


Fig. 5 Equivalent circuit of an anti-sidetone network in a Wheatstone bridge configuration.

More information can be found in the designer guide; 9398 341 10011

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Positive continuous line voltage		V_{LN}	–	12	V
Repetitive line voltage during switch-on line interruption		V_{LN}	–	13.2	V
Repetitive peak line voltage for a 1 ms pulse per 5 s	R9 = 20 Ω; R10 = 13 Ω (Fig. 15)	V_{LN}	–	28	V
Line current TEA1067(1)	R9 = 20 Ω	I_{line}	–	140	mA
Line current TEA1067T (1)	R9 = 20 Ω	I_{line}	–	140	mA
Voltage on all other pins		V_i	–	V_{CC} + 0.7	V
		$-V_i$	–	0.7	V
Total power dissipation (2)	R9 = 20 Ω				
TEA1067		P_{tot}	–	769	mW
TEA1067T		P_{tot}	–	550	mW
Storage temperature range		T_{stg}	−40	+ 125	°C
Operating ambient temperature range		T_{amb}	−25	+ 75	°C
Junction temperature		T_j	–	+ 125	°C

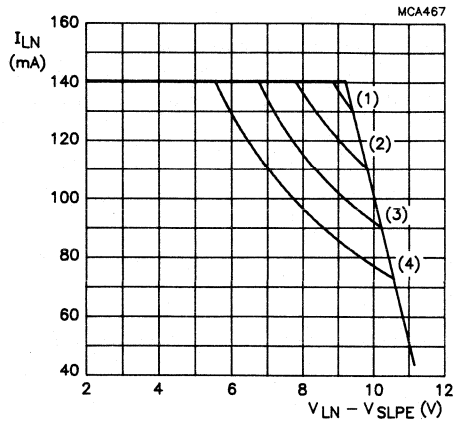
(1) Mostly dependent on the maximum required T_{amb} and on the voltage between LN and SLPE. See Figs 6 and 7 to determine the current as a function of the required voltage and the temperature.

(2) Calculated for the maximum ambient temperature specified T_{amb} = 75 °C and a maximum junction temperature of 125 °C.

THERMAL RESISTANCE

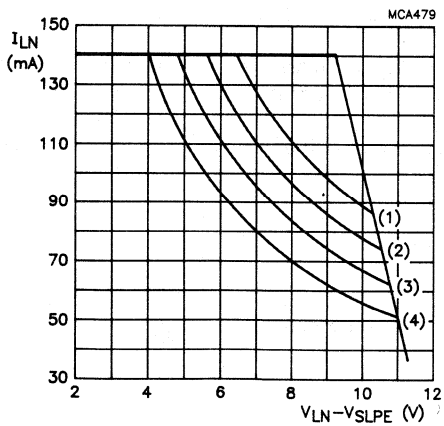
From junction to ambient in free air

TEA1067	$R_{th\ j\text{-}a}$	typ.	65	K/W
TEA1067T mounted on glass epoxy board 41 x 19 x 1.5 mm	$R_{th\ j\text{-}a}$	typ.	90	K/W



	T_{amb}	P_{tot}
(1)	45 °C	1231 mW
(2)	55 °C	1077 mW
(3)	65 °C	923 mW
(4)	75 °C	769 mW

Fig. 6 TEA1067 safe operating area.



	T_{amb}	P_{tot}
(1)	45 °C	888 mW
(2)	55 °C	777 mW
(3)	65 °C	666 mW
(4)	75 °C	555 mW

Fig. 7 TEA1067T safe operating area.

CHARACTERISTICS

I_{line} = 11 to 140 mA; V_{EE} = 0 V; f = 800 Hz; T_{amb} = 25 °C; unless otherwise specified

parameter	condition	symbol	min.	typ.	max.	unit
Supply; LN and V_{CC}						
Voltage drop over circuit, between LN and V_{EE}	microphone inputs open					
	I_{line} = 1 mA	V_{LN}	–	1.6	–	V
	I_{line} = 4 mA	V_{LN}	1.75	2.0	2.25	V
	I_{line} = 7 mA	V_{LN}	2.25	2.8	3.35	V
	I_{line} = 11 mA	V_{LN}	3.55	3.8	4.05	V
	I_{line} = 15 mA	V_{LN}	3.65	3.9	4.15	V
	I_{line} = 100 mA	V_{LN}	4.9	5.6	6.5	V
	I_{line} = 140 mA	V_{LN}	–	–	7.5	V
Variation with temperature	I_{line} = 15 mA	$\Delta V_{LN}/\Delta T$	−3	−1	1	mV/K
Voltage drop over circuit, between LN and V_{EE} with external resistor R_{VA}	I_{line} = 15 mA; R_{VA} (LN to REG) = 68 kΩ		3.1	3.4	3.7	V
	I_{line} = 15 mA; R_{VA} (REG to SLPE) = 39 kΩ		4.2	4.5	4.8	V
Supply current	PD = LOW; V_{CC} = 2.8 V	I_{CC}	–	1.0	1.35	mA
Supply current	PD = HIGH; V_{CC} = 2.8 V	I_{CC}	–	55	82	μA
Supply voltage available for peripheral circuitry	I_{line} = 15 mA; MUTE = HIGH					
	I_p = 1.4 mA	V_{CC}	2.2	2.4	–	V
	I_p = 0 mA	V_{CC}	2.95	3.2	–	V
Microphone inputs MIC+ and MIC−						
Input impedance (differential) between MIC− and MIC+		$\|Z_i\|$	51	64	77	kΩ
Input impedance (single-ended) MIC− or MIC+ to V_{EE}		$\|Z_i\|$	25.5	32	38.5	kΩ
Common mode rejection ratio		k_{CMR}	–	82	–	dB
Voltage gain MIC+/MIC− to LN	I_{line} = 15 mA; R7 = 68 kΩ	G_v	51	52	53	dB

parameter	conditions	symbol	min.	typ.	max.	unit
Microphone inputs MIC+ and MIC– (continued)						
Gain variation with frequency at f = 300 Hz and f = 3400 Hz	w.r.t. 800 Hz	ΔG_{vf}	–0.5	± 0.2	+0.5	dB
Gain variation with temperature at –25 °C and +75 °C	w.r.t. 25 °C without R6; I_{line} = 50 mA	ΔG_{vT}	–	± 0.2	–	dB
Dual-tone multi-frequency input DTMF						
Input impedance		$\lvert Z_i \rvert$	16.8	20.7	24.6	kΩ
Voltage gain from DTMF to LN	I_{line} = 15 mA; R7 = 68 kΩ	G_v	24.5	25.5	26.5	dB
Gain variation with frequency at f = 300 Hz and f = 3400 Hz	w.r.t 800 Hz	ΔG_{vf}	–0.5	±0.2	+0.5	dB
Gain variation with temperature at –25 °C and +75 °C	w.r.t. 25 °C I_{line} = 50 mA	ΔG_{vT}	–	±0.2	–	dB
Gain adjustment GAS1 and GAS2						
Gain variation of the transmitting amplifier by varying R7 between GAS1 and GAS2		ΔG_v	–8	–	0	dB
Sending amplifier output LN						
Output voltage	I_{line} = 15 mA THD = 2%	$V_{LN(rms)}$	–	1.9	–	V
	THD = 10%	$V_{LN(rms)}$	1.9	2.2	–	V
	I_{line} = 4 mA; THD = 10%	$V_{LN(rms)}$	–	0.8	–	V
	I_{line} = 7 mA; THD = 10%	$V_{LN(rms)}$	–	1.4	–	V
Noise output voltage	I_{line} = 15 mA; R7 = 68 kΩ; 200 Ω between MIC– and MIC+; psophometrically weighted (P53 curve)	$V_{no(rms)}$	–	–72	–	dBmp

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Receiving amplifier input IR						
Input impedance		$\|Z_i\|$	17	21	25	kΩ
Receiving amplifier outputs QR+ and QR−						
Output impedance (single-ended)		$\|Z_o\|$	–	4	–	Ω
Voltage gain from IR to QR+ or QR−	I_{line} = 15 mA; R4 = 100 kΩ					
single-ended	R_L (from QR+ or QR−) = 300 Ω	G_v	30	31	32	dB
differential	R_L (from QR+ or QR−) = 600 Ω	G_v	36	37	38	dB
Gain variation with frequency at f = 300 Hz and f = 3400 Hz	w.r.t. 800 Hz	ΔG_{vf}	−0.5	−0.2	0	dB
Gain variation with temperature at −25 °C and +75 °C	w.r.t. 25 °C without R6; I_{line} = 50 mA	ΔG_{vT}	–	±0.2	–	dB
Output voltage	sinewave drive I_{line} = 15 mA; I_p = 0 mA; THD = 2% R4 = 100 kΩ					
single-ended	RL = 150 Ω	$V_{o(rms)}$	0.25	0.29	–	V
	RL = 450 Ω	$V_{o(rms)}$	0.45	0.55	–	V
differential	f = 3400 Hz; series R = 100 Ω; C_L = 47 nF	$V_{o(rms)}$	0.65	0.80	–	V
Output voltage	THD = 10%; RL = 150 Ω R4 = 100 kΩ					
	I_{line} = 4 mA	$V_{o(rms)}$	–	15	–	mV
	I_{line} = 7 mA	$V_{o(rms)}$	–	130	–	mV
Noise output voltage	I_{line} = 15 mA; R4 = 100 kΩ; IR open-circuit psophometrically weighted; (P53 curve)					
single-ended	RL = 300 Ω	$V_{no(rms)}$	–	50	–	μV
differential	RL = 600 Ω	$V_{no(rms)}$	–	100	–	μV

parameter	conditions	symbol	min.	typ.	max.	unit
Gain adjustment GAR						
Gain variation of receiving amplifier achievable by varying R4 between GAR and QR		ΔG_v	−11	–	+8	dB
Mute input						
Input voltage HIGH		V_{IH}	1.5	–	V_{CC}	V
Input voltage LOW		V_{IL}	–	–	0.3	V
Input current		I_{MUTE}	–	8	15	μA
Gain reduction MIC+ or MIC− to LN	MUTE = HIGH	ΔG_v	–	70	–	dB
Voltage gain from DTMF to QR+ or QR−	MUTE = HIGH; R4 = 100 kΩ; single-ended; R_L = 300 Ω	G_v	−21	−19	−17	dB
Power-down input PD						
Input voltage HIGH		V_{IH}	1.5	–	V_{CC}	V
Input voltage LOW		V_{IL}	–	–	0.3	V
Input current		I_{PD}	–	5	10	μA
Automatic gain control input AGC Controlling the gain from IR to QR+/QR− and the gain from MIC+/MIC− to LN; R6 between AGC and V_{EE}	R6 = 110 kΩ					
Gain control range	I_{line} = 70 mA	ΔG_v	−5.5	−5.9	−6.3	dB
Highest line current for maximum gain		I_{line}	–	23	–	mA
Minimum line current for minimum gain		I_{line}	–	61	–	mA
Reduction of gain between I_{line} = 15 mA and I_{line} = 35 mA		ΔG_v	−1.0	−1.5	−2.0	dB

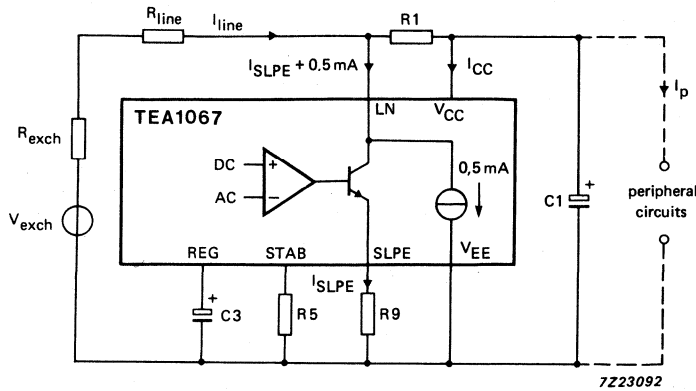
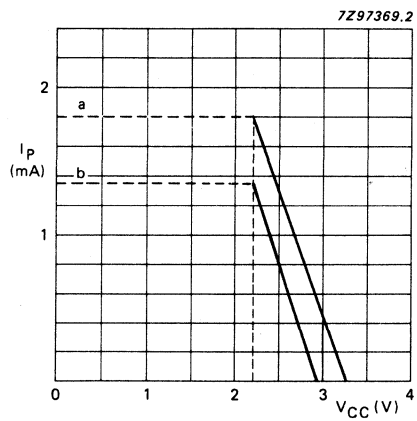


Fig. 8 Supply arrangement.



(a) I_p = 1.8 mA
(b) I_p = 1.35 mA
I_{line} = 15 mA at V_{LN} = 3.9 V
R1 = 620 Ω and R9 = 20 Ω.

Fig. 9 Typical current I_p available from V_{CC} for peripheral circuitry with $V_{CC} >= 2.2$ V. Curve (a) is valid when the receiving amplifier is not driven or when MUTE = HIGH, curve (b) is valid when MUTE = LOW and the receiving amplifier is driven; $V_{o(rms)}$ = 150 mV, R_L = 150 Ω asymmetrical.
The supply possibilities can be increased simply by setting the voltage drop over the circuit V_{LN} to a higher value by means of resistor R_{VA} connected between REG and SLPE.

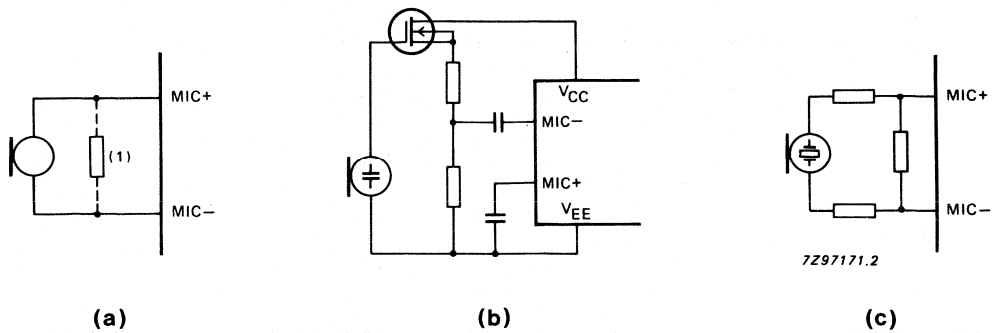


Fig. 10 Alternative microphone arrangements.

(a) Magnetic or dynamic microphone. The resistor marked (1) may be connected to decrease the terminating impedance.
(b) Electret microphone.
(c) Piezoelectric microphone.

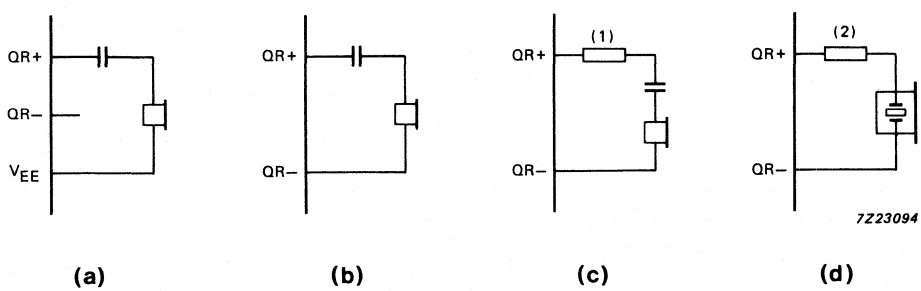


Fig. 11 Alternative receiver arrangements.

(a) Dynamic earpiece with less than 450 Ω impedance.
(b) Dynamic earpiece with more than 450 Ω impedance.
(c) Magnetic earpiece with more than 450 Ω impedance. The resistor marked (1) may be connected to prevent distortion (inductive load).
(d) Piezoelectric earpiece. The resistor marked (2) is required to increase the phase margin (capacitive load).

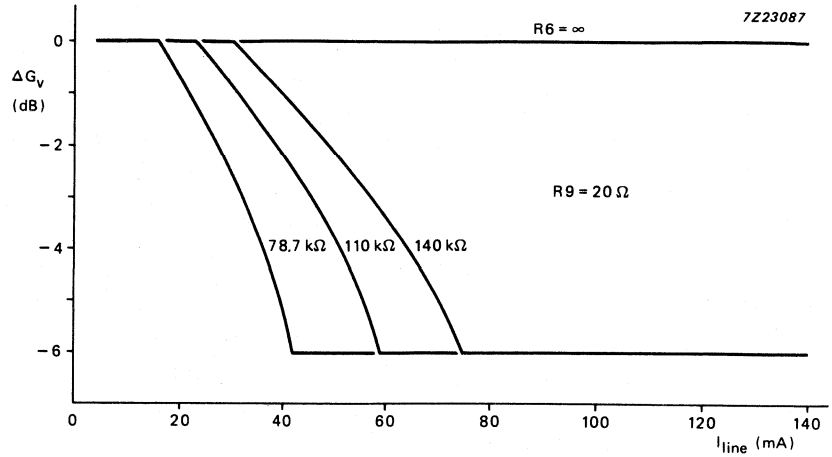


Fig. 12 Variation of gain with line current, with R6 as a parameter.

Table 1 Values of resistor R6 for optimum line loss compensation, for various usual values of exchange supply voltage (V_{exch}) and exchange feeding bridge resistance (R_{exch}); R9 = 20 Ω.

		R_{exch} (Ω)			
		400	600	800	1000
		R6 (kΩ)			
V_{exch} (V)	36	100	78.7	X	X
	48	140	110	93.1	82
	60	X	X	120	102

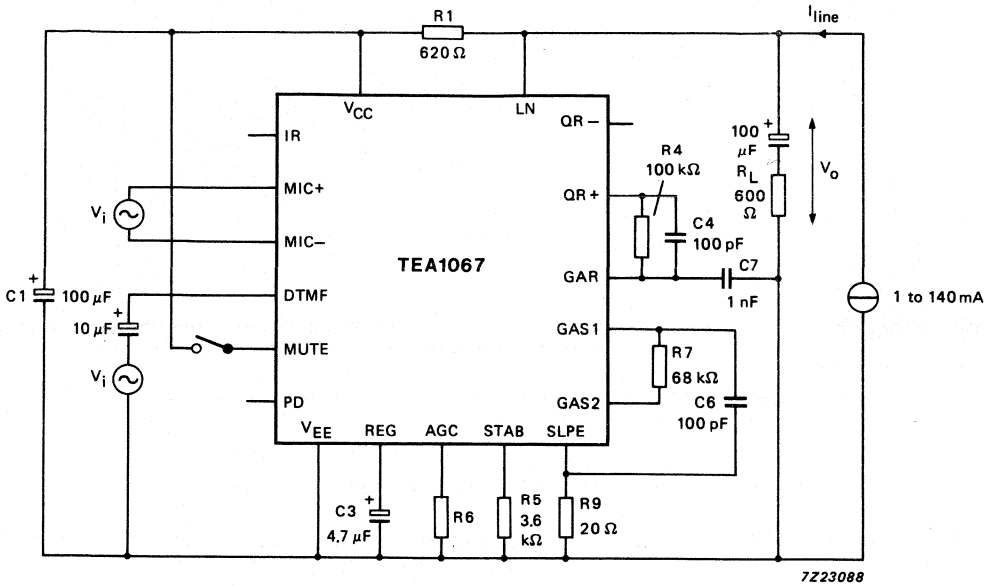


Fig. 13 Test circuit for defining voltage gain of MIC+, MIC– and DTMF inputs. Voltage gain is defined as; $G_V = 20 \log |V_o/V_i|$. For measuring the gain from MIC+ and MIC– the MUTE input should be LOW or open, for measuring the DTMF input MUTE should be HIGH. Inputs not under test should be open.

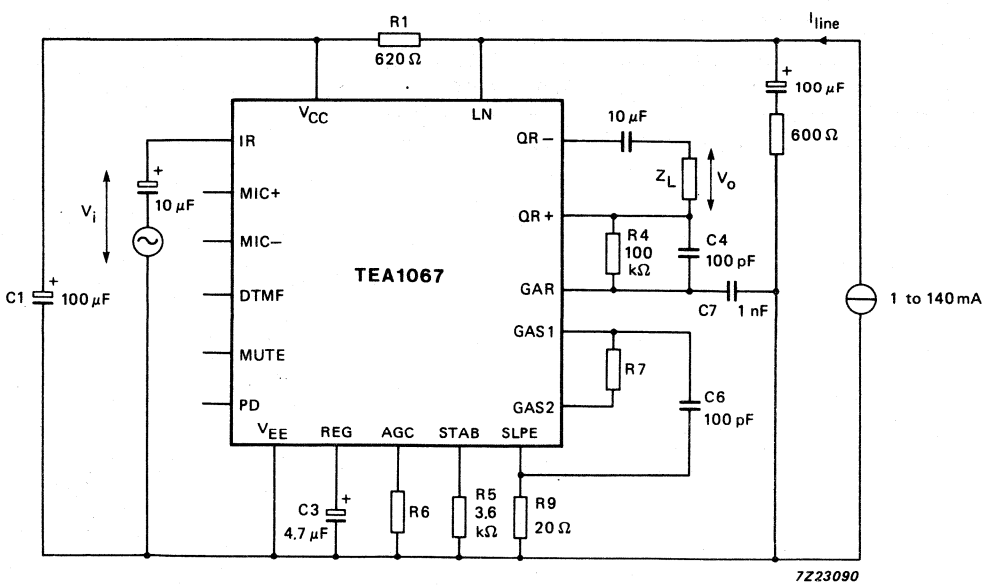


Fig. 14 Test circuit for defining voltage gain of the receiving amplifier. Voltage gain is defined as; $G_V = 20 \log |V_o/V_i|$.

APPLICATION INFORMATION

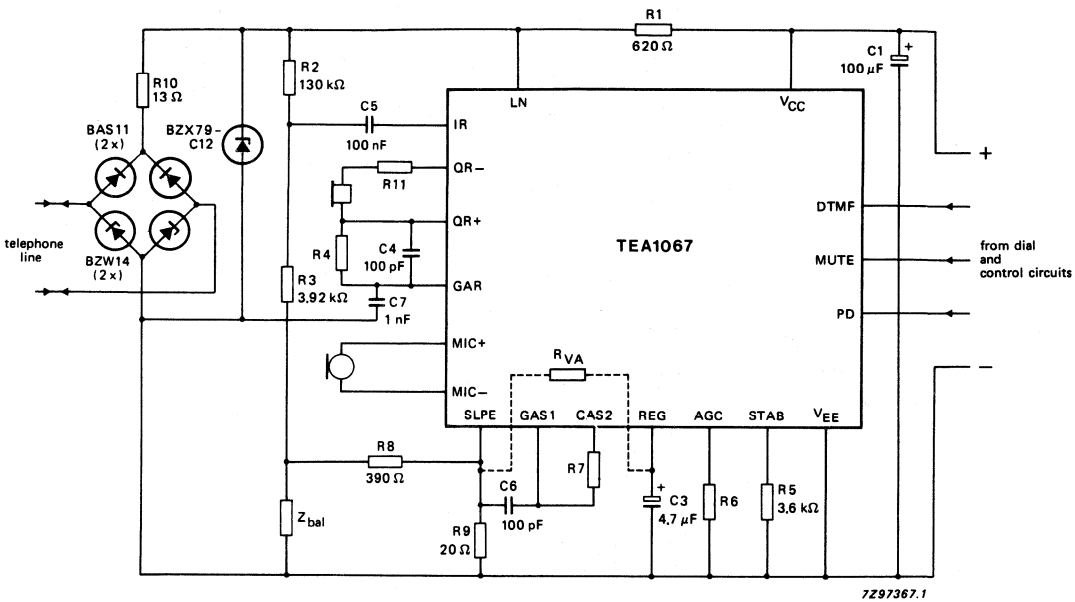


Fig. 15 Typical application of the TEA1067, shown here with a piezoelectric earpiece and DTMF dialling. The bridge to the left, the zener diode and R10 limit the current into the circuit and the voltage across the circuit during line transients. Pulse dialling or register recall require a different protection arrangement.
The DC line voltage can be set to a higher value by the resistor R_{VA} (REG to SLPE).

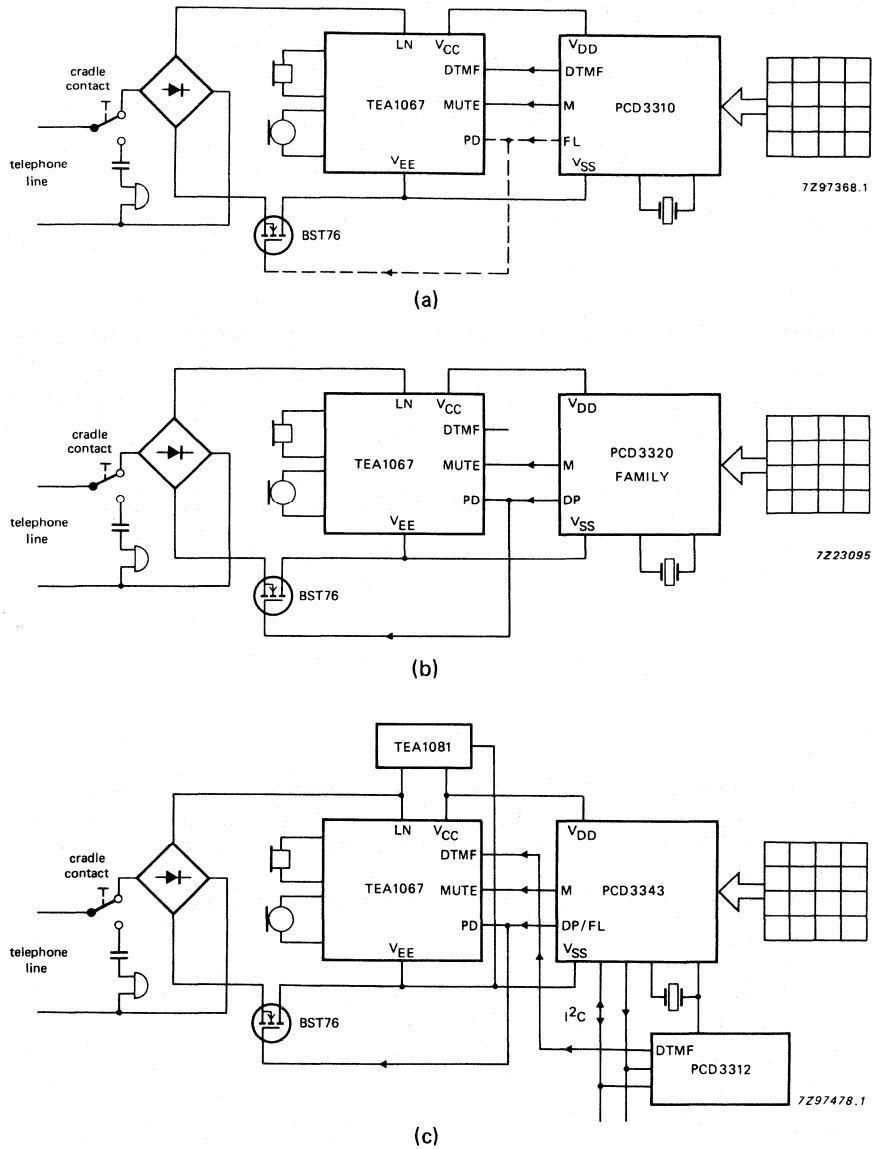


Fig. 16 Typical applications of the TEA1067 (simplified).

(a) DTMF-Pulse set with CMOS dialling circuit PCD3310.
The dashed lines show an optional flash (register recall by timed loop break).

(b) Pulse dial set with one of the PCD3320 family of CMOS interrupted current-loop dialling circuits.

(c) Dual-standard (pulse and DTMF) feature phone with the PCD3343 CMOS controller and the PCD3312 CMOS DTMF generator with I^2C-bus. Supply is provided by the TEA1081 supply circuit.

VERSATILE TELEPHONE TRANSMISSION CIRCUIT WITH DIALLER INTERFACE

GENERAL DESCRIPTION

The TEA1068 is a bipolar integrated circuit performing all speech and line interface functions required in fully electronic telephone sets. It performs electronic switching between dialling and speech.

Features

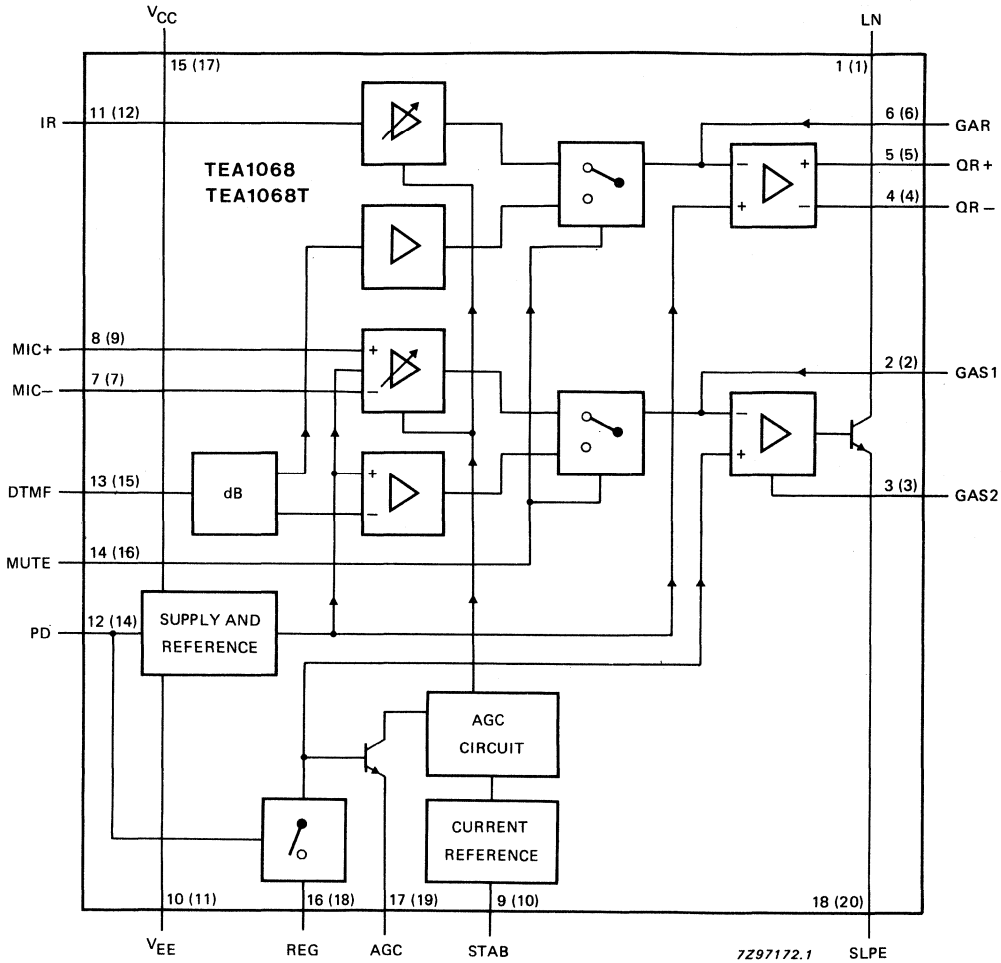
- Voltage regulator with adjustable static resistance
- Provides supply for external circuitry
- Symmetrical high-impedance inputs (64 kΩ) for dynamic, magnetic or piezoelectric microphones
- Asymmetrical high-impedance input (32 kΩ) for electret microphone
- DTMF signal input with confidence tone
- Mute input for pulse or DTMF dialling
- Power down input for pulse dial or register recall
- Receiving amplifier for magnetic, dynamic or piezoelectric earpieces
- Large gain setting range on microphone and earpiece amplifiers
- Line current dependent line loss compensation facility for microphone and earpiece amplifiers
- Gain control adaptable to exchange supply
- DC line voltage adjustment capability.

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Line voltage	I_{line} = 15 mA	V_{LN}	4.2	4.45	4.7	V
Line current operating range	normal operation					
	TEA1068	I_{line}	10	–	140	mA
	TEA1068T	I_{line}	10	–	100	mA
Internal supply current	power down					
	input LOW	I_{CC}	–	0.96	1.3	mA
	input HIGH	I_{CC}	–	55	82	μA
Supply voltage for peripherals	I_{line} = 15 mA; mute input HIGH					
	I_p = 1.2 mA	V_{CC}	2.8	3.05	–	V
	I_p = 1.7 mA	V_{CC}	2.5	–	–	V
Voltage gain range						
microphone amplifier		G_v	44	–	60	dB
receiving amplifier		G_v	17	–	39	dB
Line loss compensation gain control range		ΔG_v	5.5	5.9	6.3	dB
Exchange supply voltage range		V_{exch}	24	–	60	V
Exchange feeding bridge resistance range		R_{exch}	0.4	–	1	kΩ

PACKAGE OUTLINES

TEA1068: 18-lead DIL; plastic (SOT102).
TEA1068T: 20-lead mini-pack; plastic (SO20; SOT163A).



Figures in parenthesis refer to TEA1068T.

Fig. 1 Block diagram.

PINNING

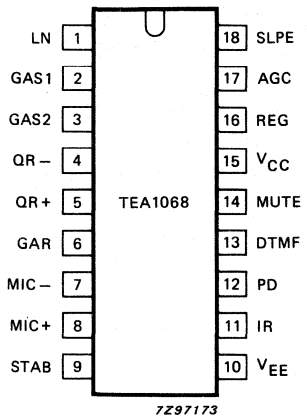


Fig. 2 (a) Pinning diagram for TEA1068 18-lead DIL version.

1	LN	positive line terminal
2	GAS1	gain adjustment; transmitting amplifier
3	GAS2	gain adjustment; transmitting amplifier
4	QR–	inverting output; receiving amplifier
5	QR+	non-inverting output receiving amplifier
6	GAR	gain adjustment; receiving amplifier
7	MIC–	inverting microphone input
8	MIC+	non-inverting microphone input
9	STAB	current stabilizer
10	V_{EE}	negative line terminal
11	IR	receiving amplifier input
12	PD	power-down input
13	DTMF	dual-tone multi-frequency input
14	MUTE	mute input
15	V_{CC}	positive supply decoupling
16	REG	voltage regulator decoupling
17	AGC	automatic gain control input
18	SLPE	slope (DC resistance) adjustment

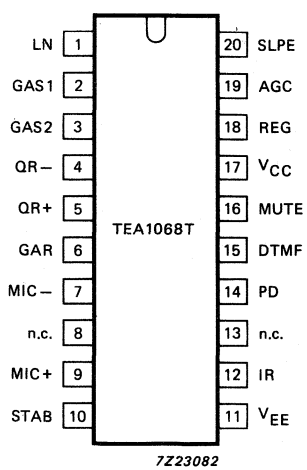


Fig. 2 (b) Pinning diagram for TEA1068T 20-lead mini-pack version.

1	LN	positive line terminal
2	GAS1	gain adjustment; transmitting amplifier
3	GAS2	gain adjustment; transmitting amplifier
4	QR–	inverting output; receiving amplifier
5	QR+	non-inverting output receiving amplifier
6	GAR	gain adjustment; receiving amplifier
7	MIC–	inverting microphone input
8	n.c.	not connected
9	MIC+	non-inverting microphone input
10	STAB	current stabilizer
11	V_{EE}	negative line terminal
12	IR	receiving amplifier input
13	n.c.	not connected
14	PD	power-down input
15	DTMF	dual-tone multi-frequency input
16	MUTE	mute input
17	V_{CC}	positive supply decoupling
18	REG	voltage regulator decoupling
19	AGC	automatic gain control input
20	SLPE	slope (DC resistance) adjustment

FUNCTIONAL DESCRIPTION

Supply; V_{CC}, LN, SLPE, REG and STAB

Power for the TEA1068 and its peripheral circuits is usually obtained from the telephone line. The IC develops its own supply at V_{CC} and regulates its voltage drop. The supply voltage V_{CC} may also be used to supply external circuits e.g. dialling and control circuits.

Decoupling of the supply voltage is performed by a capacitor between V_{CC} and V_{EE} while the internal voltage regulator is decoupled by a capacitor between REG and V_{EE}.

The DC current drawn by the device will vary in accordance with varying values of the exchange voltage (V_{exch}), the feeding bridge resistance, (R_{exch}) and the DC resistance of the telephone line (R_{line}).

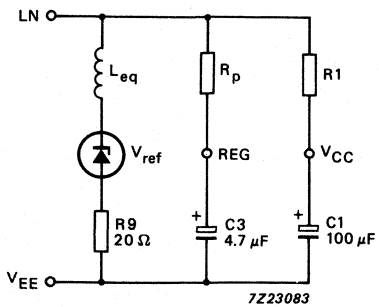
The TEA 1068 has an internal current stabilizer operating at a level determined by a 3.6 kΩ resistor connected between STAB and V_{EE} (see Fig. 8). When the line current (I_{line}) is more than 0.5 mA greater than the sum of the IC supply current (I_{CC}) and the current drawn by the peripheral circuitry connected to V_{CC} (I_p) the excess current is shunted to V_{EE} via LN.
The regulated voltage on the line terminal (V_{LN}) can be calculated as:

$$V_{LN} = V_{ref} + I_{SLPE} \times R9; \text{ or } V_{LN} = V_{ref} + [(I_{line} - I_{CC} - 0.5 \times 10^{-3}) - I_p] \times R9$$

Where V_{ref} is an internally generated temperature compensated reference voltage of 4.2 V and R9 is an external resistor connected between SLPE and V_{EE}. In normal use the value of R9 would be 20 Ω. Changing the value of R9 will also affect microphone gain, DTMF gain, gain control characteristics side-tone level and maximum output swing on LN, and the DC characteristics (especially at the lower voltages).

Under normal conditions, when $I_{SLPE} \gg I_{CC} + 0.5$ mA + I_p, the static behaviour of the circuit is that of a 4.2 V regulator diode with an internal resistance equal to that of R9. In the audio frequency range the dynamic impedance is largely determined by R1. Fig. 3 shows the equivalent impedance of the circuit.

The internal reference voltage can be adjusted by means of an external resistor (R_{VA}). This resistor connected between LN and REG will decrease the internal reference voltage, connected between REG and SLPE it will increase the internal reference voltage.
Current (I_p) available from V_{CC} for supplying peripheral circuits depends on external components and on the line current. Figure 9 shows this current for $V_{CC} > 2.2$ V and for $V_{CC} > 3$ V (being the minimum supply voltage for most CMOS circuits including voltage drop for an enable diode).
If MUTE is LOW when the receiving amplifier is driven available current is further reduced.



$R_p = 17.5\ k\Omega$
$L_{eq} = C3 \times R9 \times R_p$

Fig. 3 Equivalent impedance circuit.

Microphone inputs (MIC+ and MIC−) and gain adjustment pins (GAS1 and GAS2)

The TEA1068 has symmetrical microphone inputs. Its input impedance is 64 kΩ (2 x 32 kΩ) and its voltage gain is typically 52 dB (when R7 = 68 kΩ, see Fig. 13). Dynamic, magnetic, piezoelectric or electret (with built-in FET source followers) microphones can be used. Microphone arrangements are shown in Fig. 10.

The gain of the microphone amplifier can be adjusted between 44 dB and 60 dB. The gain is proportional to the value of R7 which is connected between GAS1 and GAS2. Stability is ensured by the external capacitor C6 which is connected between GAS1 and SLPE. The value of C6 is 100 pF but this may be increased to obtain a first-order low-pass filter. The cut-off frequency corresponds to the time constant R7 x C6.

Mute input (MUTE)

When MUTE is HIGH the DTMF input is enabled and the microphone and receiving amplifier inputs are inhibited. The reverse is true when MUTE is LOW or open-circuit. MUTE switching causes only negligable clicking on the earpiece outputs and the line.

Dual-tone multi-frequency input (DTMF)

When the DTMF input is enabled dialling tones may be sent onto the line. The voltage gain from DTMF to LN is typically 25.5 dB (when R7 = 68 kΩ) and varies with R7 in the same way as the microphone gain. The signalling tones can be heard in the telephone earpiece at a low level (confidence tone).

Receiving amplifier (IR, QR+, QR− and GAR)

The receiving amplifier has one input (IR), one non-inverting complementary output (QR+) and an inverting complementary output (QR−). These outputs may be used for single-ended or differential drive depending on the sensitivity and type of earpiece used (see Fig. 11). IR to QR + gain is typically 25 dB (when R4 = 100 kΩ), this is sufficient for low-impedance magnetic or dynamic microphones which are suited for single end drive. Using both outputs for differential drive gives an additional gain of 6 dB. This feature can be used when the earpiece impedance exceeds 450 Ω, (high-impedance dynamic or piezoelectric types).

The output voltage of the receiving amplifier is specified for continuous-wave drive. The maximum output voltage will be higher under speech conditions where the peak to RMS ratio is higher.

FUNCTIONAL DESCRIPTION (continued)

Receiving amplifier (IR, QR+, QR− and GAR) (continued)

The receiving amplifier gain can be adjusted between 17 and 33 dB with single-ended drive and between 26 and 39 dB with differential drive to match the sensitivity of the transducer in use. The gain is set by the external resistor R4 connected between GAR and QR+. Overall receive gain between LN and QR+ is calculated by subracting the anti-sidetone network attenuation, (32 dB), from the amplifier gain. Two external capacitors, C4 and C7, ensure stability. C4 is normally 100 pF and C7 is 10 x the value of C4. The value of C4 may be increased to obtain a first-order low-pass filter. The cut-off frequency will depend on the time constant R4 x C4.

Automatic gain control input (AGC)

Automatic line loss compensation is acieved by connecting a resistor (R6) between AGC and V_{EE}. The automatic gain control varies the gain of the microphone amplifier and the receiving amplifier in accordance with the DC line current. The control range is 5.9 dB. This corresponds to a line length of 5 km for a 0.5 mm diameter copper twisted-pair cable with a DC resistance of 176 Ω/km and an average attenuation 1.2 dB/km. Resistor R6 should be chosen in accordance with the exchange supply voltage and its feeding bridge resistance (see Fig. 12 and Table 1). The ratio of start and stop currents of the AGC curve is independent of the value of R6. If no automatic line loss compensation is required the AGC may be left open-circuit. The amplifiers, in this condition, will give their maximum specified gain.

Power-down input (PD)

During pulse dialling or register recall (timed loop break) the telephone line is interrupted. During these interruptions the telephone line provides no power for the transmission circuit or circuits supplied by V_{CC}. The charge held on C1 will bridge these gaps. This bridging is made easier by a HIGH level on the PD input which reduces the typical supply current from 1 mA to 55 μA and switches off the voltage regulator preventing discharge through LN. When PD is HIGH the capacitor at REG is disconnected with the effect that the voltage stabilizer will have no switch-on delay after line interruptions. This minimizes the contribution of the IC to the current waveform during pulse dialling or register recall. When this facility is not required PD may be left open-circuit.

Side-tone suppression

The anti-sidetone network, ($R1//Z_{line}$, R2, R3 and Z_{bal}), (see Fig. 4) suppresses transmitted signal in the earpiece. Compensation is maximum when the following conditions are fulfilled:

(a) $R9 \times R2 = R1 \ (R3 + [R8//Z_{bal}])$;

(b) $(Z_{bal}/[Z_{bal} + R8]) = (Z_{line}/[Z_{line} + R1])$

If fixed values are chosen for R1, R2, R3, and R9 then condition (a) will always be fulfilled when $|R8//Z_{bal}| \ll R3$. To obtain optimum side-tone suppression condition (b) has to be fulfilled resulting in;

$Z_{bal} = (R8/R1)\ Z_{line} = k.Z_{line}$ where k is a scale factor, $k = (R8/R1)$.

The scale factor (k), dependent on the value of R8, is chosen to meet the following criteria:

(a) Compatability with a standard capacitor from the E6 or E12 range for Z_{bal}

(b) $|Z_{bal}//R8| \ll R3$ to fulfill condition (a) and thus ensuring correct anti-sidetone bridge operation

(c) $|Z_{bal} + R8| \gg R9$ to avoid influencing the transmitter gain

In practice Z_{line} varies considerably with the line type and length. The value chosen for Z_{bal} should therefore be for an average line length thus giving optimum setting for short or long lines.

Example

The balanced line impedance (Z_{bal}) at which the optimum suppression is present can be calculated by: suppose Z_{line} = 210 Ω + (1265 Ω/140 nF), representing a 5 km line of 0.5 mm diameter, copper, twisted-pair cable matched to 600 Ω (176 Ω/km; 38 nF/km).
When k = 0.64 then R8 = 390 Ω; Z_{bal} = 130 Ω + (820 Ω//220 nF).

The anti-sidetone network for the TEA1060 family shown in Fig. 4 attenuates the signal received from the line by 32 dB before it enters the receiving amplifier. The attenuation is almost constant over the whole audio frequency range. Fig. 5 shows a conventional Wheatstone bridge anti-sidetone circuit that can be used as an alternative. Both bridge types can be used with either resistive or complex set impedances.

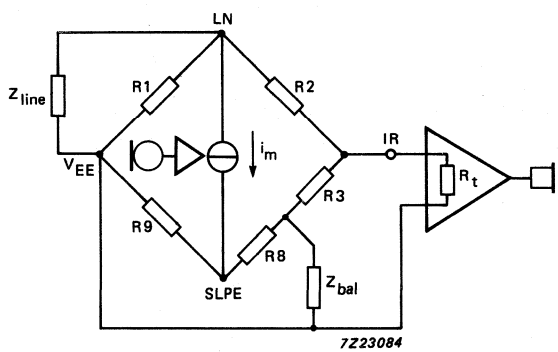


Fig. 4 Equivalent circuit of TEA1060 family anti-sidetone bridge.

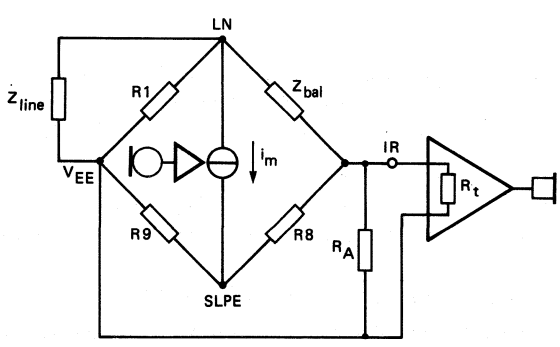


Fig. 5 Equivalent circuit of an anti-sidetone network in a Wheatstone bridge configuration.

More information can be found in the designer guide; 9398 341 10011

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Positive continuous line voltage		V_{LN}	–	12	V
Repetitive line voltage during switch-on line interruption		V_{LN}	–	13.2	V
Repetitive peak line voltage for a 1 ms pulse per 5 s	R9 = 20 Ω; R10 = 13 Ω (Fig. 15)	V_{LN}	–	28	V
Line current TEA1068 (1)	R9 = 20 Ω	I_{line}	–	140	mA
Line current TEA1068T (1)	R9 = 20 Ω	I_{line}	–	140	mA
Voltage on all other pins		V_i	–	V_{CC} + 0.7	V
		V_i	–	−0.7	V
Total power dissipation (2)	R9 = 20 Ω				
TEA1068		P_{tot}	–	769	mW
TEA1068T		P_{tot}	–	555	mW
Storage temperature range		T_{stg}	−40	+ 125	°C
Operating ambient temperature range		T_{amb}	−25	+ 75	°C
Junction temperature		T_j	–	+ 125	°C

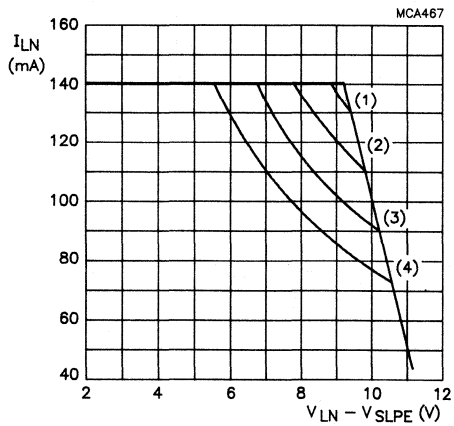
(1) Mostly dependent on the maximum required T_{amb} and on the voltage between LN and SLPE. See Figs 6 and 7 to determine the current as a function of the required voltage and the temperature.

(2) Calculated for the maximum ambient temperature specified T_{amb} = 75 °C and a maximum junction temperature of 125 °C.

THERMAL RESISTANCE

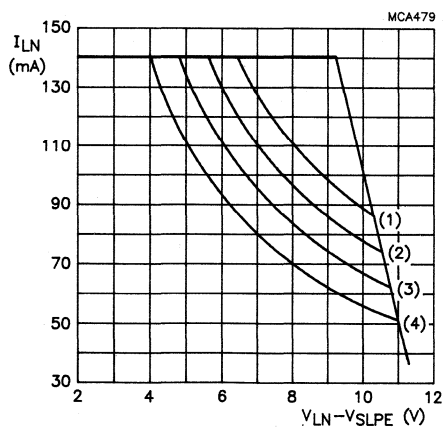
From junction to ambient in free air

TEA1068	$R_{th\ j\text{-}a}$	typ.	65	K/W
TEA1068T mounted on glass epoxy board 41 x 19 x 1.5 mm	$R_{th\ j\text{-}a}$	typ.	90	K/W



	T_{amb}	P_{tot}
(1)	45 °C	1231 mW
(2)	55 °C	1077 mW
(3)	65 °C	923 mW
(4)	75 °C	769 mW

Fig. 6 TEA1068 safe operating area.



	T_{amb}	P_{tot}
(1)	45 °C	888 mW
(2)	55 °C	777 mW
(3)	65 °C	666 mW
(4)	75 °C	555 mW

Fig. 7 TEA1068T safe operating area.

CHARACTERISTICS

I_{line} = 10 to 140 mA; V_{EE} = 0 V; f = 800 Hz, T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply, LN and V_{CC}						
Voltage drop over circuit, between LN and V_{EE}	microphone inputs open					
	I_{line} = 5 mA	V_{LN}	3.95	4.25	4.55	V
	I_{line} = 15 mA	V_{LN}	4.2	4.45	4.7	V
	I_{line} = 100 mA	V_{LN}	5.4	6.1	6.7	V
	I_{line} = 140 mA	V_{LN}	–	–	7.5	V
Variation with temperature	I_{line} = 15 mA	$\Delta V_{LN}/\Delta T$	–4	–2	0	mV/K
Voltage drop over circuit, between LN and V_{EE} with external resistor R_{VA}						
	I_{line} = 15 mA; R_{VA} (LN to REG) = 68 kΩ		3.45	3.8	4.1	V
	I_{line} = 15 mA; R_{VA} (REG to SLPE) = 39 kΩ		4.65	5.0	5.35	V
Supply current	PD = LOW; V_{CC} = 2.8 V	I_{CC}	–	0.96	1.3	mA
Supply current	PD = HIGH; V_{CC} = 2.8 V	I_{CC}	–	55	82	μA
Supply voltage available for peripheral circuitry	I_{line} = 15 mA; MUTE = HIGH					
	I_p = 1.2 mA	V_{CC}	2.8	3.05	–	V
	I_p = 0 mA	V_{CC}	3.5	3.75	–	V
Microphone inputs MIC+ and MIC–						
Input impedance (differential) between MIC– and MIC+		$\|Z_i\|$	51	64	77	kΩ
Input impedance (single-ended) MIC– or MIC+ to V_{EE}		$\|Z_i\|$	25.5	32	38.5	kΩ
Common mode rejection ratio		k_{CMR}	–	82	–	dB
Voltage gain MIC+/MIC– to LN	I_{line} = 15 mA; R7 = 68 kΩ	G_v	51	52	53	dB
Gain variation with frequency at f = 300 Hz and f = 3400 Hz	w.r.t. 800 Hz	ΔG_{vf}	–0.5	± 0.2	+0.5	dB

parameter	conditions	symbol	min.	typ.	max.	unit
Microphone inputs MIC+ and MIC– (continued)						
Gain variation with temperature at –25 °C and +75 °C	w.r.t. 25 °C; without R6; I_{line} = 50 mA	ΔG_{vT}	–	± 0.2	–	dB
Dual-tone multi-frequency input DTMF						
Input impedance		$\|Z_i\|$	16.8	20.7	24.6	kΩ
Voltage gain from DTMF ro LN	I_{line} = 15 mA; R7 = 68 kΩ	G_v	24.5	25.5	26.5	dB
Gain variation with frequency at f = 300 Hz and f = 3400 Hz	w.r.t 800 Hz	ΔG_{vf}	–0.5	± 0.2	+ 0.5	dB
Gain variation with temperature at – 25 °C and + 75 °C	w.r.t 25 °C I_{line} = 50 mA	ΔG_{vT}	–	± 0.5	–	dB
Gain adjustement GAS1 and GAS2						
Gain variation of the transmitting amplifier by varying R7 between GAS1 and GAS2		ΔG_v	–8	–	+8	dB
Sending amplifier output LN						
Output voltage	I_{line} = 15 mA THD = 2%	$V_{LN(rms)}$	1.9	2.3	–	V
	THD = 10%	$V_{LN(rms)}$	–	2.6	–	V
Noise output voltage	I_{line} = 15 mA; R7 = 68 kΩ; 200 Ω between MIC– and MIC+; psophometrically weighted (P53 curve)	$V_{no(rms)}$	–	–72	–	dBmp
Receiving amplifier input IR						
Input impedance		$\|Z_i\|$	17	21	25	kΩ

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Receiving amplifier outputs QR+ and QR−						
Output impedance (single-ended)		$\|Z_o\|$	–	4	–	Ω
Voltage gain from IR to QR+ or QR−	I_{line} = 15 mA					
single-ended	R_L (from QR+ or QR−) = 300 Ω	G_v	24	25	26	dB
differential	R_L (from QR+ or QR−) = 600 Ω	G_v	30	31	32	dB
Gain variation with frequency at f = 300 Hz and f = 3400 Hz	w.r.t. 800 Hz	ΔG_{vf}	−0.5	−0.2	0	dB
Gain variation with temperature at −25 °C and +75 °C	w.r.t. 25 °C; I_{line} = 50 mA; without R6	ΔG_{vT}	–	± 0.2	–	dB
Output voltage	sinewave drive; I_{line} = 15 mA; I_p = 0 mA; THD = 2%; R4 = 100 kΩ					
single-ended	RL = 150 Ω	$V_{o(rms)}$	0.3	0.38	–	V
	RL = 450 Ω	$V_{o(rms)}$	0.4	0.52	–	V
differential	f = 3400 Hz; series R = 100 Ω; C_L = 47 nF	$V_{o(rms)}$	0.8	1.0	–	V
Noise output voltage	I_{line} = 15 mA; R4 = 100 kΩ; IR open-circuit psophometrically weighted; (P53 curve)					
single-ended	RL = 300 Ω	$V_{no(rms)}$	–	50	–	μV
differential	RL = 600 Ω	$V_{no(rms)}$	–	100	–	μV
Gain adjustment GAR						
Gain variation of receiving amplifier achievable by varying R4 between GAR and QR		ΔG_v	−8	–	+8	dB

parameter	conditions	symbol	min.	typ.	max.	unit
Mute input						
Input voltage HIGH		V_{IH}	1.5	–	V_{CC}	V
Input voltage LOW		V_{IL}	–	–	0.3	V
Input current		I_{MUTE}	–	8	15	μA
Gain reduction MIC+ or MIC– to LN	MUTE = HIGH	G_v	–	70	–	dB
Voltage gain from DTMF to QR+ or QR–	MUTE = HIGH; R4 = 100 kΩ; single-ended; R_L = 300 Ω	G_v	–21	–19	–17	dB
Power-down input PD						
Input voltage HIGH		V_{IH}	1.5	–	V_{CC}	V
Input voltage LOW		V_{IL}	–	–	0.3	V
Input current		I_{PD}	–	5	10	μA
Automatic gain control input AGC						
Controlling the gain from IR to QR+/QR– and the gain from MIC+/MIC– to LN; R6 between AGC and V_{EE}	R6 = 110 kΩ					
Gain control range	I_{line} = 70 mA	ΔG_v	–5.5	–5.9	–6.3	dB
Highest line current for maximum gain		I_{line}	–	23	–	mA
Minimum line current for minimum gain		I_{line}	–	61	–	mA
Reduction of gain between I_{line} = 15 mA and I_{line} = 35 mA		ΔG_v	–1.0	–1.5	–2.0	dB

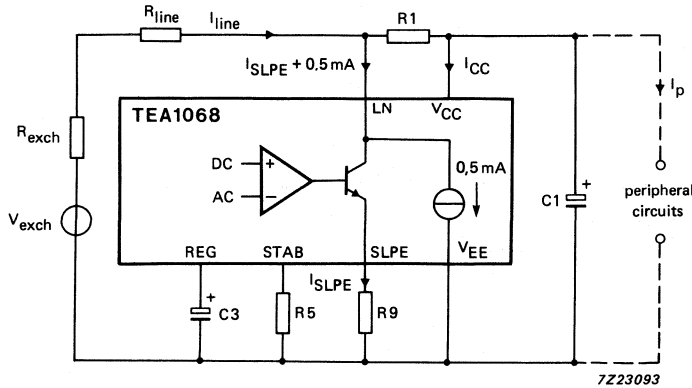


Fig. 8 Supply arrangement.

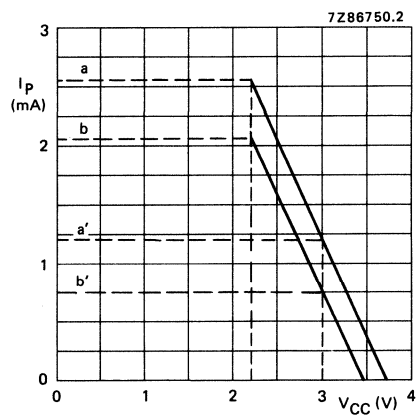


Fig. 9 Typical current I_p available from V_{CC} for peripheral circuitry with $V_{CC} >= 2.2$ V. Curve (a) is valid when the receiving amplifier is not driven or when MUTE = HIGH, curve (b) is valid when MUTE = LOW and the receiving amplifier is driven; $V_{o(rms)}$ = 150 mV, R_L = 150 Ω asymmetrical. The supply possibilities can be increased simply by setting the voltage drop over the circuit V_{LN} to a higher value by means of resistor R_{VA} connected between REG and SLPE.

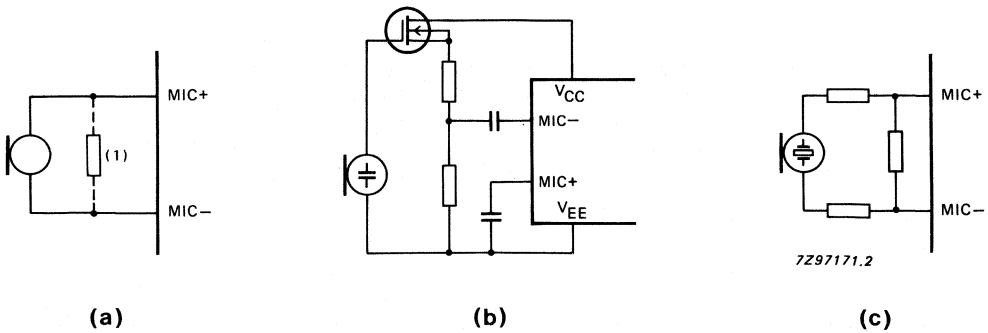


Fig. 10 Alternative microphone arrangements.

(a) Magnetic or dynamic microphone. The resistor marked (1) may be connected to decrease the terminating impedance.
(b) Electret microphone.
(c) Piezoelectric microphone.

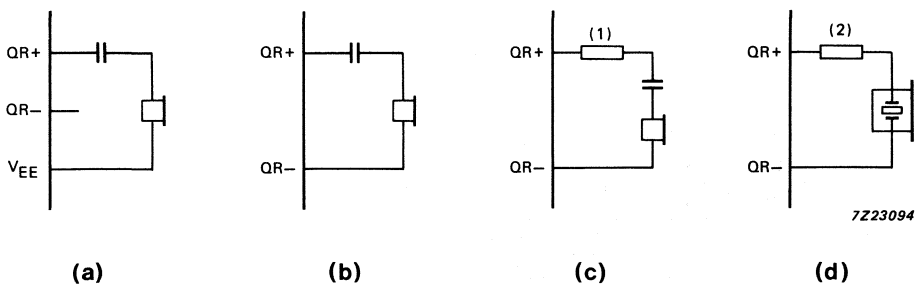


Fig. 11 Alternative receiver arrangements.

(a) Dynamic earpiece with less than 450 Ω impedance.
(b) Dynamic earpiece with more than 450 Ω impedance.
(c) Magnetic earpiece with more than 450 Ω impedance. The resistor marked (1) may be connected to prevent distortion (inductive load).
(d) Piezoelectric telephone. The resistor marked (2) is required to increase the phase margin (capacitive load).

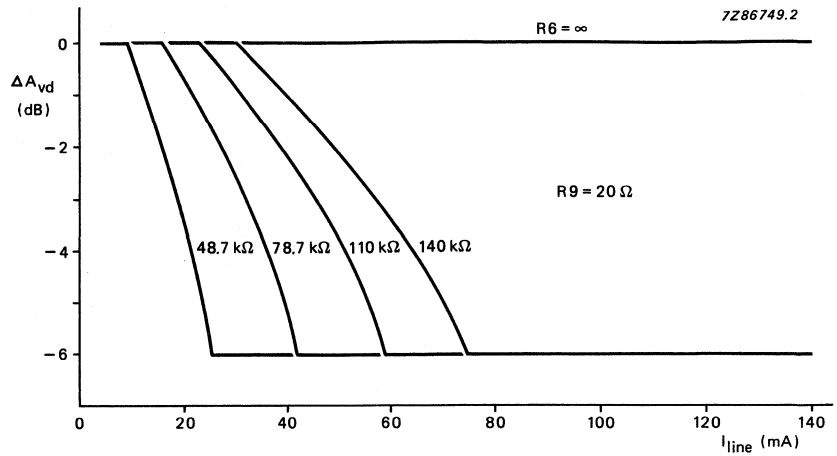


Fig. 12 Variation of gain with line current, with R6 as a parameter.

Table 1 Values of resistor R6 for optimum line loss compensation, for various usual values of exchange supply voltage (V_{exch}) and exchange feeding bridge resistance (R_{exch}); R9 = 20 Ω.

		R_{exch} (Ω)			
		400	600	800	1000
		R6 (KΩ)			
V_{exch} (V)	24	61.9	48.7	X	X
	36	100	78.7	68	60.4
	48	140	110	93.1	82
	60	X	X	120	102

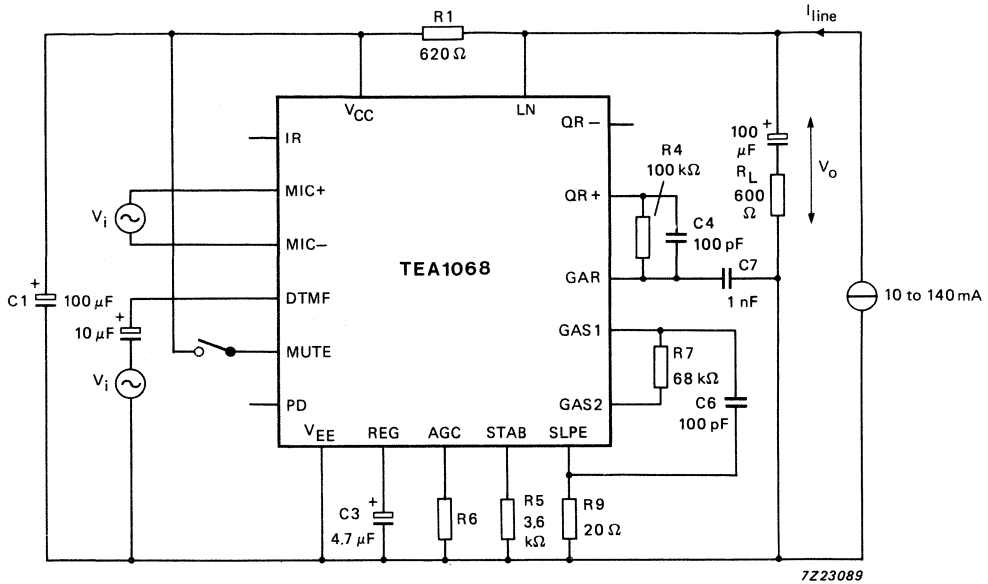


Fig. 13 Test circuit for defining voltage gain of MIC+, MIC– and DTMF inputs. Voltage gain is defined as; $G_V = 20 \log |V_o/V_i|$. For measuring the gain from MIC+ and MIC– the MUTE input should be LOW or open, for measuring the DTMF input MUTE should be HIGH. Inputs not under test should be open.

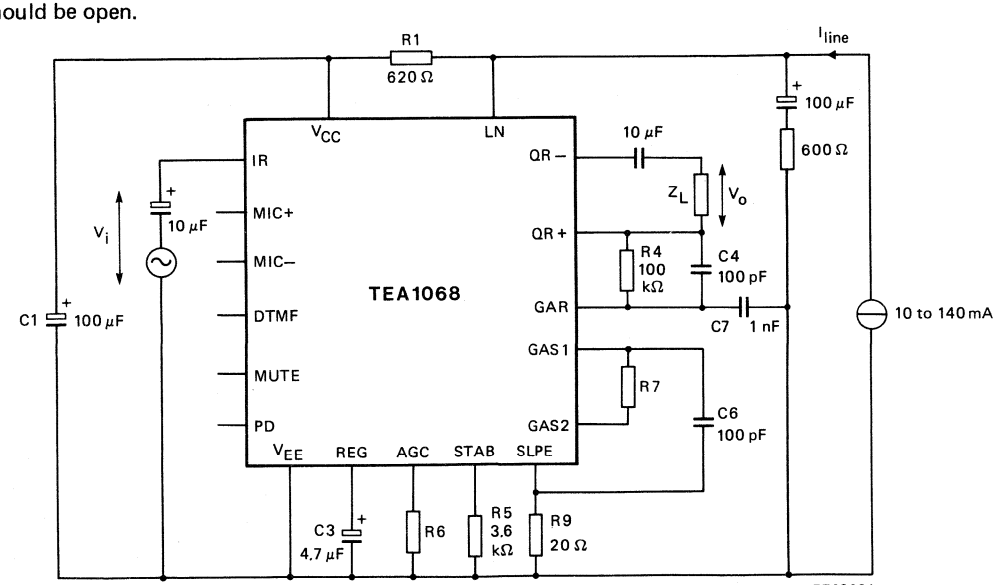


Fig. 14 Test circuit for defining voltage gain of the receiving amplifier. Voltage gain is defined as; $G_V = 20 \log |V_o/V_i|$.

APPLICATION INFORMATION

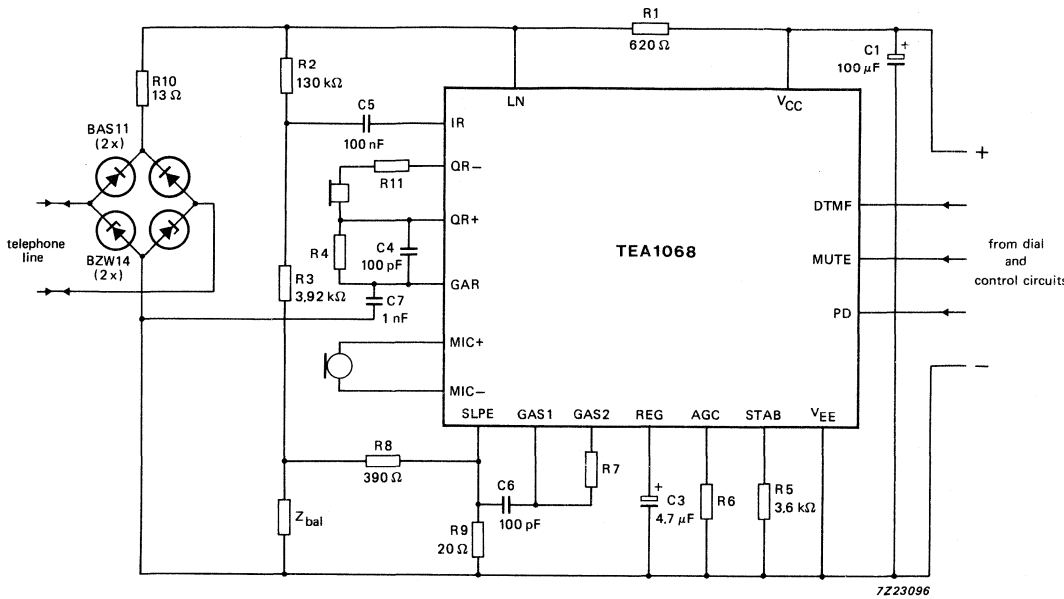


Fig. 15 Typical application of the TEA1068, shown here with a piezoelectric earpiece and DTMF dialling. The bridge to the left and R10 limit the current into the circuit and the voltage across the circuit during line transients. Pulse dialling or register recall require a different protection arrangement.

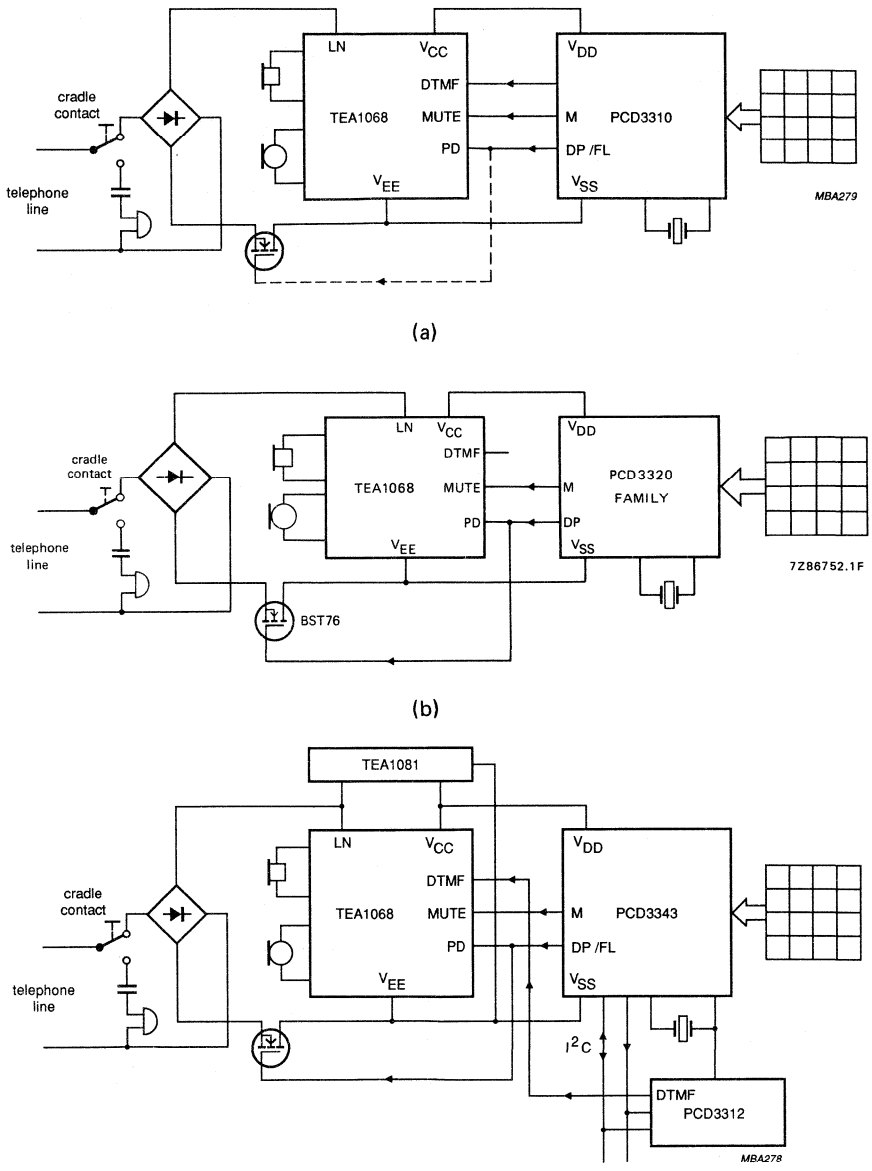


Fig. 16 Typical applications of the TEA1068 (simplified).

(a) DTMF set with a CMOS DTMF dialling circuit. The dashed lines show an optional flash (register recall by times loop break).

(b) Pulse dial set with one of the PCD3320 family of CMOS interrupted current-loop dialling circuits.

(c) Dual-standard (pulse and DTMF) feature phone with the PCD3343 CMOS telephone controller and the PCD3312 CMOS DTMF generator with I^2C-bus. The supply is provided by TEA1081 supply circuit.

SUPPLY CIRCUIT WITH POWER-DOWN FOR TELEPHONE SET PERIPHERALS

GENERAL DESCRIPTION

The TEA1081 is a bipolar integrated circuit for use in line-powered telephone sets to supply peripheral circuits for extended dialling and/or loudspeaking facilities.

The IC uses a part of the surplus line current normally drawn by the voltage regulator of the speech/transmission circuit. A power-down function isolates the IC from its load and reduces the input current.

Features

- High input impedance for audio signals
- Low DC series resistance
- High output current
- Large audio signal handling capability
- Low distortion
- Two modes of operation:
  - output voltage that follows the DC line voltage
  - regulated output voltage
- Power-down input
- Low number of external components

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Operating DC line voltage		V_{LN}	2,5	–	12	V
DC output voltage		V_O	2,0	–	10	V
Voltage drop from line to output		V_{LN}-V_O	–	0,5	–	V
Series resistance		R_S	–	20	–	Ω
Output current	V_{LN} = 4 V					
TEA1081		I_O	–	–	30	mA
TEA1081T		I_O	–	–	20	mA
AC line voltage (RMS value)	V_{LN} = 4 V; I_O = 15 mA; d = 2%	$v_{LN(rms)}$	–	1,5	–	V
Internal supply current	V_{LN} = 4 V	I_{INT}	–	0,8	–	mA
Operating ambient temperature range		T_{amb}	–25	–	+ 70	°C

PACKAGE OUTLINES

TEA1081: 8-lead dual in-line; plastic (SOT97).
TEA1081T: 8-lead mini-pack; plastic (SO8; SOT96A).

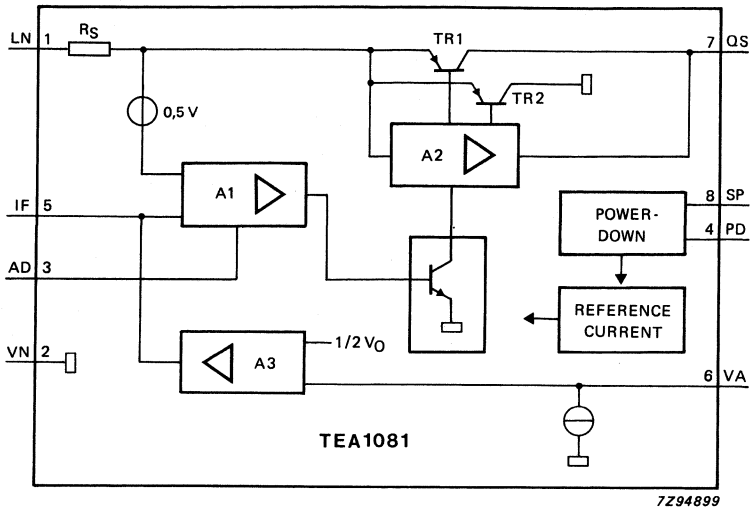


Fig. 1 Block diagram.

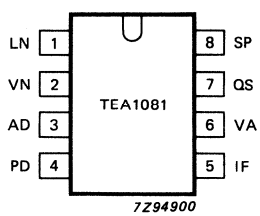


Fig. 2 Pinning diagram.

PINNING

1	LN	positive line terminal
2	VN	negative line terminal
3	AD	amplifier decoupling
4	PD	power-down input
5	IF	low pass filter input
6	VA	output voltage adjustment
7	QS	power supply output
8	SP	supply input: power-down circuit

FUNCTIONAL DESCRIPTION

The TEA1081 is a supply interface between telephone line and peripheral devices in the telephone set. The high input impedance of the circuit allows direct connection to the telephone line (via a diode bridge). An inductor function is obtained by amplifier A1, resistor R_S (Fig. 1) and an external low-pass RC filter.

Under the control of amplifier A2, transistor TR1 supplies peripheral devices and transistor TR2 minimizes line signal distortion by momentarily diverting input current to ground whenever the instantaneous value of the line voltage drops below the output voltage.

Internal circuits are biased by a temperature and line voltage compensated reference current source.

The power-down circuit isolates the supply circuit from external circuitry.

Line terminals: LN, VN (pins 1, 2)

The input terminals LN and VN can be connected directly to the line. The minimum DC line voltage required at the input is given by

$$V_{LN} = I_1 \times R_S + V_{LN\,min} + v_{LN(P)} \quad (V)$$

in which

I_1 = input current
R_S = internal series resistance
$v_{LN\,min}$ = minimum instantaneous line voltage (1,4 V at I_O = 5 mA)
$v_{LN(P)}$ = required peak level of AC line voltage

The internal current (I_{INT}) at I_O = 0 mA is typically 0,8 mA at V_{LN} = 4 V and reaches a maximum of 1,4 mA at V_{LN} = 12 V.

Supply terminals: QS, VA (pins 7, 6)

Peripheral devices are supplied from QS (pin 7). Two modes of output voltage regulation are available:

Output voltage follows line voltage (Fig. 3)

The TEA1081 operates in this mode when there is no external resistor (R_V) between QS and VA (pins 6 and 7).

The output voltage follows the line voltage and is expressed by

$$V_O = V_{LN} - (I_1 \times R_S + 0{,}5) \quad (V)$$

in which

V_{LN} = line voltage
I_1 = input current
R_S = internal series resistance

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

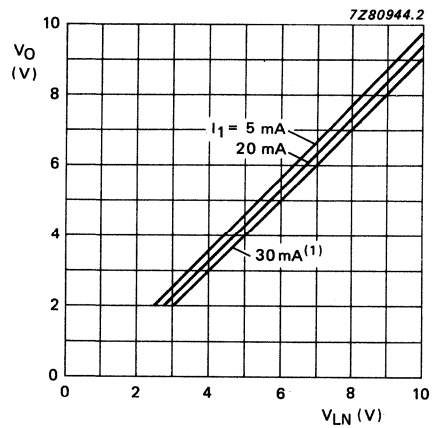
Regulated output voltage (Fig. 4)

The circuit operates in this mode when an external resistor (R_V) is connected between QS and VA (pins 6 and 7, see Fig. 6).

The output voltage is held constant at $V_O = 2 \times I_6 \times R_V$ (V)

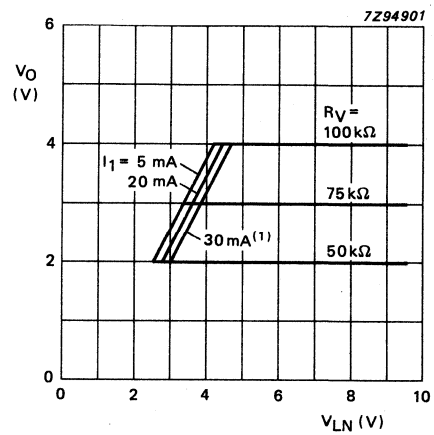
as soon as the line voltage $V_{LN} > (2 \cdot I_6 \cdot R_v + I_1 \cdot R_S + 0{,}5)$ (V)

The control current I_6 is typically 20 μA.



(1) I_1 = 30 mA; not valid for TEA1081T

Fig. 3 Output voltage as a function of line voltage (application without R_V).



(1) I_1 = 30 mA; not valid for TEA1081T

Fig. 4 Output voltage as a function of line voltage (R_V connected between QS and VA).

Input and output currents I_1, I_O (pins 1 and 7)

The maximum available current into pin 1 (I_1) is determined by:

- the minimum line current ($I_{LINE\ min}$) that is available for the telephone set;
- the specified minimum input current ($I_{LN\ min}$) for the speech/transmission circuit.

That is $I_{1\ max} = I_{LINE\ min} - I_{LN\ min}$.

At $v_{LN(rms)} < 150$ mV, the input current I_1 is approximately:

$$I_1 = I_{INT} + k \cdot I_O \quad \text{(mA)}$$

in which

I_{INT} = internal supply current (0,8 mA at V_{LN} = 4 V);
k = correction factor (k < 1,1 for the specified output current range).

With large line signals the instantaneous line voltage may drop below $V_O + 0{,}4$ V. Normally (when $v_{LN} > V_O + 0{,}4$ V), instantaneous current flows from LN to QS (pin 1 to pin 7) to the output load. When $v_{LN} < V_O + 0{,}4$ V, the instantaneous current is diverted to pin 2 to prevent distortion of the line signal.

Input current at $v_{LN(rms)} = 1$ V and without R_V approximates to

$$I_1 = I_{INT} + 2\,I_O \quad \text{(mA)}$$

The maximum supply current (within the specified output current limits) available for peripheral devices is shown by

$$I_{O\,max} = \frac{I_{LINE\,min} - I_{LN\,min} - I_{INT}}{2}$$

in which

$I_{LINE\,min}$ is the minimum line current of the telephone set;

$I_{LN\,min}$ is the specified minimum input current of the speech/transmission circuit.

Input low-pass filter: IF (pin 5)

The input impedance between LN and VN at audio frequencies is determined mainly by the filter elements C_L (between pins 1 and 5), R_L (between pins 5 and 7) and the internal resistor R_S (typical value 20 Ω). At audio frequencies the TEA1081 behaves as an inductor of the value $L_I = C_L \cdot R_L \cdot R_S$ (H). The typical value of L_I at $C_L = 2{,}2\ \mu$F and $R_L = 100$ kΩ is 4,4 H.

Amplifier decoupling: AD (pin 3)

To ensure stability, a 68 pF decoupling capacitor is required between AD (pin 3) and LN (pin 1). If $I_{Omin} < 1{,}5$ mA, a 47 pF capacitor has to be added between AD (pin 3) and VA (pin 6).

Power-down inputs: PD, SP (pins 4 and 8)

During pulse dialling or register recall, or if the input current to pin 1 is insufficient to maintain the output current, the supply to peripheral devices can be switched off by activating the PD input at pin 4. With PD = HIGH, the input current is reduced to (typ.) 40 μA at $V_{LN} = 4$ V and the internal circuits are isolated from the load at QS (pin 7).

The power-down circuit is supplied via the SP input (pin 8). SP can be wired to QS in conditions where $V_O > V_{SP\,min}$ during line interruptions. When $V_O < V_{SP\,min}$, SP should be wired to an external supply point (e.g. to V_{CC} of the TEA1060 family circuit).

When power-down is not required, the PD and SP inputs can be left open-circuit.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Positive line voltage	continuous	V_{LN}	–	12	V
	during switch-on or line interruptions	V_{LN}	–	12,5	V
Repetitive line voltage peaks	1 ms/5 s; 12 Ω resistor in series with pin 1	V_{LN}	–	28	V
Voltage on all other terminals		V	V_{VN}–0,5	V_{LN}+0,5	V
Input current (DC)	TEA1081	I_1	–	120	mA
Input current (DC)	TEA1081T	I_1	–	80	mA
Current into all other terminals		I_I	–1	+1	mA
Total power dissipation		P_{tot}	see Fig. 5		
Storage temperature range		T_{stg}	–40	+125	°C
Operating ambient temperature range		T_{amb}	–25	+70	°C
Junction temperature		T_j	–	+125	°C

THERMAL RESISTANCE

From junction to ambient in free air

TEA1081 $R_{th\ j\text{-}a}$ = 120 K/W

TEA1081T (circuit mounted on printed circuit board of 50 x 50 x 1,5 mm) $R_{th\ j\text{-}a}$ = 260 K/W

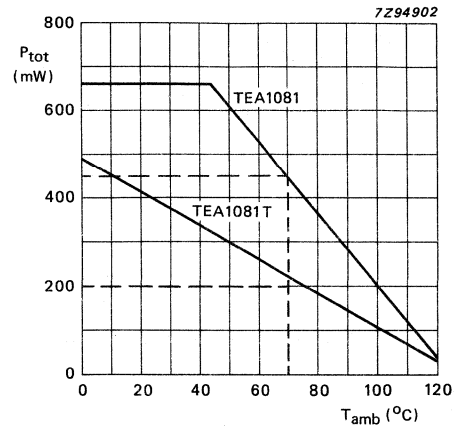


Fig. 5 Power derating curves.

CHARACTERISTICS

V_{LN} = 4 V; $v_{LN(rms)}$ = 100 mV; I_O = 5 mA; f = 300 to 3400 Hz; R_L = 100 kΩ; C_L = 2,2 μF; R_V = 75 kΩ; T_{amb} = 25 °C; unless otherwise specified; see Fig. 6.

parameter	conditions	symbol	min.	typ.	max.	unit
Operating DC line voltage		V_{LN}	2,5	–	12	V
Min. instantaneous line voltage		V_{LN}	–	–	1,4	V
Max. instantaneous line voltage		V_{LN}	12	–	–	V
Characteristics with R_V = 75 kΩ connected between pins 6 and 7 and C_L = 10 μF						
Input current (pin 1)						
	v_{LN} = 0 V	I_1	–	5,8	–	mA
	$v_{LN(rms)}$ = 1,5 V; I_O = 15 mA	I_1	–	30	–	mA
Output voltage (pin 7)		V_O	–	3	–	V
Variation of output voltage over the ranges of:						
line voltage	V_{LN} = 4 to 6 V	ΔV_O	–	100	–	mV
temperature	T_{amb} = +25 to −25 °C	ΔV_O	–	−100	–	mV
	T_{amb} = +25 to +75 °C	ΔV_O	–	−100	–	mV
output current	I_O = 5 to 20 mA	ΔV_O	–	−100	–	mV
Control current (pin 6)		I_6	–	20	–	μA

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Characteristics without R_V						
Input current (pin 1)	v_{LN} = 0 V	I_1	–	6,0	–	mA
	$v_{LN(rms)}$ = 1,5 V; I_O = 15 mA	I_1	–	31	–	mA
Voltage drop (pin 1 to pin 7)	I_O = 0 mA	V_{LN}-V_O	–	0,5	–	V
	I_O = 15 mA; $v_{LN(rms)}$ = 1,5 V	V_{LN}-V_O	–	1,1	–	V
Output current (pin 7)						
	TEA1081	I_O	–	–	30	mA
	TEA1081T	I_O	–	–	20	mA
Internal series resistance		R_S	–	20	–	Ω
Internal supply current	I_O = 0 mA; PD = LOW; V_{SP} = V_O	I_{INT}	–	0,8	1,4	mA
	PD = HIGH (note 1); V_{SP} > 2 V	I_{INT}	–	40	60	μA
Total distortion	$v_{LN(rms)}$= 1,5 V	d_{tot}	–	–	2	%
Balance return loss	600 Ω reference	BRL	25	–	–	dB
Harmonic levels of line voltage	f = 500 Hz; v_{LN} = 0 dBm; Z_{line} = 600 Ω					
	second harmonic	v_{LN-2H}	–	–58	–	dBm
	third harmonic	v_{LN-3H}	–	–60	–	dBm
Noise voltage on input terminal	v_{LN} = 0 mV; R_L = 600 Ω; P53 curve	$v_{ni(rms)}$	–	–83	–	dBmp
Power-down input (pin 4)						
Input voltage HIGH		V_{IH}	1,5	–	V_{SP}	V
Input voltage LOW		V_{IL}	–	–	0,3	V
Input current		I_4	–	–	10	μA
Power-down input (pin 8)						
Supply voltage for power-down		V_8	2	–	V_{LN}	V
Supply current to power-down circuit	V_8 = 3 V	I_8	–	–	70	μA

Note 1: Power-down circuit supplied via external source.

APPLICATION INFORMATION

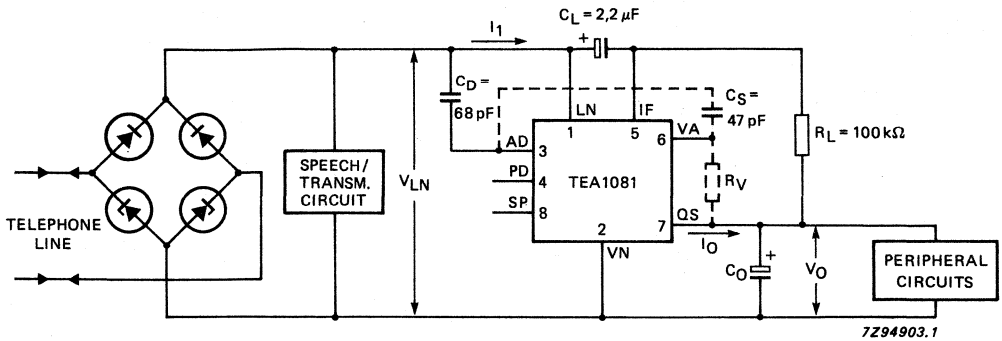


Fig. 6 Application diagram.

DEVELOPMENT DATA

Call progress monitor for line powered telephone sets

TEA1083/TEA1083A

FEATURES

- Internal supply
  - Optimum current split-up
  . Low constant current (adjustable) in transmission IC
  . Nearly all line current available for monitoring
  - Stabilized supply voltage
- Loudspeaker amplifier with a fixed gain of 35 dB
- Volume controled by potentiometer
- Power-down input (TEA1083A only)
- Loudspeaker enable input.

GENERAL DESCRIPTION

The TEA1083/83A is a bipolar IC which has been designed for use in line powered telephone sets. It is intended to offer a monitoring facility of the line signal via a loudspeaker during on-hook dialling. The TEA1083/83A is intended for use in conjunction with a transmission circuit of the TEA1060 family.
The device uses a part of the available line current via the internal supply circuit.
The loudspeaker amplifier, which consists of a preamplifier and a power amplifier, amplifies the received line signals from the transmission circuit when enabled via the LSE input. The loudspeaker amplifier can also be used to amplify dialling tones from the dialler IC.
The power amplifier contains a push-pull output stage to drive the loudspeaker in a Single Ended Load (SEL) configuration.
The internal voltage stabilizer can be used to supply external devices.
By activating the power-down (PD) input of the TEA1083A, the current consumption of the circuit will be reduced, this enables pulse dialling or flash (register recall).
An internal start circuit ensures normal start-up of the transmission IC.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{SUP}	input current range		3.0	–	120	mA
V_{BB}	stabilized supply current		–	2.95	–	V
I_{SUP}	current consumption	PD = HIGH; TEA1083A only	–	50	–	µA
G_v	voltage gain of loudspeaker amplifier		–	35	–	dB
I_{SUP}	minimum input current	P_O = 10 mW (typ) into 50 Ω	–	10	–	mA
T_{amb}	operating ambient temperature range		–25	–	+75	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA1083	8	DIL	plastic	SOT97D
TEA1083A	16	DIL	plastic	SOT38
TEA1083AT	16	SOL	plastic	SOT162AG

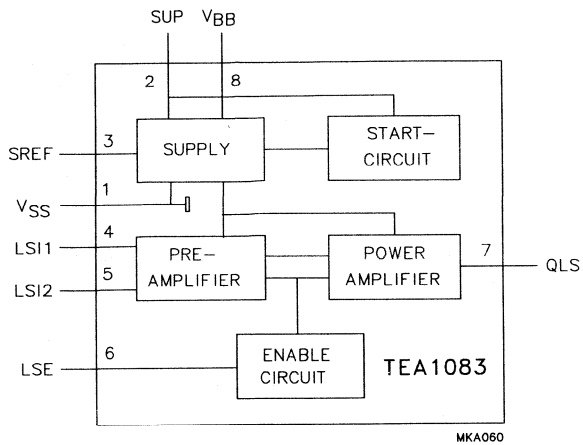


Fig.1 Block diagram (TEA1083).

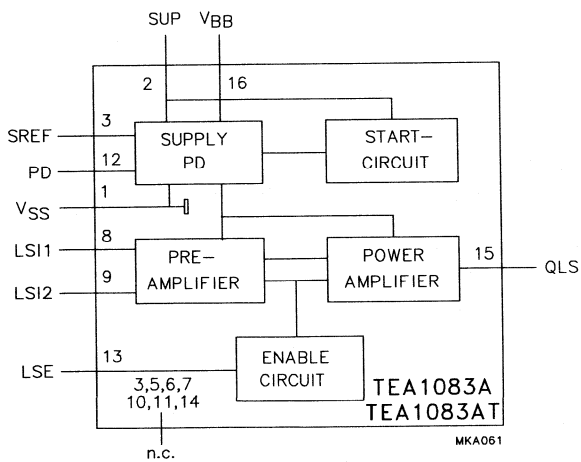


Fig.2 Block diagram (TEA1083A/AT).

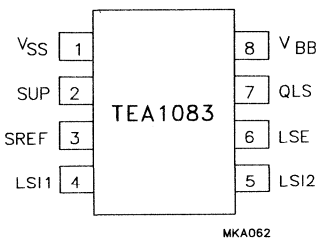


Fig.3 Pin configuration (TEA1083).

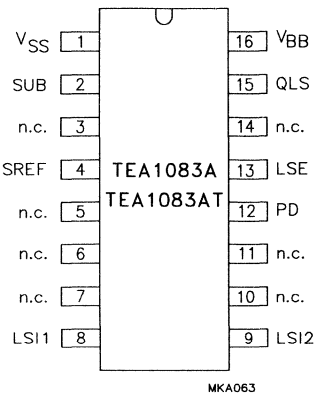


Fig.4 Pin configuration (TEA1083A/AT).

PINNING

SYMBOL	PIN DIL16	PIN DIL8	DESCRIPTION
V_{SS}	1	1	negative supply terminal
SUP	2	2	positive supply terminal
n.c.	3	–	not connected
SREF	4	3	supply reference input
n.c.	5	–	not connected
n.c.	6	–	not connected
n.c.	7	–	not connected
LSI1	8	4	loudspeaker amplifier input 1
LSI2	9	5	loudspeaker amplifier input 2
n.c.	10	–	not connected
n.c.	11	–	not connected
PD	12	–	power-down input
LSE	13	6	loudspeaker enable input
n.c.	14	–	not connected
QLS	15	7	loudspeaker amplifier output
V_{BB}	16	8	stabilized supply voltage

Table 1 Comparison of the TEA108X family

PRODUCT	NOTES	TEA1082	TEA1083	TEA1083A	TEA1085/85A
Application area	note 1	call progress monitoring			listening-in
PD facility		X	–	X	X
MUTE or LSE facility	note 2	–	X	X	X
dynamic limiter		–	–	–	X
howling limiter		–	–	–	X
V_{BB} setting		–	–	–	X
SEL	note 3	X	X	X	X
BTL	note 3	–	–	–	X
number of pins	note 4	8	8	16	24

Notes to Table 1

1. A call progress monitor is recommended by the European Telecommunications Standards Institute (ETSI) for telephone sets with automatic on-hook dialling facilities so that audible, or visual, progress of a call attempt can be monitored. In accordance with the ETSI (at a frequency of 440 Hz and a line level of 20 dBm (600 Ω)), a minimum level of 50 dBA shall be guaranteed at a distance of 50 cm from the set. This corresponds to a minimum level of approximately 100 mV (RMS) ($P_O \geq 0.2$ mW) across a loudspeaker; Philips type AD2071/Z50.

   A listening-in set has to offer the user more facilities e.g. howling limiting to reduce annoying loudspeaker and line signals. Dynamic limiting of the loudspeaker signal, with respect to supply conditions, can also be required. Acoustic output levels for listening-in sets are approximately 70 to 75 dBA. This corresponds to a loudspeaker level of approximately 1 mV (RMS) ($P_O \approx 20$ mW).
2. The MUTE function of the TEA1085A has a logic input; the MUTE function of the TEA1085 has a toggle input.
3. SEL: loudspeaker connected in a single-ended-load configuration

   BTL: loudspeaker connected in a bridge-tied-load configuration
4. Consult the product specification for the package outline/s.

FUNCTIONAL DESCRIPTION

The TEA1083/83A is normally used in conjunction with a transmission circuit of the TEA1060 family. The circuit must be connected between the positive line terminal (pin 2) and pin SLPE of the transmission IC. The transmission characteristics (impedance, gain settings etc) are not affected.
An interconnection between the TEA1083/83A and a member of the TEA1060 family is illustrated in Fig.5.

Supplies SUP, SREF, V_{BB} and V_{SS}

In Fig.6 the line current is divided into I_{TR} for the transmission IC and I_{SUP} for the monitoring circuit TEA1083/83A.

I_{TR} is constant:

$$I_{TR} = V_{int}/R20$$

$$I_{SUP} = I_{line} - I_{CC} - I_{TR}$$

Where:

- V_{int} is an internal temperature compensated reference voltage of 500 mV(typ) between pins SUP and SREF
- R20 is a resistor connected between SUP and SREF
- I_{CC} is the internal current consumption of the TEA106X (approximately 1 mA).

A practical value for resistor R20 is 150 Ω; this produces a current of approximately 3.3 mA(typ) for I_{TR} and I_{SUP} is approximately equal to $I_{line} - 4.3$ mA.

The circuit stabilizes its own supply voltage at V_{BB}. Transistor TR1 provides the supplies for the internal circuits. Transistor TR2 is used to minimize signal distortion on the line by momentarily diverting the input current to V_{SS} whenever the instantaneous value of the voltage at V_{SUP} drops below the supply voltage V_{BB}. V_{BB} is fixed to a typical value of 2.95 V.
The supply at V_{BB} is decoupled with respect to V_{SS} by a 220 µF capacitor (C20).

The DC voltage ($V_{SUP} - V_{SS}$) is determined by the transmission IC and V_{int}; thus $V_{SUP} - V_{SS} = V_{LN-SLPE} + V_{int}$. The reference voltage of the transmission IC has to be adjusted to a level where $V_{SUP} - V_{BB(max)}$ is greater than 400 mV. The minimum voltage space between SUP and V_{BB} (400 mV) is required to maintain a 'high' efficiency of the internal supply for mean speech levels. $V_{BB(max)}$ is the specified maximum level.

The internal current consumption of the TEA1083/83A (I_{SUP0}) is typically 2.5 mA (where $V_{SUP} - V_{SS} = 3.6$ V). The current I_{SUP0} consists of currents I_{BIAS} (approximately 0.4 mA) for the circuitry connected to SUP and I_{BB0} (approximately 2.1 mA) for the internal circuitry connected to V_{BB} (see Fig.6).

LOUDSPEAKER AMPLIFIER (LSI1/LSI2 and QLS)

The TEA1083/83A has symmetrical inputs at LSI1 and LSI2. The input signal is normally taken from the earpiece output of the transmission circuit (see Fig.5) and/or from the signal output of the DTMF generator via a resistive attenuator.
The attenuation factor must be chosen in accordance with the output levels from the transmission IC and/or DTMF generator and, in accordance with the required output power and permitted signal distortion from the loudspeaker signal.

The output QLS drives the loudspeaker as a single-ended load. The output stage has been optimised for use with a 50 Ω loudspeaker (e.g. Philips type AD2071). The loudspeaker amplifier is enabled when the LSE input goes HIGH. The gain of the amplifier is fixed at 35 dB.

Volume control of the loudspeaker signal can be obtained by using a level control at the input (see Fig.5).

The maximum voltage swing at the QLS output is $V_{O(p-p)} = 2.5$ V (typical with 50 Ω load). The input level V_{LSI} is approximately 16 mV(rms) and the supply current $I_{SUP} > 11$ mA. In this condition the signal is limited by the available voltage space (V_{BB}). Higher input levels and/or lower supply currents will result in an increase of the harmonic distortion due to signal clipping.

With a limit of 2.5 V(p-p), the maximum output swing is dependent on the supply current and loudspeaker impedance. It can be approximated, for low distortions, by the following equation:

$$V_{O(p-p)} = 2 \times (I_{SUP} - I_{SUPO}) \times \pi \times R_{LS}$$

Where;

- $V_{O(p-p)}$ = the peak-to-peak level of the loudspeaker
- R_{LS} = the loudspeaker impedance
- I_{SUPO} = 2.5 mA (typ.)

POWER-DOWN INPUT (PD)

During pulse dialling or register recall (timed loop break) the telephone line is interrupted, thereby breaking the supply current to the transmission IC. The capacitor connected to V_{BB} provides the supply for the TEA1083/83A during the supply breaks.

By making the PD input HIGH during the loop break, the requirement on the capacitor is eased and, consequently, the internal current consumption I_{BB0} (see Fig.5) is reduced from 2.1 mA to 400 µA typically. Transistors TR1 and TR2 are inhibited during power-down and the bias current is reduced from approximately 400 µA to approximately 50 µA with V_{SUP} =3.6 V in the following equation:

$$I_{SUP(PD)} = I_{BIAS(PD)} = (V_{SUP} - 2V_d)/Ra$$

Where $3.6 < V_{SUP} < V_{BB} + 3$ V

$2V_d$ is the voltage drop across 2 internal diodes (approximately 1.3 V)

Ra is an internal resistor (typical 50 kΩ)

LOUDSPEAKER ENABLE INPUT (LSE)

The LSE input has a pull-down structure. It switches the loudspeaker amplifier, in the monitoring condition, by applying a HIGH level at the input. The amplifier is in the standby condition when LSE is LOW (input open-circuit or connected to V_{SS}.

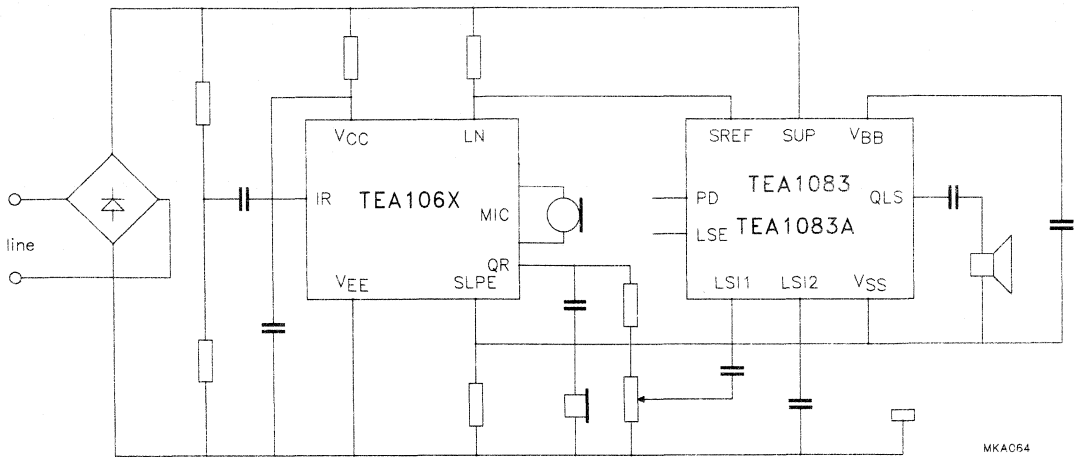


Fig.5 Interconnection with a transmission IC of the TEA106X family.

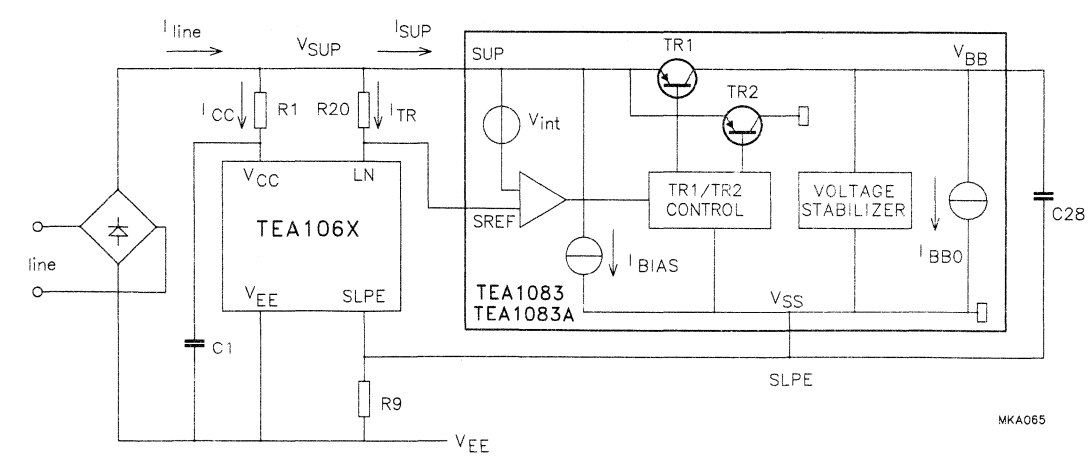


Fig.6 Supply arrangement.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{SUP}	Supply voltage				
	continuous		–	12	V
	during switch-on or line interruption		–	13.2	V
V_{SUP}	Repetitive supply voltage from 1 ms to 5 s with 12 Ω current limiting resistor in series with supply		–	28	V
V_{SREF}	Supply reference voltage		V_{SS}–0.5	V_{SUP}+0.5	V
V	Voltage on all other pins		V_{SS}–0.5	V_{BB}+0.5	V
I_{SUP}	Supply current	see Fig.6	–	120	mA
P_{tot}	Total power dissipation	T_{amb} = 75 °C; T_j = 125 °C			
	TEA1083		–	500	mW
	TEA1083A		–	769	mW
	TEA1083AT		–	555	mW
T_{stg}	Storage temperature range		–40	+125	°C
T_{amb}	Operating ambient temperature range		–25	+75	°C
T_j	Junction temperature		–	+125	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air (TEA1083)	100 K/W
	from junction to ambient in free air (TEA1083A)	65 K/W
	from junction to ambient in free air (TEA1083AT)	90 K/W

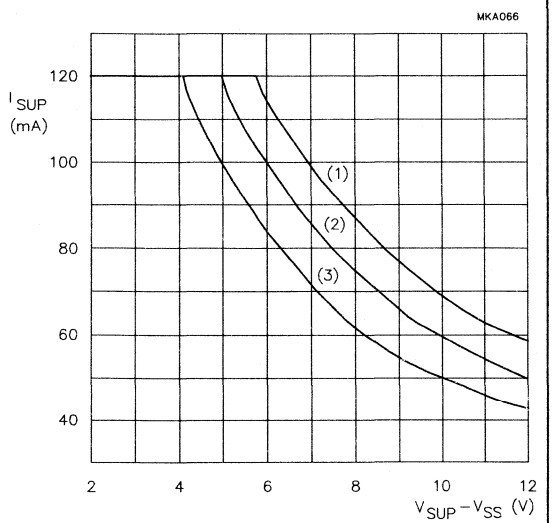


Fig.7 Safe operating area; see Table 2 (TEA1083).

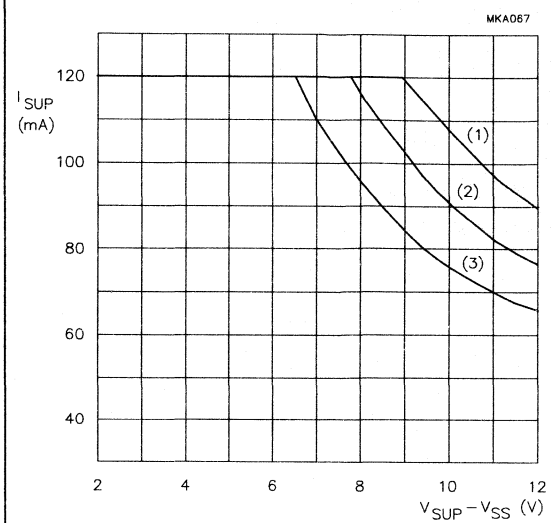


Fig.8 Safe operating area; see Table 3 (TEA1083A).

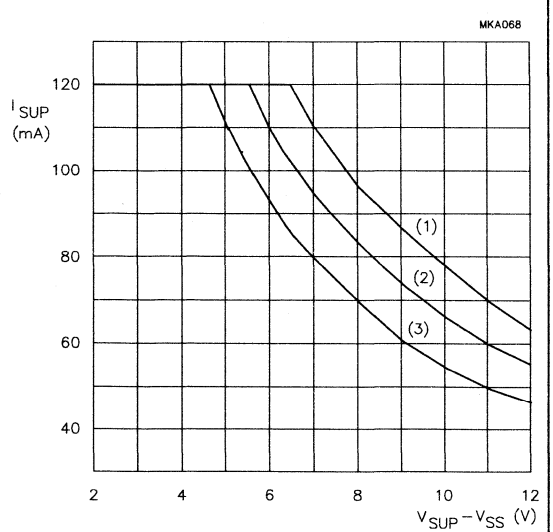


Fig.9 Safe operating area; see Table 4 (TEA1083AT).

Table 2

CURVE	T_{amb}	P_{tot}
1	55 °C	700 mW
2	65 °C	600 mW
3	75 °C	500 mW

Table 3

CURVE	T_{amb}	P_{tot}
1	55 °C	1077 mW
2	65 °C	923 mW
3	75 °C	769 mW

Table 4

CURVE	T_{amb}	P_{tot}
1	55 °C	777 mW
2	65 °C	666 mW
3	75 °C	555 mW

CHARACTERISTICS

V_{SUP} = 3.6 V; V_{SS} = 0 V; I_{SUP} = 15 mA; V_{SUP} = 0 V (RMS); f = 800 Hz; T_{amb} = 25 °C; PD = LOW; LSE = HIGH; loudspeaker amplifier load = 50 Ω; all measurements taken in test circuit Fig.10; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{SUP}	Minimum DC input voltage		–	V_{BB}+0.6	–	V
$V_{SUP-SREF}$	Internal reference voltage		400	500	600	mV
V_{BB}	Stabilized supply voltage	I_{SUP} = 15 mA	2.75	2.95	3.15	V
ΔV_{BB}	Variation of supply voltage	from I_{SUP} = 15 to 120 mA	–	15	–	mV
$\Delta V_{BB}/\Delta T$	Variation of supply voltage with temperature, referred to 25 °C	T_{amb} = –25 to +75 °C; I_{sup} = 15 mA	–	±0.2	–	mV/K
I_{SUP}	Minimum operating current		–	2.5	4.0	mA
THD	Distortion of AC signal between SUP and V_{EE}	$V_{SUP(RMS)}$ = 1 V	–	0.3	–	%
$V_{no(RMS)}$	Noise between SUP and V_{EE} (RMS value)	psophometrically weighted (P53 curve)	–	–71	–	dBmp
	Current consumption in power-down condition	PD = HIGH				
I_{SUP}	V_{SUP} = 3.6 V		–	50	tbf	µA
I_{BB}	V_{BB} = 2.95 V		–	400	tbf	µA
Loudspeaker amplifier inputs LSI1 and LSI2						
Z_i	input impedance (LSI1 and LSI2)	single ended	7.5	9.5	11.5	kΩ
		differential (LSI1 to LSI2)	15	19	23	kΩ
G_v	Voltage gain from LSI1/2 to QLS	I_{SUP} = 15 mA; V_i = 2 mV(RMS)	34	35	36	dB
ΔG_v	Total gain variation with input signal from 2 mV(RMS) to 10 mV(RMS)		–	0.2	–	dB
$\Delta G/\Delta T$	Total gain variation with temperature referred to 25 °C	T_{amb} = –25 to +75 °C	–	±0.4	–	dB
Output capabilities						
$V_{O(p-p)}$	Maximum output voltage (peak-to-peak value)	THD = 3 %; 50 Ω load	2.0	2.5	–	V
$V_{O(p-p)}$	Output voltage (peak-to-peak value)	V_i = 10 mV(RMS); I_{SUP} = 15 mA; V_{SUP}–V_{EE} = 1 V(RMS)	–	1.6	–	V
$V_{no(RMS)}$	Noise output voltage (RMS value)	1 kΩ between inputs LSI1 and LSI2; psophometrically weighted (P53 curve)	–	250	–	µV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power-down input (PD) (TEA1083A only)						
V_{IL}	LOW level input voltage		0	–	0.3	V
V_{IH}	HIGH level input voltage		1.5	–	V_{BB}	V
I_{PD}	Input current	PD = HIGH	–	2.3	2.8	µA
LSE input						
V_{IL}	LOW level input voltage		0	–	0.3	V
V_{IH}	HIGH level input voltage		1.5	–	V_{BB}	V
I_I	Input current	LSE = HIGH	–	5	10	µA
ΔG	Reduction of gain from LSI1/LSI2 to QLS	LSE = LOW	60	tbf	–	dB

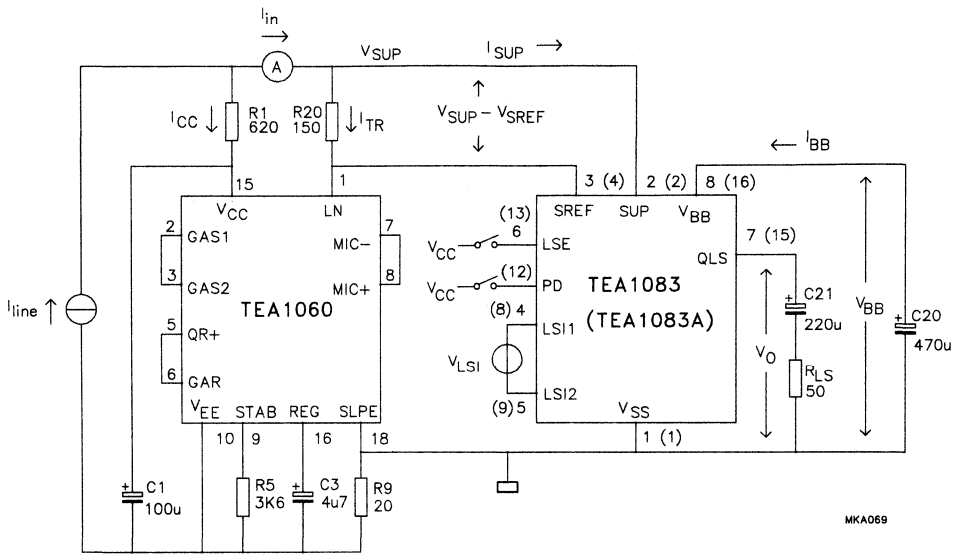


Fig.10 Test circuit.

Notes to figure 10

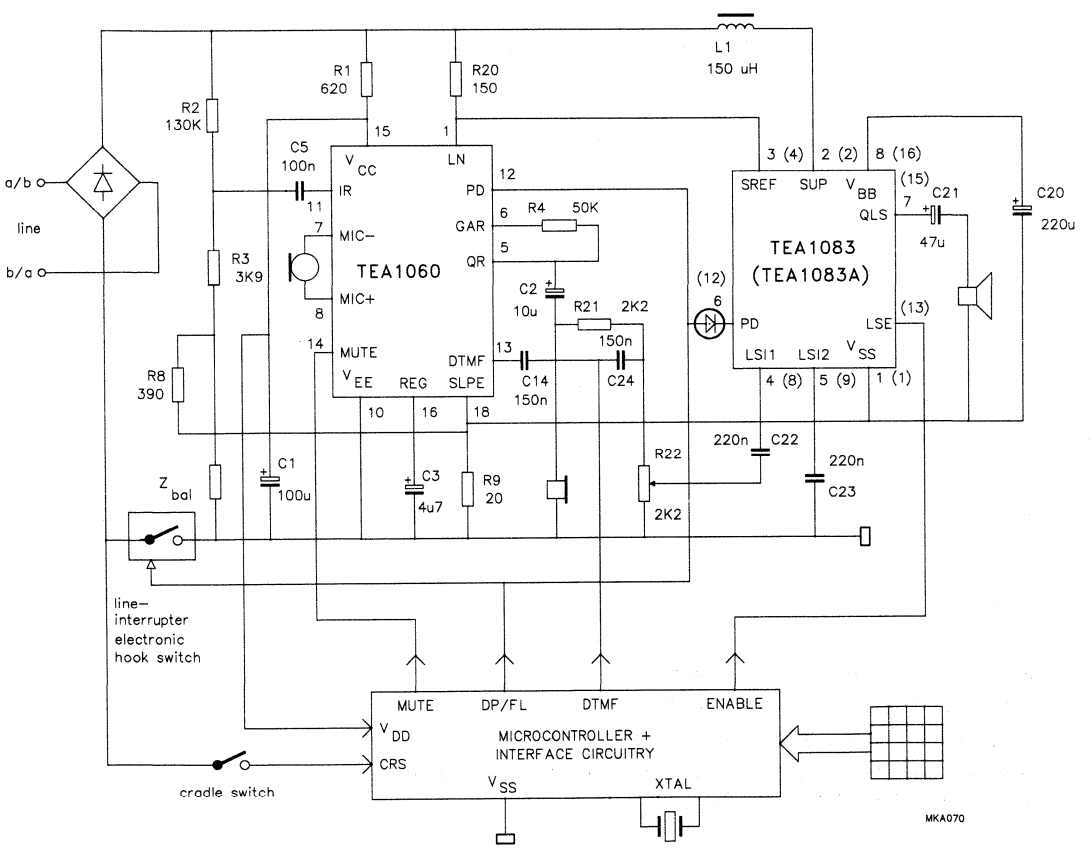
1. $I_{SUP} = I_{IN} - I_{TR}$
2. $G_v = 20 \log \left| \frac{V_O}{V_{LSI}} \right|$
3. $I_{TR} = \frac{V_{SUP-SREF}}{R20}$
4. The pin numbers in parenthesis refer to the TEA1083
5. LSE has to be HIGH to measure the voltage gain
6. PD has to be HIGH to measure in PD conditions
7. The pins not shown in the TEA1060 are left open-circuit
8. An impedance in series with pin SUP (e.g. an ammeter) should be avoided as it interferes with the values of I_{TR} and I_{SUP}.

APPLICATION INFORMATION

An application of the TEA1083/83A, in conjunction with a member of the TEA1060 family, is illustrated in figure 11. The TEA1083/83A is used for call progress monitoring during on-hook dialling. The dialling facilities are performed by a microcontroller (e.g. PCD3344, PCD3349).

Only the most important components have been shown. For detailed information refer to a data sheet of the TEA1060 family.

The electronic hook switch can be replaced by a mechanical system (hook switch) with a hold/release function which is intended for on-hook dialling.



Pin numbers in parenthesis refer to the TEA1083.

Fig.11 Application example when the TEA1083/83A is used in conjunction with the TEA1060.

Listening-in circuit for line-powered telephone sets

TEA1085/TEA1085A

FEATURES

- Internal supply
  optimum current split-up
  - low constant current (adjustable) in transmission IC
  - nearly all line current available for listening-in
  adjustable supply voltage
- Loudspeaker amplifier
  dynamic limiter providing low distortion and the highest possible output power
  SE or BTL drive for loudspeaker
  volume control by potentiometer and/or logic inputs (e.g. microcontroller drive)
  fixed gain of 35 dB
- Larsen level limiter
  low sensitivity for own speech due to 3rd-order filter and attack delay
  adjustable voltage thresholds
- Power down input
- MUTE input
  TEA1085/TEA1085A
  - clickfree switching between listening-in mode and standby mode
  TEA1085
  - toggle function
  - start-up in standby condition
  TEA1085A
  - logic level input

GENERERAL DESCRIPTION

The TEA1085 and TEA1085A are bipolar ICs which have been designed for use in line-powered telephone sets and provide a listening-in facility for the received line signal via a loudspeaker. Nearly all the line current can be used for powering the loudspeaker.
The circuits incorporate a supply circuit, loudspeaker amplifier dynamic limiter, MUTE circuit, power-down facility and logic inputs for gain setting. The devices also incorporate a Larsen Level Limiter to reduce howling effects.
The ICs are intended for use in conjunction with a transmission circuit of the TEA1060 family.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA1085/TEA1085A	24	DIL	plastic	SOT101B
TEA1085T/TEA1085AT	24	SO24	plastic	SOT137A

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{SUP}	input current range		4	–	120	mA
V_{BB}	stabilized supply voltage		–	3.6	–	V
I_{SUP}	current consumption	PD = HIGH	–	55	–	µA
G_v	voltage gain loudspeaker amplifier					
		SE	–	35	–	dB
		BTL	–	41	–	dB
ΔG_v	maximum gain reduction with logic inputs (3 steps)		–	18	–	dB
I_{SUP}	minimum input current					
		P_{OUT} = 20 mW typ. into 50 Ω SE	–	15	17	mA
		P_{OUT} = 40 mW typ. into 50 Ω BTL	–	–	32	mA
$t_{ad(RMS)}$	Larsen limiter attack delay time V_{DTI} jumps from 0 to ≥ 100 mV (RMS value)		100	–	200	ms
$V_{DTI(RMS)}$	Larsen limiter threshold level	Larsen mode	–	7	–	mV
G_v	Larsen limiter preamplifier gain setting range		30	–	52	dB
T_{amb}	operating ambient temperature range		–25	–	+75	°C

Listening-in circuit for line-powered telephone sets

TEA1085/TEA1085A

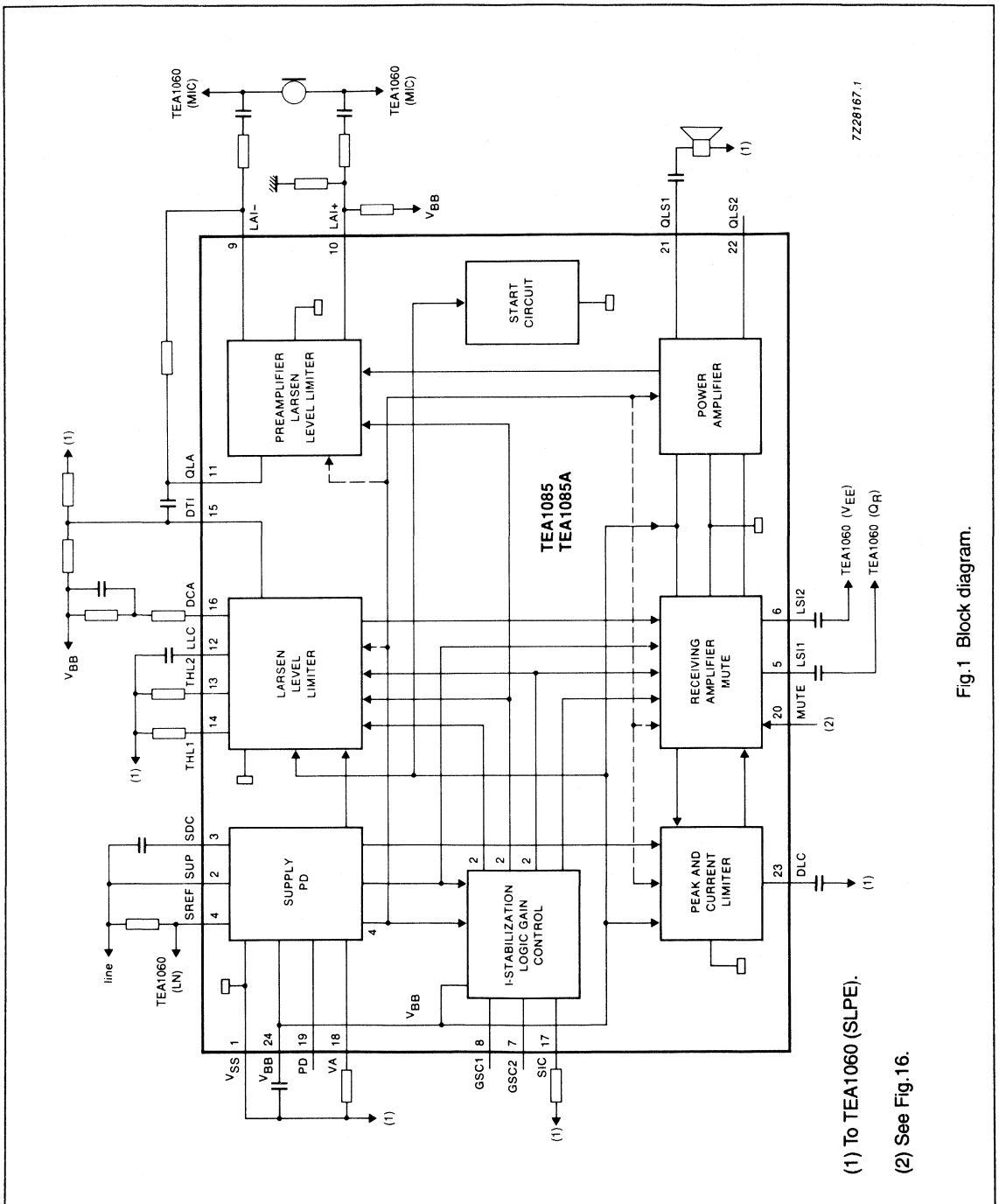


Fig.1 Block diagram.

SYMBOL	PIN	DESCRIPTION
V_{SS}	1	negative supply
SUP	2	positive supply
SDC	3	supply amplifier decoupling
SREF	4	supply reference input
LSI1	5	loudspeaker amplifier input 1
LSI2	6	loudspeaker amplifier input 2
GSC2	7	logic input 2 for gain select
GSC1	8	logic input 1 for gain select
LAI−	9	Larsen limiter preamplifier inverting input
LAI+	10	Larsen limiter preamplifier non-inverting input
QLA	11	Larsen limiter preamplifier output
LLC	12	Larsen limiter capacitor
THL2	13	Larsen limiter residual threshold level
THL1	14	Larsen limiter attack delay threshold level
DTI	15	Larsen limiter detector input
DCA	16	Larsen limiter detector current adjustment
SIC	17	Larsen limiter current stabilizer
VA	18	V_{BB} voltage adjustment
PD	19	power-down input
MUTE	20	MUTE input
QLS1	21	loudspeaker amplifier output 1
QLS2	22	loudspeaker amplifier output 2
DLC	23	dynamic limiter capacitor
V_{BB}	24	stabilized supply decoupling

PIN CONFIGURATION

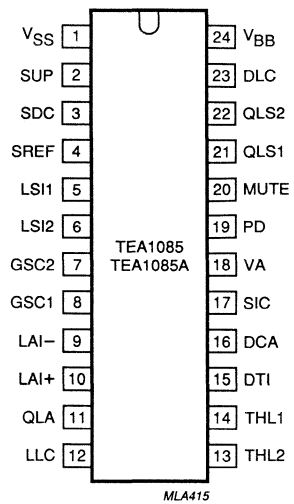


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Figure 1 illustrates a block diagram of the TEA1085/TEA1085A with external components and connections to the transmission IC.

The TEA1085/TEA1085A are bipolar ICs which have been designed for use in line-powered telephone sets and provide a listening-in facility for the received line signal via a loudspeaker. Nearly all the line current can be used for powering the loudspeaker.

The loudspeaker amplifier consists of a preamplifier, to amplify the earpiece signal from the transmission circuit and, a double push-pull output stage to drive the loudspeaker in the BTL (bridge tied load) or SE (single ended) configuration. The gain of the preamplifier is controlled by a dynamic limiter which prevents high distortion of the loudspeaker signal. This is achieved by preventing clipping of the loudspeaker signal, with respect to the supply voltage, and at too low supply current. Two logic inputs can be used to reduce the gain in 3 steps.

Because of acoustic feedback from the loudspeaker to the microphone, howling signals (Larsen effect) can occur on the telephone line and in the loudspeaker. When the Larsen signal exceeds a voltage and time duration threshold the Larsen level limiter (LLL) will reduce the Larsen signal to a low level within a short period of time by reducing the gain of the receiving preamplifier. This is achieved by using the microphone signal as an input signal which is processed in the LLL via a preamplifier and 3rd-order filter.

The MUTE input can be used to enable or disable the loudspeaker amplifier.

The MUTE function of the TEA1085 has a toggle input to permit the use of a simple push-button switch.

The MUTE function of the TEA1085A has a logic input to operate with a microcontroller.

By activating the power-down input the current consumption of the circuit will be reduced, this enables pulse dialling or flash (register recall).

An internal start circuit ensures normal start-up of the transmission IC and start-up of the listening-in IC in the standby mode.

The TEA1085/TEA1085A are intended for use in conjunction with a member of the TEA1060 family and should be connected between LINE and SLPE of the transmission IC. The transmission characteristics (impedance, gain settings, for example) are not affected. The interconnection between the two ICs is illustrated in Fig.3.

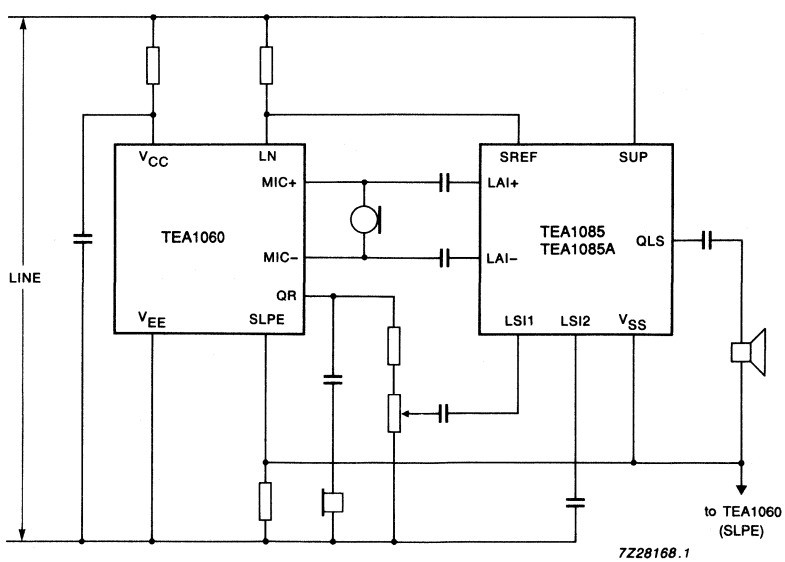
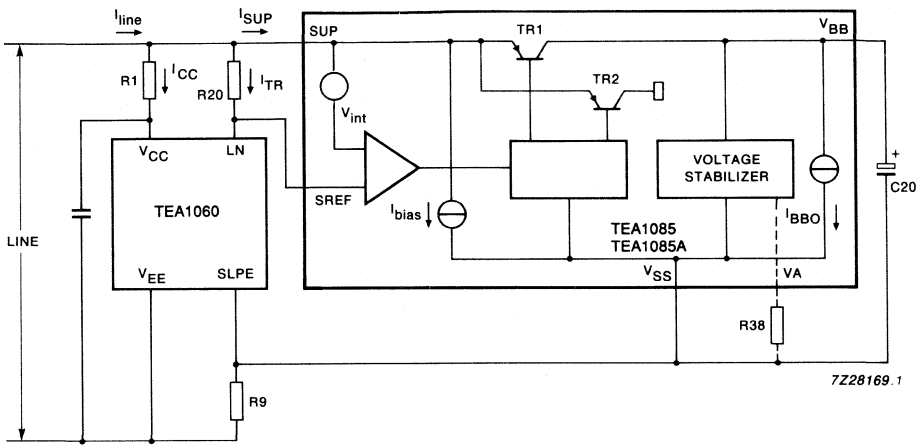


Fig.3 Interconnection of the TEA1085/TEA1085A with the TEA1060.

Supply; SUP, SREF, V_{BB}, V_{SS} and VA

The line current is divided into I_{TR} for the TEA1060 and I_{SUP} for the TEA1085/TEA1085A. The supply arrangement is illustrated in Fig.4.



I_{TR} is constant: $I_{TR} = V_{int}/R20$; $I_{SUP} = I_{line} - I_{CC} - I_{TR}$

Fig.4 Supply arrangement.

Where:

V_{int} is an internal temperature compensated reference voltage with a typical value of 315 mV between SUP and SREF

R20 is a resistor between SUP and SREF

I_{CC} is the internal current consumption of the TEA106X (≈ 1 mA)

A practical value for R20 is 150 Ω. This value of resistance produces a value for I_{TR} = 2 mA and $I_{SUP} = I_{line}$ −3 mA.

The TEA1085/TEA1085A stabilizes its own supply voltage at V_{BB}. Transistor TR1 provides the supplies for the internal circuits. TR2 is used to minimize the signal distortion on the line by momentarily diverting the input current to V_{SS} whenever the instantaneous value of the voltage V_{SUP} drops below the supply voltage V_{BB}. V_{BB} is fixed to a typical value of 3.6 V but can be increased by means of an external resistor (R38) connected between VA and V_{SS} or decreased by connecting this resistor between VA and V_{BB}. The minimum level on V_{BB} is restricted to 3.0 V; the level of the V_{BB} limiter is also affected (see application report for further information). The supply at V_{BB} is decoupled by a 470 µF capacitor.

The DC voltage ($V_{SUP} - V_{SS}$) is determined by the transmission IC ($V_{LN-SLPE}$); thus $V_{SUP} - V_{SS} = V_{LN-SLPE} + V_{int}$. The minimum DC voltage that can be applied to this input is $V_{BB(max)}$ + 0.4 V.

Where: $V_{BB(max)}$ is the worst case supply voltage (this depends on the setting of R38, which is connected between VA and V_{SS}).

The internal current consumption of the TEA1085/TEA1085A (I_{SUP0}) is typically 4.2 mA (where $V_{SUP} - V_{SS}$ = 4.5 V, MUTE off). Thus the current available for powering the loudspeaker is $I_{SUP} - I_{SUP0}$.
The current I_{SUP0} consists of a bias current of ≈ 0.4 mA for the circuitry connected to SUP and current I_{BB0} of ≈ 3.8 mA which is used for the circuitry connected to V_{BB} (see Fig.4).

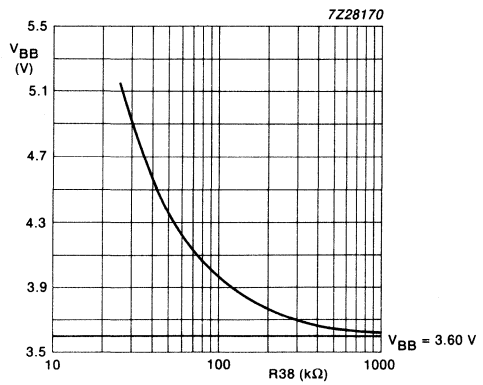


Fig.5 Stabilized supply voltage as a function of R38.

Supply amplifier stability (SDC) pin 3

To ensure stability of the TEA1085/TEA1085A, in combination with a transmission IC of the TEA1060 family, a 47 pF capacitor connected between SDC and SUP and a 150 μH coil connected between SUP and the positive line terminal (Fig.16) is required.

Loudspeaker amplifier (LSI1/LSI2 and QLS1/QLS2) pins 5/6, 21/22

The TEA1085/TEA1085A have symetrical inputs at LSI1 and LSI2. The input signal is normally taken from the earpiece output of the transmission circuit via a resistive attenuator (see Fig.3). The amount of attenuation must be chosen in accordance with the receive gain of the transmission IC (which depends on the sensitivity of the earpiece transducer). The maximum input signal level is 450 mV(RMS) at T_{amb} = +25 °C.
The outputs QLS1 and QLS2 can be used for single ended drive (SE) or bridge tied load drive (BTL). The output stages have been optimized for use with a 50 Ω loudspeaker (eg Philips type AD2071).
The gain of the amplifier is fixed to ≈ 35 dB for the SE drive and ≈ 41 dB for the BTL drive (when the inputs for logic control are left open-circuit or are connected to V_{SS}).
The volume control can be obtained by using a potentiometer at the input and/or by the logic control function.

Logic gain control (GSC1 and GSC2) pins 7 and 8

The logic inputs GSC1 and GSC2 can be used to reduce the gain of the loudspeaker amplifier by means of the logic gain control function in 3 steps of 6 dB.

Table 1 Data for microcontroller drive of logic inputs

GSC2	GSC1	gain (dB)	gain reduction (dB)
0	0	35	0
0	1	28.7	6.3
1	0	22.2	12.2
1	1	17	18

Where:

0 = connection to V_{SS} or left open-circuit
1 = applying a voltage ≥ V_{SS} + 1.5 V

Dynamic limiter (DLC) pin 23

To prevent distortion of the signal at the loudspeaker outputs the gain of the amplifier is reduced rapidly when:

- the peaks of the signal at the loudspeaker outputs exceed an internaly determined threshold (voltage limiter)
- the DC current into SUP is insufficient (current limiter)
- the voltage at V_{BB} decreases below an internally determined threshold, typically 2.9 V (V_{BB} limiter)

The time in which the gain reduction is effected is the 'attack time'; this is very short in the first and third instance and relatively long in the second instance. The circuit will remain in the gain-reduced condition until the peaks of the output signal remain below the threshold level. The gain will then return to a nominal level after a time determined by the capacitor connected to DLC (release time).

MUTE input (MUTE) pin 20; TEA1085A

This MUTE is provided with a logic input to operate with a microcontroller for instance.
The loudspeaker amplifier is disabled when the MUTE input is LOW (connected to V_{SS} or open input). A HIGH level at the MUTE input enables the amplifier in the listening-in mode.

MUTE input (MUTE) pin 20; TEA1085

The MUTE function is provided with a toggle input and is designed to switch between the standby condition and the listening-in condition on the rising edge of the input MUTE signal (see Fig.6).
In the basic application the MUTE input must be LOW (connected to V_{SS}). A simple push-button can be used to operate the MUTE toggle (see Fig.7). Debouncing can be realized by means of a small capacitor connected between MUTE and V_{SS}.
An internal start circuit ensures that the circuit always starts up in the standby condition.

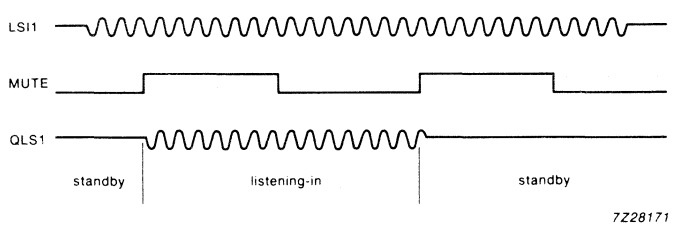
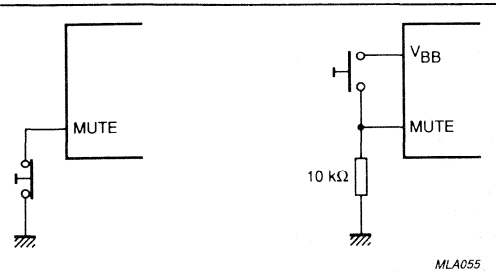


Fig.6 Mute toggle function of the TEA1085.



(a) Break contact. (b) Make contact.

Fig.7 Mute switch alternatives with the TEA1085.

Power down input (PD) pin 19

During pulse dialling or register recall (timed loop break) the telephone line is interrupted, thereby breaking the supply to the transmission and listening-in circuits. The capacitor connected to V_{BB} provides the supply for the listening-in circuit during the supply breaks.
By making the PD input HIGH during the loop break the requirement on the capacitor is eased and, consequently, the internal (standby) current consumption I_{BBO} (Fig.4) at V_{BB} is reduced from 3.8 mA to 400 μA typical. So that the transmission circuit is not affected transistors TR1 and TR2 are inhibited and the bias current is reduced from ≈ 0.4 mA to ≈ 55 μA with V_{SUP} = 4.5 V in the following equation:

$I_{SUP(PD)} = I_{BIAS(PD)} = (V_{SUP} - 2V_d)/Ra$

(where $4.2\ V < V_{SUP} < V_{BB} + 3\ V$)

$2V_d$ = the voltage drop across 2 internal diodes (≈ 1.3 V)
Ra = an internal resistor of typical 60 kΩ

Larsen limiter current stabilizer (SIC) pin 17

A current reference is set by resistor R36 between SIC and V_{SS}. The preferred value is 120 kΩ. The internal reference current is given by the following equation:

$I_{SIC} = 1.25/R36$; when R36 = 120 kΩ, I_{SIC} = 10.5 μA

Changing the value of R36 will affect the timing of the Larsen level limiter system.

Larsen limiter preamplifier (LAI1/LAI2 and QLA) pins 9/10 and 11

This circuit amplifies the microphone signal to a level suitable for the Larsen limiter detector. The gain is set by external components (see Fig.8).
Normally the gain is set to the same level as the microphone amplifier of the transmission circuit, this ensures that the output signal level at output QLA is equal to the line signal level.

The gain between QLA and the microphone input is given by the following equation (the high-pass filter is not taken into account):

$A_{pre} = V_{QLA}/V_M = R29/R26$; in the basic application R25 = R26 = 10 kΩ

The gain can be adjusted between 30 dB (R29 = 316 kΩ) and 52 dB (R29 = 4 MΩ). The impedance result of R28 and R27 in parallel must be equal to R29 (e.g. R27 = R28 = 2 x R29)

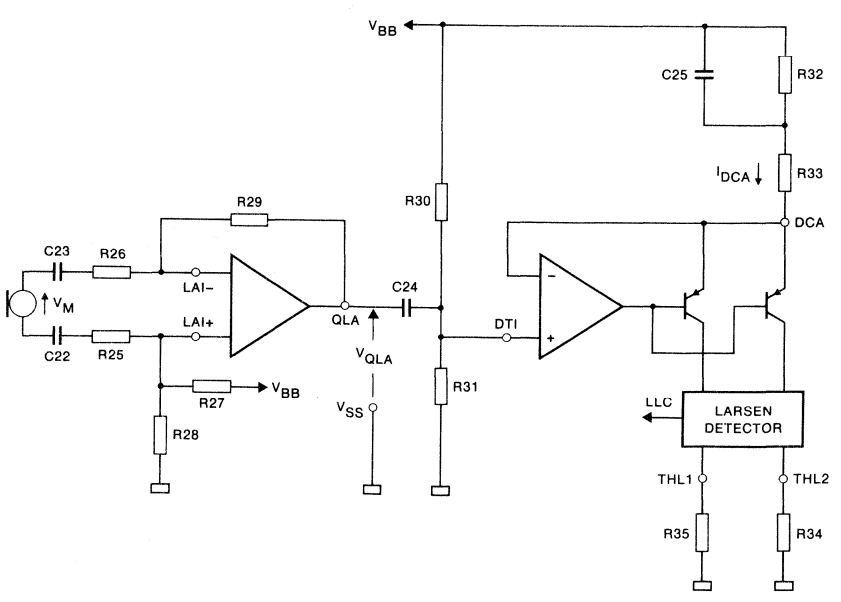


Fig.8 Larsen limiter preamplifier and voltage/current converter. 7Z28173

Larsen limiter detector (DTI and DCA) pins 15 and 16

The QLA output signal is AC coupled to the detector input DTI. DTI is biased by potential divider R30 and R31. The voltage applied to DTI of the Larsen level limiter is converted into a current for further processing in this circuit. Current adjustment is achieved using the network connected between DCA and V_{BB} (see Fig.8).

The equation for DC current is:

$$I_{DCA} = \frac{R30}{R30 + R31} \times V_{BB} \times \frac{1}{R32 + R33}$$

The equation for AC current is:

$$i_{DCA} = \frac{V_{DTI}}{R33} \text{ for } f > \tfrac{1}{2}\pi R33C25$$

In the basic application:

R30 = 100 kΩ, R31 = 220 kΩ, R33 = 500 Ω, R32 = 100 kΩ and C25 = 330 nF

This results in I_{DCA} = 11 μA and the equation:

$$\frac{i_{DCA}}{V_{DTI}} + 2 \text{ (mA/V)}$$

High-pass filter

A third order high-pass filter is created between the microphone input voltage and the current flowing into DCA. The cut-off frequencies (see Fig.9) of the three sections are:

$$f1 = \frac{1}{2\pi R_{eg} C24} \text{ where } R_{eq} = \frac{R30 \times R31}{R30 + R31}$$

$$f2 = \frac{1}{2\pi R33 C24} \qquad f3 = \frac{1}{2\pi R26 C23} = 1/(2\pi R25C22)$$

Where: R25 = R26 and C22 = C23

The filter reduces the sensitivity of the system to own speech.
Normal speech is in the frequency range 300 Hz to 3400 Hz, however, the Larsen signal normally occurs at a frequency > 3 kHz.
With the component values as used in the basic application (see Fig.16); f1 = 500 Hz, f2 = 1 kHz and f3 = 3 kHz

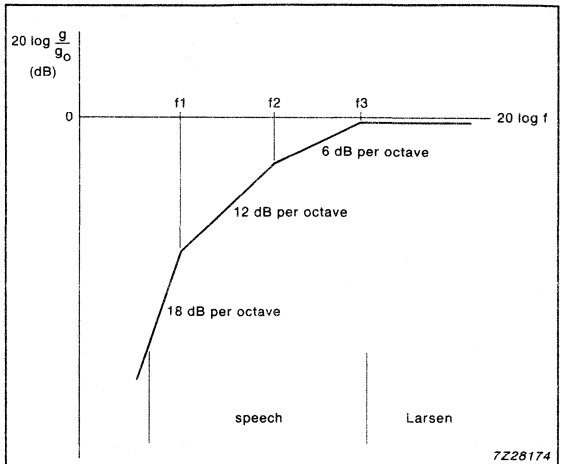


Fig.9 Third-order high-pass filter.

Where:

$$g = \frac{i_{DCA}}{V_m} \qquad g_O = \frac{A_{pre}}{R33}$$

Larsen limiter capacitor (LLC) pin 12

A 1 μF capacitor (C26) is connected externally between V_{SS} and LLC to determine the attack and release timing of the Larsen level limiter in the listen-in and Larsen mode. The timing is also dependent on the value of the resistor connected between SIC and V_{SS}.

Larsen level limiter threshold (THL1 and THL2) pins 13 and 14

When the signal at DTI exceeds the first threshold level the capacitor connected to LLC will start to discharge. The first threshold level is determined by the value of the resistor, R35, connected to THL1 and V_{SS}. The amount of discharge of C26 depends on how much the level of the signal at DTI exceeds the first threshold level (for normal speech the discharge is small).
The Larsen effect is generally defined as a signal level of ≥ 100 mV(RMS),on line, for a period of more than 100 ms. The Larsen signal must be reduced to a low level within 200 ms. For Larsen signal levels (f > f3 in Fig.9) of ≥ 100 mV(RMS) at DTI and, with the component values of Fig.16, the system will switch from the listen-in mode to the Larsen mode in a time period of 100 ms to 200 ms; consequently, the initial Larsen effect will last only for a short period of time.

This reaction time is the 'attack delay time' and ensures minimum sensitivity of the system for own speech.

The first threshold level at DTI is determined by the equation:

$$V_{DTh} = (\frac{1.25}{R25} - \frac{I_{DCA}}{2}) \times 2 \times R33 \text{ (if f > f3 in Fig.9)}$$

Where: I_{DCA} = the DC current into DCA

With the component values given in Fig.16, I_{DCA} = 11 µA thus V_{DTI1} = 18.8 mV.

Listen-in mode

During normal speech the discharge of the capacitor connected to LLC is not sufficient to reach the threshold level whereby the system switches to the Larsen mode. This is because normal speech is not continuous, the discharge of C26 is slow (attack delay) and the charge is fast.
The slope of V_{LLC} during charge is given in the equation:

$$S_{1i} = \frac{\Delta V_{LLC}}{\Delta_\tau} = \frac{1.25}{C26 \times R36} \text{ (V/s)}$$

With C26 = 1 µF and R36 = 120 kΩ this results in S_{1i} = 10 V/s.

Discharge of the capacitor at LLC occurs when the signal at DTI exceeds V_{DTI1}, thus for a continuous signal at DTI the attack delay time t_{ad} (see Fig.10) is determined by the equation:

$$t_{ad} = \frac{C26 \times R36}{2 \times (3 \times k - 1)}$$

Where k = t1/T

The duty cycle is determined by the time in which the first threshold level (V_{DTI1}) is exceeded by the signal level at DTI (see Fig.11) thus for large signals; k ≤ 0.5.
With the component values given in Fig.16; k ≥ 0.457 for signals ≥ 100 mV(RMS).
Consequently 120 ms ≤ t_{ad} ≤ 160 ms, for V_{DTI} ≥ 100 mV(RMS)

Larsen mode

After the 'attack delay time' the circuit switches from the listen-in mode to the Larsen mode. The gain of the loudspeaker amplifier is reduced quickly to a value (t_{LAa} = Larsen attack time see Fig.10) whereby the residual Larsen signal is determined by a second threshold level. This level can be set by resistor R34 connected between THL2 and V_{SS}. The second threshold level must always be selected at a lower level than the first threshold level thus R34 > R35.
The time taken to effect gain reduction is very short. In the Larsen mode the circuit acts as a dynamic limiter with peak detector and regulates the gain so that the signal level at DTI is determined by the second threshold level V_{DTI2}.
The second threshold level at DTI is determined by the equation:

$$V_{DTI2} = (\frac{1.25}{R34} - \frac{I_{DCA}}{2}) \times 2 \times R33 \text{ (if f > f3 in Fig.9)}$$

Where: I_{DCA} = the DC current into DCA

With the component values given in Fig.16, V_{DTI2} = 6.9 mV.

The charge current in the Larsen mode is reduced to half the charge current in the listen-in mode.

The slope of V_{LLC} during charge (see Fig.10) is given in the equation:

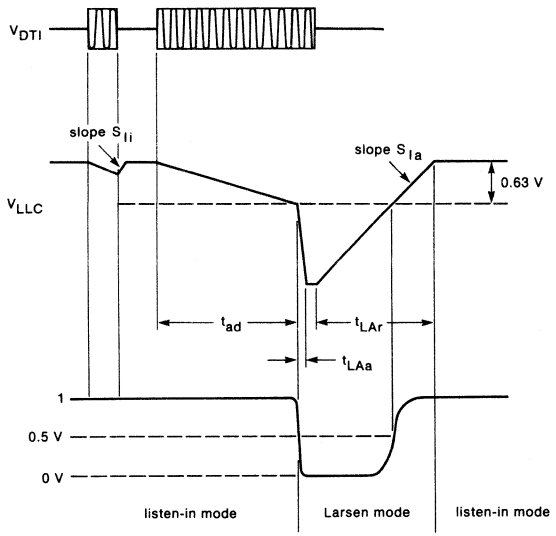
$$S_{la} = \frac{\Delta V_{LLC}}{\Delta_\tau} = \frac{1.25}{2 \times C26 \times R34} \text{ (V/s)}$$

Where: C26 = 1 µF and R36 = 100 kΩ, S_{la} = 5 V/s

When the Larsen effect stops (total open-loop gain < 1) the gain of the loudspeaker amplifier will return to its normal value in a time period known as the 'Larsen release time' (t_{LAr}). This time period is determined by capacitor C26 connected to LLC and resistor R36 connected to SIC.

Where: C26 = 1 µF and R36 = 120 kΩ, t_{LAr} = 250 ms

In practice the choice of the threshold levels (determined by R35 and R34) depends on the sensitivity of the microphone and loudspeaker, the send and receive gains, sidetone suppression and the acoustical properties which are determined by the cabinet of the telephone set.

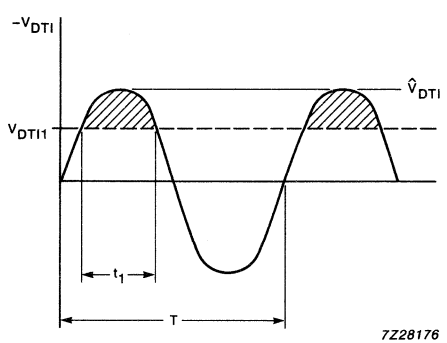


Where:

Change of receive gain = $\frac{G_v}{G_{vo}}$

Nominal receive gain = 20 log G_{vo} = 35 dB

Fig.10 Dynamic behaviour of Larsen limiter (in open-loop condition).



Where:

$k = \frac{t_1}{T}$

$k = 0.5 - \frac{\arcsin\left(\frac{V_{DTI1}}{\hat{V}_{DTI}}\right)}{\pi}$

Fig.11 Definition of duty cycle k.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

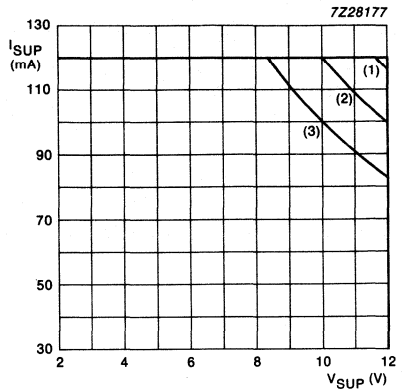
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{SUP}	positive supply voltage				
	continous		–	12	V
	during switch-on or line interruption		–	13.2	V
	repetitive supply voltage from 1 ms to 5 s	with 12 Ω current limiting resistor in series with supply	–	28	V
V_{SREF}	supply reference voltage		V_{SS}–0.5	V_{SUP}+0.5	V
V_n	voltage on all other pins		V_{SS}–0.5	V_{BB}+0.5	V
I_{SUP}	supply current				
	TEA1085/TEA1085A	see Fig.12	–	120	mA
	TEA1085T/TEA1085AT	see Fig.13	–	120	mA
P_{tot}	total power dissipation	T_{amb} = 75 °C; T_j = 125 °C			
	TEA1085/TEA1085A		–	1	W
	TEA1085T/TEA1085AT		–	666	mW
T_{amb}	operating ambient temperature range		–25	+75	°C
T_{stg}	storage temperature range		–40	+125	°C
T_j	junction temperature		–	+125	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air		
	TEA1085/TEA1085A		50 K/W
	TEA1085T/TEA1085AT	note 1	75 K/W

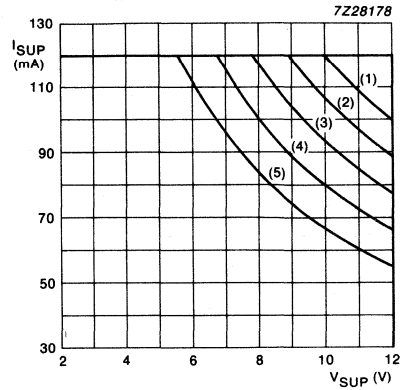
Note

1. Device mounted on a glass epoxy board 40.1 x 19.1 1.5 mm.



(1) T_{amb} = 55 °C; P_{tot} = 1.4 W.
(2) T_{amb} = 65 °C; P_{tot} = 1.2 W.
(3) T_{amb} = 75 °C; P_{tot} = 1.0 W.

Fig.12 TEA1085/TEA1085A safe operating area.



(1) T_{amb} = 35 °C; P_{tot} = 1.2 W.
(2) T_{amb} = 45 °C; P_{tot} = 1.07 W.
(3) T_{amb} = 55 °C; P_{tot} = 0.93 W.
(4) T_{amb} = 65 °C; P_{tot} = 0.8 W.
(5) T_{amb} = 75 °C; P_{tot} = 0.666 W.

Fig.13 TEA1085T/TEA1085AT safe operating area.

CHARACTERISTICS

V_{SREF} = 4.2 V; V_{SS} = 0 V; I_{SUP} = 15 mA; V_{SUP} = 0 V(RMS); f = 800 Hz; T_{amb} = 25 °C; PD = LOW; MUTE (TEA1085) = OFF (listening-in mode); MUTE (TEA1085A) = HIGH (listening-in mode); GSC1 = GSC2 = LOW; 50 Ω loudspeaker; no R38; test circuit Fig.14; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{SUP}	minimum DC input voltage		–	V_{BB}+0.7	–	V
$V_{SUP-SREF}$	internal reference voltage		275	315	355	mV
V_{BB}	stabilized supply voltage	no R38; I_{SUP} = 15 mA	3.4	3.6	3.8	V
ΔV_{BB}	variation from I_{SUP} = 15 to 120 mA		–	10	–	mV
		R38 = 39.2 kΩ between pins V_{SS} and VA; V_{SREF} = 5.2 V; I_{SUP} = 15 mA	4.2	4.45	4.7	V
$\Delta V_{BB}/\Delta T$	variation with temperature	no R38; I_{SUP} = 15 mA	tbf	–0.2	tbf	V
I_{SUP}	minimum operating current		–	4.2	5.5	mA
THD	distortion of AC signal on SUP	$V_{SUP(RMS)}$ = 1 V	–	0.3	–	%
$V_{no(RMS)}$	noise between SUP and V_{EE}		–	–72	–	dBmp
	current consumption in power-down condition	PD = HIGH				
I_{SUP}		V_{SUP} = 4.5 V	–	55	75	μA
I_{BB}		V_{BB} = 3.6 V	–	400	550	μA
Loudspeaker amplifier inputs LSI1 and LSI2						
$\lvert Z_i \rvert$	input impedance					
		single ended	7.5	9.5	11.5	kΩ
		differential	15	19	23	kΩ
G_v	voltage gain with 50 Ω load	I_{SUP} = 15 mA; V_i = 1.8 mV(RMS)				
		single ended	34	35	36	dB
		BTL output	39.9	40.9	41.9	dB
ΔG_v	variation with signal level	I_{SUP} = 50 mA; V_i = 1.8 mV(RMS) and 14 mV(RMS)				
		single ended	–	+0.1	0.4	dB
		BTL output	–	+0.2	0.6	dB
ΔG_v	variation with frequency referred to 1 kHz	f = 300 Hz and 3400 Hz; V_i = 1.8 mV(RMS)				
		single ended	–	± 0.1	–	dB
		BTL output	–	± 0.1	–	dB

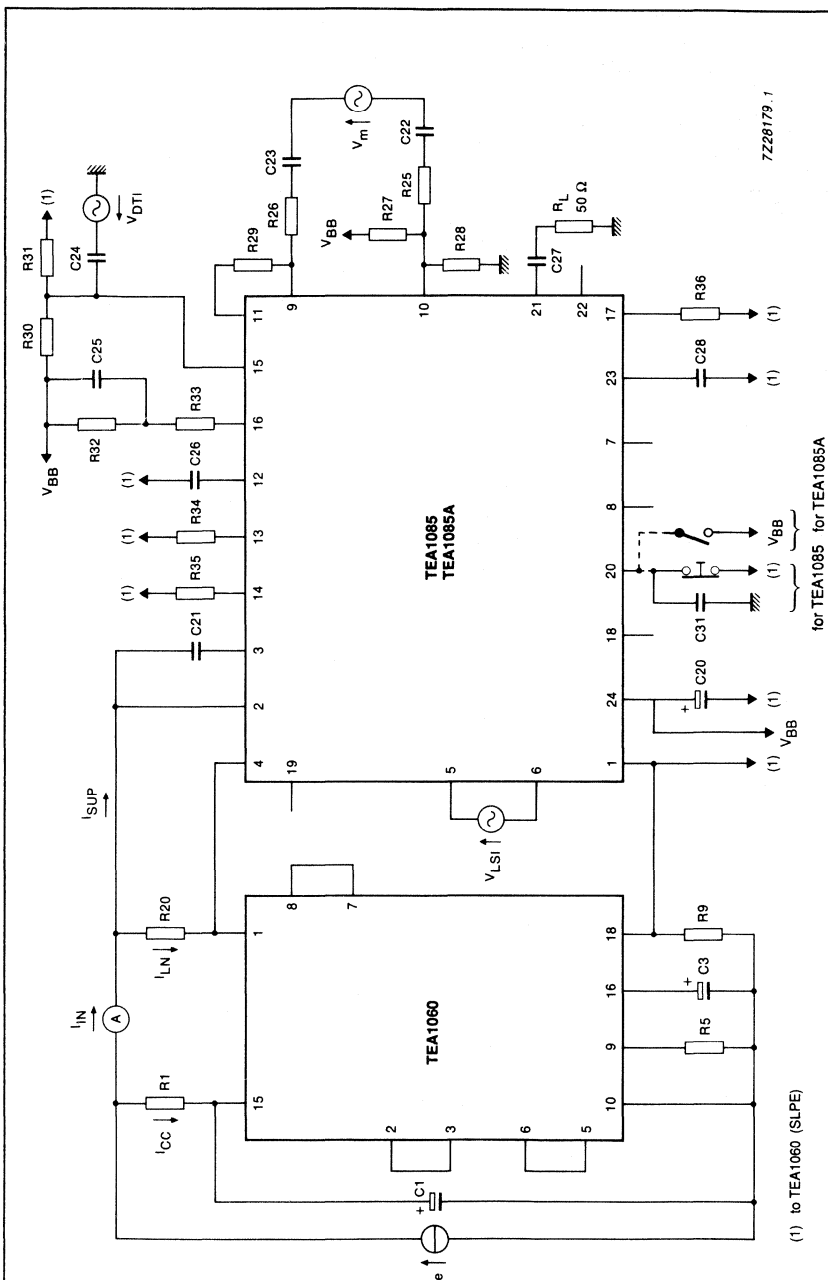
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ΔG_v	variation with temperature referred to 25 °C	T_{amb} = −25 to +75 °C				
		single ended	–	± 0.4	–	dB
		BTL output	–	± 0.5	–	dB
Loudspeaker outputs QLS1 and QLS2						
$V_{o(p-p)}$	output voltage (peak-to-peak value)	V_i = 22 mV(RMS)				
	single ended	I_{SUP} = 9 mA; note 1	1.2	1.45	–	V
		I_{SUP} = 17 mA; note 2	2.5	2.9	–	V
	bridge-tied load	I_{SUP} = 23.5 mA; note 2	2.5	2.9	–	V
		I_{SUP} = 32 mA; note 3	3.5	4.0	–	V
THD	total harmonic distortion	V_i = 22 mV(RMS)				
	single ended	I_{SUP} = 9 mA	–	0.4	2	%
		I_{SUP} = 17 mA	–	0.7	2	%
	bridge tied load	I_{SUP} = 23.5 mA	–	0.4	2	%
$V_{o(p-p)}$	output voltage (peak-to-peak value)	V_i = 22 mV(RMS)				
	single ended	I_{SUP} = 17 mA; V_{SUP}-V_{EE} = 1 V(RMS)	1.75	2.15	–	V
Dynamic limiter						
THD	total harmonic distortion	V_i = 22 mV(RMS) +10 dB				
	single ended	I_{SUP} = 9 mA	–	0.5	10	%
		I_{SUP} = 17 mA	–	1.2	10	%
	bridge tied load	I_{SUP} = 23.5 mA	–	0.6	10	%
	dynamic behaviour of limiter	single ended load				
t_{att}	attack time; V_i jumps from 10 mV(RMS) to 65 mV(RMS)					
	voltage limiter	I_{SUP} = 17 mA	–	2	5	ms
	current limiter	I_{SUP} = 12 mA	–	500	tbf	ms
	V_{BB} limiter	I_{SUP} = 9 mA	–	10	–	ms
t_{rel}	release time; V_i jumps from 65 mV(RMS) to 10 mV(RMS)	I_{SUP} = 17 mA	tbf	75	tbf	ms
V_{BBO}	threshold V_{BB} limiter below which gain reduction starts	I_{SUP} = 9 mA	tbf	2.95	tbf	V
$V_{no(RMS)}$	noise output voltage	1 kΩ between inputs LSI1, LSI2; psophometrically weighted (P53 curve)				
	single ended		–	170	–	µV
	bridge tied load		–	350	–	µV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Logic gain control						
ΔG_v	reduction of voltage gain	V_i = 1.8 mV(RMS)				
	GSC2 = 0, GSC1 = 1		5.8	6.3	6.8	dB
	GSC2 = 1, GSC1 = 0		11.7	12.2	12.7	dB
	GSC2 = 1, GSC1 = 1		17	18	19	dB
Larsen limiter preamplifier						
	operational amplifier					
G_{v0}	open-loop gain		–	92	–	dB
f_{p1}	1st pole		–	120	–	Hz
f_{p2}	2nd pole		–	3.3	–	MHz
G_B	unity gain bandwidth		–	4	–	MHz
G_v	voltage gain	f = 3 kHz; R26 = 10 kΩ; R29 = 4 MΩ	51	52	53	dB
G_v	gain adjustment range		30	–	52	dB
Larsen limiter detector						
	voltage to current convertor					
V_{DCA}-V_{DTI}	DC offset voltage	V_{BB}-V_{DTI} = 1 V	–25	1	+25	mV
G_v	voltage gain from DTI to DCA	V_{DTI} = 100 mV(RMS); f = 3 kHz	tbf	–0.8	tbf	dB
V_{THL1}	DC voltage at THL1	R35 = 51 kΩ	1.8	1.25	1.33	V
V_{THL2}	DC voltage at THL2	R34 = 100 kΩ	1.8	1.25	1.33	V
	dynamic behaviour with a burst at DTI	f = 3 kHz; see Fig.15				
t_{LIr}	listen-in release time	see Fig.15(a)	tbf	40	tbf	ms
t_{ad}	attack delay time	see Fig.15(b)				
	V_{DTI} jumps from 0 to 100 mV (RMS value)		–	160	200	ms
	V_{DTI} jumps from 0 to 1 V (RMS value)		100	120	–	ms
t_{LAa}	Larsen attack time	see Fig.15(b); V_{DTI} = 100 mV(RMS)	–	20	tbf	ms
t_{LAr}	Larsen release time	see Fig.15(b)				
	V_{DTI} jumps from 100 mV to 0 mV (RMS value)		tbf	250	tbf	ms
V_{LLC}	DC voltage at LLC	V_{DTI} = 0 V	1.75	1.9	2.0	V
$-\Delta V_{LLC}$	reduction of V_{LLC} to attack Larsen mode		0.59	0.63	0.68	V
ΔG_v	gain reduction	V_{LLC} = 0.7 V	60	tbf	tbf	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
MUTE INPUT; TEA1085						
	(toggle function, positive edge triggered set-reset flip-flop)					
V_{IL}	LOW level input voltage		0	–	0.3	V
V_{IH}	HIGH level input voltage		1.5	–	V_{BB}+0.4	V
I_{MUTE}	input current	MUTE = LOW	–	–22	–28	μA
t_W	minimum input pulse width		–	50	–	μs
P_R	minimum pulse repetition time		–	2	–	ms
$V_{BB(MUTE)}$	supply voltage below which MUTE toggle is reset		tbf	2	tbf	V
ΔG_v	reduction of gain from LSI1, LSI2 to QLS1, QLS2	MUTE = ON	60	100	–	dB
MUTE INPUT; TEA1085A						
V_{IL}	LOW level input voltage		0	–	0.3	V
V_{IH}	HIGH level input voltage		1.5	–	V_{BB}+0.4	V
I_{MUTE}	input current	MUTE = HIGH	–	10	20	μA
ΔG_v	reduction of gain from LSI1, LSI2 to QLS1, QLS2	MUTE = HIGH	60	100	–	dB
POWER DOWN INPUT						
V_{IL}	LOW level input voltage		0	–	0.3	V
V_{IH}	HIGH level input voltage		1.5	–	V_{BB}+0.4	V
I_{PD}	input current	PD = HIGH	–	2.3	2.8	μA
LOGIC INPUTS GSC1 and GSC2						
V_{IL}	LOW level input voltage		0	–	0.3	V
V_{IH}	HIGH level input voltage		1.5	–	V_{BB}+0.4	V
I_{GSC}	input current	GSC = HIGH	–	6	8	μA

Notes to the characteristics

1. Typical output power is 5 mW into 50 Ω
2. Typical output power is 20 mW into 50 Ω
3. Typical output power is 40 mW into 50 Ω



The DC current is divided as follows:

$$I_{SUP} = I_{IN} - \frac{V_{SUP-SREF}}{R20}$$

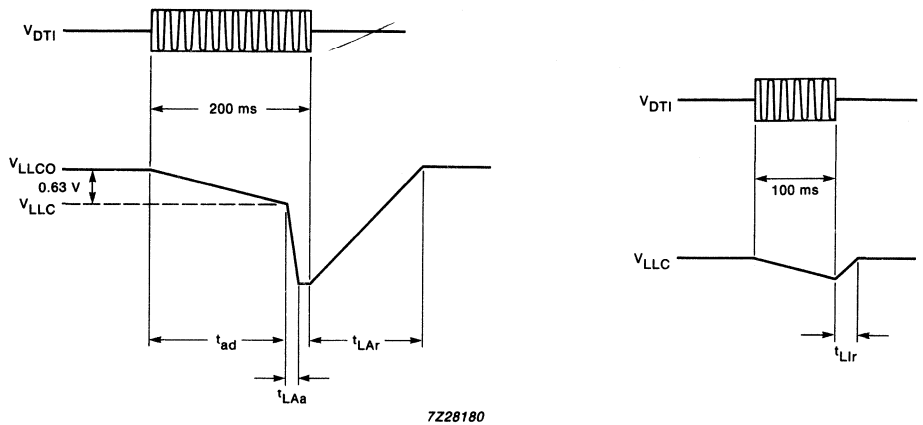
$$I_{LN} = \frac{V_{SUP-SREF}}{R20}$$

The pins not shown in the TEA1060 are left open. An impedance in series with pin SUP (e.g. an ammeter) should be avoided as it interferes with the value of I_{LN}.

Fig.14 Test circuit.

Table 2 Component values in test circuit Fig.14

COMPONENT	CONDITION	VALUE	UNIT
Resistor			
R1		620	Ω
R5		3.6	kΩ
R9		20	Ω
R20		150	Ω
R25		10	kΩ
R26		10	kΩ
R27		8	MΩ
R28		8	MΩ
R29		4	MΩ
R30		100	kΩ
R31		220	kΩ
R32		100	kΩ
R33		500	Ω
R34		100	kΩ
R35		51	kΩ
R36		120	kΩ
Capacitor			
C1		100	µF
C3		4.7	µF
C20		470	µF
C21		68	pF
C22		2.2	µF
C23		2.2	µF
C24		100	nF
C25		330	nF
C26		1	µF
C27		220	µF
C28		330	nF
C31	TEA1085 only	10	nF



(a) Listen-in release time (t_{LIr}); V_{DTI} = 100 mV(RMS); f = 3 kHz.

(b) Attack delay (t_{ad}), Larsen attack time (t_{LAa}), Larsen release time (t_{LAr}); V_{DTI} = 100 mV(RMS) and 1 V(RMS); f = 3 kHz.

Fig.15 Test signals for Larsen level limiter.

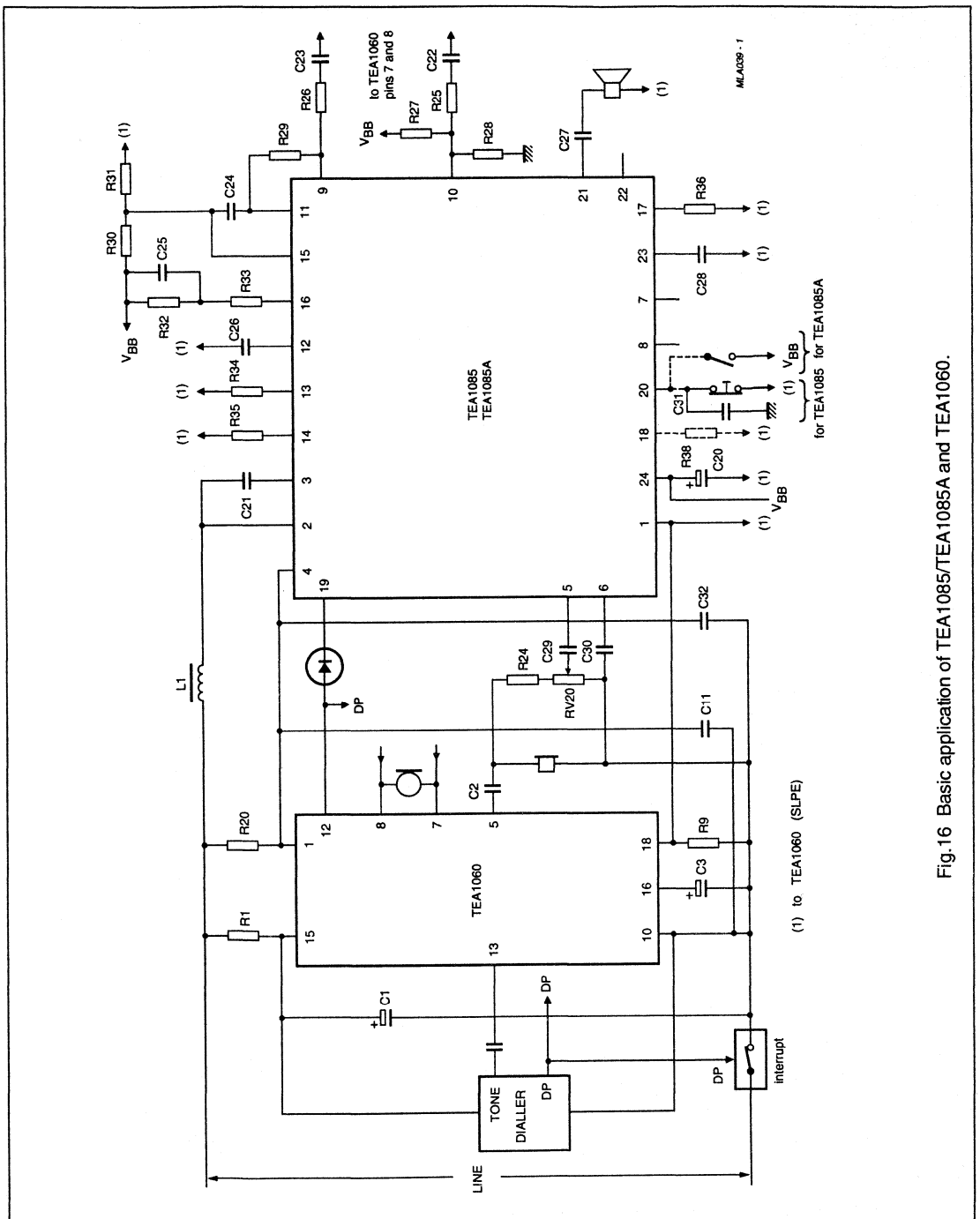


Fig.16 Basic application of TEA1085/TEA1085A and TEA1060.

APPLICATION INFORMATION

The basic application circuit of the TEA1085/TEA1085A is illustrated in Fig.16. Only the most important components of the TEA1060 part are shown, other components and their values are given in the TEA1060 Data sheet.
The supply pin (V_{BB}) of the TEA1085/TEA1085A can also be used to supply peripheral circuits (e.g. microcontrollers, diallers etc.). Further information will be published in the TEA1085 application report.

Table 3 Component values in application circuit Fig.16

COMPONENT	CONDITION	VALUE	UNIT
Resistor			
R20		150	Ω
R24	note 1	1	kΩ
R25		10	kΩ
R26		10	kΩ
R27	note 1	3.3	MΩ
R28	note 1	3.3	MΩ
R29	note 1	1.65	MΩ
R30		100	kΩ
R31		220	kΩ
R32		100	kΩ
R33		500	Ω
R34		100	kΩ
R35		51	kΩ
R36		120	kΩ
RV20	note 1	1	kΩ
Capacitor			
C11		4.7	nF
C20		470	µF
C21		47	pF
C22		4.7	nF
C23		4.7	nF
C24		4.7	nF
C25		330	nF
C26		1	µF
C27		47	µF
C28		330	nF
C29		220	nF
C30		220	nF
C31	TEA1085 only	10	nF
Coil			
L1		150	µH

Note to Table 3

1. Value depends on the gain setting of the transmission circuit.

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	April 1991

TEA1088T

SMPS battery charger control circuit

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC11 OR DATA SHEET

FEATURES

- SMPS control circuit
  fixed frequency/duty factor regulation
  emitter drive for power switch
  current mode control
  dynamic primary current limiting
- Charge control circuit
  accurate output current setting
  fast, two stages, charge mode
  two hours fast charge protection limit
  trickle charge mode for full batteries
- Voltage control circuit
  voltage regulation for connected mains and load
- Battery monitor circuit
  accurate fully charged detection (–dV phenomenon)
  LOW-level detection and indication
  protection against faulty batteries, short or open-circuit
  data output for condition of charge processing
  very LOW stand-by current, < 10 μA

GENERAL DESCRIPTION

The TEA1088T is a control circuit which has been designed for use in a battery charger and/or monitor system. The device incorporates all the control and protection functions that are required in a switched-mode power supply used to deliver charge current. The circuit also achieves direct drive to the emitter of the SMPS power transistor.
The battery monitor circuit includes a reliable battery-full detector which controls the switch-over from fast charge to trickle charge mode and, in the discharge mode, a battery-LOW detector with two outputs for an LED or buzzer warning indicator.
Protections are provided against open-circuit, short-circuit or faulty batteries.
The device is primarily designed to control two batteries in series. The number of cells can be extended by using a tap.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA1088T	16	SO16	plastic	SOT162A

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
V_6	supply voltage	charge	5.5	-	31.0	V
I_6	supply current	charge	-	-	19	mA
I_{10}	supply current	discharge	-	-	12	mA
I_{10}	stand by current		-	-	10	µA
I_1	SMPS transistor bias current		-	–2	-	mA
V_2-V_3	saturation voltage emitter switch	I_2 = 350 mA	0.9	-	1.4	V
V_{10}	battery voltage range	2 cells	1.8	-	4.0	V
V_{11}	threshold battery LOW indication		1.17	-	1.33	V
$I_{13,14}$	LED output currents	$V_{13,14}$ = 0.5 V	21	30	39	mA
V_{10}	voltage range of battery full detection		2.3	-	4.3	V
V_{10}	threshold for full indication		-	–22	-	mV

Hands-Free IC TEA1093; TEA1093T

FEATURES

- Line powered supply with:
  adjustable stabilized supply voltage
  power down function
- Microphone channel with:
  externally adjustable gain
  microphone mute function
- Loudspeaker channel with:
  externally adjustable gain
  dynamic limiter to prevent distortion
  rail-to-rail output stages for single-ended or bridge-tied load drive
  logarithmic volume control via linear potentiometer
  loudspeaker mute function
- Duplex controller consisting of:
  signal envelope and noise envelope monitors for both channels with:
    externally adjustable sensitivity
    externally adjustable signal envelope time constant
    externally adjustable noise envelope time constant
  decision logic with:
    externally adjustable switch-over timing
    externally adjustable idle mode timing
    dial tone detector in receive channel
  voice switch control with:
    adjustable switching range
    constant sum of gain during switching
    constant sum of gain at different volume settings

APPLICATIONS

- Line powered telephone sets with hands-free/listening-in functions.

GENERAL DESCRIPTION

The TEA1093; TEA1093T is a bipolar circuit intended for use in line-powered telephone sets. In conjunction with a member of the TEA1060 family transmission circuits, the device offers a hands-free function for line powered telephone sets. It incorporates a supply, a microphone amplifier, a loudspeaker amplifier and a duplex controller with signal and noise monitors on both channels.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA1093	28	DIL	plastic	SOT117N
TEA1093T	28	SOL	plastic	SOT136A

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{SUP}	operating input current on pin SUP		6.8	–	140	mA
V_{BB}	stabilized supply voltage		3.45	3.6	3.75	V
I_{BB}	current consumption from pin V_{BB} in power-down condition	PD = HIGH; V_{BB} = 3.6 V	–	400	550	µA
I_{SUP}	current consumption from pin SUP in power-down condition	PD = HIGH; V_{SUP} = 4.5 V	–	55	75	µA
A_{tx}	voltage gain from MIC to MOUT in transmit mode	V_{MIC} = 1 mV (RMS); R_{GAT} = 30.1 kΩ	13.3	15	16.7	dB
ΔA_{txr}	gain adjustment with R_{GAT}		−10	–	+10	dB
A_{rx}	voltage gain in receive mode	V_{RIN} = 20 mV (RMS); R_{GAR} = 66.5 kΩ; R_L = 50 Ω				
	from RIN1-RIN2 to LSP1 or LSP2, single-ended load		16	18	20	dB
	from RIN1-RIN2 to LSP1-LSP2, bridge-tied load		22	24	26	dB
ΔA_{rxr}	gain adjustment with R_{GAR}		−15	–	+15	dB
$V_{O(p-p)}$	bridge-tied load (peak-to-peak value)	V_{RIN} = 150 mV (RMS); R_L = 33 Ω; note 1	–	5.15	–	V
SWRA	switching range		37	40	43	dB
ΔSWRA	switching range adjustment with R_{SWR} referred to R_{SWR} = 365 kΩ		−40	–	+12	dB
T_{amb}	operating ambient temperature		−25	–	+75	°C

Note to the quick reference data

1. Corresponds to 100 mW output power.

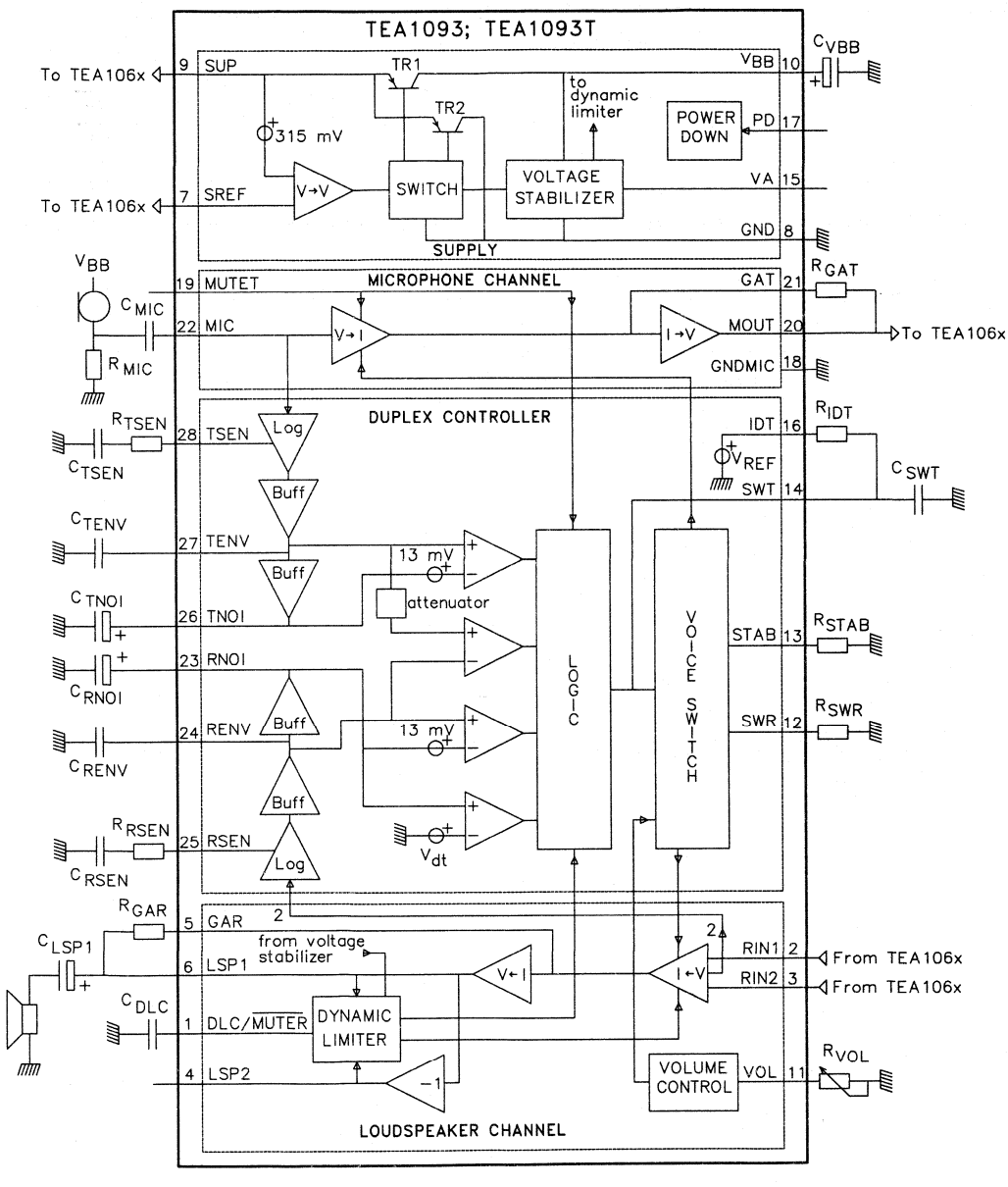


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
DLC/$\overline{\text{MUTER}}$	1	dynamic limiter timing adjustment, receiver channel mute input
RIN1	2	receiver amplifier input 1
RIN2	3	receiver amplifier input 2
LSP2	4	loudspeaker amplifier output 2
GAR	5	receiver gain adjustment
LSP1	6	loudspeaker amplifier output 1
SREF	7	supply reference input
GND	8	ground reference
SUP	9	supply input
V_{BB}	10	supply output
VOL	11	receiver volume adjustment
SWR	12	switching range adjustment
STAB	13	reference current adjustment
SWT	14	switch-over timing adjustment
VA	15	V_{BB} voltage adjustment
IDT	16	idle mode timing adjustment
PD	17	power-down input
GNDMIC	18	ground reference for the microphone amplifier
MUTET	19	transmit channel mute input
MOUT	20	microphone amplifier output
GAT	21	microphone gain adjustment
MIC	22	microphone input
RNOI	23	receive noise envelope timing adjustment
RENV	24	receive signal envelope timing adjustment
RSEN	25	receive signal envelope sensitivity adjustment
TNOI	26	transmit noise envelope timing adjustment
TENV	27	transmit signal envelope timing adjustment
TSEN	28	transmit signal envelope sensitivity adjustment

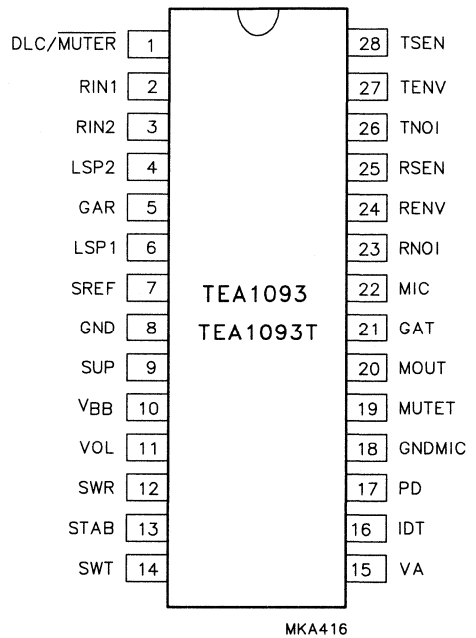


Fig.2 Pin configuration.

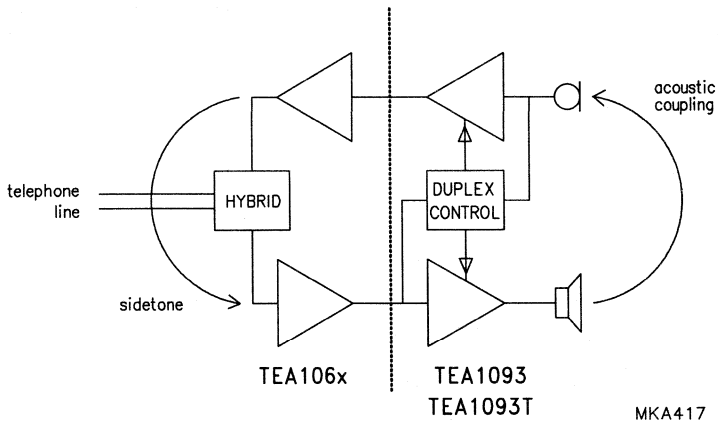


Fig.3 Hands-free telephone set principle.

FUNCTIONAL DESCRIPTION

The values given in this chapter are typical values except when otherwise specified.

A principle diagram of the TEA106x is shown on the left side of Fig.3. The TEA106x is a transmission circuit of the TEA1060 family intended for hand-set operation. It incorporates a receiving amplifier for the earpiece, a transmit amplifier for the microphone and a hybrid. For more details on the TEA1060 family, please refer to data handbook IC03. The right side of Fig.3 shows a principle diagram of the TEA1093; TEA1093T, a hands-free add-on circuit with a microphone amplifier, a loudspeaker amplifier and a duplex controller.

As can be seen from Fig.3, a loop is formed via the sidetone network in the transmission circuit and the acoustic coupling between loudspeaker and microphone of the hands-free circuit. When this loop gain is greater than 1, howling is introduced. In a full duplex application, this would be the case. The loop-gain has to be much lower than 1 and therefore has to be decreased to avoid howling. This is achieved by the duplex controller. The duplex controller of the TEA1093; TEA1093T detects which channel has the 'largest' signal and then controls the gains of the microphone amplifier and the loudspeaker amplifier so that the sum of the gains remains constant. As a result, the circuit can be in three stable modes:

1. Transmit mode (Tx mode): the gain of the microphone amplifier is at its maximum and the gain of the loudspeaker amplifier is at its minimum.
2. Receive mode (Rx mode): the gain of the loudspeaker amplifier is at its maximum and the gain of the microphone amplifier is at its minimum.
3. Idle mode: the gain of the amplifiers is halfway between their maximum and minimum value.

The difference between the maximum gain and minimum gain is called the switching range.

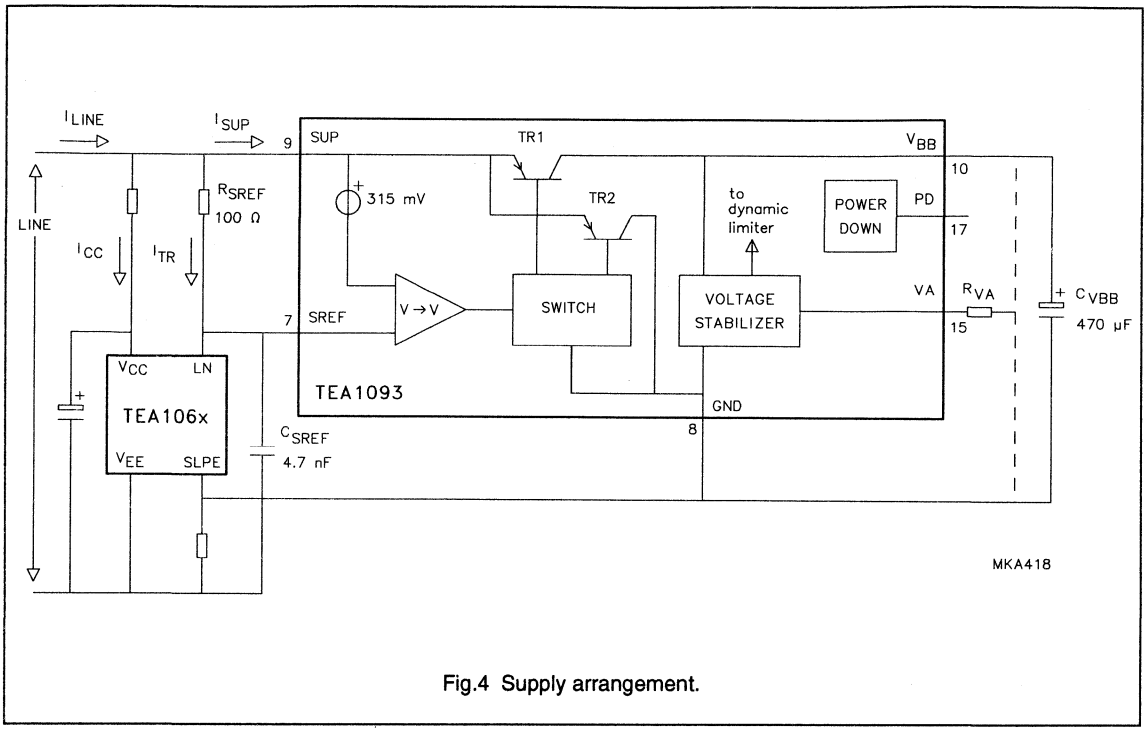


Fig.4 Supply arrangement.

Supply pins: SUP, SREF, V_{BB}, GND, VA and PD

As can be seen from Fig.4, the line current is divided between the speech-transmission circuit ($I_{TR} + I_{CC}$) and the TEA1093; TEA1093T circuit (I_{SUP}). It can be shown that:

$I_{SUP} = I_{LINE} - I_{TR} - I_{CC}$

Where:

$I_{TR} = V_{SUP\text{-}SREF}/R_{SREF}$

$V_{SUP\text{-}SREF} = 315$ mV

$R_{SREF} = 100\ \Omega$

$I_{CC} \approx 1$ mA

It follows that $I_{SUP} \approx I_{LINE} - 4$ mA.

The TEA1093; TEA1093T stabilizes its own supply voltage of 3.6 V at V_{BB}. The voltage on V_{BB} can be adjusted by means of an external resistor R_{VA}. When R_{VA} is connected between pin VA and GND, the voltage on V_{BB} is increased, when connected between pin VA and V_{BB}, it is decreased. This is shown in Fig.5. A capacitor of 4.7 nF (C_{SREF}) is required to ensure stability of the supply block. When V_{SUP} is greater than V_{BB} + 0.4 V, the current I_{SUP} is supplied to V_{BB} via TR1. When V_{SUP} is less, the current is shunted to GND via TR2, which prevents distortion on the line.

To reduce current consumption during pulse dialling or register recall (flash), the TEA1093; TEA1093T is provided with a power-down (PD) input. When the voltage on PD is HIGH, the current consumption from SUP is 55 µA and from V_{BB} it is 400 µA. Therefore a capacitor of 470 µF (C_{VBB}) is sufficient to power the TEA1093; TEA1093T during pulse dialling.

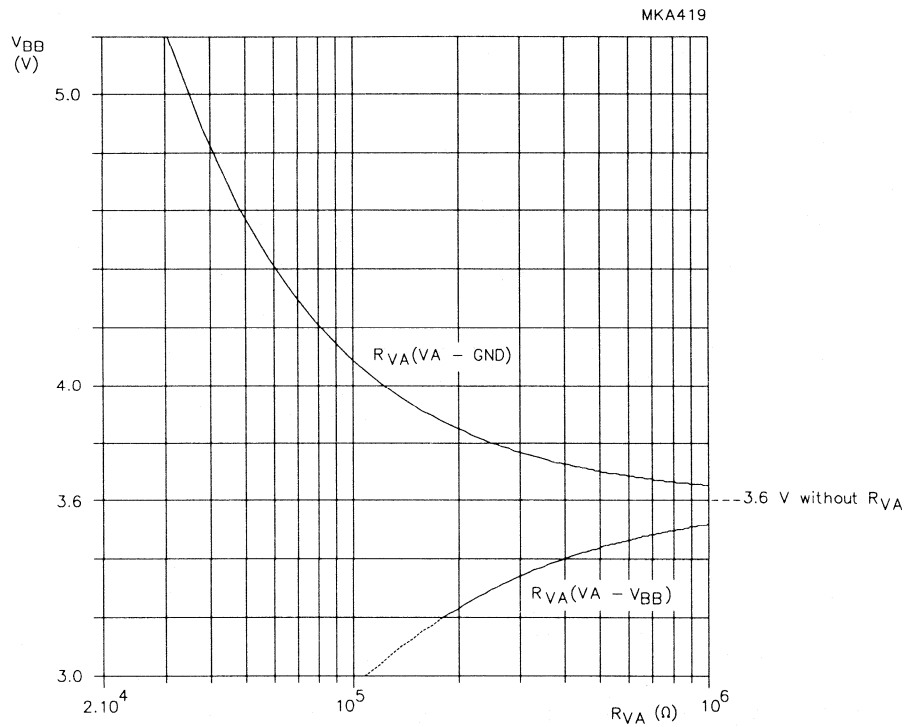


Fig.5 V_{BB} as a function of R_{VA}.

Microphone channel pins: MIC, GAT, MOUT, GNDMIC and MUTET

The TEA1093; TEA1093T has an asymmetrical microphone input MIC with an input resistance of 20 kΩ. The gain of the input stage varies according to the mode of the TEA1093; TEA1093T. In the transmit mode, the gain is at its maximum; in the receive mode, it is at its minimum and in the idle mode, it is halfway between maximum and minimum. Switch-over from one mode to the other is smooth and click-free. The output capability at pin MOUT is 20 μA (RMS).

In the transmit mode, the overall gain of the microphone amplifier (from pin MIC to MOUT) can be adjusted from 5 dB up to 25 dB to suit application specific requirements. The gain is proportional to the value of R_{GAT} and equals 15 dB typical with R_{GAT} = 30.1 kΩ.

A capacitor must be connected in parallel with R_{GAT} to ensure stability of the microphone amplifier. Together with R_{GAT}, it also provides a first order low-pass filter.

By applying a HIGH level on pin MUTET, the microphone amplifier is muted and the TEA1093; TEA1093T is automatically forced into the receive mode.

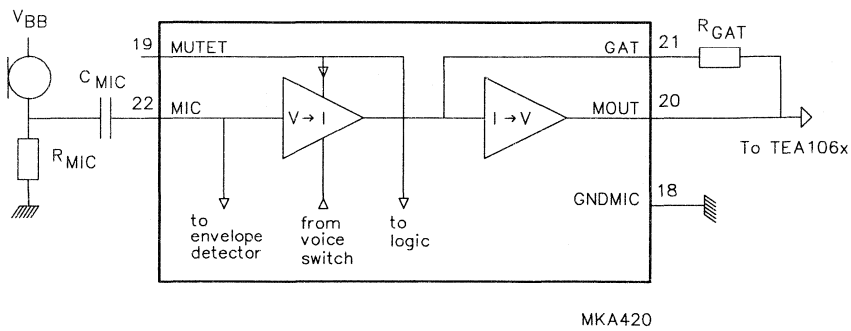


Fig.6 Microphone channel.

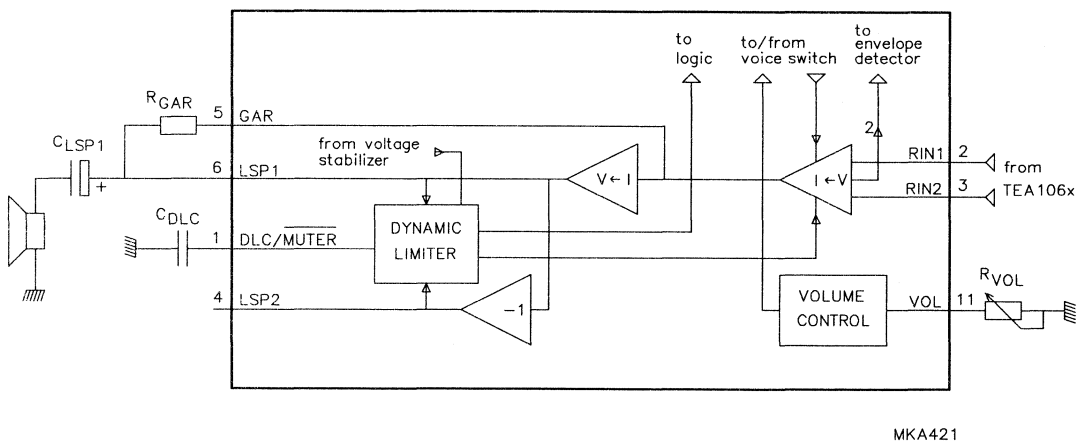


Fig.7 Loudspeaker channel.

Loudspeaker channel

LOUDSPEAKER AMPLIFIERS PINS: RIN1, RIN2, GAR, LSP1 AND LSP2

The TEA1093; TEA1093T has symmetrical inputs for the loudspeaker amplifier with an input resistance of 40 kΩ between RIN1 and RIN2 (twice 20 kΩ). The input stage can accommodate signals up to 390 mV (RMS) at room temperature for 2% of total harmonic distortion (THD). The gain of the input stage varies according to the mode of the TEA1093; TEA1093T. In the receive mode, the gain is at its maximum; in the transmit mode, it is at its minimum and in the idle mode, it is halfway between maximum and minimum. Switch-over from one mode to the other is smooth and click-free. The rail-to-rail output stage is designed to power a loudspeaker which is connected as a single-ended load (between LSP1 and GND) or as a bridge-tied load (between LSP1 and LSP2).

In the receive mode, the overall gain of the loudspeaker amplifier can be adjusted from 3 dB up to 39 dB to suit application specific requirements. The gain from RIN1-RIN2 to LSP1 is proportional to the value of R_{GAR}

and equals 18 dB with R_{GAR} = 66.5 kΩ. The second output LSP2 is in opposite phase with LSP1. Therefore, in the basic application, the gain from RIN1-RIN2 to LSP1-LSP2 equals 24 dB typical with R_{GAR} = 66.5 kΩ. A capacitor connected in parallel with R_{GAR} can be used to provide a first order low-pass filter.

VOLUME CONTROL: PIN VOL

The loudspeaker amplifier gain can be adjusted with the potentiometer R_{VOL}. A linear potentiometer can be used to obtain logarithmic control on the gain of the loudspeaker amplifier. Each 950 Ω increase of R_{VOL} results in a gain loss of 3 dB. The maximum gain reduction with the volume control is internally limited to the switching range.

DYNAMIC LIMITER: PIN DLC/$\overline{\text{MUTER}}$

The dynamic limiter of the TEA1093; TEA1093T prevents clipping of the loudspeaker output stages and protects the functioning of the circuit when the supply conditions fall below a certain level.

Hard clipping of the loudspeaker output stages is prevented by rapidly reducing the gain when the output stages start to saturate. The time in which gain reduction is effected (clipping attack time) is a few ms. The circuit stays in the reduced gain mode until the peaks of the loudspeaker signals no longer cause saturation. The gain of the loudspeaker amplifier then returns to its normal value within the clipping release time (a few 100 ms). Both attack and release times are proportional to the value of the capacitor C_{DLC}. The total harmonic distortion of the loudspeaker output stages, in reduced gain mode, stays below 5% up to 10 dB (minimum) of input voltage overdrive (providing V_{RIN} is below 390 mV (RMS)).

When the supply conditions are below the required level, the gain of the loudspeaker amplifier is reduced in order to prevent the TEA1093; TEA1093T from malfunctioning. Only the gain of the loudspeaker amplifier is affected since it is considered to be the major power consuming part of the TEA1093; TEA1093T.

When the TEA1093; TEA1093T experiences a loss of current, the supply voltage V_{BB} decreases. In this event, the gain of the loudspeaker amplifier is slowly reduced (a few seconds). When the supply voltage continues to decrease and drops below an internal voltage threshold of 2.75 V, the gain of the loudspeaker amplifier is rapidly reduced (approximately 1 ms). When normal supply conditions are resumed, the gain of the loudspeaker amplifier is increased again. This system ensures that in the event of large continuous signals, all current is used to power the loudspeaker while the voltage on pin V_{BB} remains at its nominal value.

By forcing a level lower than 0.2 V on pin DLC/$\overline{\text{MUTER}}$, the loudspeaker amplifier is muted and the TEA1093; TEA1093T is automatically forced into transmit mode.

Duplex controller

SIGNAL AND NOISE ENVELOPE DETECTORS PINS: TSEN, TENV, TNOI, RSEN, RENV AND RNOI

The signal envelopes are used to monitor the signal level strength in both channels. The noise envelopes are used to monitor background noise in both channels. The signal and noise envelopes provide inputs for the decision logic. The signal and noise envelopes are shown in Fig.8.

For the transmit channel, the input signal at MIC is 40 dB amplified to TSEN. For the receive channel, the differential signal of RIN1-RIN2 is 0 dB amplified to RSEN. The signals from TSEN and RSEN are logarithmically compressed and buffered to TENV and RENV respectively. The sensitivity of the envelope detectors is set with R_{TSEN} and R_{RSEN}. The capacitors connected in series with the two resistors block any DC component and form a first order high-pass filter. In the basic application, see Fig.16, it is assumed that V_{MIC} = 1 mV (RMS) and V_{RIN} = 100 mV (RMS) nominal and both R_{TSEN} and R_{RSEN} have a value of 10 kΩ. With the value of C_{TSEN} and C_{RSEN} at 100 nF, the cut-off frequency is at 160 Hz.

The buffer amplifiers leading the compressed signals to TENV and RENV have a maximum source current of 120 μA and a maximum sink current of 1 μA. Together with the capacitor C_{TENV} and C_{RENV}, the timing of the signal envelope monitors can be set. In the basic application, the value of both capacitors is 470 nF. Because of the logarithmic compression, each 6 dB signal increase means 18 mV increase of the voltage on the envelopes TENV or RENV at room temperature. Thus, timings can be expressed in dB/ms. At room temperature, the 120 μA sourced current corresponds to a maximum rise-slope of the signal envelope of 85 dB/ms. This is enough to track normal speech signals. The 1 μA current sunk by TENV or RENV corresponds to a maximum fall-slope of 0.7 dB/ms. This is enough for a smooth envelope and also eliminates the effect of echoes on switching behaviour.

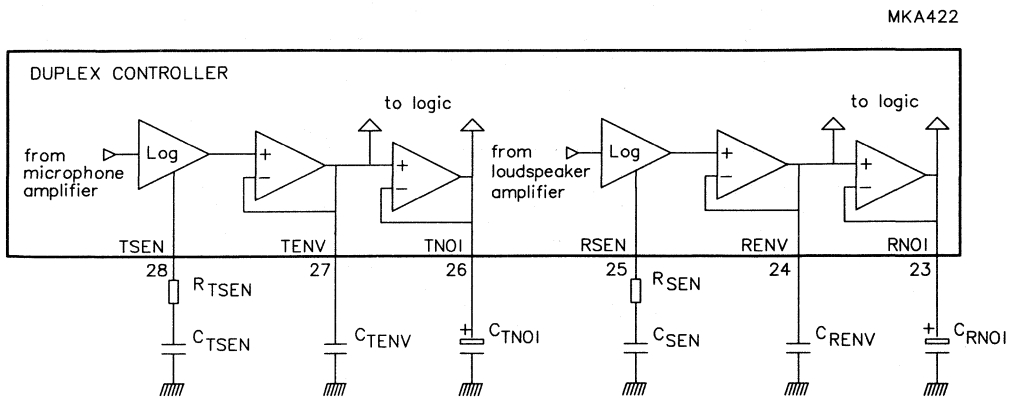


Fig.8 Signal and noise envelope detectors.

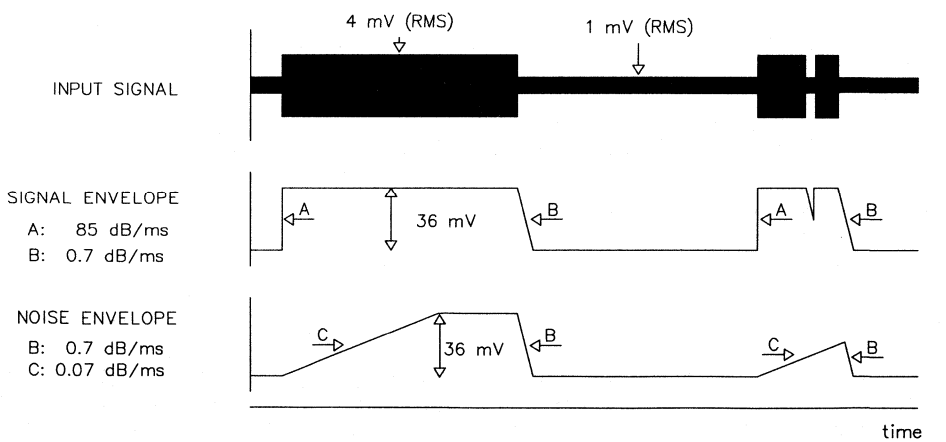


Fig.9 Signal and noise envelope waveform.

MKA423.1

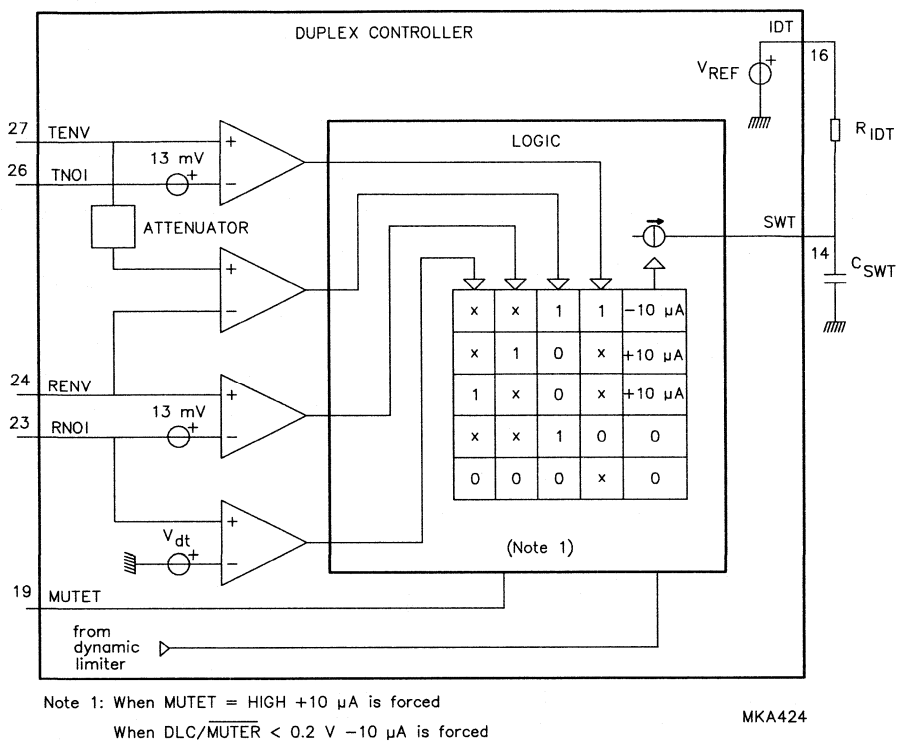


Fig.10 Decision logic.

To determine the noise level, the signal on TENV and RENV are buffered to TNOI and RNOI. These buffers have a maximum source current of 1 µA and a maximum sink current of 120 µA . Together with the capacitors C_{TNOI} and C_{RNOI}, the timing can be set. In the basic application of Fig.16, the value of both capacitors is 4.7 µF. At room temperature, the 1 µA sourced current corresponds to a maximum rise-slope of the noise envelope of approximately 0.07 dB/ms. This is small enough to track background noise and not to be influenced by speech bursts. The 120smu;A current that is sunk corresponds to a maximum fall-slope of approximately 8.5 dB/ms. However, during the decrease of the signal envelope, the noise envelope tracks the signal envelope so it will never fall faster than approximately 0.7 dB/ms. The behaviour of the signal envelope and noise envelope monitors is illustrated in Fig.9.

Decision logic pins: IDT and SWT

The TEA1093; TEA1093T selects its mode of operation (transmit, receive or idle mode) by comparing the signal and the noise envelopes of both channels. This is executed by the decision logic. The resulting voltage on pin SWT is the input for the voice-switch.

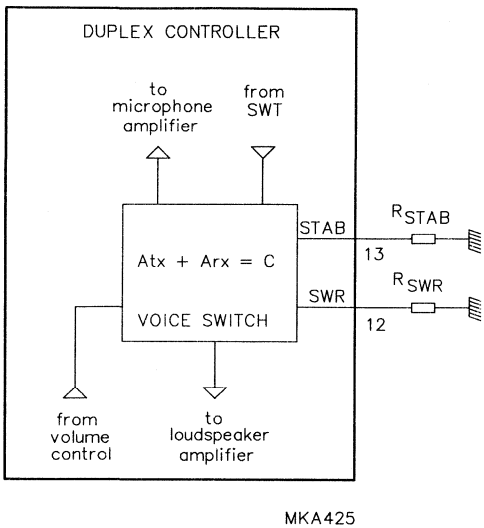


Fig.11 Voice switch.

To facilitate the distinction between signal and noise, the signal is considered as speech when its envelope is more than 4.3 dB above the noise envelope. At room temperature, this is equal to a voltage difference $V_{ENV-NOI}$ = 13 mV. This so called speech/noise threshold is implemented in both channels.

The signal on MIC contains both speech and the signal coming from the loudspeaker (acoustic coupling). When receiving, the contribution from the loudspeaker overrules the speech. As a result, the signal envelope on TENV is formed mainly by the loudspeaker signal. To correct this, an attenuator is connected between TENV and the TENV/RENV comparator. Its attenuation equals that applied to the microphone amplifier.

When a dial tone is present on the line, without monitoring, the tone would be recognized as noise because it is a signal with a constant amplitude. This would cause the TEA1093; TEA1093T to go into the idle mode and the user of the set would hear the dial tone fade away. To prevent this, a dial tone detector is incorporated which, in standard application, does not consider input signals at RIN1-RIN2 as noise when they have a level greater than 127 mV (RMS). This level is proportional to R_{RSEN}.

As can be seen from Fig.10, the output of the decision logic is a current source. The logic table gives the relationship between the inputs and the value of the current source. It can charge or discharge the capacitor C_{SWT} with a current of 10 µA (switch-over). If the current is zero, the voltage on SWT becomes equal to the voltage on IDT via the high-ohmic resistor R_{IDT} (idling). The resulting voltage difference between SWT and IDT determines the mode of the TEA1093; TEA1093T and can vary between –400 mV and +400 mV:

$V_{SWT-IDT} < -180$ mV (transmit mode)
$V_{SWT-IDT} = 0$ mV (idle mode)
$V_{SWT-IDT} > +180$ mV (receive mode)

The switch-over timing can be set with C_{SWT}, the idle mode timing with C_{SWT} and R_{IDT}. In the basic application given in Fig.16, C_{SWT} is chosen at 220 nF and R_{IDT} is chosen 2.2 MΩ. This enables a switch-over time from transmit to receive mode or vice-versa of approximately 13 ms (580 mV swing on SWT). The switch-over time from idle mode to transmit mode or receive mode is approximately 4 ms (180 mV swing on SWT).

The switch-over time from receive mode or transmit mode to idle mode is equal to 4 x R_{IDT} C_{SWT} and is approximately 2 s (idle mode time).

The inputs MUTET and DLC/$\overline{\text{MUTER}}$ overrule the decision logic. When MUTET goes HIGH, the capacitor C_{SWT} is charged with 10 µA resulting in the receive mode. When the voltage on pin DLC/$\overline{\text{MUTER}}$ is made lower than 0.2 V, the capacitor is discharged with 10 µA resulting in the transmit mode.

VOICE-SWITCH PINS: STAB AND SWR

A diagram of the voice-switch is illustrated in Fig.11. With the voltage on SWT, the TEA1093; TEA1093T voice-switch regulates the gains of the transmit and the receive channel so that the sum of both is kept constant.

In the transmit mode, the gain of the microphone amplifier is at its maximum and the gain of the loudspeaker amplifier is at its minimum. In the receive mode, the opposite applies. In the idle mode, both microphone and loudspeaker amplifier gain are halfway.

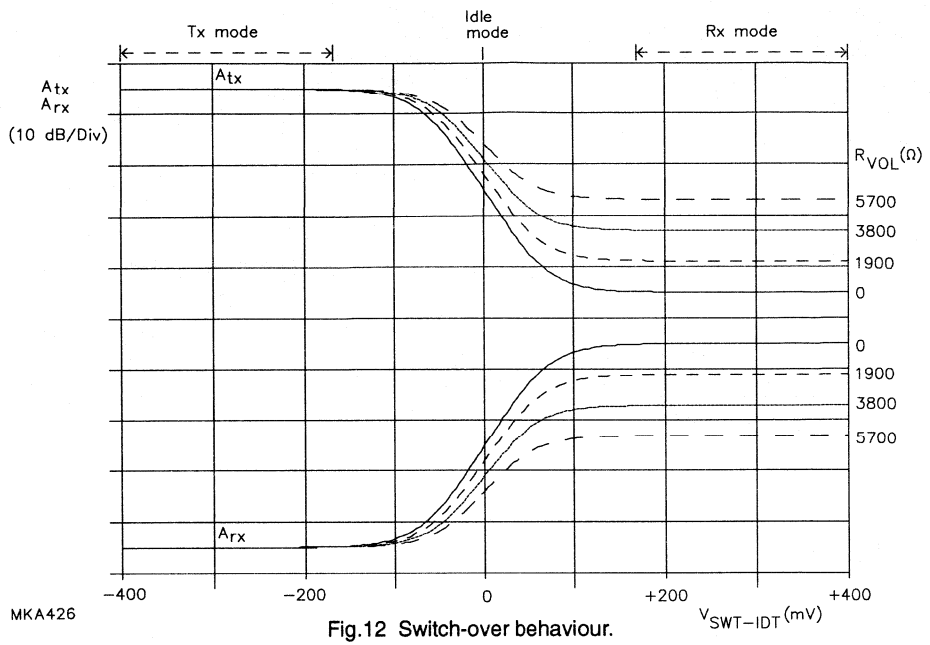


Fig.12 Switch-over behaviour.

The difference between maximum and minimum is the so called switching range. This range is determined by the ratio of R_{SWR} and R_{STAB} and is adjustable between 0 and 52 dB. R_{STAB} should be 3.65 kΩ and sets an internally used reference current. In the basic application diagram given in Fig.16, R_{SWR} is 365 kΩ which results in a switching range of 40 dB. The switch-over behaviour is illustrated in Fig.12.

In the receive mode, the gain of the loudspeaker amplifier can be reduced using the volume control. Since the voice-switch keeps the sum of the gains constant, the gain of the microphone amplifier is increased at the same time (see dashed curves in Fig.12). In the transmit mode, however, the volume control has no influence on the gain of the microphone amplifier or the gain of the loudspeaker amplifier. Consequently, the switching range is reduced when the volume is reduced. At maximum reduction of volume, the switching range becomes 0 dB.

When the gain of the loudspeaker amplifier is reduced by the volume control to the lowest possible value, the switching range becomes 0 dB.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_n	maximum voltage on all pins; except pins SUP, SREF, V_{BB}, RIN1 and RIN2		$V_{GND} - 0.4$	$V_{BB} + 0.4$	V
V_{RIN}	maximum voltage on pin RIN1 or RIN2		$V_{GND} - 1.2$	$V_{BB} + 0.4$	V
V_{BB}	maximum voltage on pin V_{BB}		$V_{GND} - 0.4$	12	V
V_{SREF}	maximum voltage on pin SREF		$V_{GND} - 0.4$	$V_{SUP} + 0.4$	V
V_{SUP}	maximum voltage on pin SUP		$V_{GND} - 0.4$	12	V
I_{SUP}	maximum current in pin SUP	see also Figs 13 and 14	–	140	mA
P_{tot}	total power dissipation	see also Figs 13 and 14; T_{amb} = 75 °C			
	TEA1093		–	910	mW
	TEA1093T		–	670	mW
T_{stg}	storage temperature		–40	+125	°C
T_{amb}	operating ambient temperature		–25	+75	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j-a}$	from junction to ambient in free air	
	TEA1093	55 K/W
	TEA1093T	75 K/W

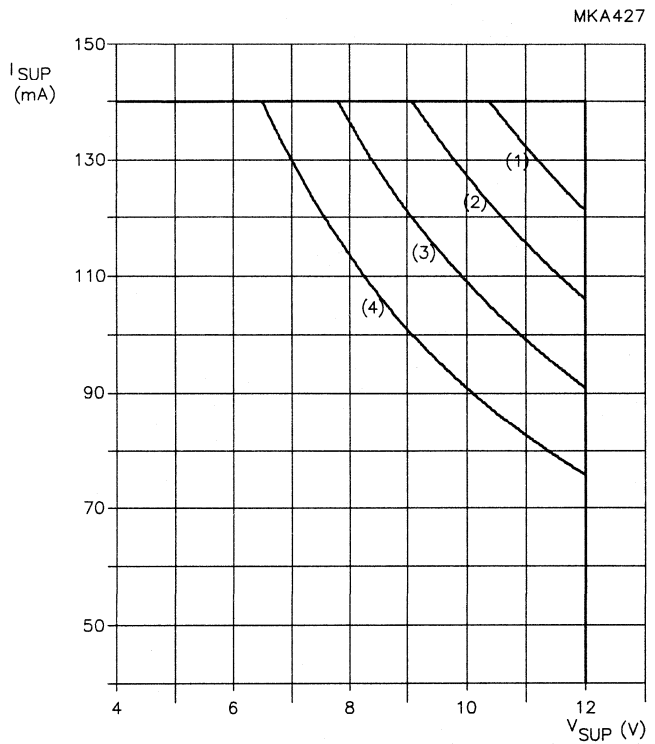


Fig.13 TEA1093 safe operating area.

LINE	T_{amb}	P_{tot}
(1)	45 °C	1.45 W
(2)	55 °C	1.27 W
(3)	65 °C	1.09 W
(4)	75 °C	0.91 W

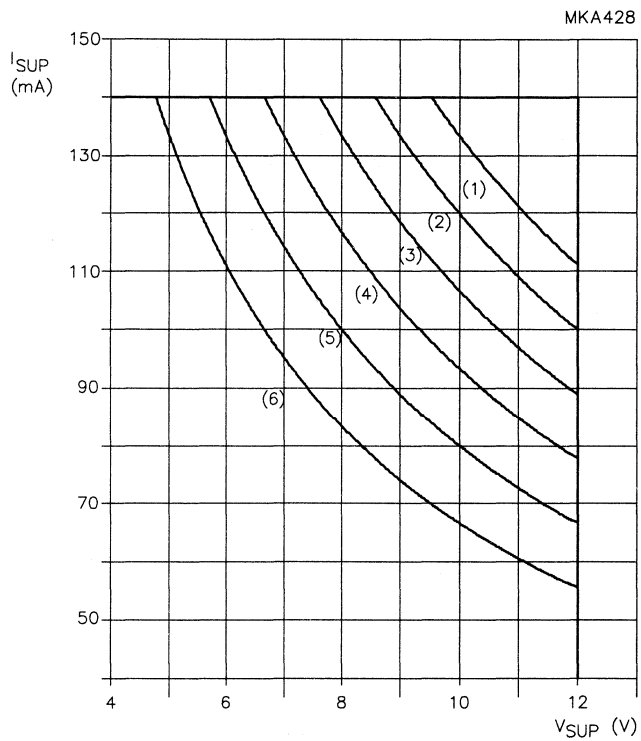


Fig.14 TEA1093T safe operating area.

LINE	T_{amb}	P_{tot}
(1)	25 °C	1.33 W
(2)	35 °C	1.20 W
(3)	45 °C	1.07 W
(4)	55 °C	0.93 W
(5)	65 °C	0.80 W
(6)	75 °C	0.67 W

CHARACTERISTICS

V_{SREF} = 4.2 V; V_{GND} = 0 V; I_{SUP} = 15 mA; V_{SUP} = 0 V (RMS); f = 1 kHz; T_{amb} = 25 °C; PD = LOW; MUTET = LOW; R_L = 50 Ω; R_{VOL} = 0 Ω; measured in test circuit of Fig.15 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (VA, SREF, SUP, V_{BB}, GND and PD)						
V_{BB}	stabilized supply voltage		3.45	3.6	3.75	V
ΔV_{BBi}	V_{BB} variation with I_{SUP}	I_{SUP} = 15 to 140 mA	–	20	–	mV
ΔV_{BBt}	V_{BB} variation with temperature referred to 25 °C	T_{amb} = −25 to +75 °C	–	±20	–	mV
V_{BB}	V_{BB} adjustment; R_{VA}					
	between VA and V_{BB}	R_{VA} = 180 kΩ	3.0	3.2	3.4	V
	between VA and GND	R_{VA} = 56 kΩ; V_{SREF} = 4.9 V	4.25	4.5	4.75	V
I_{SUP}	minimum operating current		–	5.5	6.8	mA
$V_{SUP} - V_{BB}$	minimum DC voltage drop between pin SUP and V_{BB}		0.4	–	–	V
$V_{SUP-SREF}$	internal reference voltage		275	315	355	mV
THD	total harmonic distortion of AC signal on SUP	V_{SUP} =1 V (RMS)	–	0.5	–	%
Power-down input PD						
V_{IL}	LOW level input voltage		V_{GND} − 0.4	–	0.3	V
V_{IH}	HIGH level input voltage		1.5	–	V_{BB} + 0.4	V
I_{PD}	input current	PD = HIGH	–	2.5	5	µA
I_{SUP}	current consumption from pin SUP in power down condition	PD = HIGH; V_{SUP} = 4.5 V	–	55	75	µA
I_{BB}	current consumption from pin VBB in power down condition	PD = HIGH; V_{BB} = 3.6 V	–	400	550	µA
Microphone channel (MIC, GAT, MOUT, MUTET and GNDMIC)						
MICROPHONE AMPLIFIER						
$\|Z_i\|$	input impedance between pin MIC and GND		17	20	23	kΩ
G_{tx}	voltage gain from pin MIC to MOUT in transmit mode	V_{MIC} = 1 mV (RMS)	13.3	15	16.7	dB
ΔG_{txr}	gain adjustment with R_{GAT}		−10	–	+10	dB
ΔG_{txt}	gain variation with temperature referred to 25 °C	V_{MIC} = 1 mV (RMS); T_{amb} = −25 to +75 °C	–	±0.3	–	dB
ΔG_{txf}	gain variation with frequency referred to 1 kHz	V_{MIC} = 1 mV (RMS); f = 300 to 3400 Hz	–	±0.3	–	dB
V_{notx}	noise output voltage at pin MOUT; pin MIC connected to GND through 200 Ω in series with 10 µF	psophometrically weighted (P53 curve)	–	−100	–	dBmp

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
TRANSMIT MUTE INPUT MUTET						
V_{IL}	LOW level input voltage		V_{GND} − 0.4	−	0.3	V
V_{IH}	HIGH level input voltage		1.5	−	V_{BB} + 0.4	V
I_{MUTET}	input current	MUTET = HIGH	−	2.5	5	µA
ΔG_{txm}	gain reduction with MUTET active	MUTET = HIGH	−	80	−	dB
Loudspeaker channel (RIN1, RIN2, GAR, LSP1, LSP2 and DLC/$\overline{\text{MUTER}}$)						
LOUDSPEAKER AMPLIFIER						
$\lvert Z_i \rvert$	input impedance					
	between pin RIN1 or RIN2 and GND		17	20	23	kΩ
	between pin RIN1 and RIN2		34	40	46	kΩ
G_{rx}	voltage gain in receive mode	V_{RIN} = 20 mV (RMS)				
	from RIN1-RIN2 to LSP1-LSP2; bridge-tied load (BTL)		22	24	26	dB
	from RIN1-RIN2 to LSP1 or LSP2; single-ended load (SEL)		16	18	20	dB
ΔG_{rxr}	gain adjustment with R_{GAR}		−15	−	+15	dB
ΔG_{rxt}	gain variation with temperature referred to 25 °C	V_{RIN} = 20 mV (RMS); T_{amb} = −25 to 75°C	−	±0.3	−	dB
ΔG_{rxf}	gain variation with frequency referred to 1 kHz	V_{RIN} = 20 mV (RMS); f = 300 to 3400 Hz	−	±0.3	−	dB
$V_{RINM(RMS)}$	maximum input voltage between RIN1-RIN2 for 2% THD in input stage (RMS value)	R_{GAR} = 11.8 kΩ	−	390	−	mV
$V_{norx(RMS)}$	noise output voltage at pin LSP1 or LSP2, inputs RIN1 and RIN2 shorted through 200 Ω in series with 10 µF (RMS value)	psophometrically weighted (P53 curve)	−	80	−	µV
CMRR	common mode rejection ratio		−	50	−	dB
Δatt_{rxv}	attenuation variation related to ΔR_{VOL} = 950 Ω when total attenuation does not exceed the switching range		−	3	−	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
OUTPUT CAPABILITY						
$V_{O(p-p)}$	single-ended load (peak-to-peak value)	V_{RIN} = 150 mV (RMS)				
		I_{SUP} = 11 mA; note 1	1.2	1.45	–	V
		I_{SUP} = 16.5 mA; note 2	2.5	2.9	–	V
$V_{O(p-p)}$	bridge-tied load (peak-to-peak value)	V_{RIN} = 150 mV (RMS)				
		I_{SUP} = 27 mA; note 2	2.5	2.9	–	V
		I_{SUP} = 35 mA; note 3	3.5	4.0	–	V
		I_{SUP} = 62 mA; note 4; R_L = 33 Ω	–	5.15	–	V
DYNAMIC LIMITER						
t_{att}	attack time when V_{RIN} jumps from 20 mV to 20 mV + 10 dB	R_{GAR} = 374 kΩ; I_{SUP} = 20 mA	–	–	5	ms
t_{rel}	release time when V_{RIN} jumps from 20 mV + 10 dB to 20 mV	R_{GAR} = 374 kΩ; I_{SUP} = 20 mA	–	250	–	ms
THD	total harmonic distortion at V_{RIN} = 20 mV + 10 dB	R_{GAR} = 374 kΩ; I_{SUP} = 20 mA; $t > t_{att}$	–	0.9	5	%
V_{BBT}	V_{BB} limiter threshold		–	2.75	–	V
t_{attvbb}	attack time when V_{BB} jumps below V_{BBT}		–	1	–	ms
MUTE RECEIVE						
V_{DLCth}	voltage required on pin DLC/$\overline{\text{MUTER}}$ to obtain mute receive condition		V_{GND} – 0.4	–	0.2	V
I_{DLCth}	current sourced by pin DLC/$\overline{\text{MUTER}}$ in mute receive condition	V_{DLC} = 0.2 V	–	80	–	µA
ΔG_{rxm}	gain reduction in mute receive condition	V_{DLC} < 0.2 V	–	80	–	dB
Envelope and noise detectors (TSEN, TENV, RSEN and RENV)						
PREAMPLIFIERS						
G_{TSEN}	voltage gain from MIC to TSEN		38.3	40	41.7	dB
G_{RSEN}	voltage gain from RIN1-RIN2 to RSEN		–1.7	0	+1.7	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
LOGARITHMIC COMPRESSOR AND SENSITIVITY ADJUSTMENT						
D_{TSEN}	detection sensitivity on pin TSEN; voltage change on pin TENV when doubling the current from TSEN	I_{TSEN} = 0.8 to 160 μA	–	18	–	mV
D_{RSEN}	detection sensitivity on pin RSEN; voltage change on pin RENV when doubling the current from RSEN	I_{RSEN} = 0.8 to 160 μA	–	18	–	mV
SIGNAL ENVELOPE DETECTORS						
I_{srcENV}	maximum current sourced from pin TENV or RENV		–	120	–	μA
I_{snkENV}	maximum current sunk by pin TENV or RENV		0.8	1	1.2	μA
$V_{diffENV}$	voltage difference between pin RENV and TENV when 10 μA sourced from both RSEN and TSEN	envelope detectors tracking; note 5	–	±3	–	mV
NOISE ENVELOPE DETECTORS						
I_{srcNOI}	maximum current sourced from pin TNOI or RNOI		0.8	1	1.2	μA
I_{snkNOI}	maximum current sunk by pin TNOI or RNOI		–	120	–	μA
$V_{diffNOI}$	voltage difference between pin RNOI and TNOI when 5 μA sourced from both RSEN and TSEN	noise detectors tracking; note 5	–	±3	–	mV
DIAL TONE DETECTOR						
$V_{RINDT(RMS)}$	threshold level at pin RIN1-RIN2 (RMS value)		–	127	–	mV
Decision logic (IDT and SWT)						
SIGNAL RECOGNITION						
S/N_{rxth}	voltage between pin RENV and RNOI to switch-over from receive to idle mode	$V_{RIN} < V_{RINDT}$; note 6	–	13	–	mV
S/N_{txth}	voltage between pin TENV and TNOI to switch-over from transmit to idle mode	note 6	–	13	–	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SWITCH-OVER						
I_{srcSWT}	current sourced from pin SWT when switching to receive mode		8	10	12	µA
I_{snkSWT}	current sunk by pin SWT when switching to transmit mode		8	10	12	µA
$I_{idleSWT}$	current sourced from pin SWT in idle mode		–	0	–	µA
Voice switch (STAB and SWR)						
SWRA	switching range		37	40	43	dB
ΔSWRA	switching range adjustment with R_{SWR} referred to R_{SWR} = 365 kΩ		–40	–	12	dB
|ΔA|	gain variation from transmit mode to idle mode on both channels		18	20	22	dB
G_{tr}	gain tracking (G_{tx} + G_{rx}) during switching referred to idle mode		–	±0.5	–	dB

Notes to the characteristics

1. Corresponds to 5 mW output power.
2. Corresponds to 20 mW output power.
3. Corresponds to 40 mW output power.
4. Corresponds to 100 mW output power.
5. Corresponds to ±1 dB tracking.
6. Corresponds to 4.3 dB NOISE/SPEECH recognition level.

HANDLING

ESD according to MIL STD883C- Method 3015 (HBM 150 Ω, 100 pF), 3 pulses + and 3 pulses - on each pin versus ground.
Class 2: 2000 to 3999 V.

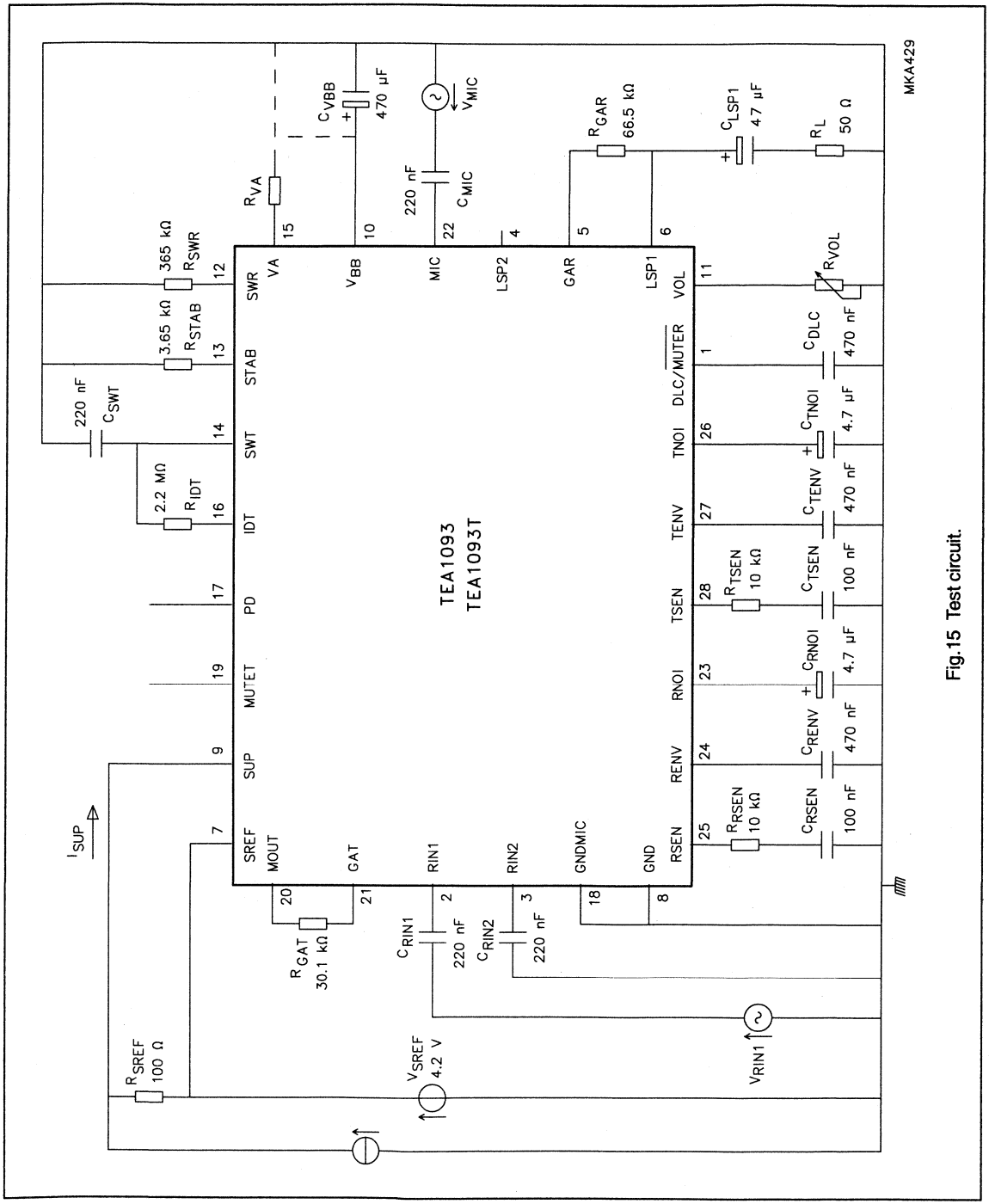


Fig.15 Test circuit.

APPLICATION INFORMATION

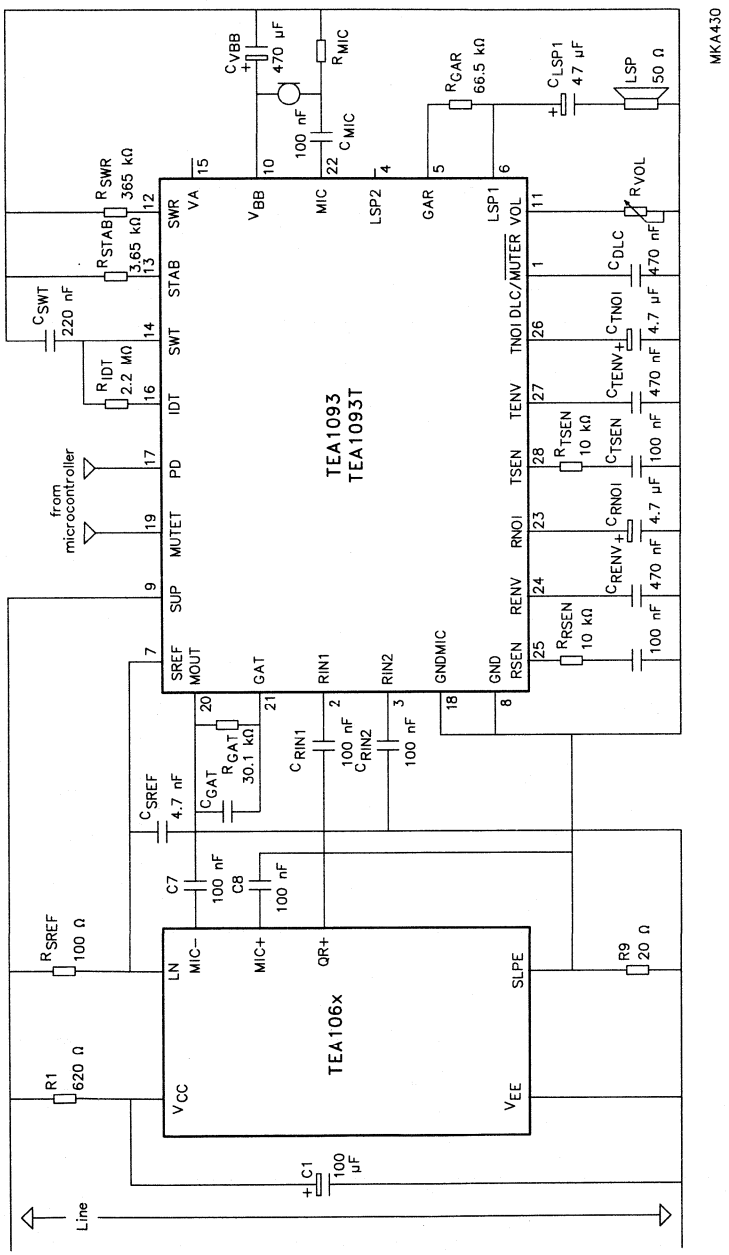


Fig.16 Basic application diagram.

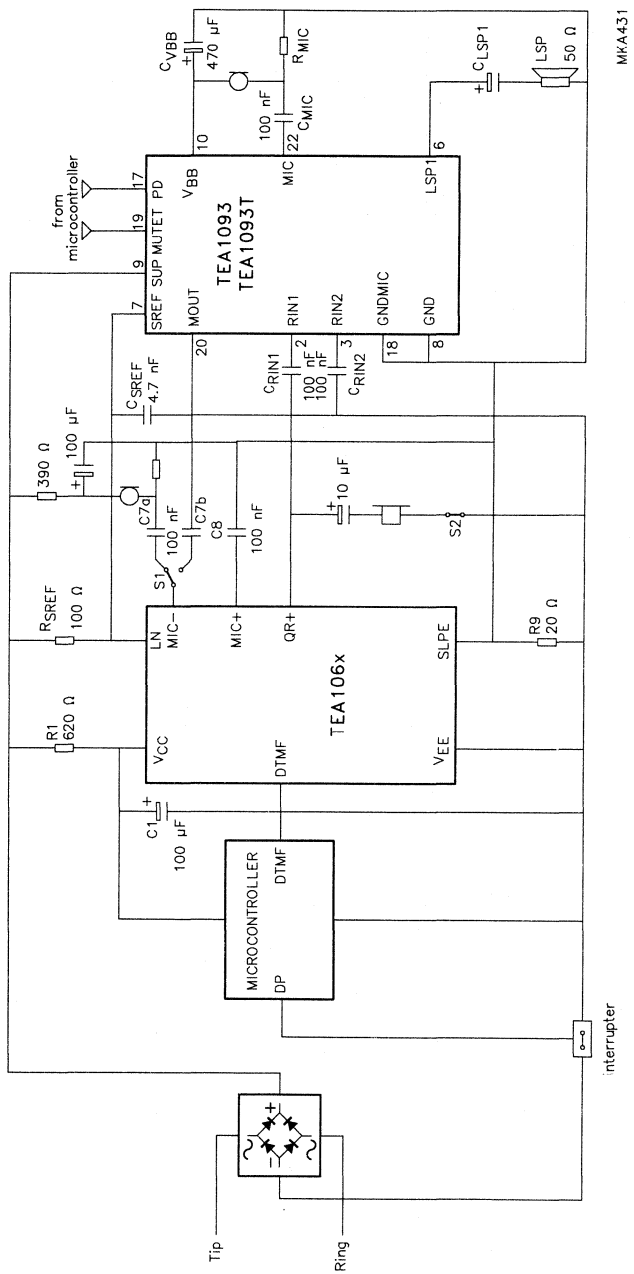


Fig.17 Application example.

Speech and listening-in IC TEA1096; TEA1096A

FEATURES

- Line interface functions with:
  Active set impedance (adjustable)
  Voltage regulator with adjustable DC voltage
  Low voltage circuit for parallel operation
- Interface to peripheral circuits with:
  Supply output for microcontroller
  Stabilized supply voltage (V_{BB}) for listening-in which is;
    available for peripheral circuits
    adjustable DC voltage
  (TEA1096 only)
  DTMF signal input
  Power-down input for pulse dialling
  Mute input to disable speech during dialling
- Microphone amplifier with:
  Symmetrical high impedance inputs
  External adjustable gain
  AGC line-loss compensation
  Dynamic limiter
  Microphone mute function
- Receiver amplifier with:
  External adjustable gain
  Confidence tone during dialling
  Double antisidetone circuit for long and short line
  AGC line-loss compensation
  Earpiece protection by soft clipping
- Listening-in circuit with:
  Loudspeaker amplifier
  Dynamic limiter to prevent distortion at any supply condition
  Volume control via a potentiometer
  Fixed gain of 35.5 dB
  Disable function
  Gain control input (TEA1096A only).

APPLICATIONS

- Line powered telephone sets with line monitoring and listening-in function.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA1096	28	DIL	plastic	SOT117N
TEA1096A	28	DIL	plastic	SOT117N
TEA1096T	28	SOL	plastic	SOT136A
TEA1096AT	28	SOL	plastic	SOT136A

GENERAL DESCRIPTION

The TEA1096; TEA1096A is a bipolar IC for use in line-powered telephone sets. The device offers speech/transmission function and a listening-in facility of the received line signal via the loudspeaker.

The device incorporates a line interface block, a microphone and DTMF amplifier, a receiving amplifier, a stabilized supply, a loudspeaker amplifier and a dynamic limiter in the transmission as well as in the listening-in channel.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{line}	line current operating range	normal condition with reduced performance	15 tbf	– –	140 15	mA mA
$I_{DD(NO)}$	current consumption from pin V_{DD} during normal operation	PD = LOW	–	2.2	–	mA
$I_{DD(PD)}$	current consumption from capacitor C_{VDD} in power-down conditions	PD = HIGH	–	150	tbf	µA
$I_{BB(PD)}$	current consumption from capacitor C_{VBB} in power-down conditions	PD = HIGH	–	340	tbf	µA
V_{SLPE}	stabilized voltage line interface		tbf	4.3	tbf	V
V_{DD}	supply voltage for speech and microcontroller	R_{VDD} = 390 Ω I_P = 0 mA I_P = 1 mA	 tbf tbf	 3.45 3.05	 tbf	 V V
V_{BB}	stabilized supply voltage		3.4	3.6	3.8	V
GV_{tx}	voltage gain from pin MICP, MICM to LN	v_{MIC} = 1 mV(RMS); R_{GAS} = 90.9 kΩ; I_{line} = 15 mA	51	52	53	dB
ΔG_{txr}	gain adjustment with R_{GAS}		−19	–	0	dB
G_{rx}	voltage gain from pin LN to QRP, QRM	v_{LN} = 50 mV(RMS); R_{GAR} = 90.9 kΩ; I_{line} = 15 mA	−3	−2	−1	dB
ΔG_{rxr}	gain adjustment with R_{GAR}		−12	–	8	dB
ΔG_{trx}	line loss compensation	R_{AGC} = 100 kΩ	5.6	6	6.4	
G_{tx}	voltage gain from pin LSI to QLS	v_{LSI} = 10 mV(RMS)	34	35.5	37	dB
$V_{LN(p-p)}$	maximum output voltage swing on pin LN (peak-to-peak value)		–	3.5	4.3	V
I_{line}	minimum input current	P_O = 20 mW(typ); R_{QLS} = 50 Ω	tbf	tbf	tbf	mA
T_{amb}	operating ambient temperature		−25	–	+70	°C

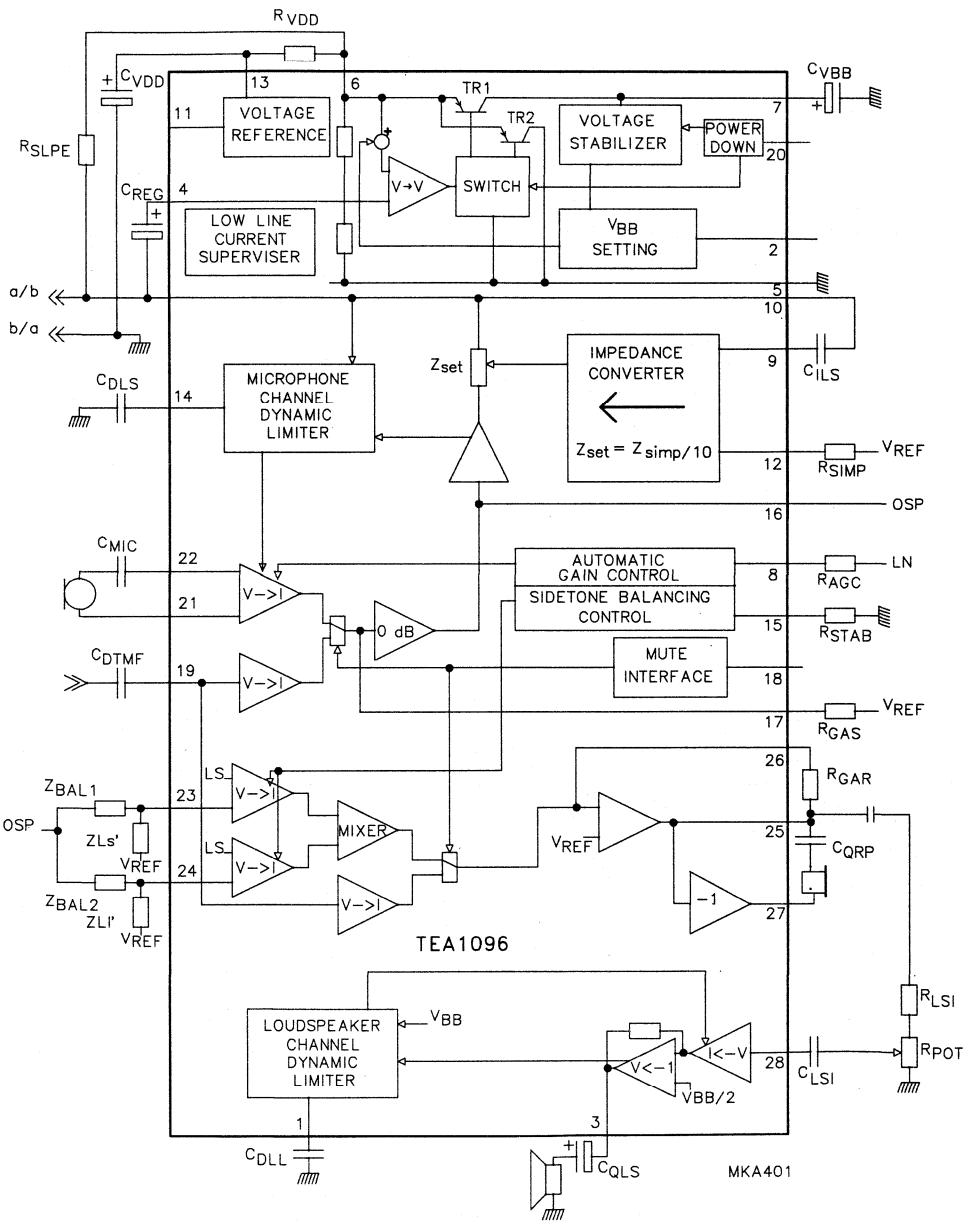


Fig.1 Block diagram (TEA1096).

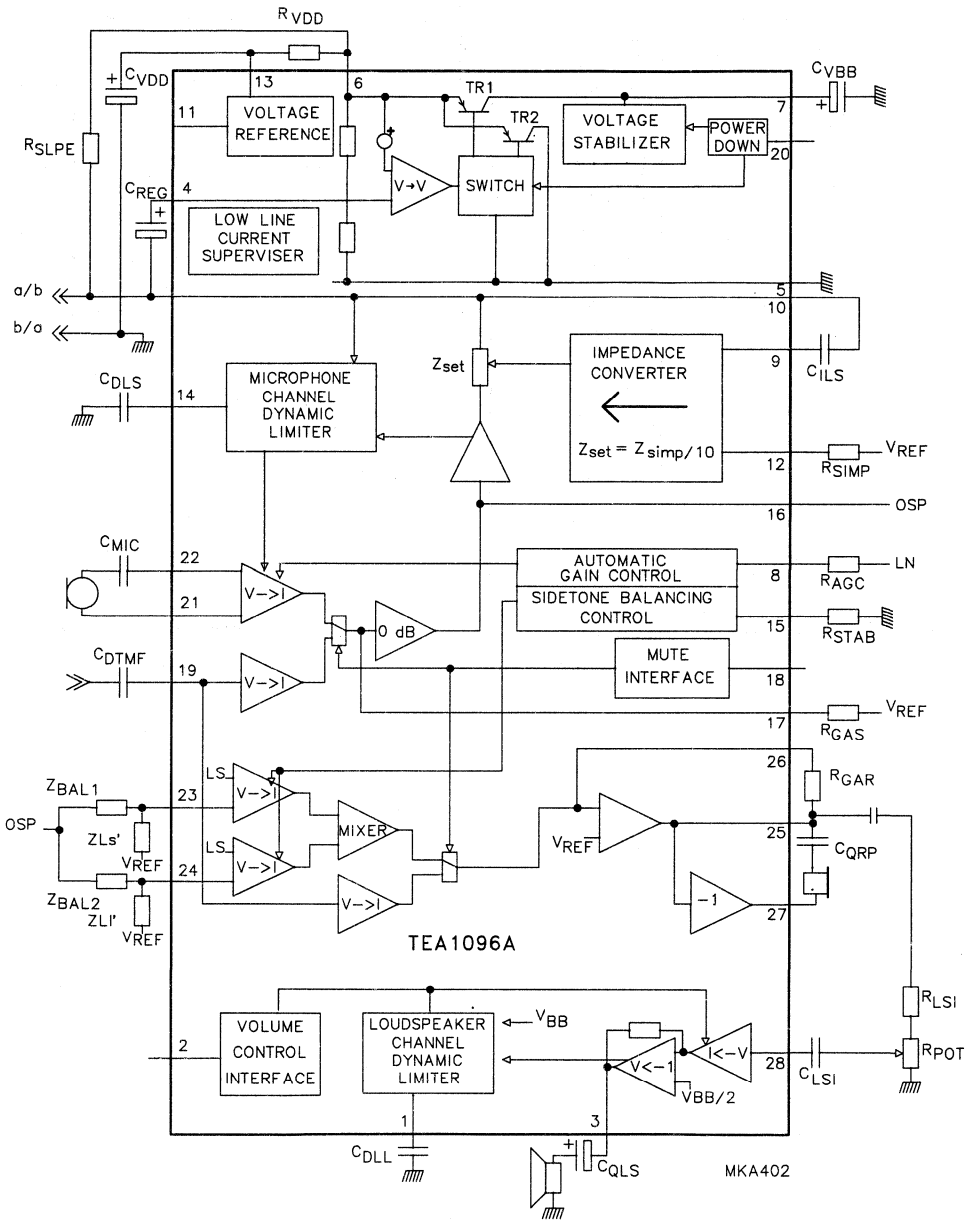


Fig.2 Block diagram (TEA1096A).

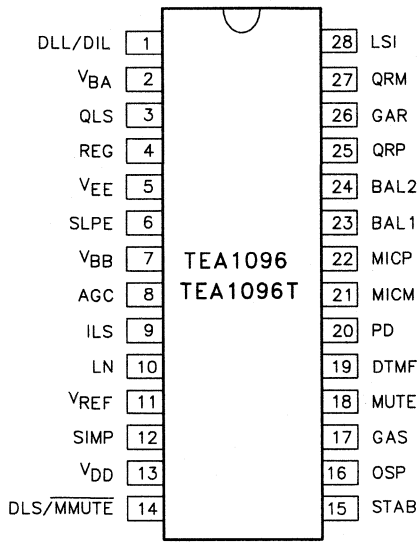


Fig.3 Pin configuration (TEA1096).

Fig.4 Pin configuration (TEA1096A).

PINNING

SYMBOL	PIN TEA1096	PIN TEA1096A	DESCRIPTION
DLL/DIL	1	1	dynamic limiter and disable input for loudspeaker amplifier
V_{BA}	2		V_{BB} voltage adjustment
VCI		2	volume control input for loudspeaker amplifier
QLS	3	3	loudspeaker amplifier output
REG	4	4	decoupling line voltage stabilizer
V_{EE}	5	5	negative line connection (ground reference)
SLPE	6	6	stabilized voltage, connection for slope resistor
V_{BB}	7	7	stabilized supply voltage
AGC	8	8	automatic gain control
ILS	9	9	input line signal
LN	10	10	positive line connection
V_{REF}	11	11	reference voltage output
SIMP	12	12	set impedance input
V_{DD}	13	13	supply voltage for speech part/peripherals
DLS/$\overline{\text{MMUTE}}$	14	14	dynamic limiter for sending and microphone mute
STAB	15	15	reference current adjustment
OSP	16	16	sending preamplifier output
GAS	17	17	sending gain adjustment
MUTE	18	18	mute input to select speech or DTMF dialling
DTMF	19	19	dual tone frequency input
PD	20	20	power-down input
MICM	21	21	inverting microphone amplifier input
MICP	22	22	non inverting microphone amplifier input
BAL1	23	23	connection for balance network 1
BAL2	24	24	connection for balance network 2
QRP	25	25	non inverting receiving amplifier output
GAR	26	26	receiving gain adjustment
QRM	27	27	inverting receiving amplifier output (no gain adjustment)
LSI	28	28	loudspeaker amplifier input

Battery monitor for NiCd and NiMH chargers

TEA1100; TEA1100T

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC11 OR DATA SHEET

FEATURES

- Accurate regulation of charge current settings in co-operation with a switched mode power supply
- Accurate detection of fully charged batteries by currentless battery voltage sensing
- Switch over from fast to normal charging when batteries are fully charged
- Adjustable fast charging level (1 C to 5 C)
- Adjustable normal charging level (0.05 C to 0.25 C)
- Temperature guarding by means of an NTC resistor
- Tracking of maximum fast charging time with fast charging current level
- Protections against short-circuited and open batteries
- Large battery voltage range
- Both DC and PWM outputs with polarity switch

APPLICATIONS

- Charge systems for NiCd and NiMH batteries

GENERAL DESCRIPTION

The TEA1100 is manufactured in a BICMOS process intended to be used as a battery monitor circuit in charge systems for NiCd and NiMH batteries.

The circuit has to be situated on the secondary side in mains-isolated systems where it monitors the battery voltage and the charge current. The circuit drives, by means of an opto-coupler or a pulse transformer interface, an SMPS circuit, situated on the primary side of the system, thus controlling the charge current of the batteries. The circuit can drive the external power transistor in switched mode systems, which have a DC power source, via a driver stage.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA1100	16	DIL	plastic	SOT38G
TEA1100T	16	SO16L	plastic	SOT162A

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage range		5.65	–	11.5	V
I_P	supply current	outputs off	–	–	4.1	mA
V_{VAC}	voltage range of battery-full detection		0.385	–	3.85	V
dV_{VAC}/V_{VAC}	–dV detection level w.r.t. top value	note 1	–	1	–	%
I_{VAC}	input current battery monitor		–	–	1	nA
V_{VAC}	voltage protection battery low battery high		 – –	 0.3 4.25	 – –	 V V
 I_{ref} I_n	charging level fast normal	$I_{charge} = R1/R_s \times I$; see Fig. 3 $I = I_{ref}$ $I = 1/p \times 0.1 \times I_n$ (p = prescale factor)	 20 10	 – –	 100 50	 µA µA
f_{OSC}	oscillator frequency		10	–	100	kHz

Note to the quick reference data

1. The –dV detection level can be adjusted by use of an external voltage regulator diode to increase the sensitivity.

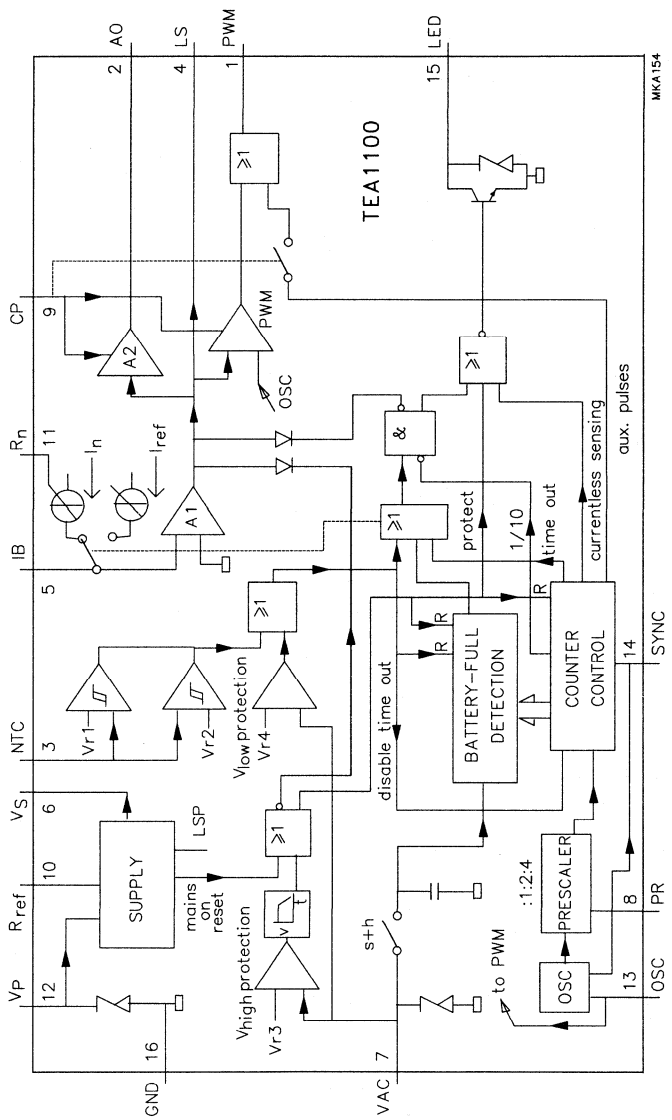


Fig.1 Block diagram.

LOW POWER DIGITAL UHF PAGING RECEIVER

GENERAL DESCRIPTION

The UAA2050T is a very low power UHF and VHF radio receiver circuit, primarily intended for use in paging receivers (27 MHz to 470 MHz) for wide-area digital paging systems employing direct FM non-return-to-zero (NRZ) frequency-shift keying (FSK) modulation.

Used in conjunction with the PCA5000T decoder for POCSAG paging systems, it offers an extremely advanced radio paging concept.

The radio receiver design is based on the offset receiver principle. The receiver provides fully filtered and squared data to drive the decoder and can be turned off completely by external inputs.

Features

- Low noise preamplifier ensuring high RF sensitivity
- Few external components required
- Low current consumption
- Wide operating supply voltage range
- Power on/off mode selectable via the enable input (RE)
- Low battery voltage detector
- Crystal controlled receiver frequency (AFC)
- Fully compatible with all FSK modulated systems (512 and 1200 bits/s)
- Uses low cost crystal

QUICK REFERENCE DATA

parameter	condition	symbol	min.	typ.	max.	unit
Supply voltage range		$V_P = V_{7-15}$	1.9	–	3.5	V
Supply voltage for preamplifier		$V_{23,24-15}$	1.0	–	3.5	V
Total supply current		I_{tot}	2.25	–	3.76	mA
Supply current OFF		$-I_{OFF}$	–	–	1.0	µA
RF sensitivity (RMS value)	1 x 10^{-2} bit error rate	EMF/2	–	0.18	0.25	µV
Preamplifier noise figure	note 1; f = 470 MHz	NF	–	4.5	–	dB
Operating ambient temperature range		T_{amb}	−10	–	+70	°C

Note to the Quick reference data

1. Including the transforming network.

PACKAGE OUTLINE

28-lead mini-pack; plastic (SO28; SOT136A).

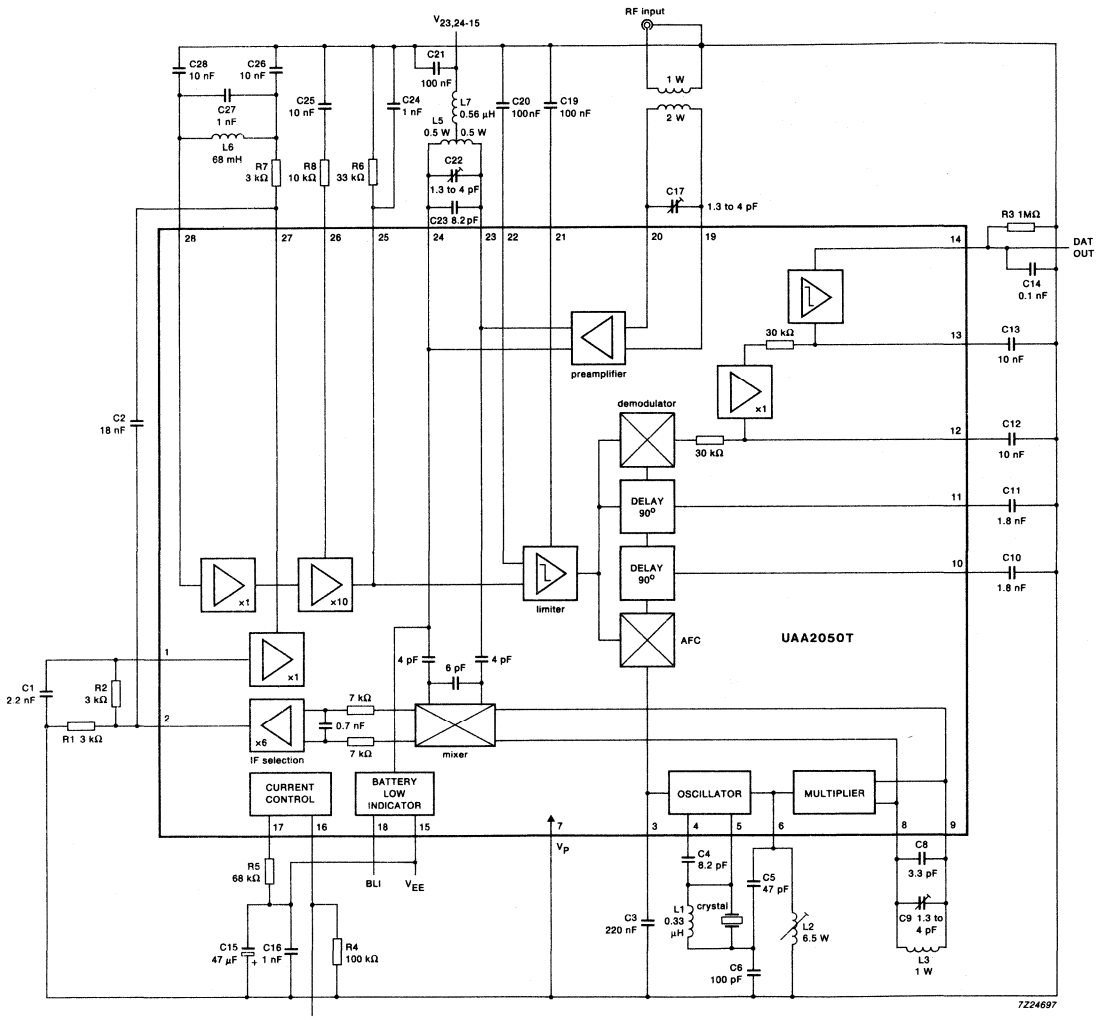


Fig.1 Block diagram (showing UHF external components).

DEVELOPMENT DATA

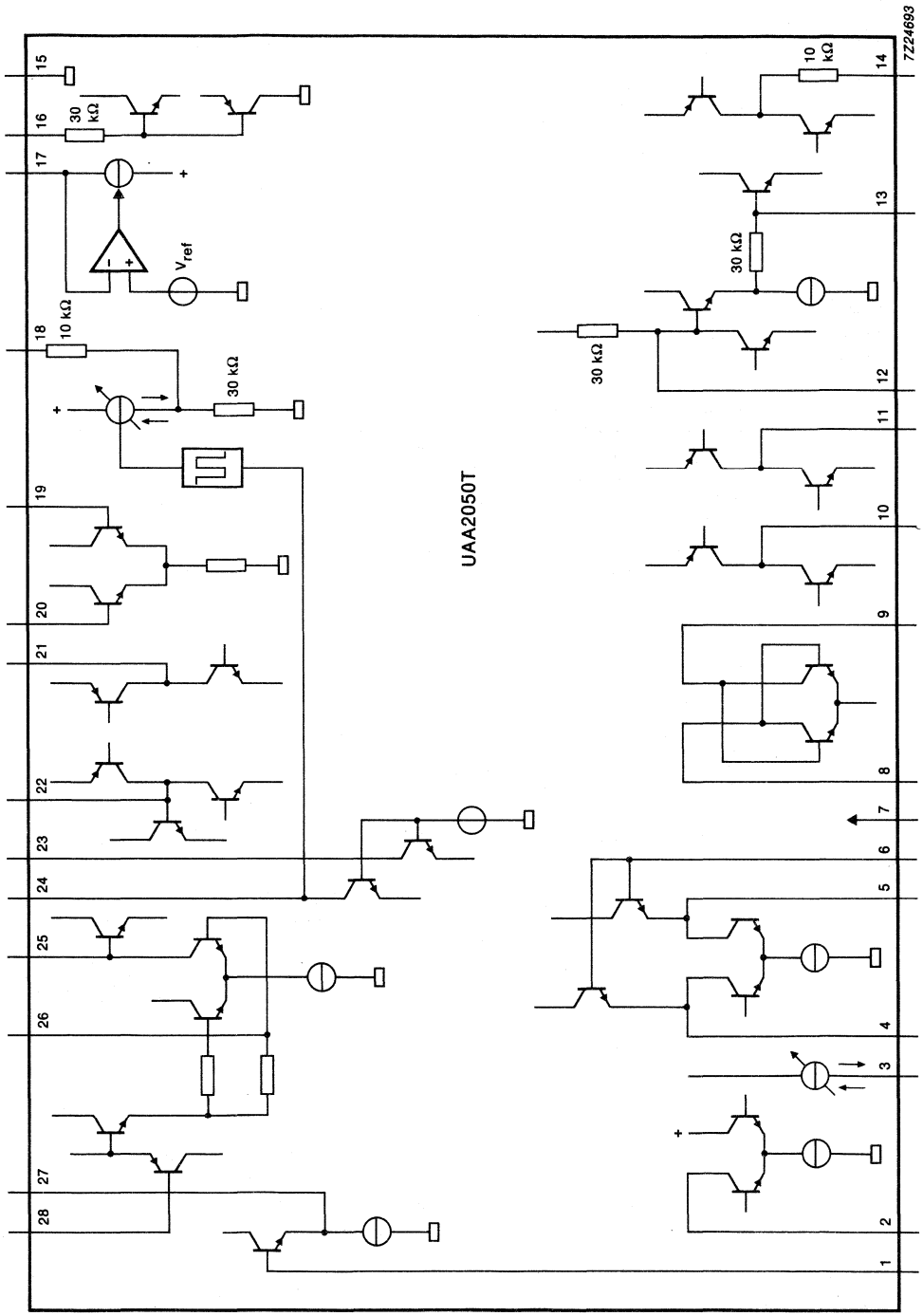


Fig.2 Pinning diagram and equivalent circuits.

PINNING

pin	mnemonic	description
1	IFF2	IF filter 2
2	IFF1	IF filter 1
3	AFC	AFC (test point 1)
4	OSC IN	oscillator input
5	OSC AFC	oscillator AFC range
6	OSC OUT	oscillator output
7	V_P	supply voltage (positive)
8	MC1	multiplier coil
9	MC2	multiplier coil
10	AFCD	AFC delay
11	DEMODD	demodulator delay
12	DAT F1	data filter 1
13	DAT F2	data filter 2
14	DAT OUT	data output
15	V_{EE}	supply voltage (negative)
16	RE	receiver enable input
17	CC	current control input
18	BLI	battery low indicator output
19	PREAMP1	preamplifier input 1
20	PREAMP2	preamplifier input 2
21	LC2	limiter decoupling 2
22	LC1	limiter decoupling 1
23	MIX1	mixer input 1 (preamplifier output)
24	MIX2	mixer input 2 (preamplifier output)
25	LIM IN	limiter input (test point 2)
26	IFF5	IF filter 5
27	IFF3	IF filter 3
28	IFF4	IF filter 4

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC134)

parameter	condition	symbol	min.	max.	unit
Supply voltage		$V_P = V_{7-15}$	−0.3	+5.0	V
Supply voltage for preamplifier		$V_{23,24-15}$	−0.3	+5.0	V
Operating ambient temperature range		T_{amb}	−10	+70	°C
Storage temperature range		T_{stg}	−55	+125	°C
Electrostatic handling; human body model*	except pins 19 and 20	V_{ESD}	−1000	+1000	V
	only pins 19 and 20	V_{ESD}	−500	+1000	V

DEVELOPMENT DATA

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

DC CHARACTERISTICS

V_P = 2.0 V; $V_{23,24-15}$ = 1.1 V; all voltages referenced to V_{EE}; T_{amb} = −10 to +55 °C; typical values measured at T_{amb} = 25 °C; test circuit as Fig.4; L2 and L3 short-circuited; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		$V_P = V_{7-15}$	1.9	2.0	3.5	V
Supply voltage for preamplifier	$V_{23,24-15} \leqslant V_P$	$V_{23,24-15}$	1.0	1.1	3.5	V
Supply current	$V_{RE} \geqslant V_P - 0.6$ V	I_7	1.9	2.5	3.2	mA
Supply current for preamplifier	$V_{RE} \geqslant V_P - 0.6$ V	$I_{23,24}$	0.35	0.45	0.56	mA
Supply current OFF	$V_{RE} \leqslant 0.4$ V	I_{OFF}	–	–	1.0	µA
Receiver enable (RE)						
POWER-OFF MODE:						
input voltage		$V_{RE} = V_{16-15}$	–	–	0.4	V
input current	V_{RE} = 0.4 V	I_{16}	–	–	1.0	µA
POWER-ON MODE:						
input voltage		$V_{RE} = V_{16-15}$	$V_P - 0.6$ V	–	–	V
input current	V_{RE} = 1.4 V	I_{16}	–	1.0	5.0	µA
Data output (DAT OUT)						
Output voltage HIGH	$I_{14} = \pm 10$ µA	V_{14-15}	$V_P - 0.7$ V	–	–	V
Output voltage LOW	$I_{14} = \pm 10$ µA	V_{14-15}	–	–	0.5	V
Battery voltage low indicator						
Detection voltage	see Fig.3	V_{DET} V_{DET}	1.10 1.90	1.17 2.00	1.24 2.10	V V
Output voltage HIGH	1.0 V ⩽ V_{24-15} ⩽ 1.10 V; 1.85 V ⩽ V_{24-15} ⩽ 1.90 V; $I_{18} = \pm 7$ µA	V_{OH}	$V_P - 0.5$ V	–	–	V
Output voltage LOW	1.24 V ⩽ V_{24-15} ⩽ 1.65 V; 2.10 V ⩽ V_{24-15}; $I_{18} = \pm 7$ µA	V_{OL}	–	–	0.5	V

Note to the DC characteristics

1. V_{18-15} goes HIGH if V_{24-15} is less than V_{DET}.

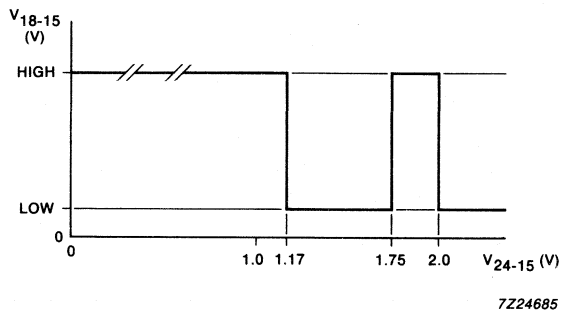


Fig.3 Typical battery low indicator thresholds.

DEVELOPMENT DATA

AC CHARACTERISTICS (UHF)

For AC test procedures refer to section 'TEST INFORMATION'. V_P = 2.0 V; $V_{23,24-15}$ = 1.1 V; all voltages referenced to V_{EE}; T_{amb} = −10 to +55 °C; typical values measured at T_{amb} = 25 °C; test circuit as Fig.4 and printed-circuit board layout as Fig.7; test signal: f = 469.200 MHz: deviation = ±4.5 kHz: modulation = 256 Hz rectangular; channel spacing = 25 kHz; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
UHF sensitivity range (RMS value)	note 1; 1 x 10^{-2} bit error rate	EMF/2	–	0.18	0.25	µV
		EMF/2	–	−122	−119	dBm
	T_{amb} = −10 to +70 °C	EMF/2	–	–	−116	dBm
Adjacent channel selectivity		αa	60	67	–	dB
	T_{amb} = −10 to +70 °C	αa	50	–	–	dB
Co-channel selectivity		αc	8	–	–	dB
Spurious response rejection		αs	55	58	–	dB
Intermodulation response		IM	50	60	–	dB
Blocking	Δf ≥ ±4 MHz	EMF	80	83	–	dBµV
AFC lock-in range		±Δf	3	–	–	kHz
Preamplifier	see Fig.9					
Noise Figure	note 2	NF	–	4.5	–	dB
Third order intercept point		IP3	–	−20	–	dBm
Available power gain		G_p	–	6	–	dB
1 dB compression point (RMS value)		EMF/2	–	10	–	mV
VHF RF sensitivity range (RMS value)	see Fig.10; f = 173.95 MHz; 1 x 10^{-2} bit error rate	EMF/2	–	0.14	–	µV
		EMF/2	–	−124	–	dBm

Notes to the AC characteristics

1. A simple digital method of performing an approximate bit error rate (BER) measurement with a counter is shown in Fig.5. At high signal levels (10 µV) the counter should read the exact frequency of the data input to the signal generator (256 Hz). As the signal level is reduced, errors occur at the receiver output and effectively changes the output frequency read by the counter (error duration is nearly always less than one bit length).
   The input signal level (V_{ref}) is reduced until the bit error rate is ≤ 1 x 10^{-2} (5 bit errors for 512 bit/s system). The frequency from the data output signal will change from 256 Hz (512 bit/s system) to 261 Hz. This RF-level is the reference for the following tests (V_{ref}).

2. Including the transforming network.

TEST INFORMATION

Tuning procedure for AC tests

1. After performing the DC tests, prepare the device for AC testing (as shown in Fig. 4).

2. Connect pin 3 to a voltage source of $V_{3-7} = -0.5$ V. Measure the multiplier frequency with a counter or spectrum analyzer connected to the link winding of L3. Tune L2 to set the crystal oscillator to a frequency of:

   $$\frac{\text{Received frequency} + 2.2\ \text{kHz}}{5} \quad (\pm 100\ \text{Hz})$$

   For a received frequency of f = 469.200 MHz, the oscillator frequency (f_{OSC}) = 93.840 MHz.

3. Remove the test voltage source and turn on the signal generator (f = 469.200 MHz; deviation = ±4.5 kHz; rectangular 256 Hz modulation; RF input level = 1 mV).

   Note During the following tests the RF signal generator level should be reduced as the receiver is tuned, to ensure the peak-to-peak output voltage at pin 25 lies between 20 mV and 100 mV.

4. Tune C9 (multiplier) to obtain a peak audio output voltage on pin 25.

5. Tune C22 (Mixer input) to obtain a peak audio output voltage on pin 25.

6. Disconnect the frequency counter from the multiplier output. Measure the voltage at pin 3 and check if it is within the range of −0.48 V to −0.52 V. If it is outside this range then adjust L2 (oscillator) until it is within the limits.

7. Check with an oscilloscope that clean data is appearing on the data output (pin 14) and proceed with the AC tests.

Test conditions

The data output signal corresponds to the sensitivity definition.

Where:

f_1 is the modulated test signal
f_2 is the unmodulated test signal
f_{cs} is the channel spacing (25 kHz)
V_1 is the signal generator 1 output
V_2 is the signal generator 2 output
V_{ref} is defined in 'Notes to the AC characteristics'.

1. Adjacent channel selectivity (see Fig.6);
   - generator 1: modulated test signal; $V_1 = V_{ref} + 3dB$
   - generator 2: unmodulated test signal; $V_2 = V_1 + 60$ dB ($f_2 = f_1 \pm \Delta f_{cs}$).

2. Co-channel selectivity (see Fig.6);
   - generator 1: modulated test signal; $V_1 = V_{ref} + 3$ dB
   - generator 2: unmodulated test signal; $V_2 = V_1 - 8$ dB ($f_2 = f_1 \pm 3$ kHz maximum).

3. Spurious response rejection (see Fig.6);
   - generator 1: modulated test signal; $V_1 = V_{ref} + 3$ dB
   - generator 2: unmodulated test signal; $V_2 = V_1 + 55$ dB (f_2 =100 kHz to 1 GHz; $|f_2 - f_1| \geqslant 2\Delta f_{cs}$).

4. Intermodulation response (see Fig.6);
   - generator 1: modulated test signal; $f_1 = 469.2$ MHz $\pm 2 \times n \times \Delta f_{cs}$) n = 1 to 4 .
   - generator 2: unmodulated test signal; $f_2 = 469.2$ MHz $\pm n \times \Delta f_{cs}$). n = 1 to 4.

   Output voltages of both generators increase with the same level, until a data output signal corresponding to the sensitivity definition is reached. The level must be 50 dB above the V_{ref} + 3 dB level.

5. Blocking (see Fig.6);
   - generator 1: modulated test signal; V_1 (EMF) = 3 dBμV
   - generator 2: unmodulated test signal; V_2 (EMF) = 80 dBμV ($f_2 = f_1 \pm \Delta f$; $\Delta f \geqslant 4$ MHz)

6. AFC lock-in-range (see Fig.5);
   - generator 1: modulated test signal; $V_1 = V_{ref} + 3$ dB ($f_1 = 469.2$ MHz ± 3 kHz)

DEVELOPMENT DATA

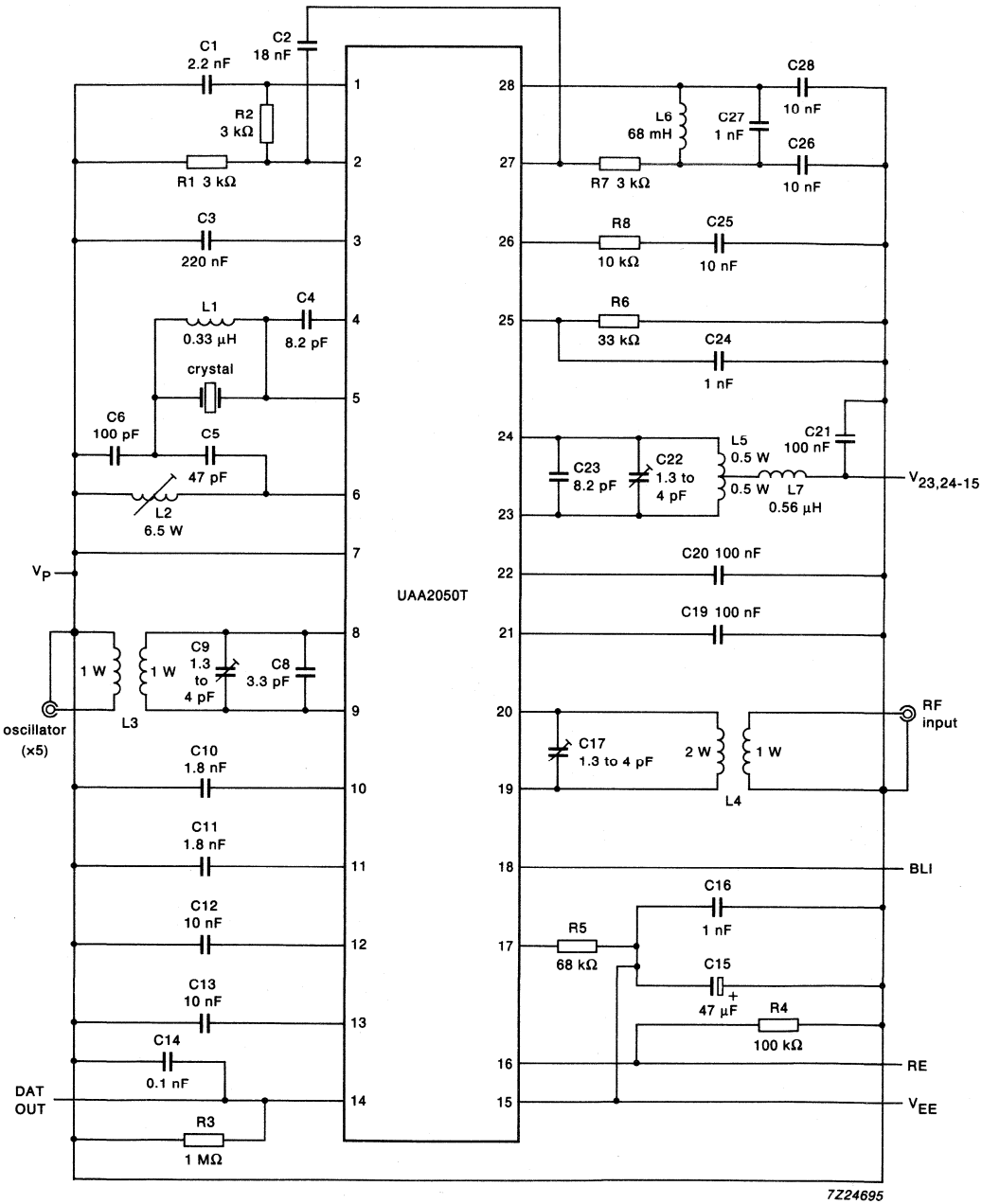


Fig.4 Test circuit (UHF).

Crystal data

Test frequency for the receiver chip is 469.2 MHz, crystal frequency is 93.838 MHz.

Static capacitance C0 (max.) = 4 pF
Dynamic capacitance C1 = 0.4 fF ±20%
Dynamic resistance R1 (max.) = 75 Ω
Temperature drift = $\pm 5 \times 10^{-6}$.

Inductors

L3, L4 and L5: wound with 0.9 mm silvered wire, without pot or core and diameter of 4.5 mm.

L1 = 0.33 µH chip inductor (at 25 MHz minimum value of Q = 12)
L2 = 6.5 turns
L3 = 1 turn
L4 = 2 turns
L5 = 1 turn
L6 = inductor, Philips microchoke (at 10 kHz minimum value of Q = 10)

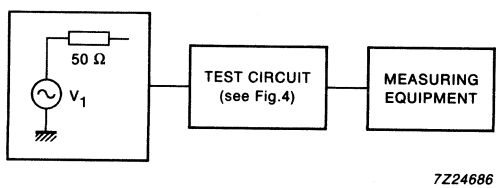


Fig.5 Test figure A.

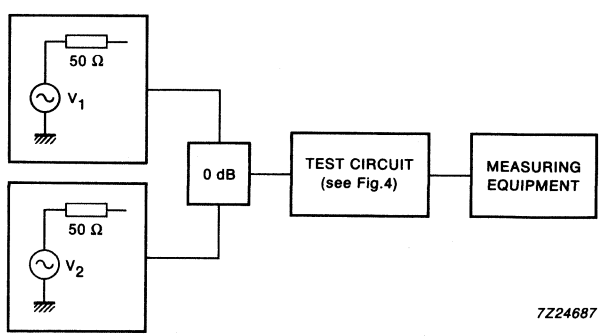
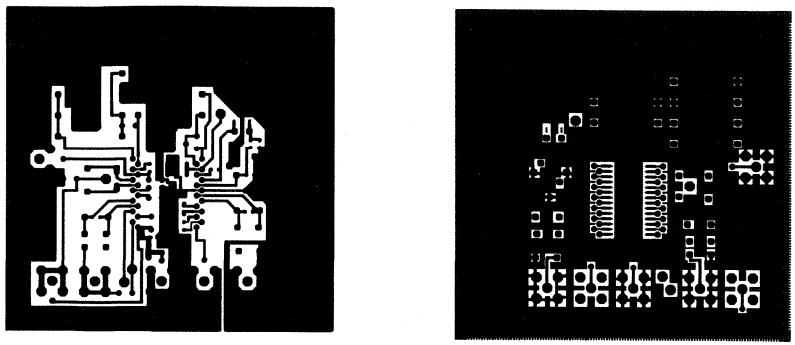


Fig.6 Test figure B.



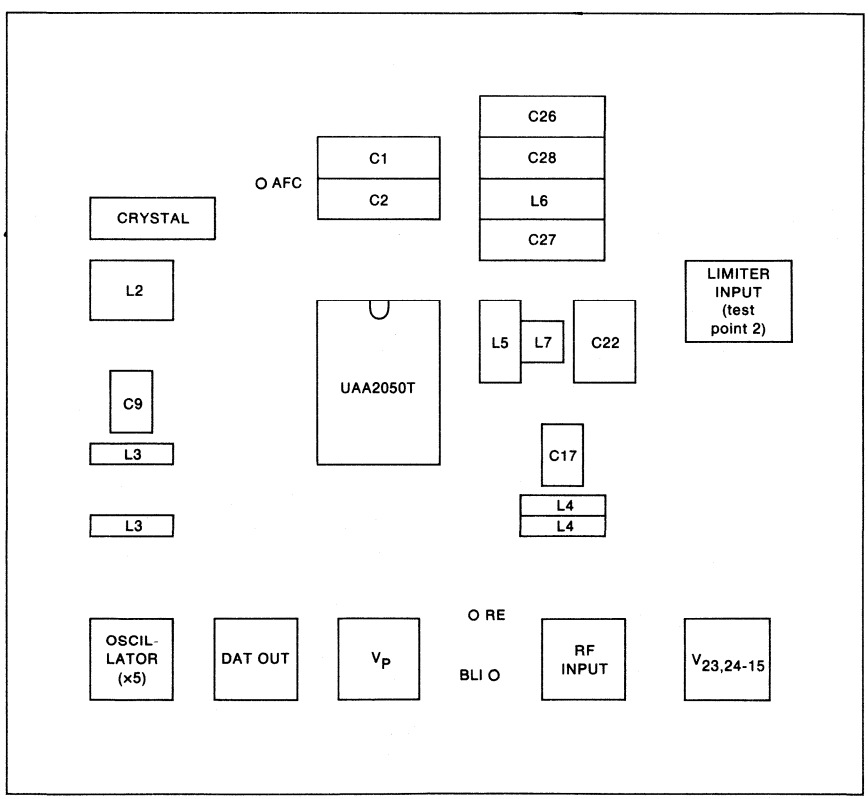
(a) underside

(b) top side

7Z24689

Fig. 7 Printed-circuit board for UHF range (see Fig.4).

DEVELOPMENT DATA



7Z24690

Fig. 8 Printed-circuit board for UHF range (component arrangement).

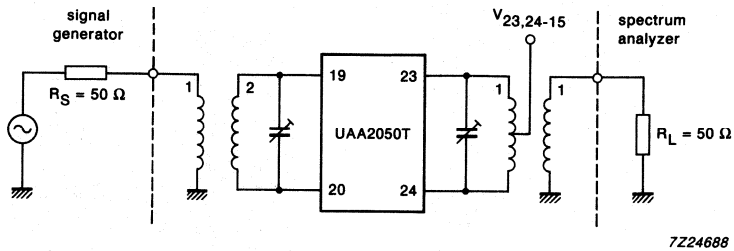


Fig.9 Test circuit for the preamplifier.

DEVELOPMENT DATA

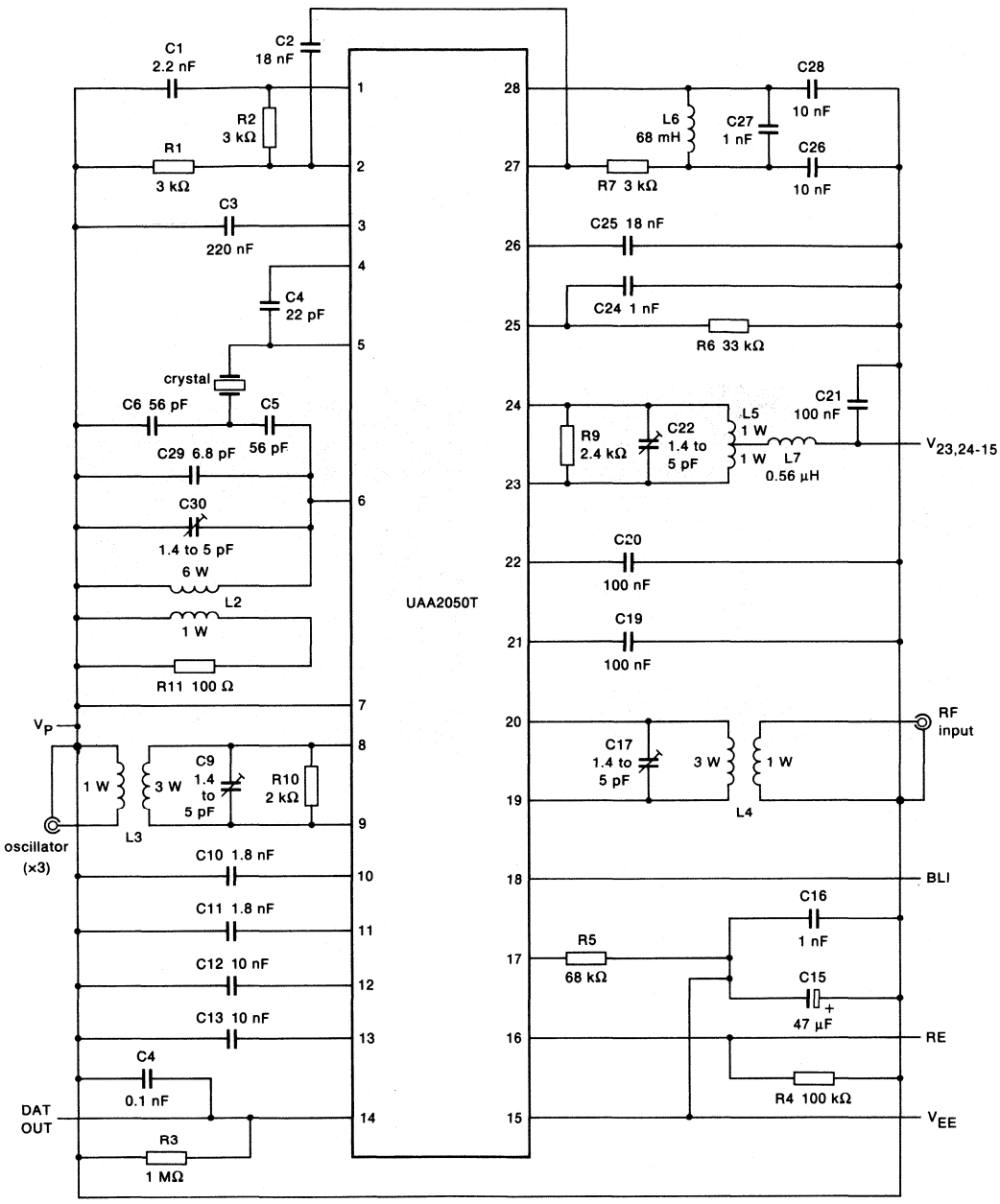


Fig.10 Test circuit (VHF).

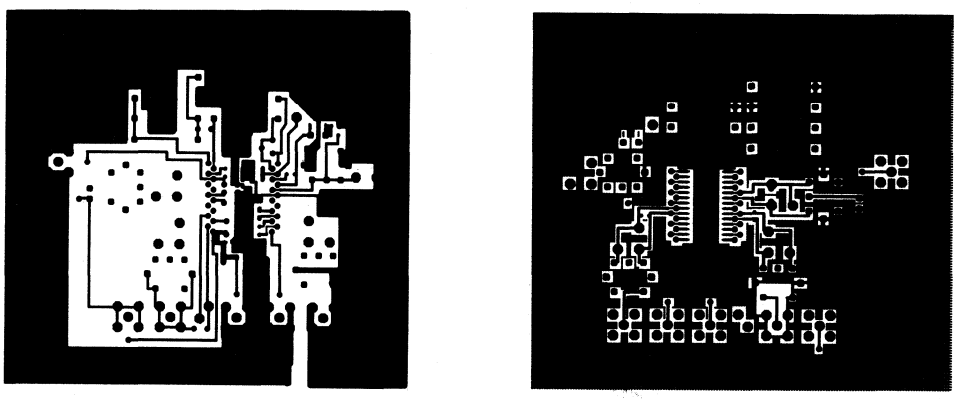
Crystal data

Test frequency for the receiver chip is 173.95 MHz, crystal frequency is 57.9859 MHz.

Inductors

L2, L3, L4 and L5: wound with 0.3 mm enamelled copper wire on Toko 4.5 mm diameter former, without pot or core. Screening cans are also used.

L2 = 6 turns, 2 turns per groove; link winding, 1 turn over the centre of the other winding
L3 = 3 turns, 1 turns per groove; link winding, 1 turn at the bottom of the former
L4 = 3 turns, 1 turns per groove; link winding, 1 turn at the centre of the other winding
L5 = 2 turns
L6 = inductor, Philips microchoke (at 10 kHz minimum value of Q = 10)



(a) underside

(b) top side

7Z24691

Fig. 11 Printed-circuit board for VHF range (see Fig.10).

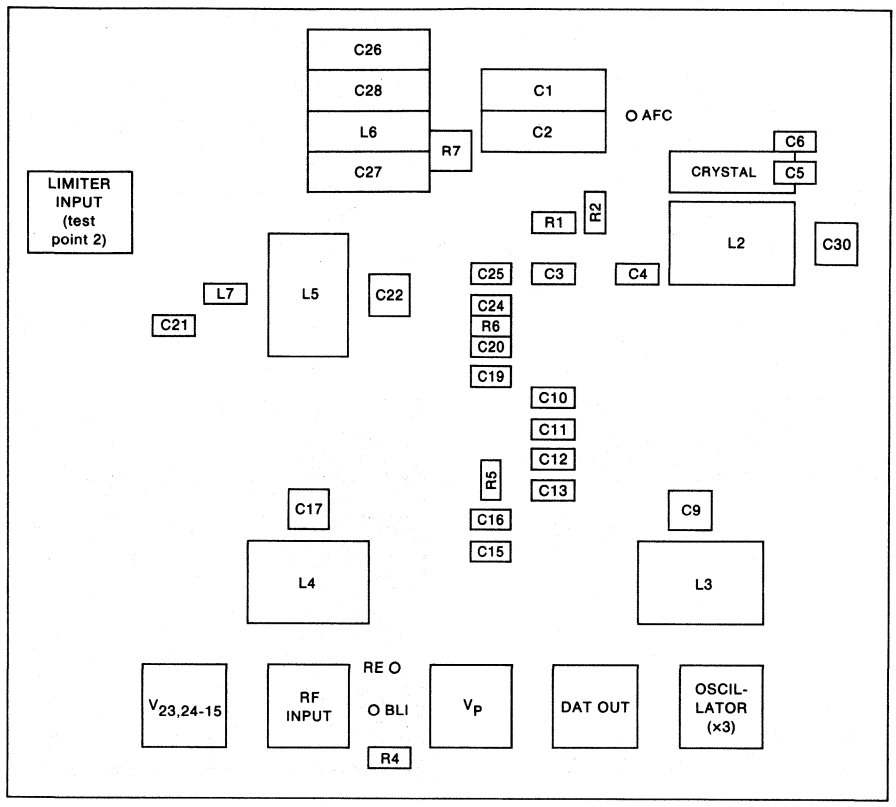


Fig. 12 Printed-circuit board for VHF range (component arrangement).

APPLICATION INFORMATION

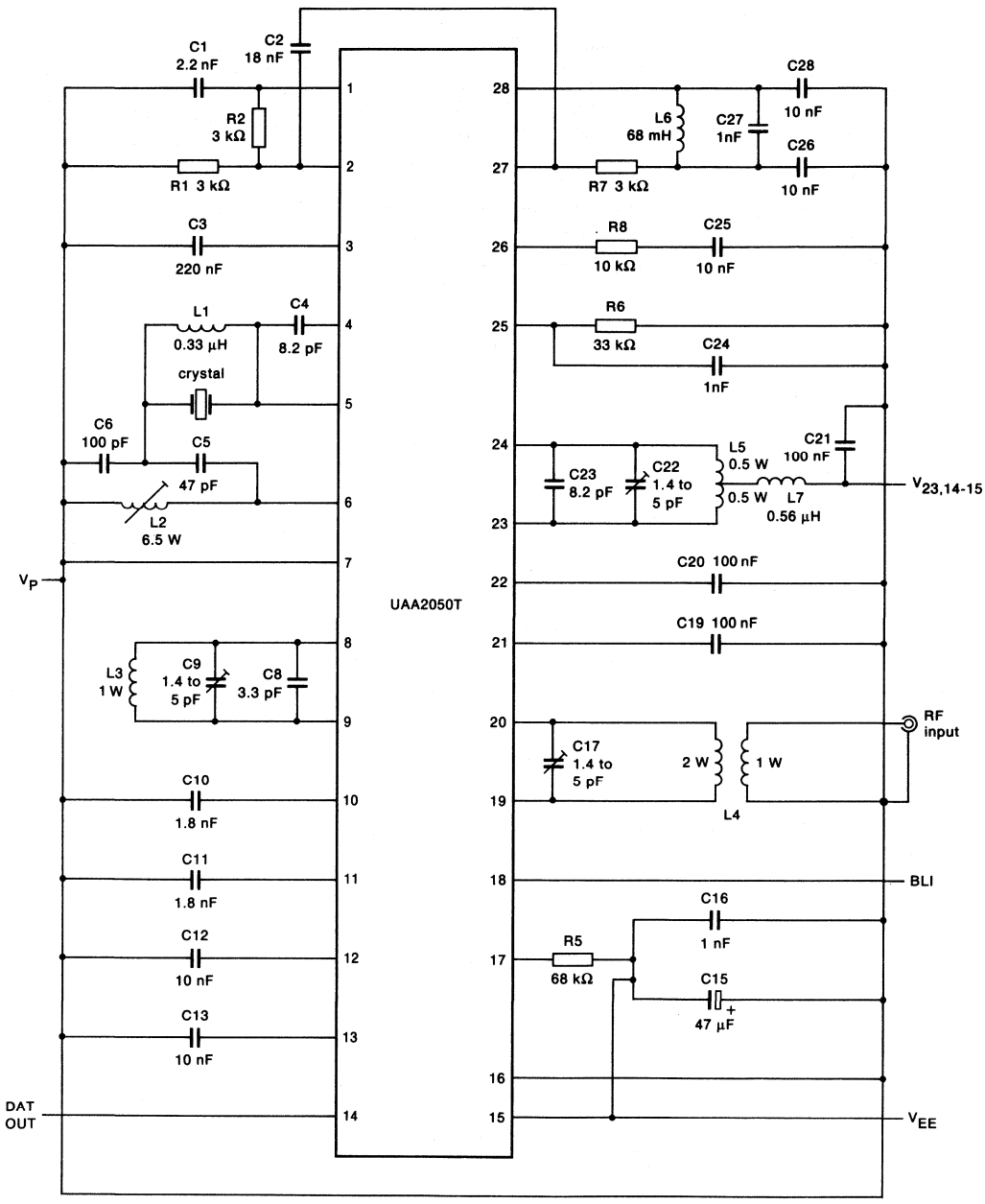


Fig.13 Application diagram (UHF).

Note to Fig.13

For information concerning the crystal oscillator and inductors, refer to Fig.4.

900 MHz front-end for GSM applications

UAA2072M

FEATURES

- Low noise amplifier
- Dual quadrature mixers for image rejection
- I and Q combining networks at a fixed IF
- Down conversion transmit mixer
- Serial interface for programming

APPLICATIONS

- Digital portable receivers
- GSM systems

GENERAL DESCRIPTION

The UAA2072M is a low-power front-end intended for use in mobile transceivers that comply with GSM systems. Most of the critical RF circuitry is grouped on one chip by implementing a dual balanced mixer architecture thereby providing integrated image rejection.
The circuit can be tuned in application via a 3-wire serial bus to obtain optimum image rejection. A down-mixing circuit, which is used to implement a closed-loop transmit modulation architecture is also available on chip.
Fast power-up and power-down switching capability for supply current saving has also been implemented on chip. The UAA2072M offers 26 dB of power gain.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	positive supply voltage	4.5	4.8	5.3	V
I_{CCrx}	receive supply current	–	29	–	mA
I_{CCtx}	transmit supply current	–	12	–	mA
$I_{CC(PD)}$	supply current in stand-by	–	–	50	µA
T_{amb}	operating ambient temperature	−20	–	+70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
UAA2072M	20	SSOP20	plastic	SOT266A

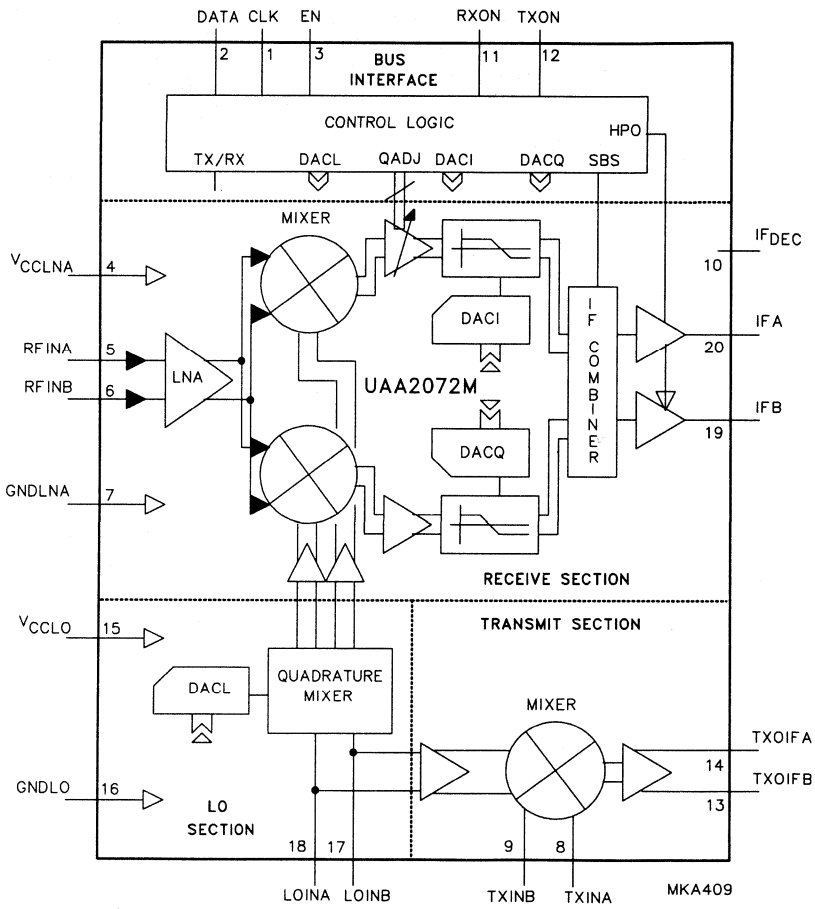


Fig.1 Block diagram.

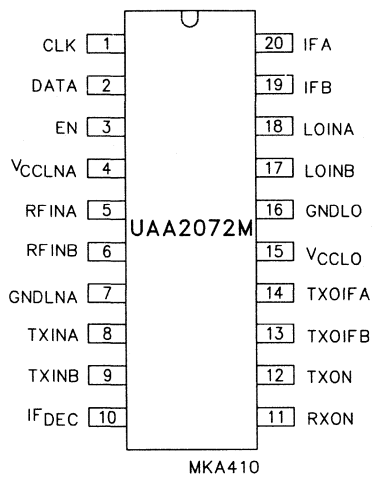


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
CLK	1	programming bus clock input
DATA	2	programming bus data input
EN	3	programming bus enable input (active LOW)
V_{CCLNA}	4	positive supply for LNA, IF parts and Tx mixer
RFINA	5	RF balanced input A
RFINB	6	RF balanced input B
GNDLNA	7	ground for Rx parts
TXINA	8	balanced transmit mixer input A
TXINB	9	balanced transmit mixer input B
IF_{DEC}	10	IF decoupling
RXON	11	hardware power-on for receive parts
TXON	12	hardware power-on for transmit parts
TXOIFB	13	balanced transmit mixer IF output B
TXOIFA	14	balanced transmit mixer IF output A
V_{CCLO}	15	positive supply for LO parts
GNDLO	16	ground for LO parts
LOINB	17	balanced LO input B
LOINA	18	balanced LO input A
IFB	19	IF output B (balanced with IFA)
IFA	20	IF output A (balanced with IFB)

Advanced pager receiver UAA2080T

FEATURES

- Wide frequency range up to 512 MHz
- High sensitivity
- High dynamic range
- Electronically adjustable filters on chip
- Wide frequency offset range and wide deviation range
- Fully POCSAG compatible
- Power on/off mode selectable by the chip enable input
- Low supply voltage; low power consumption
- High integration level

GENERAL DESCRIPTION

The UAA2080T is a high performance low power radio receiver circuit primarily intended for VHF and UHF (25 to 512 MHz) pager receivers for wide area digital paging systems, employing direct FM non-return-to-zero (NRZ) frequency shift keying (FSK). The receiver design is based on the "direct conversion" principle where the input signal is mixed directly down to the base band by a local oscillator on the signal frequency. Two complete signal paths with signals of 90° phase difference are required to demodulate the signal. The circuit makes extensive use of on-chip capacitors to minimize the number of external components.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 9)		1.9	2.05	3.5	V
I_P	supply current (pin 9)		2.3	2.7	3.2	mA
$I_{P\ off}$	stand-by current (pin 9)		–	–	3	µA
$P_{i\ ref}$	RF input sensitivity (pin 3)	BER <3/100; f_i = 470 MHz; ± 4.0 kHz deviation; data rate 1200 bits/s	–	–124.5	–121.5	dBm
$V_{P\ det}$	supply voltage threshold for battery LOW indicator		1.95	2.05	2.15	V
T_{amb}	operating ambient temperature range		–10	–	55	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
UAA2080T	28	mini-pack	plastic	SOT136A

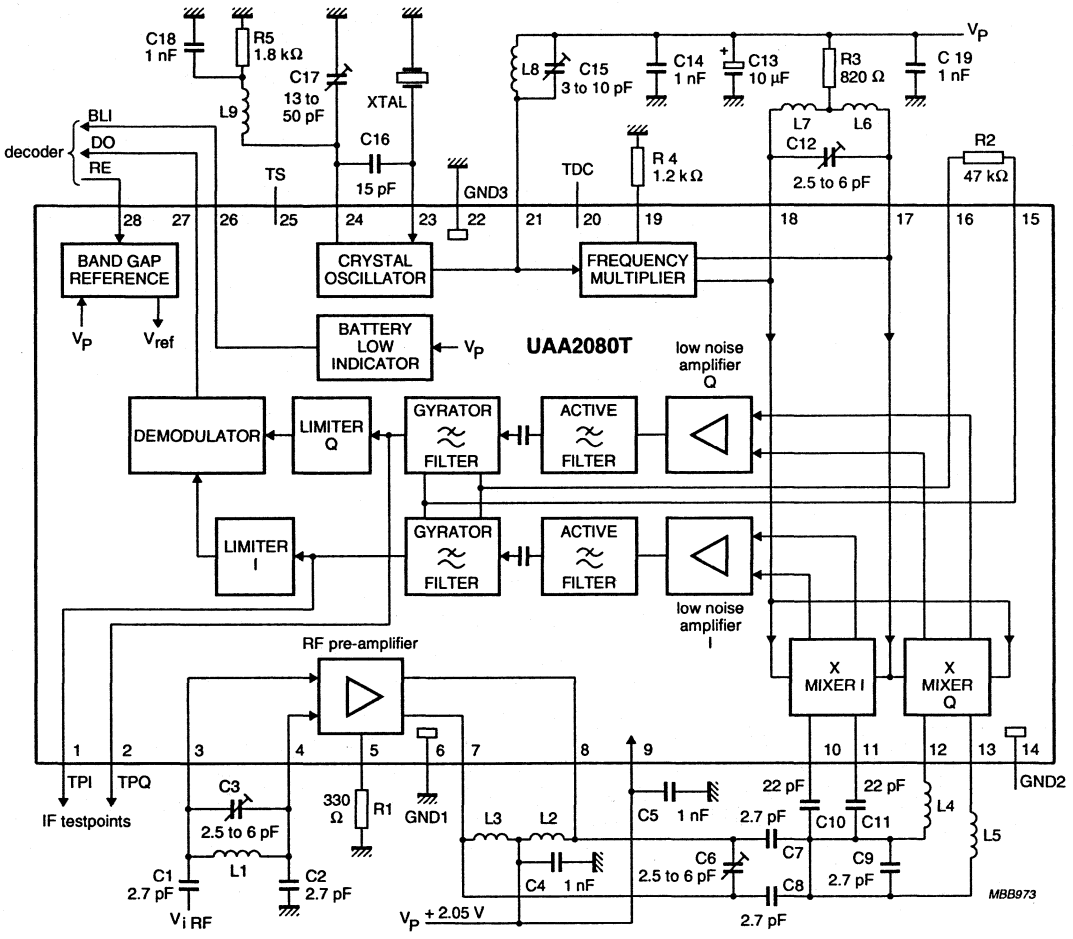


Fig.1 Block, test and application diagram (f = 469.95 MHz).

Note to the components shown in Fig.1.

Inductances:	L1	12.5 nH	± 5 %	(Q_{min} = 145 at 470 MHz)
	L2, L3, L6, L7	8 nH	± 10 %	(Q_{min} = 50 at 470 MHz; TC = + 25 to + 125 ppm/K)
	L4, L5	40 nH	± 10 %	(Q_{min} = 40 at 470 MHz; TC = + 25 to + 125 ppm/K)
	L8	100 nH	± 10 %	(Q_{min} = 30 at 156 MHz; TC = + 25 to + 125 ppm/K)
	L9	560 nH	± 10 %	(Q_{min} = 40 at 78 MHz; TC = + 25 to + 125 ppm/K)
Resistors:	R1 to R5		tolerance ± 2 %	(TC = + 50 ppm/K)
Capacitors:	C1, C2, C7, C8, C9		tolerance ± 5 %	(TC = 0 ± 30 ppm/K; tan $\delta \leq 30 \times 10^{-4}$ at 1 MHz)
	C3, C6, C12		–	(TC = 0 ± 200 ppm/K; tan $\delta \leq 20 \times 10^{-4}$ at 1 MHz)
	C4, C5, C14, C18, C19		tolerance ± 10 %	(TC = 0 ± 30 ppm/K; tan $\delta \leq 10 \times 10^{-4}$ at 1 MHz)
	C10, C11		tolerance ± 5 %	(TC = 0 ± 30 ppm/K; tan $\delta \leq 21 \times 10^{-4}$ at 1 MHz)
	C13		tolerance ± 20 %	
	C15		–	(TC = 0 ± 300 ppm/K; tan $\delta \leq 20 \times 10^{-4}$ at 1 MHz)
	C16		tolerance ± 30 %	(TC = 0 ± 30 ppm/K; tan $\delta \leq 26 \times 10^{-4}$ at 1 MHz)
	C17		–	(TC = +1700 ± 500 ppm/K; tan $\delta \leq 50 \times 10^{-4}$ at 1 MHz)
Crystal XTAL:	f = 78.325 MHz (crystal with 8 pF load), 3rd overtone, pullability > 2.75 ppm/pF (change in frequency between series resonance and resonance with 8 pF series capacitor at 25 °C), dynamic resistance R1 < 30 Ω, Δf = ± 5 ppm for - 10 to 60 °C with 25 °C reference, calibration plus aging tolerance: –5 to +15 ppm.			

PINNING

SYMBOL	PIN	DESCRIPTION
TPI	1	IF test point (I-channel)
TPQ	2	IF test point (Q-channel)
VI1RF	3	pre-amplifier RF input 1
VI2RF	4	pre-amplifier RF input 2
RRFA	5	external emitter resistor of pre-amplifier
GND1	6	ground 1 (0 V)
VO2RF	7	pre-amplifier RF output 2
VO1RF	8	pre-amplifier RF output 1
V_P	9	positive supply voltage
VI2MI	10	I-channel mixer input 2
VI1MI	11	I-channel mixer input 1
VI1MQ	12	Q-channel mixer input 1
VI2MQ	13	Q-channel mixer input 2
GND2	14	ground 2 (0 V)
COM	15	gyrator filter resistor (common line)
RGYR	16	gyrator filter resistor
VO1MUL	17	frequency multiplier output 1
VO2MUL	18	frequency multiplier output 2
RMUL	19	external emitter resistor for frequency multiplier
TDC	20	DC test point (no external connection at normal operation)
OSC	21	oscillator collector
GND3	22	ground 3 (0 V)
OSB	23	oscillator base (crystal input)
OSE	24	oscillator emitter
TS	25	test switch (no external connection at normal operation)
BLI	26	battery LOW indicator output
DO	27	DATA output
RE	28	receiver enable input

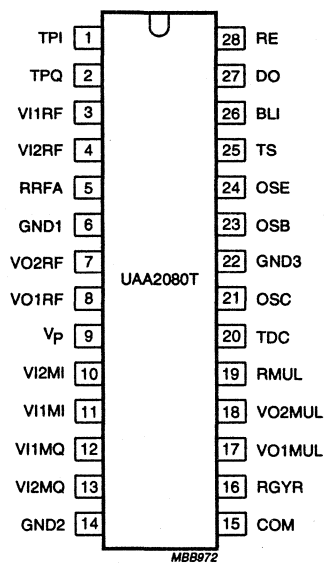


Fig.2 Pin configuration.

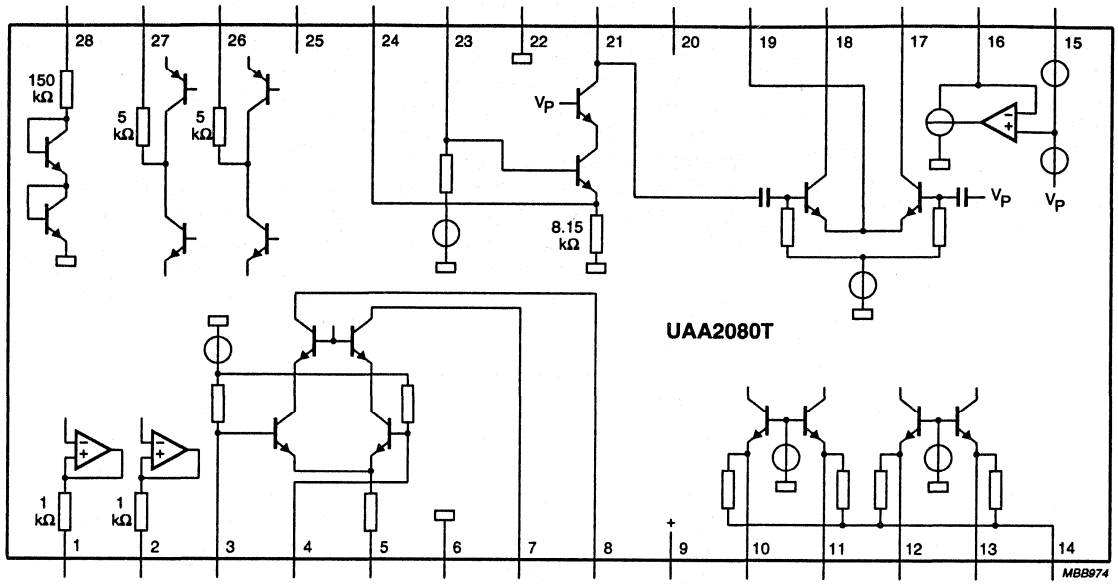


Fig.3 Internal circuits.

FUNCTIONAL DESCRIPTION

The complete circuit consists of the following functional blocks as shown in Fig.1:

Radio Frequency Amplifier

The RF amplifier is an emitter-coupled pair driving a balanced cascode stage, which drives an external balanced tuned circuit. Its bias current is set by an external resistor R1 (330 Ω) to typically 770 μA. With this bias current and at UHF (470 MHz) the optimum source resistance is 1 kΩ. The capacitors C1 and C2 transform a 50 Ω source resistance to this optimum value. The output drives a tuned circuit with capacitive divider (C7, C8 and C9) to provide maximum power transfer to the phase-splitting network and the mixers.

Mixers

The double balanced mixers consist of common base input stages and upper switching stages driven from the frequency multiplier. The input impedance (300 Ω) of each mixer acts together with external components (C10, C11; L4, L5 respectively) as phase shifter/power splitter to provide a differential phase shift of 90 degrees between the I-channel and the Q-channel.

Oscillator

The oscillator is based on a transistor in common collector configuration. It is followed by a cascode stage driving a tuned circuit which provides the signal for the frequency multiplier. The oscillator bias current (typically 250 μA) is determind by the external resistor R5 (1.8 kΩ). The oscillator frequency is controlled by an external 3rd overtone crystal in parallel resonance mode. External capacitors between base and emitter (C16) and from emitter to ground (C17) make the oscillator transistor appear as having a negative resistance for small signals; this causes the oscillator to start. A parallel resonant circuit (L9 and C18) connected to the emitter of the oscillator transistor prevents oscillation at the fundamental frequency of the crystal. The resonant circuit at output pin 21 selects the second harmonic of the oscillator frequency. In other applications a different multiplication factor may be chosen.

Frequency Multiplier

The frequency multiplier is an emitter-coupled pair driving an external balanced tuned circuit. Its bias current is set by an external resistor R4 (1.2 kΩ) to typically 350 μA. The oscillator signal is internally AC-coupled to one input of the emitter-coupled pair while the other input is internally grounded via a capacitor. The frequency multiplier output signal between pins 17 and 18 drives the upper switching stages of the mixers. The bias voltage on pins 17 and 18 is set by an external resistor R3 (820 Ω) to allow sufficient voltage swing at the mixer outputs.

Low Noise Amplifiers, Active Filters and Gyrator Filters

The low noise amplifiers ensure that the noise of the following stages does not affect the overall noise figure. The following active filters before the gyrator filters reduce the levels of large signals from adjacent channels. Internal AC-couplings block DC-offsets from the gyrator filter inputs.

The gyrator filters implement the transfer function of a 7th-order elliptic filter. Their cut-off frequencies are determind by the external resistor R2 (47 kΩ). The gyrator filter output signals are available on IF test points TPI and TPQ (pins 1 and 2).

Limiters

The gyrator filter output signals are amplified in the limiter amplifiers to get IF signals with removed amplitude information.

Demodulator

The limiter amplifier output signals are fed to the demodulator. The demodulator output DO (on pin 27) is going LOW or HIGH depending upon which of the input signals leads the other one.

Battery LOW Indicator

The battery LOW indicator senses the supply voltage and sets its output to HIGH when the supply voltage is less than $V_{P\ det}$ (typically 2.05 V). Low battery warning is available at pin 26.

Band Gap Reference

The whole chip can be powered-up and powered-down by enabling and disabling the band gap reference via the receiver enable pin 28.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).
Ground pins 6, 14 and 22 connected together.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_p	positive supply voltage (pin 9)	−0.3	8	V
T_{stg}	storage temperature range	−55	125	°C
T_{amb}	operating ambient temperature range	−10	70	°C
V_{ESD}	Electrostatic handling (note 1) pins 3 and 4	−	+2000 −1500	V
	pin 5	−	+2000 −500	V
	pins 7 and 8	−	+250 −2000	V
	pin 9	−	+500 −1000	V
	pins 23 and 24	−	+1500 −500	V
	other pins	−	±2000	V

Note to the Limiting Values

1. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor.

DC CHARACTERISTICS

V_P = 2.05 V; T_{amb} = −10 to 55 °C (typical values at T_{amb} = 25 °C); measurements taken in test circuit Fig.1 with XTAL at pin 23 disconnected unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 9)		1.9	2.05	3.5	V
I_P	supply current (pin 9)	V_{RE} = HIGH	2.3	2.7	3.2	mA
$I_{P\ off}$	stand-by current (pin 9)	V_{RE} = LOW	–	–	3	µA
Receiver enable input (pin 28)						
V_{RE}	HIGH level input voltage(receiver active)		1.4	–	V_P	V
	LOW level input voltage (receiver inactive)		0	–	0.3	V
I_{RE}	HIGH level input current	$V_{RE} = V_P$ = 3.5 V	–	–	20	µA
	LOW level input current	V_{RE} = 0	0	–	−1.0	µA
Battery LOW indicator output (pin 26)						
V_{BLI}	HIGH level output voltage	$V_P < V_{P\ det}$; I_{BLI} = −10.0 µA	V_P - 0.5	–	–	V
	LOW level output voltage	$V_P < V_{P\ det}$; I_{BLI} = +10 µA	–	–	0.5	V
$V_{P\ det}$	low battery warning threshold		1.95	2.05	2.15	V
Demodulator output (pin 27)						
V_{DO}	HIGH level output voltage	I_{DO} = −10 µA	V_P - 0.5	–	–	V
	LOW level output voltage	I_{DO} = +10 µA	–	–	0.5	V

AC CHARACTERISTICS

V_P = 2.05 V; T_{amb} = 25 °C; test circuit Fig.1; $f_{i\,RF}$ = 469.95 MHz with ± 4.0 kHz deviation; 1200 baud pseudo random bit sequence modulation (t_r = 250 ± 25 µs measured between 10% and 90% of voltage amplitude) and 20 kHz channel spacing; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Radio frequency input						
$P_{i\,ref}$	input sensitivity ($P_{i\,ref}$ is the maximum available power at the input of the test board)	BER < 3/100; note 1	–	–124.5	–121.5	dBm
		T_{amb} = –10 to 55 °C; note 2	–	–	–118.5	dBm
		V_P = 1.9 V	–	–	–115.5	dBm
Mixers to demodulator						
α_a	adjacent channel selectivity	T_{amb} = 25 °C	67	70	–	dB
		T_{amb} = –10 to 55 °C	65	–	–	dB
α_{ci}	IF filter channel imbalance		–	–	2	dB
α_c	co-channel rejection		–	4	7	dB
α_{sp}	spurious immunity		50	60	–	dB
α_{im}	intermodulation immunity		55	60	–	dB
α_{bl}	blocking immunity	Δf > ±1 MHz; note 3	75	82	–	dB
f_{offset}	frequency offset range (3dB degradation in sensitivity)	deviation f = ±4.0 kHz	±2	–	–	kHz
		deviation f = ±4.5 kHz	±2.5	–	–	kHz
Δf_{dev}	deviation range (3 dB degradation in sensitivity)		2.5	–	7.0	kHz
t_{on}	receiver turn-on time	data valid after setting RE input HIGH; note 4	–	–	5	ms

Notes to the AC Characteristics

1. The bit error rate BER is measured using the test facility shown in Fig.5.
2. Capacitor C17 requires re-adjustment to compensate temperature drift.
3. Δf is the frequency offset between the wanted signal and the interfering signal.
4. Turn-on time is defined as the time from RE (pin 28) going HIGH to the reception of valid data on DO output (pin 27). Turn-on time is measured using an external oscillator (turn-on time using the internal oscillator is dependent upon the oscillator circuitry).

TEST INFORMATION

Tuning procedure for AC tests

1. Turn on the signal generator : f = 469.954 MHz, no modulation, $V_{i\ RF}$ = 1 mV RMS.
2. Measure the IF with a counter connected to test point TPI (pin 1). Tune C17 to set the crystal oscillator to achieve IF = 4 kHz. Change the generator frequency to f = 469.946 MHz and check that IF is also 4 kHz. For a received input frequency $f_{i\ RF}$ = 469.950 MHz the crystal frequency is f_{osc} = 78.325 MHz (for definition of crystal frequency, see remarks to the components in Fig.1).
3. Set the signal generator to nominal frequency and turn on the modulation (f = 469.950 MHz, deviation ±4.0 kHz, 600 Hz square wave modulation, $V_{i\ RF}$ = 1 mV RMS). Note that the RF signal should be reduced in the following tests, as the receiver is tuned, to ensure $V_{o\ IF}$ = 10 to 50 mV (p-p) on test point pins 1 or 2 (TPI or TPQ).
4. Tune C15 (oscillator output circuit) and C12 (frequency multiplier output) to obtain a peak audio voltage on TPI (pin 1).
5. Tune C3 and C6 (RF input and mixer input) to obtain a peak audio voltage on TPI (pin 1).
6. Check that the output signal on TPQ (pin 2) is within 3 dB in amplitude and at 90 (±20) degrees relative phase of the signal on TPI (pin 1).
7. Check that data signal appears on output DO (pin 27) and proceed with the AC test.

AC Test Conditions

The reference signal level for the following tests is defined as the input level in dBm to give a Bit Error Rate BER ≤ 3/100 (corresponding with 36 bit errors per second for 1200 bit/s). The following tests are executed without load on test points TPQ and TPI.

Definitions:

modulated test signal 1

f	=	469.950 MHz
deviation	=	±4.0 kHz
modulation	=	1200 baud pseudo random bit sequence
rise time	=	250 ±25 µs (between 10% and 90% of final value)

modulated test signal 2

deviation	=	±2.4 kHz
modulation	=	400 Hz sine wave

f1	=	frequency of signal generator 1
f2	=	frequency of signal generator 2
f3	=	frequency of signal generator 3
Δf_{cs}	=	channel spacing (20 kHz)
P1	=	maximum available power from signal generator 1 at the test board input
P2	=	maximum available power from signal generator 2 at the test board input
P3	=	maximum available power from signal generator 3 at the test board input
$P_{i\ ref}$	=	previously defined in the AC Characteristics

1. Adjacent channel selectivity, Fig.4(b) (f2 = f1 $\pm\Delta f_{cs}$)
   generator 1: modulated test signal 1; P1 = $P_{i\ ref}$ + 3dB
   generator 2: modulated test signal 2; P2 = P1 + 67 dB ($\alpha_{a\ min}$)

2. Co-channel selectivity, Fig.4(b) (f2 = f1 ± up to 3 kHz)
   generator 1: modulated test signal 1; P1 = $P_{i\ ref}$ + 3dB
   generator 3: modulated test signal 2; P2 = P1 - 7 dB ($\alpha_{c\ max}$)

3. Spurious immunity, Fig.4(b) (f2 = 100 kHz to 2 GHz)
   generator 1: modulated test signal 1; P1 = $P_{i\ ref}$ + 3 dB
   generator 2: modulated test signal 2; P2 = P1 + 50 dB ($\alpha_{sp\ min}$)

4. Intermodulation immunity, Fig.4(c) (f2 = f1 $\pm\Delta f_{cs}$; f3 = f1 $\pm 2^{*}\Delta f_{cs}$)
   generator 1: modulated test signal 1; P1 = $P_{i\ ref}$ + 3 dB
   generator 2: unmodulated; P2 = P1 + 55 dB ($\alpha_{im\ min}$)
   generator 3: modulated test signal 2; P3 = P2

5. Blocking, Fig.4(b) (f2 = f1 ±1MHz)
   generator 1: modulated test signal 1; P1 = $P_{i\ ref}$ + 3 dB
   generator 2: modulated test signal 2; P2 = P1 + 75 dB ($\alpha_{bl\ min}$)

6. Frequency offset range, Fig.4(a) (deviation = ±4.0 kHz, f1 = 469.950 MHz ±2 kHz; $f_{offset\ min}$)
   generator 1: modulated test signal 1; P1 = $P_{i\ ref}$ + 3 dB

7. Deviation range, Fig.4(a) (deviation = ±2.5 to ±7 kHz; $\Delta f_{dev\ min}$ to $\Delta f_{dev\ max}$)
   generator 1: modulated test signal 1; P1 = $P_{i\ ref}$ + 3dB

8. Receiver turn-on time, Fig.4(a)
   generator 1: modulated test signal 1; P1 = $P_{i\ ref}$ + 10 dB.
   The BER measurement is started 5 ms ($t_{on\ max}$) after RE to HIGH (pin 28); BER is then measured for 100 bits (BER ≤ 3/100).

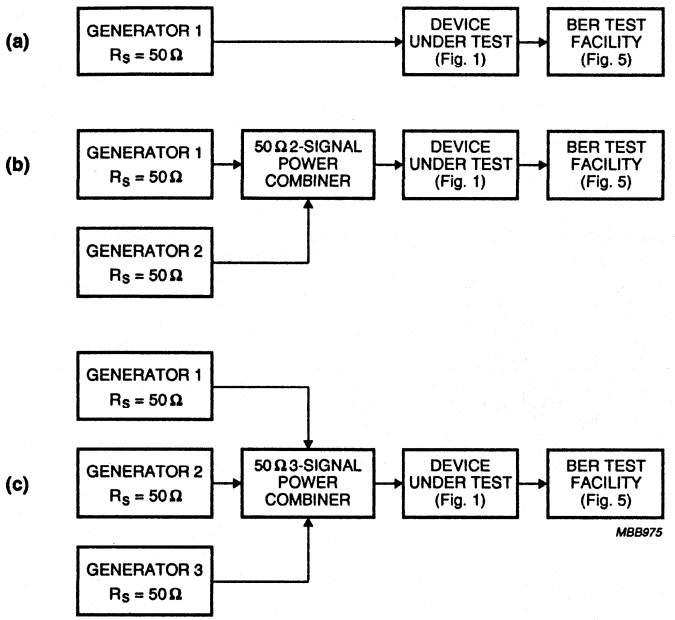


Fig.4 Test configurations: (a) one generator, (b) two generators, (c) three generators.

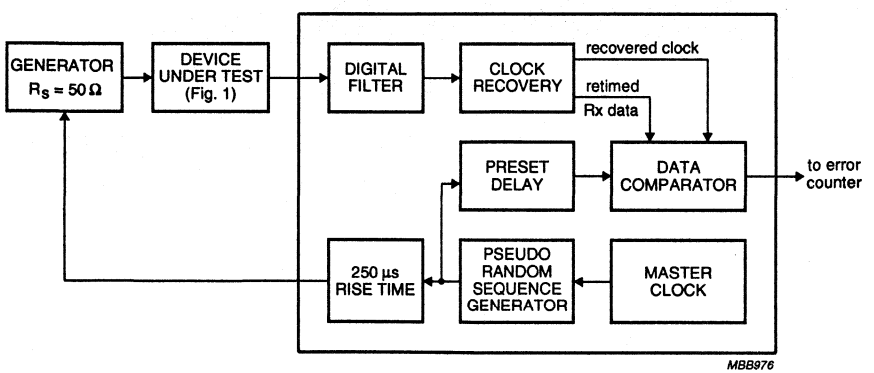


Fig.5 BER test facility.

PCB LAYOUT OF TEST CIRCUIT (Fig.1)

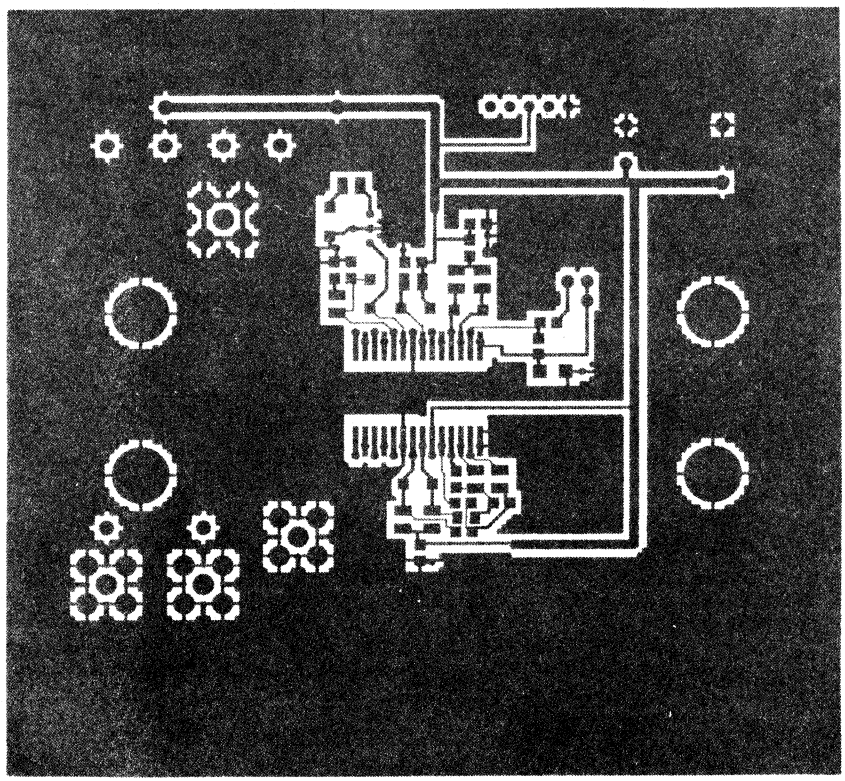


Fig.6 Test circuit; top layout.

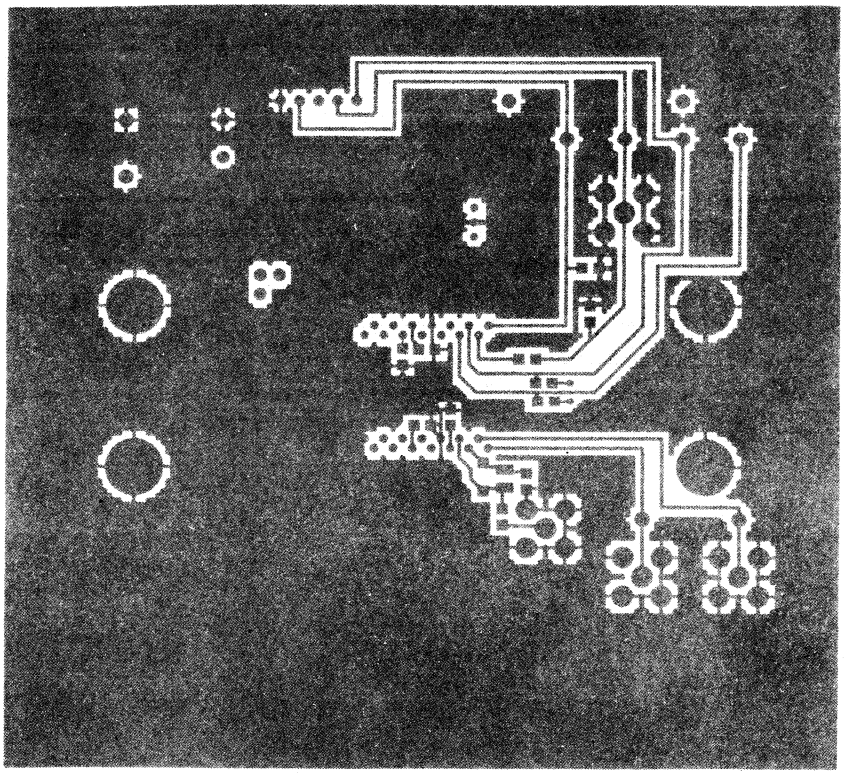


Fig.7 Test circuit; bottom layout.

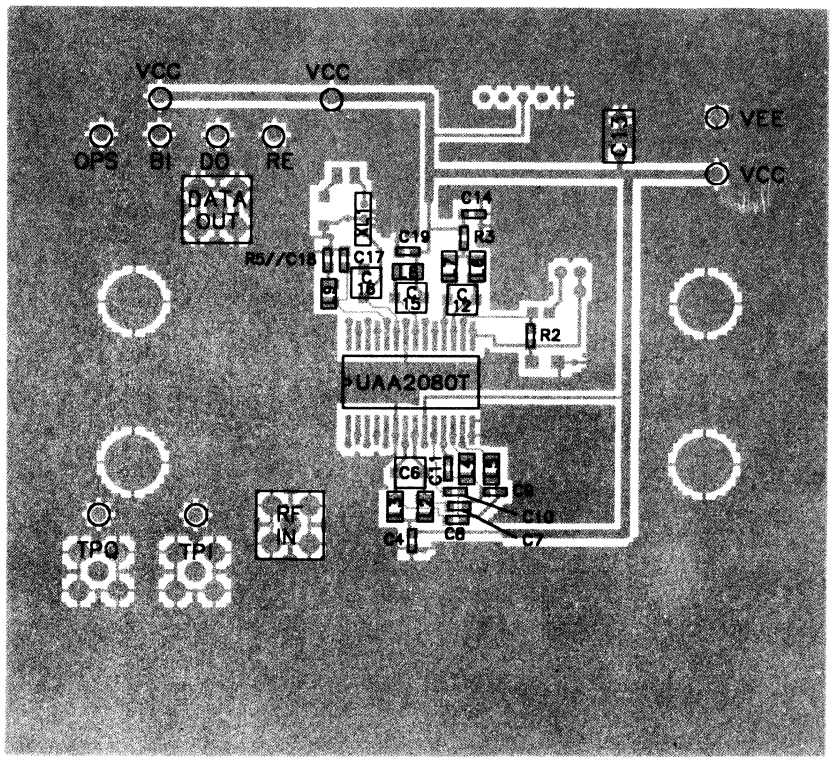


Fig.8 Test circuit; top layout with components (VEE = GND; VCC = V_P; BI = BLI).

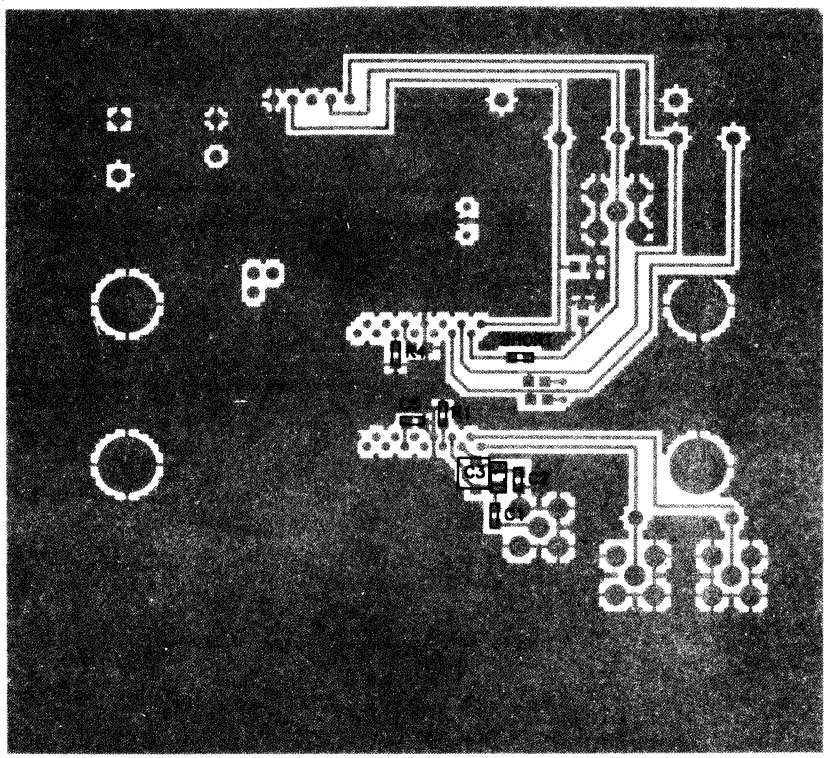


Fig.9 Test circuit; bottom layout with components.

DATA PROCESSOR FOR CELLULAR RADIO RECEIVER (DPROCR)

GENERAL DESCRIPTION

The UMA1001T is a low power CMOS LSI device incorporating the data receiving, data processing, and SAT functions (including on-chip filtering) for an AMPS or TACS hand-held portable cellular radio telephone.

Features

- Single chip solution to all the data handling and supervisory functions
- Configurable to both AMPS and TACS
- I^2C serial bus control
- All analog interface and filtering functions fully implemented on chip
- Robust SAT decoding and transponding circuitry
- Low current consumption
- Small physical size
- Minimum external peripheral components required

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 28)	V_{DD}	4.5	5.0	5.5	V
Supply current (pin 28) normal operation	I_{DD}	–	2	–	mA
Operating ambient temperature range	T_{amb}	−40	–	+ 85	°C

PACKAGE OUTLINE

28-lead mini-pack; plastic (SO28; SOT136A).

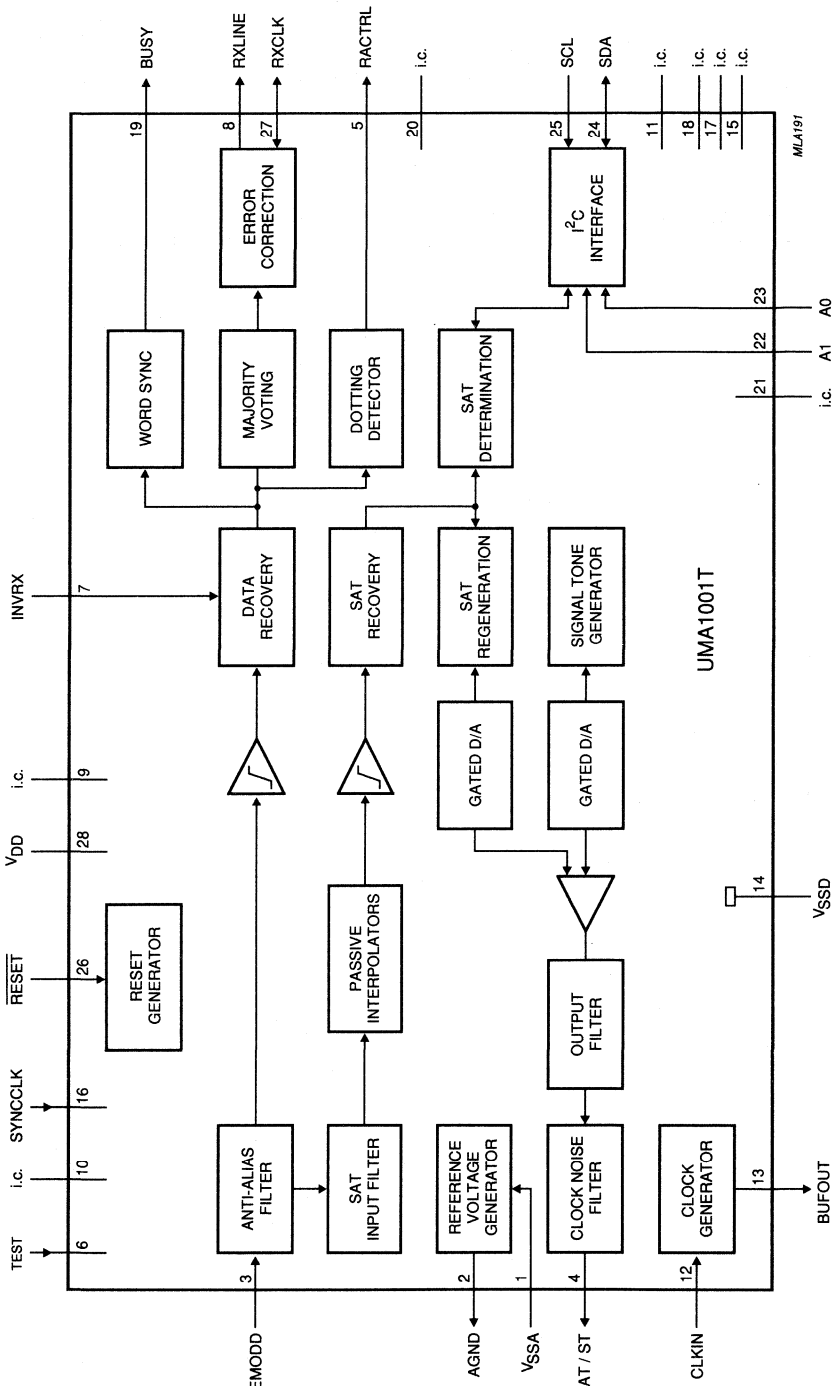


Fig. 1 Block diagram.

DEVELOPMENT DATA

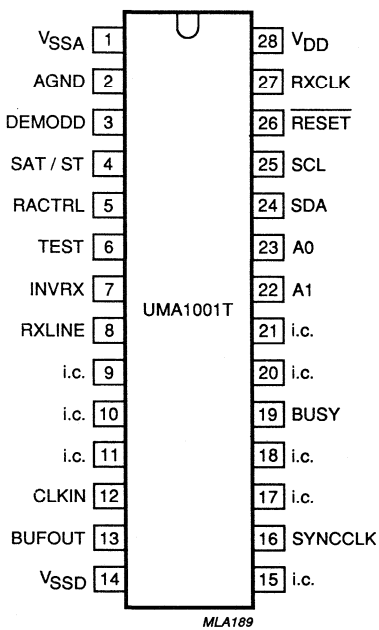


Fig.2 Pinning diagram.

PINNING

1	V_{SSA}	analog negative supply (0 V)
2	AGND	$(V_{DD} - V_{SSA})/2$ analog reference ground
3	DEMODD	received data signal input
4	SAT/ST	transmitted SAT and ST output
5	RACTRL	received audio control output
6	TEST	SCAN Control input - used for power-on reset
7	INVRX	inverts sense of received data stream
8	RXLINE	received data signal output
9	i.c.	internally connected; must be left open-circuit
10	i.c.	
11	i.c.	
12	CLKIN	1.2 MHz external master clock input
13	BUFOUT	buffered output of internal clock oscillator
14	V_{SSD}	digital ground
15	i.c.	internally connected; must be left open-circuit
16	SYNCCLK	SCAN CLOCK Control input - used for power-on reset
17	i.c.	internally connected; must be connected to V_{DD}
18	i.c.	internally connected; must be connected to V_{DD}
19	BUSY	reverse control channel status putput
20	i.c.	internally connected; must be left open-circuit
21	i.c.	internally connected; must be connected to V_{DD}
22	A1	address input 1 - used for power-on reset (I^2C-bus)
23	A0	address input 0 (I^2C-bus)
24	SDA	serial data input/output (I^2C-bus)
25	SCL	serial clock input (I^2C-bus)
26	$\overline{RESET}$	master rest input
27	RXCLK	received data clock input
28	V_{DD}	positive supply voltage (+ 5 V)

CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = −40 to +85 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		V_{DD}	4.5	5.0	5.5	V
Supply current	normal operation	I_{DD}	–	2.0	–	mA
Digital inputs	note 1					
Input voltage LOW		V_{IL}	0	–	0.3 V_{DD}	V
Input voltage HIGH		V_{IH}	0.7 V_{DD}	–	V_{DD} + 0.3	V
Input capacitance		C_I	–	–	6	pF
Digital outputs	note 1					
Output voltage LOW	I_{sink} = 1 mA	V_{OL}	–	–	0.4	V
Output voltage HIGH	I_{source} = 1 mA	V_{OH}	V_{DD}−0.4	–	–	V
Open-drain outputs	note 2					
Output voltage LOW	I_{sink} = 2 mA	V_{OL}	–	–	0.4	V
Open-drain SDA						
Output voltage LOW	I_{sink} = 3 mA	V_{OL}	–	–	0.4	V

Notes to the characteristics

1. All digital inputs and outputs of DPROCR are compatible with standard CMOS devices and the following general characteristics apply.
2. Open-drain outputs have no internal pull-up resistors.

FUNCTIONAL DESCRIPTION

General

The UMA1001T(DPROCR) is a single chip CMOS device which handles the received data and supervisory functions of an AMPS or TACS subscriber set.
These functions are:

- Data reception and transmission
- Control and voice channel exchanges
- Error detection, correction and decoding
- Supervisory Audio Tone decoding and transponding
- Signalling Tone generation

In an AMPS or TACS cellular telephone system, mobile stations communicate with a base over full duplex RF channels. A call is initially set up using one out of a number of dedicated control channels. This establishes a duplex voice connection using a pair of voice channels. Any further transmission of control data occurs on these voice channels by briefly blanking the audio and simultaneously transmitting the data. The data burst is brief and barely noticable by the user. A data rate of 10 kbit/s is used in the AMPS system and 8 kbits/s in TACS. The signalling formats for both Forward Channels (base to mobile) and Reverse Channels (mobile to base) are shown in Fig. 3.

A function known as Supervisory Audio Tone (SAT), a set of 3 audio tones (5970, 6000 and 6030 Hz), is used to indicate the presence of the mobile on the designated voice channel. This signal, which is analagous to the On-Hook signal on land lines, is sent out to the mobile by the base station on the Forward Voice Channel. The signal must be accurately recovered and transponded back to the base station to complete the 'loop'. At the base station this signal is used to ascertain the overall quality of the communication link.

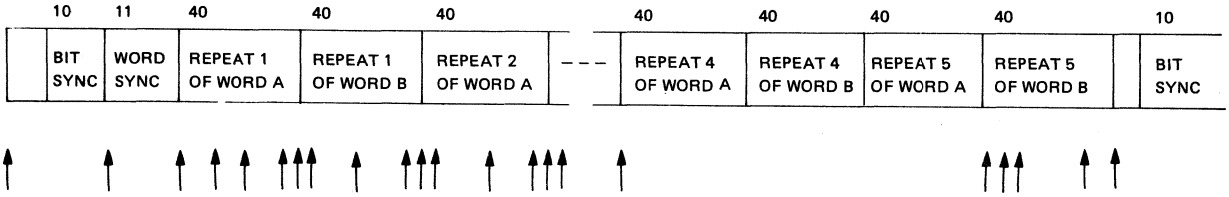
Another voice channel associated signal is Signalling Tone (ST). This tone (8 kHz TACS, 10 kHz AMPS) is generated by the mobile and is sent in conjunction with SAT on the Reverse Voice Channel to serve as an acknowledgement signal to a number of system orders.

The key requirements of a hand held portable cellular set are:

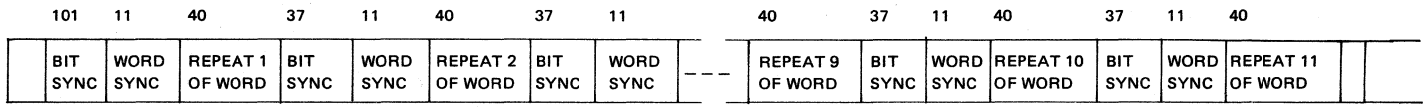
- small physical size
- minimum number of interconnections (serial bus)
- low power consumption
- low cost

The DPROCR is a member of our Cellular Radio chip set, based on the I^2C-bus, which meets these requirements. A cellular radio system schematic using the chip set is shown in Fig. 4.

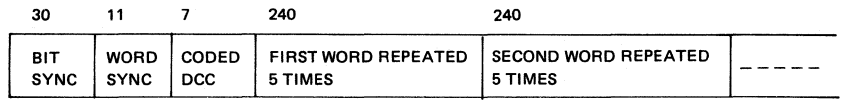
The DPROCR does not perform the reverse voice or control data transmission function.
The microcontroller must contain the hardware and software to frame, BCH and Manchester encode the transmitted data. It must also be capable of generating the data with sufficient timing accuracy.
For a complete solution to data transmission and reception the UMA1000 (DPROC) has to be used.



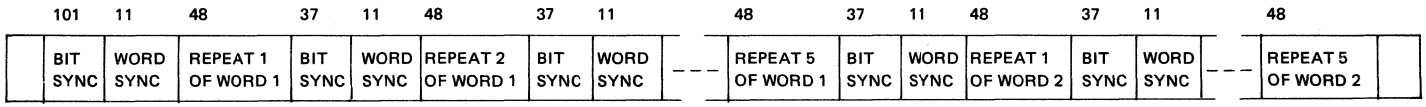
(a) forward control channel



(b) forward voice channel



(c) reverse control channel



(d) reverse voice channel

Fig. 3 Signalling formats.

DEVELOPMENT DATA

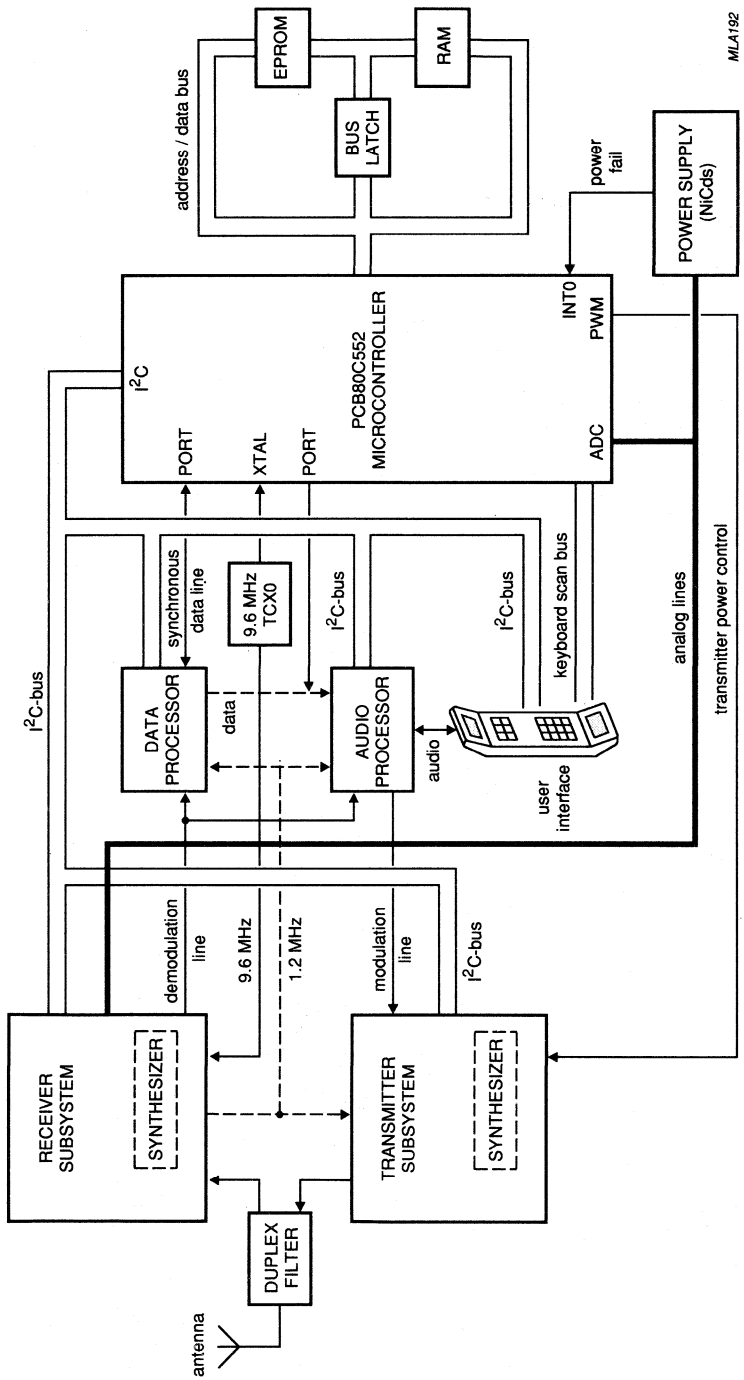


Fig. 4 Cellular radio system schematic.

EXTERNAL PIN DESCRIPTION

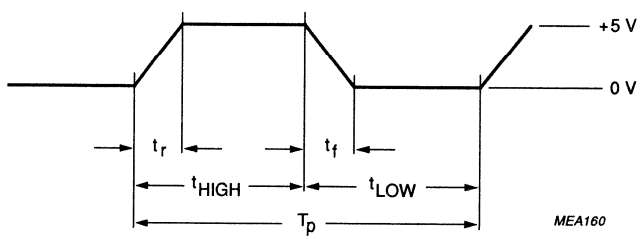
Supply (V_{DD}; V_{SSA}; V_{SSD}; AGND)

V_{DD} : Positive supply voltage for digital and analog circuitry (± 5 V +10%)
V_{SSA} : Negative supply voltage for analog circuitry (0 V)
V_{SSD} : Digital ground (0 V)
AGND: Internally generated reference ground used by internal analog circuitry. Voltage level $(V_{DD} - V_{SSA})/2 \pm 2\%$.

Both V_{SSA} and V_{SSD} must be connected to common ground.

System clock (CLKIN; BUFOUT)

CLKIN is a digital input for the externally generated 1.2 MHz master clock. This signal should be accurate to 100×10^{-6} and have a worst case of 60 : 40 mark-space ratio. BUFOUT is the buffered output of the clock oscillator and provides the option of generating the clock signal on chip by connecting a 1.2 MHz crystal between BUFOUT and CLKIN.



parameter	symbol	min.	typ.	max.	unit
Clock period time	T_p	833.25	833.33	833.42	ns
HIGH time	t_{HIGH}	40%	50%	60%	T_p
LOW time	t_{LOW}	–	$T_p - t_{HIGH}$	–	
Rise time	t_r	–	50	–	ns
Fall time	t_f	–	50	–	ns

I^2C serial data link (SDA; SCL)

SDA is the bi-directional data line; SCL the clock input from an I^2C master. These constitute a typical I^2C link and conform to standard characteristics as defined in the I^2C-bus specification.

- data rate: up to 100 kbit/s

Slave Address Select (A0; A1)

Selection of the device slave address is achieved by connecting A0 to either V_{SSD} or V_{DD} and connecting A1 to either pin 16 and pin 6 or to V_{DD}. The slave address is defined in accordance with the I^2C specifications as shown in Fig. 5.

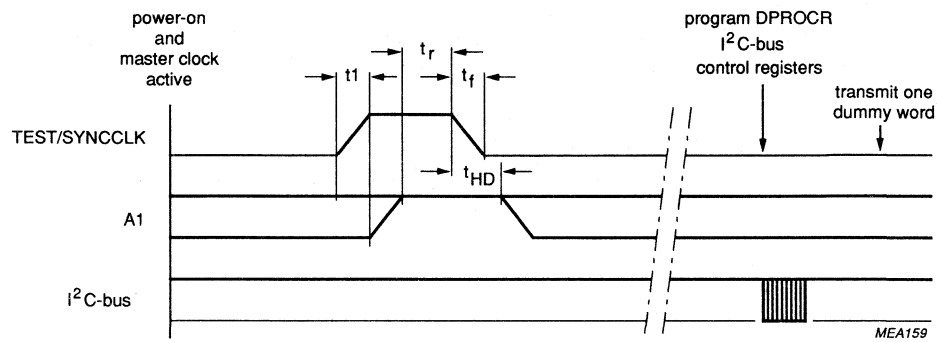
1	1	0	1	1	A1	A0	R/$\overline{W}$

Fig. 5 Device slave address.

Power-up state

DPROCR will not respond reliability to any inputs (including ($\overline{\text{RESET}}$) until 100 μs after the power supply has settled within the specified tolerance. The analog sections of the device will have stabilized within 5 ms. No power-on reset is provided, therefore before the device can enter normal operation TEST and SYNCCLK must be pulsed HIGH. The reset pulse on these pins must have a minimum period of 250 μs and the fall time of the negative going edge must be faster than 1 μs. Pin A1 must remain HIGH during this reset period therefore if the A1 bit of the I^2C address is required to be logic 0. A1 may be connected to TEST and SYNCCLK. If it is required to be at logic 1 then A1 may be permanently connected to V_{DD}. If it is required that A0 = logic 1, then a normal master reset (pin 26) sequence must follow the power-on reset sequence to get the internal registers in the defined state.

Fig.6 shows the power-on reset sequence.



Where:

t1 = time not critical
t_r = reset time = 250 μs max.
t_f = pulse fall time = 1 μs max.
t_{HD} = A1 hold time = 0 μs min.

Note

The RF transmitter is OFF during reset sequence.

Fig.6 Power-on reset programming sequence.

Master reset ($\overline{\text{RESET}}$)

$\overline{\text{RESET}}$ is an asynchronous active LOW master reset input, with a minimum active pulse width of 2 μs which may be used to reset certain logic within DPROCR to a predefined state as illustrated in Tables 1 and 2. Alternatively, DPROCR may be set into a known initial state be setting the I^2C control register as required. The internal reset sequence after a negative pulse on $\overline{\text{RESET}}$ takes 250 μs.

Table 1 Predefined state of the digital output pins

output	state
RXLINE	HIGH
RACTRL	HIGH
BUSY	HIGH

Table 2 Predefined state of the I^2C registers

register	bit							
	7	6	5	4	3	2	1	0
control	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
SATD	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
TST	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW

Data Transfer Link (RXLINE and RXCLK)

RXLINE and RXCLK provide a dedicated serial data link for the transfer of system data message between DPROCR and the system controller at variable rates of up to 200 kbits/s.

- RXCLK : clock input from system controller
- RXLINE : data output from DPROCR to system controller
- data rate : up to 200 kbits/s

Note

A minimum mean data transfer rate for the received data of 2.1 kbits/s (AMPS) and 1.7 kbits/s (TACS) is required to ensure contiguity of message words.

The format for received data words is shown in Fig. 14. The received data timing is illustrated in Fig. 15.

Receiver Audio Enable (RACTRL)

RACTRL is an open-drain digital output used to blank the audio path to the earpiece when a sequence of dotting and word sync is detected.

- output level HIGH : audio enabled
- output level LOW : audio muted

Reverse Control Channel Status (BUSY)

BUSY is a digital output giving the status of the Reverse Control Channel. This is determined by a majority decision on the result of the last 3 consecutive Busy-Idle bits and has the following logic levels:

- output level HIGH : channel busy
- output level LOW : channel idle

On a voice channel BUSY indicates channel idle.

Invert Receive Data (INVRX)

Enables an additional inverter in the receive data path. This allows RF demodulators with high or low local oscillators to be used. The TACS and AMPS specifications define a NRZ encoded logic 1 as a LOW-to-HIGH transition in the centre of a data bit period. The polarity of the demodulated data stream into DPROC depends on the receiver local oscillator.

- input HIGH : data inverted
- input LOW : data normal

Transmitted Data Output (SAT/ST)

Data is an analog output which provides SAT and signalling tone. This signal should normally be AC coupled into the Audio/Data summer.

- DC level : analog ground (AGND)
- signal level : 2 V (p-p) *
- signal tolerance : 2% + supply voltage variation (ΔV_{DD})
- minimum load impedance : 10 kΩ
- maximum load capacitance : 2 nF
- maximum output impedance : 50 Ω

Received Data Input (DEMODD)

Demodd inputs analog data and SAT signals from the RF demodulator. This pin should normally be AC coupled.

- DC level : analog ground (AGND)
- maximum data level : 1 V (p-p)
- nominal data level : 250 mV (p-p)
- minimum data level : 200 mV (p-p)
- minimum SAT level : 50 mV (p-p)
- input impedance : > 1 MΩ

DEVELOPMENT DATA

* Signal level with filtered signalling tone.

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

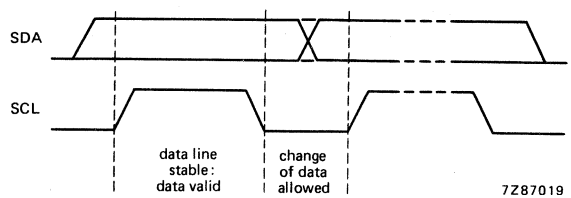


Fig. 7 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

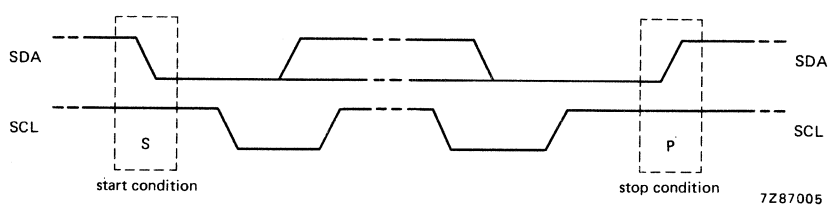


Fig. 8 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

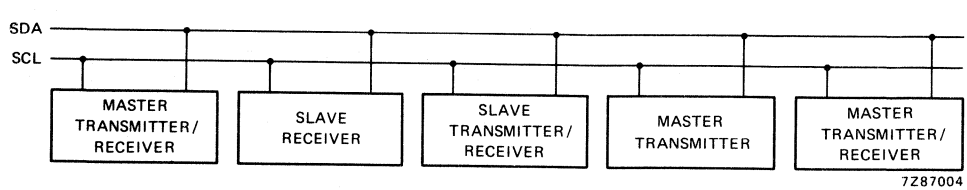


Fig. 9 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

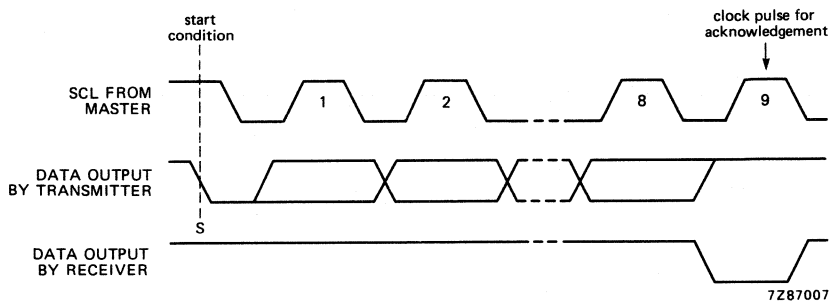


Fig. 10 Acknowledgement on the I^2C-bus.

Timing specifications

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 10.

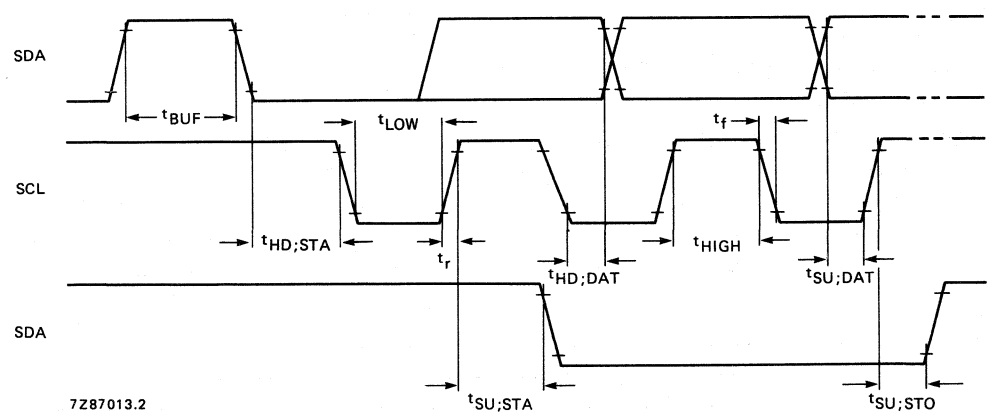


Fig. 11 Timing.

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4.7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_r	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_f	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{DD} to V_{SS}.

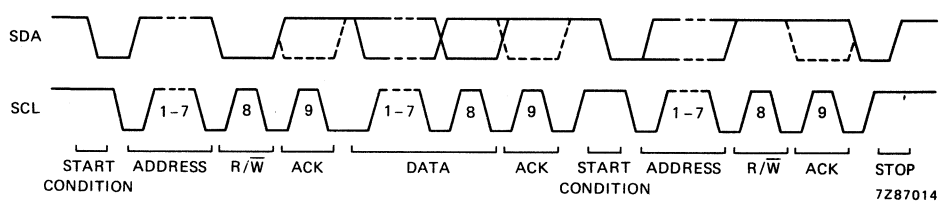


Fig. 12 Complete data transfer.

Where:

Clock t_{LOWmin}	4.7 μs
$t_{HIGHmin}$	4 μs

The dashed line is the acknowledgement of the receiver

Max. number of bytes	Unrestricted
Premature termination of transfer	Allowed by generation of STOP condition
Acknowledge clock bit	Must be provided by the master

I²C REGISTERS

General

The I²C register block resides internally within the I²C interface block and contains various items of status and control information which are transferred to and from DPROCR via the I²C-bus. The block is organized into four 8-bit registers:

- Status Register — contains read only items
- Control Register
- SAT Programmable Phase Shift Register — contain write only items
- TEST Register

Note

In normal operation the SAT delay register and the TEST register require programming only after a device reset.

Table 3 Register map

register	bit							
	7	6	5	4	3	2	1	0
status	–	–	WSYNC	BUSY	–	–	MSCC1	MSCC0
control	–	SERV	STS	0	0	FVC	STEN	SATEN
SATD	<---------- SAT delay data ---------->							

S	DPROCR ADR	R	A	STATUS	A	P

(a) read from DPROCR status register

S	DPROCR ADR	W	A	CONTROL	A	P

(b) write to DPROCR control register

S	DPROCR ADR	W	A	CONTROL	A	SAT DELAY	A	TEST	A	P

(c) write to all DPROCR registers

Where:

S	: START condition
W	: read/write bit (logic 0 = write)
R	: read/write bit (logic 1 = read)
A	: acknowledge bit
P	: STOP condition
DPROC ADR	: slave address of DPROCR
TEST	: must be programmed to logic 0 for normal operation

Fig.13 I²C data format.

Status Register

This is a read only register containing DPROCR status information.

Measured SAT Colour Code (MSCC1; MSCC0)

MSCC1 and MSCC0 provide information about the current measured SAT colour code in accordance with Table 4.

Table 4 Measured SAT Colour Code

MSCC1	MSCC0	SAT frequency (Hz)
0	0	5970
0	1	6000
1	0	6030
1	1	no valid SAT

Reverse Control Channel Status (BUSY)

BUSY gives the status of the Reverse Control Channel. This is determined by a majority decision on the result of the last 3 consecutive Busy-Idle bits on the Forward Control Channel.

- logic 1 : channel busy
- logic 0 : channel idle

On a voice channel the BUSY bit defaults to the set state.

Note

This signal is also routed to the BUSY output pin.

Word Synchronization Indicator (WSYNC)

WSYNC indicates whether DPROCR has acquired frame synchronization according to the Forward Control Channel format.

- logic 1 : frame synchronization acquired
- logic 0 : no frame synchronization

Control Register

This is a write only register containing DPROC control information.

SAT Path Enable (SATEN)

SATEN enables the SAT transponded signal to be output on external pin DATA.

- logic 1 : SAT tone enabled
- logic 0 : SAT tone inhibited

Signalling Tone (ST) Path Enable (STEN)

STEN enables the Signalling Tone to be output on external pin Data.

- logic 1 : ST enabled
- logic 0 : ST inhibited

I^2C REGISTERS (continued)

Channel Format Select (FVC)

FVC selects the required channel format.

- logic 1 : Voice channel format
- logic 0 : Control channel format

System Type Select (STS)

STS selects required system format.

- logic 1 : AMPS
- logic 0 : TACS

Note

Toggling this signal also resets the receive logic in DPROC.

Serving System Select (SERV)

SERV selects which of the serving system data streams (A or B) is accepted.

- logic 1 : system A selected
- logic 0 : system B selected

SAT Programmable Delay Register (SATD)

SATD programs the value of phase shift which is applied to the SAT tones in the SAT Regeneration Block. This value will be determined and programmed into the System Controller during manufacture. The recovered SAT is delayed in time by approximately 0.8 μs x value in the register which corresponds to approximately 1.8 degrees x value in the register. The total phase shift is limited to 360 degrees. For normal use in AMPS and TACS, this function is not necessary and should programmed to zero.

DIGITAL CIRCUIT BLOCKS

General

The majority of the digital circuitry within the DPROCR device is identical for both AMPS and TACS. The device has little additional redundancy to implement both systems. The functions of these blocks are described in the following sections and relate to those shown in Fig. 1.

Data Recovery

The Data Recovery Block receives wideband Manchester encoded data in sampled and sliced form from the Strobed Comparator Block, on which it performs the following functions:

- clock recovery
- Manchester decoding
- data regeneration

The Clock Recovery Block extracts an 8 or 10 kHz (TACS or AMPS) phase locked clock signal from the Manchester encoded data stream. This is implemented using a digital phase-locked loop (PLL) which has an adjustable "bandwidth" to provide both fast acquisition and low jitter.

Manchester decoding is performed by exclusive ORing the recovered Manchester encoded data with the recovered clock.

The NRZ data regeneration is performed by a digital integrate and dump circuit. This consists of an up/down counter that counts 1.2 MHz cycles during the data period. The sense of the count is determined by the result of the Manchester Decoder output. The number of counts is sampled at the end of a data period. If this number exceeds a threshold the data is latched as a 1 otherwise it is latched as a 0.

SAT Processing

The Supervisory Audio Tone processing consists of the following functions:

- SAT recovery
- SAT determination
- SAT regeneration

SAT recovery

The SAT Recovery Block receives a filtered and sliced SAT signal which must be recovered before being routed to the Determination and Regeneration Blocks.
The recovery is performed using a digital phase-locked loop.

SAT determination

The SAT Determination Block indicates which, if any, of the valid SAT tones is detected from the recovered SAT. The AMPS and TACS specifications require that a determination is made at least every 250 ms. Determination involves counting the number of cycles of the regenerated SAT in this time period. This count is then compared to a set of four known counts which define the boundaries between the SAT frequencies and the SAT not valid events. The result is then coded into the I^2C status registers MSCC0 and MSCC1 as shown in Table 5.

Table 5 Status registers MSCC0, MSCC1; decoded SAT frequencies

register		SAT frequency band (Hz ± 4 Hz)	decoded SAT (Hz)
MSCC0	MSCC1		
1	1	< 5956	not valid
0	0	5956 to 5986	5970
0	1	5986 to 6014	6000
1	0	6014 to 6046	6030
1	1	> 6046	not valid

SAT regeneration

The SAT Regeneration Block generates a digital SAT stream from the recovered SAT stream for transponding back to the base station. The AMPS and TACS specifications require the SAT to be transponded with a maximum phase shift of 20 degrees between the point the modulated RF signal enters the mobile from the base station, and the point the modulated RF leaves the mobile. A variable phase compensation circuit is provided in DPROCR to shift the recovered SAT through 0 to 360 degrees before being passed to the output summing network. The degree of phase shift is determined during manufacture of the set and the required additional phase shift is stored in non-volatile RAM and programmed via I^2C at each power-on cycle. The phase correction is performed by a counter delay method using signals which are phase locked to the recovered SAT.

DEVELOPMENT DATA

Dotting Detector

The Dotting Detector Block determines whether a data inversion (dotting) pattern has been received on the Forward Voice Channel. The detection of 32 bits of data inversion indicates that the Clock Recovery Block has acquired bit synchronization and that the narrow bandwidth mode on the clock recovery phase-locked loop is selected. This signal is also used to indicate that a data burst is expected and activates the audio mute RACTRL for the duration of the burst. The RACTRL signal is triggered by the detection of a WSYNC sequence after bit synchronization has been acquired.

Word Synchronization Detector

The Word Synchronization Block performs the following functions:

- Frame synchronization
- Reverse Control Channel status (B/I determination)
- Valid Serving System determination

These functions are associated solely with the Forward Control Channel and have no meaning on the Forward Voice Channel.

Information in a data stream is identified by its position with respect to a unique synchronization word. This synchronization word is an 11 bit-Barker code which has a low probability of simulation in an error environment, and can be easily detected. Data received is only considered valid at times when DPROCR has achieved frame synchronization. In this condition the block leaves its search mode and enters its lock mode. This is indicated by bit WSYNC being set HIGH. In order to achieve this two consecutive synchronization words separated by 463 bits must be detected. Once in lock mode, the synchronization word detector is examined every 463 bits and only loses frame synchronization after 5 consecutive unsuccessful attempts at detecting the synchronization word have been made. At this point bit WSYNC is cleared and the device is returned to its search mode. On the Forward Voice Channel detection of the synchronization word indicates that the following 40 bits are valid data. Information detailing the status of the Reverse Control Channel is given by the Busy/Idle bits. These occur at intervals of 11 bits within the frame, the first occurring immediately following the synchronization word. The status of the channel is determined by a majority decision on the last three consecutive Busy/Idle bits.

Majority Voting Block

The Majority Voting Block performs the following functions:

- identifying position and validity of frames in the received data stream
- extracting 5 repeats of each word from a valid frame
- performing a bit-wise majority decision on the five repeats of the data word

The validity of the frames is determined by setting a counter in operation which times out and resets the circuitry after 920 or 463 bit periods from detecting valid word synchronization. The time out period selected depends on whether DPROCR is monitoring the Forward Voice or Control Channel respectively.

Up to five repeats of the message word are searched for and extracted by DPROCR. On the forward Voice Channel DPROCR will extract the first five words that occur for which a correct synchronization word is found. These words can occur in any position in the frame. A serial majority vote is performed as the fifth word is being extracted.

Error Correction Block

The Error Correction Block performs the following functions:

- extraction of a valid message from the Majority-Voted Word
- computation of the S1 and S3 syndromes
- correction of up to one error in the word
- communication of received data to the System Controller via the Received Data Serial Link.

Interpretation of parity of a received word is obtained from knowledge of the syndromes of the word. The syndromes are calculated using feedback shift registers with two characteristic equations:

$$1 + X + X^6 \text{ and } 1 + X + X^2 + X^4 + X^6$$

Once the syndromes of a received word are known, it is possible to determine if a correctable error is present. DPROCR only corrects up to one error although the code used has a Hamming distance of five. The occurence of two or more errors is signalled by setting the BCH error flag, which is communicated to the System Controller via the Received Data Serial Link.

Signal Tone Generation (ST)

The 8 or 10 kHz (TACS or AMPS) tone generator can be switched into the DPROCR outputs as the Signalling Tone stream under I^2C control.

Received Data Serial Link

The Received Data Serial Link transfers data and control information from DPROCR to the System Controller. The data is transferred on RXLINE under control of a clock signal RXCLK, generated by the System Controller. The system controller is informed of the arrival of a decoded data word in the DPROCR output register by RXLINE being driven LOW. If the system controller chooses to ignore the received data or only partially clock the data out, the DPROCR will reset the receive buffer for the next word after the period RWIN (see Fig. 15).

Data Format

Each Received Data word consists of 4 bytes. The word format is shown in Fig. 14. The sense and function of the fields is shown in Table 6.

Table 6 Received Data word

bit	title	sense	function
31	start	LOW	identifies start of word
30	BCH error	active HIGH	indicates that an uncorrected BCH error is associated with the word
29 to 2	received data	binary data	received data word
1	RXLINE error	LOW	if detected as HIGH indicates that a transmission error has occured on the microprocessor to DPROCR serial link
0	stop	HIGH	identifies end of the word

Link Protocol

The Received Data protocol is described by the timing diagram Fig. 15 and has the following parameters:

- maximum receive window (RWIN)
  Control Channel (TACS) = 47 ms
  Control Channel (AMPS) = 37 ms
- minimum clock period ($t_{CLK(min)}$) = 2 μs
- minimum clock hold-off (t_{wait}) = 100 μs

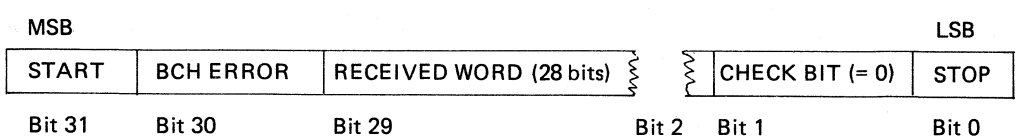


Fig. 14 Received data word.

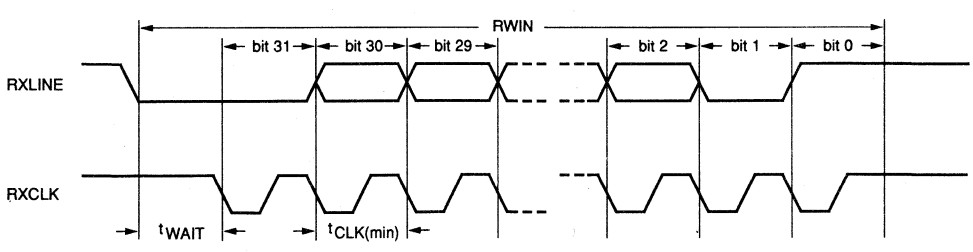


Fig. 15 DPROCR to microcontroller link; received data timing.

ANALOG CIRCUIT BLOCKS

General

The analog signal processing functions on DPROCR are implemented using switched-capacitor techniques. The main filtering functions are operated at 300 kHz, and these circuits are 'interfaced' to the continuous time and sampled digital domains by distributed RC active filters, passive interpolators and comparators.

The distributed RC sections, the Anti-Alias Filter and the Clock Noise Filter, are non-critical and are designed to tolerate process spreads. The critical filtering in the SAT Filter and the Output Filter, is performed by 300 kHz switched-capacitor circuitry. The Passive Interpolators increase the sampling rate from 300 kHz to 1.2 MHz. The sampled analog signals from the Passive Interpolators are converted to sampled 2-state digital signals by the Strobed Comparators. The Gated Digital-to-Analog converters and Analog Summer blocks perform resynchronization and sub-sampling of the digitally generated DPROCR output signals, and conversion to the sampled analog domain.

These analog sections of the device are shown in Fig. 1.

Reference Voltage Generator

The Reference Voltage Generator generates the analog ground reference voltage (AGND) used internally within the DPROCR device. To minimize noise AGND must be externally decoupled to V_{SSA} as shown in Fig. 16.

Anti-Alias Filter

The Anti-Alias Filter is placed before the SAT sampling block to prevent any unwanted signals or high-frequency noise present on the DEMODD pin being aliased into the pass-band by the sampling action of the switched-capacitor filter. To achieve this the Anti-Alias Filter is a continuous time-distributed RC-active low-pass filter.

SAT Input Filter

The SAT Input Filter is a switched-capacitor filter which provides band-pass filtering of the SAT signals from the DEMODD pin to improve the SAT signal-to-noise ratio prior to recovery and transponding.

Passive Interpolator

The function of the Passive Interpolator is to increase the sampling rate at the output of the switched-capacitor filters. This reduces the coarseness of the zero crossing information which would otherwise cause unacceptable isochronous distortion in the recovered signal.

Strobed Comparators

The Strobed Comparators form the analog-to-digital interface for the received data and SAT signals from the DEMODD pin. These comparators act as limiting amplifiers wich convert the filtered sampled analog signals into 2-state sampled digital signals containing only the zero-crossing information from the analog signal.

ANALOG CIRCUIT BLOCKS (continued)

Gated Digital-to-Analog and Analog Summer

The Gated Digital-to-Analog converters and Analog Summer form the interface between the digital and analog circuitry on the transmit path of DPROCR. It is at this point that the three sampled digital signals, containing SAT and ST, are combined to form a composite signal. The data streams are enabled by the I^2C signals STEN and SATEN. The digital-to-analog conversion and sub-sampling operation is performed by the Gated Digital-to-Analog converters and Analog Summer. The relative signal weights applied in the summer (with respect to the data path) are shown in Table 7.

Table 7 Relative signal weights

signal	relative output level AMPS and TACS
ST	1.0
SAT	0.25

Output Filter

The Output Filter is a switched-capacitor filter which performs band-limiting of the DPROCR output signals in accordance with the AMPS and TACS specifications. The required below band roll-off is achieved via external AC coupling from the SAT/ST pin.

Clock Noise Filter

The filter is a non-critical continuous time-distributed RC-active low-pass filter used to remove any switching transient residues from the output signal.

APPLICATION INFORMATION

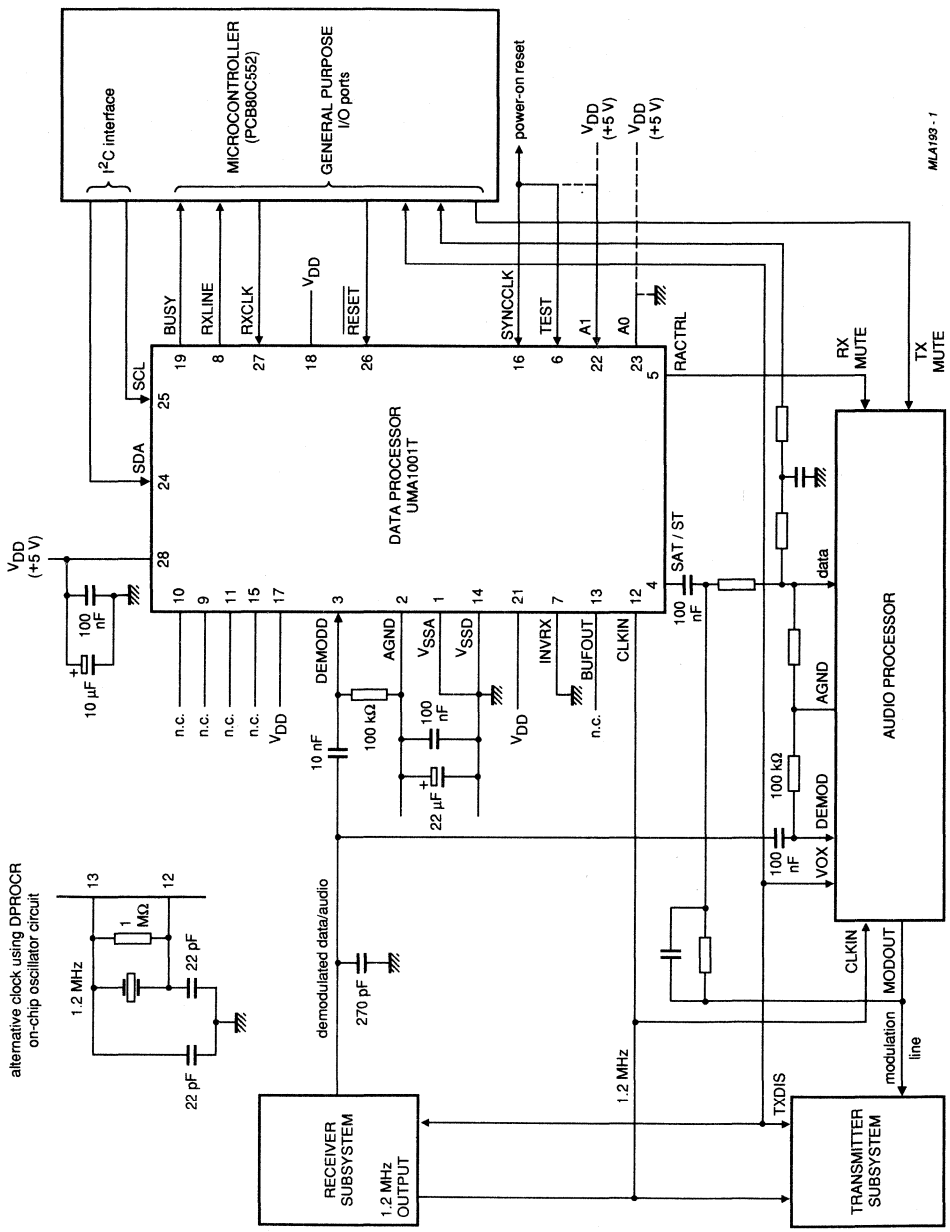


Fig.16 DPROCR application circuit.

Dual low-power frequency synthesizer

UMA1005T

FEATURES

- Fast locking by "Fractional-N" divider
- Auxiliary synthesizer
- Digital phase comparator with proportional and integral charge pump output
- High speed serial input
- Low power consumption
- Programmable charge pump currents

APPLICATIONS

- Mobile telephony
- Portable battery-powered radio equipment

DESCRIPTION

The UMA1005 is a low power, high performance frequency synthesizer in CMOS technology. This integrated circuit is designed to achieve 10 to 2000 kHz channel spacing. The channel is selected via a high speed serial interface.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
UMA1005T	20	SSOP20	plastic	SOT266AG

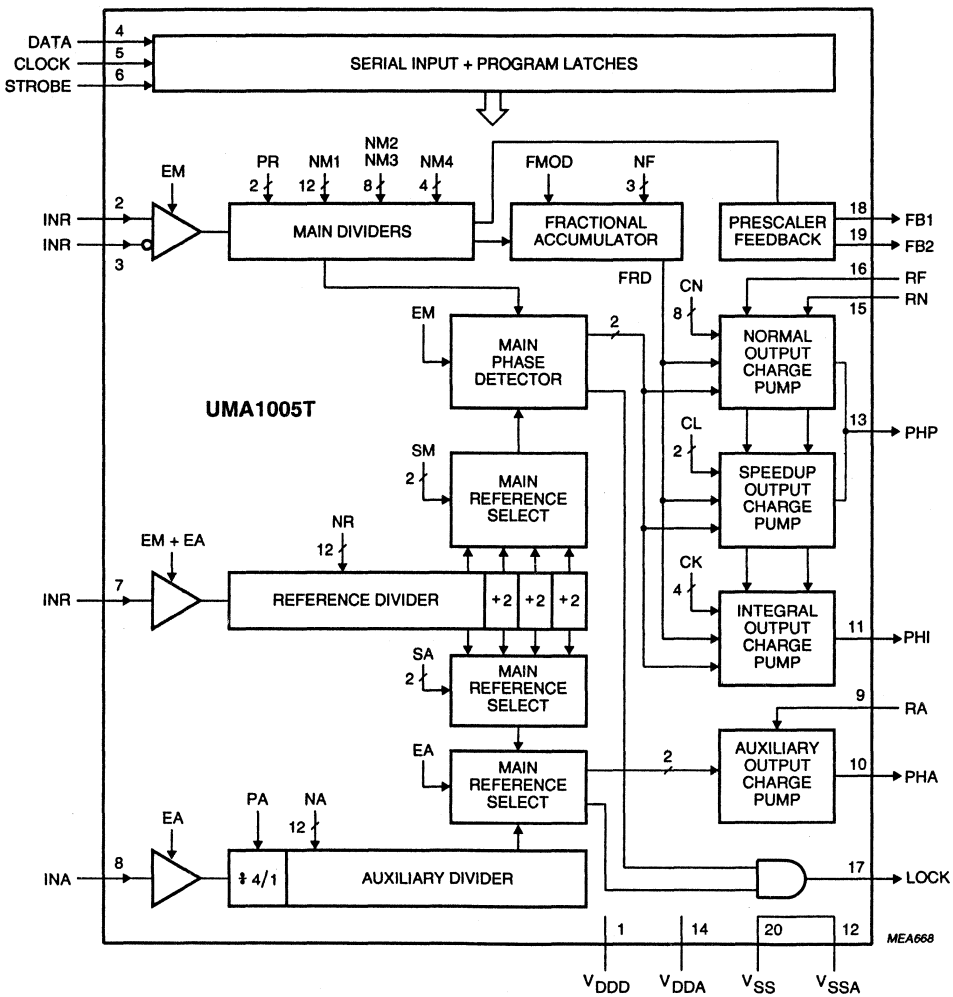


Fig.1 Block diagram.

PINNING

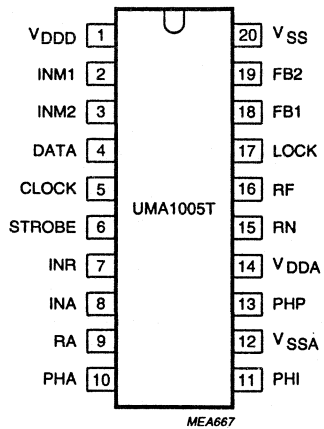


Fig.2 Pin configuration.

SYMBOL	PIN	DESCRIPTION
V_{DDD}	1	digital supply voltage
INM1	2	main divider positive input; rising edge active
INM2	3	main divider negative input; falling edge active
DATA	4	serial data input line
CLOCK	5	serial clock input line
STROBE	6	serial strobe input line
INR	7	reference divider input line; rising edge active
INA	8	auxiliary divider input line; rising edge active
RA	9	auxiliary current setting; resistor to V_{SS}
PHA	10	auxiliary phase detector output
PHI	11	integral phase detector output
V_{SSA}	12	analog ground; internally connected to V_{SS}
PHP	13	proportional phase detector output
V_{DDA}	14	analog supply voltage
RN	15	main current setting; resistor to V_{SS}
RF	16	fractional compensation current setting; resistor to V_{SS}
LOCK	17	lock detector output
FB1	18	feedback output 1 for prescaler modulus control
FB2	19	feedback output 2 for prescaler modulus control
V_{SS}	20	common ground connection

Low-power frequency synthesizer for mobile radio communications

UMA1014

FEATURES

- Single chip synthesizer; compatible with Philips cellular radio chipset
- Fully programmable RF divider
- I²C interface for two-line serial bus
- On-chip crystal oscillator/TCXO buffer from 3 to 16 MHz
- 16 reference division ratios allowing 5 to 100 kHz channel spacing
- 1/8 crystal frequency output
- On-chip out-of-lock indication
- Two extra VCO control outputs
- Latched synthesizer alarm output
- Status register including out-of-lock indication and power failure
- Power-down mode.

GENERAL DESCRIPTION

The UMA1014 is a low-power universal synthesizer which has been designed for use in channelized radio communication. The IC is manufactured in bipolar technology and is designed to operate at 5 to 100 kHz channel spacing with an RF input from 50 to 1100 MHz. The channel is programmed via a standard I²C-bus. A low-power sensitive RF divider is incorporated together with a dead-zone eliminated, 3-state phase comparator. The low-noise charge pump delivers 1 mA or 1/2 mA output current to enable a better compromise between fast switching and loop bandwidth. A power-down circuit enables the synthesizer to be set to idle mode.

APPLICATIONS

- Cellular mobile radio (NMT, AMPS, TACS)
- Private mobile radio (PMR)
- Cordless telephones

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}, V_{CP}	supply voltage range	4.5	5.0	5.5	V
$I_{CC} + I_{CP}$	supply current	–	13	–	mA
I_{CCpd}	I_{CC} in power-down	–	2.5	–	mA
f_{ref}	phase comparator reference frequency	5	–	100	kHz
f_{RF}	RF input frequency	50	–	1100	MHz
T_{amb}	operating ambient temperature range	–40	–	85	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
UMA1014T	16	SO16	plastic	SOT109A

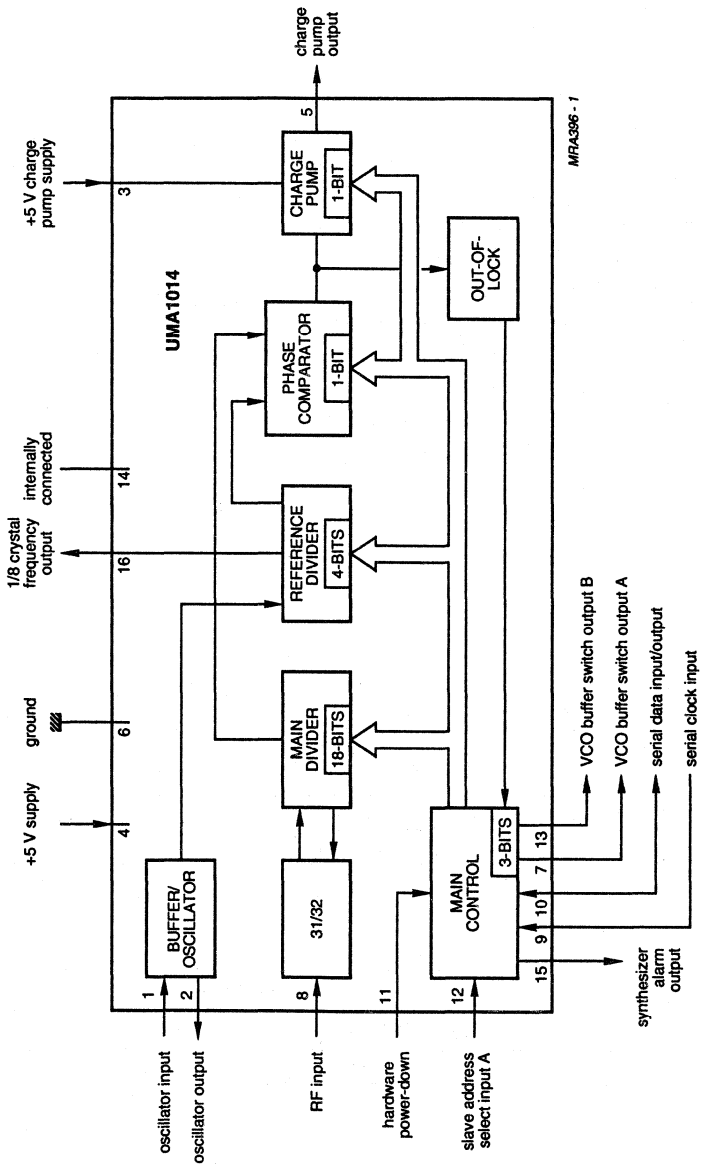


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
OSCIN	1	oscillator or TCXO input
OSCOUT	2	oscillator output
V_{CP}	3	5 V charge pump supply
V_{CC}	4	5 V supply
PCD	5	charge pump output
GND	6	ground
VCOA	7	VCO buffer switch output A (including out-of-lock)
RF	8	RF input
SCL	9	serial clock input
SDA	10	serial data input/output
$\overline{HPD}$	11	hardware power-down (active LOW)
SAA	12	slave address select input A
VCOB	13	VCO buffer switch output B
i.c.	14	internally connected
SYA	15	synthesizer alarm output
FX8	16	1/8 crystal frequency output

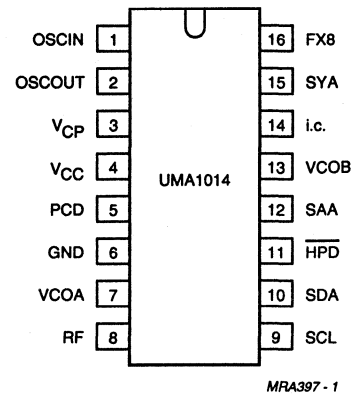


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The UMA1014 is a low-power frequency synthesizer for radio communication which operates in the 50 to 1100 MHz range. The device includes an oscillator/buffer circuit, a reference divider, an RF divider, a 3-state phase comparator, a charge pump and a main control circuit to transfer the serial data into the four internal 8-bit registers. The V_{CC} supply feeds the logic part, the V_{CP} supply feeds the charge-pump only. Both supplies are +5 V (±10%). The power-down facility puts the synthesizer in the idle mode (all current supplies are switched off except in the control part). This allows any I²C transfer and all information in the registers is retained thus enabling fast power-up.

Main divider

The main divider is a pulse swallow type counter which is fully programmable. After a sensitive input amplifier (50 mV, −13 dBm), the RF signal is applied to a 31/32 duo-modulus counter. The output is then used as the clock for the 5-bit swallow counter R = (MD4 to MD0) and the 13-bit main counter N = (MD17 to MD5). The ratio is transferred via the I²C-bus to the registers B, C and D, and then buffered in an 18-bit latch. The ratio in the divider chain is updated with the new information when the least significant bit is received (i.e. D0). This update is synchronized to the output of the divider in order to limit the phase error during small jumps of the synthesized frequency.

The main divider can be programmed to any value between 2048 and 262143 (i.e. $2^{18}-1$). If ratio X, below 2048, is sent to the divider, the ratio (X + 2048) will be programmed. When it is required to switch between adjacent channels it is possible to program register D only, thus allowing shorter I²C programming time.

Oscillator

The oscillator is a common collector Colpitts type with external capacitive feedback. The oscillator has very small temperature drift and high voltage supply rejection. A TCXO or other type of clock can be used to drive the oscillator by connecting the source (preferably AC-coupled) to pin 1 and leaving pin 2 open-circuit. The oscillator acts as a buffer in this mode and requires no additional external components. The signal from the clock source should have a minimum space width of 31 ns.

Reference divider

The reference divider is semi-programmable with 16 division ratios which can be selected via the I²C-bus. The programming uses four bits of the register A (A3 to A0) as listed in Table 2. These ratios allow the use of a large number of crystal frequencies from 3 MHz up to 16 MHz. All main channel spacings can be obtained with a single crystal/TXCO frequency of 9.6 MHz.

Phase comparator

A diagram of the phase comparator and charge pump is illustrated in Fig.3.

The phase comparator is both a phase and frequency detector. The detector comprises dual flip-flops together with logic circuitry to eliminate the dead-zone. When a phase error is detected the UP or DOWN signal goes HIGH. This switches on the corresponding current generator which produces a source or sink current for the loop filter. When no phase error is detected PCD goes high impedance. The final tuning voltage for the VCO is provided by the loop filter. The charge pump current is programmable via the I²C-bus. When IPCD (bit 5) is set to logic 1 the charge pump delivers 1 mA; when IPCD is set to logic 0 the charge pump delivers 0.5 mA.

The phase comparator has a phase inverter logic input (PHI). This allows the use of inverted or non-inverted loop filter configurations. It is thus possible to use a passive loop filter which offers higher performances without an operational amplifier. The function of the phase comparator is given in Table 3 and a typical transfer curve is illustrated in Fig.4.

Out-of-lock detector

An out-of-lock detector using the UP and DOWN signals from the phase comparator is included on-chip. The pin VCOA is an open collector output which is forced LOW during an out-of-lock condition. The same information is also available via the I²C-bus in the status register (bit OOL). When the phase error (measured at the phase comparator) is greater than approximately 200 ns, an out-of-lock condition is immediately flagged. The flag is only released after 6 reference cycles when the phase error is less than 200 ns.

Table 1 Division ratio in the main divider

MAIN COUNTER: N								SWALLOW COUNTER: R		
MD17	MD16	MD15	...	MD8	MD7	...	MD5	MD4	...	MD0
B1	B0	C7	...	C0	D7	...	D5	D4	...	D0
MSB										LSB

Table 2 Reference divider programming

A3(RD3)	A2(RD2)	A1(RD1)	A0(RD0)	REFERENCE DIVISION RATIO	CHANNEL SPACING FOR 9.6 MHz AT OSCIN
0	0	0	0	128	75 kHz
0	0	0	1	160	60 kHz
0	0	1	0	192	50 kHz
0	0	1	1	240	40 kHz
0	1	0	0	256	37.5 kHz
0	1	0	1	320	30 kHz
0	1	1	0	384	25 kHz
0	1	1	1	480	20 kHz
1	0	0	0	512	18.75 kHz
1	0	0	1	640	15 kHz
1	0	1	0	768	12.5 kHz
1	0	1	1	960	10 kHz
1	1	0	0	1024	9.375 kHz
1	1	0	1	1280	7.5 kHz
1	1	1	0	1536	6.25 kHz
1	1	1	1	1920	5 kHz

Table 3 Operation of the phase comparator

	PHI = 0 (PASSIVE LOOP FILTER)			PHI = 1 (ACTIVE LOOP FILTER)		
	$f_{ref} < f_{var}$	$f_{ref} > f_{var}$	$f_{ref} = f_{var}$	$f_{ref} < f_{var}$	$f_{ref} > f_{var}$	$f_{ref} = f_{var}$
UP	0	1	0	1	0	0
DOWN	1	0	0	0	1	0
I_{pcd}	−1 mA	1 mA	< ±5 nA	1 mA	−1 mA	< ±5 nA

MAIN CONTROL

The control part consists mainly of the I²C-bus control interface and a set of four registers A, B, C and D. The serial input data (SDA) is converted into 8-bit parallel words and stored in the appropriate registers. The data transmission to the synthesizer is executed in the burst mode with the following format:

//slave addr./subaddr./data1/data2/.../datan// ; n up to 4

Data byte 1 is written in the register indicated by the subaddress. An auto-increment circuit, if enabled (AVI = 1), then provides the correct addressing for the ensuing data bytes. Since the length of the data burst is not fixed, it is possible to program only one register or the whole set. The registers are structured in such a way so that the burst, for normal operation, is kept as short as possible. The bits that are only programmed during the set-up (reference division ratio, power-down, phase inversion and current on PCD) are stored in registers A and B.

In the slave address six bits are fixed, the remaining two bits depend on the application.

Table 4 Slave address

1	1	0	0	0	1	$\overline{SAA}$	R/$\overline{W}$

SAA is the slave address. When SAA goes HIGH then $\overline{SAA}$ = 0, when SAA goes LOW then $\overline{SAA}$ = 1. This allows the use of two UMA1014s on the same bus but using a different address. R/$\overline{W}$ should be set to logic 0 when writing to the synthesizer or set to logic 1 when reading the status register.

The subaddress includes the register pointer, and sets the two flags related to the auto-increment (AVI) and the alarm disable (DI)

Table 5 Subaddress

X	X	X	DI	AVI	X	SB1	SB0

Where:

X = not used

DI (Disable Interrupt):
DI = 1 disables the alarm on SYA
DI = 0 enables the alarm.

AVI (Auto Value Increment):
AVI = 1 enables the automatic increment
AVI = 0 disables the auto-increment.

SB1/SB0 are the pointers of the register where DATA1 will be written (see Table 6).

When the auto-increment is disabled (AVI = 0), the subaddress pointer will maintain the same value during the I²C-bus transfer. All the data bytes will then be written consecutively in the register pointed by the subaddress.

Table 6 Pointer of the registers

SB1	SB0	REGISTER POINTED
0	0	A
0	1	B
1	0	C
1	1	D

Status register and synthesizer alarm

When an out-of-lock condition or a power dip occurs, SYA, which is an open collector output, is forced LOW and latched. The pin SYA will be released after the status register is read via the I²C-bus.

The status register contains the following information:

Table 7 Status register

0	0	0	OOL	0	LOOL	LPD	DI

Where:

OOL = momentary out-of-lock
LOOL = latched out-of-lock
LPD = latched power dip
DI = disable interrupt (of the last write cycle)

The I²C-bus protocol to read this internal register is a single byte without subaddressing:

//slave address (R/$\overline{W}$ = 1)/status register (read)//

Table 8 Bit allocation

REGISTER	POINTER	BIT ALLOCATION								PRESET
		7	6	5	4	3	2	1	0	
A	00	PD	X	IPCD	X	RD3	RD2	RD1	RD0	00001110
B	01	1	0	1	PHI	VCOB	VCOA	MD17	MD16	10100101
C	10	MD15	MD14	MD13	MD12	MD11	MD10	MD9	MD8	00111000
D	11	MD7	MD6	MD5	MD4	MD3	MD2	MD1	MD0	10000000

Where X = not used

Table 9 Register allocation

REGISTER NAME	BIT NAME	FUNCTION		PRESET VALUE
A	PD	power down	PD = 0 normal operation	0
	IPCD	programmable charge pump current	IPCD = 1 = 1 mA; IPCD = 0 = 0.5 mA	0
	RD3...RD0	reference ratio	see Table 2	1110; r = 1536
B	PHI	phase inverter	PHI = 0 passive loop filter	0
	VCOA	VCO switch A	set pin 7	1
	VCOB	VCO switch B	set pin 13	0
	MD17, MD16	bits 17 and 16	MSB of main divider ratio	01
C	MD15 to MD8	bits 15 to 8	main divider ratio	00111000
D	MD7 to MD0	bits 7 to 0	main divider ratio	10000000; r = 80000

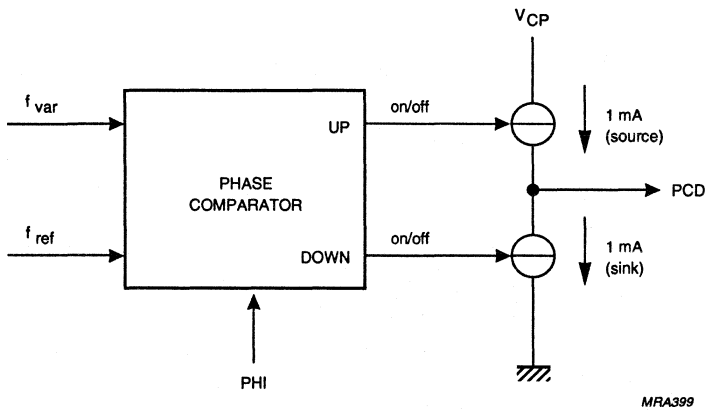


Fig.3 Phase comparator block diagram.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage range	−0.3	7.0	V
V_i	voltage range to ground (all pins)	0	V_{CC}	V
T_{stg}	IC storage temperature range	−55	+125	°C
T_{amb}	operating ambient temperature range	−40	+85	°C

HANDLING

Every pin referenced to ground withstands ESD (HMB) tests in accordance with MIL-STD-883C method 3015 class 2. Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling Integrated Circuits.

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

CHARACTERISTICS

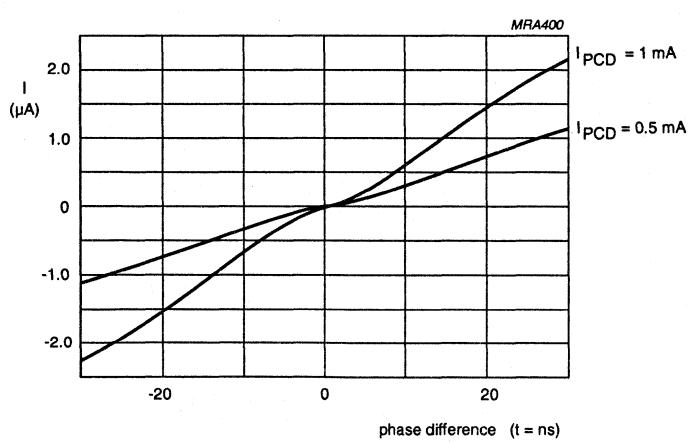
T_{amb} = 25 °C; V_{CC} = 4.5 to 5.5 V; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pins V_{CC} and V_{CP})						
V_{CC}	supply voltage range		4.5	–	5.5	V
I_{CC}	supply current		–	11.5	13.5	mA
I_{CCpd}	supply current	power-down	–	2.5	3.3	mA
V_{CP}	charge pump supply voltage		4.5	–	5.5	V
I_{CP}	charge pump supply current	IPCD = 0.5 mA	–	1.4	1.8	mA
I_{CPpd}	charge pump supply current	power-down	–	0.01	–	mA
RF dividers (pin RF)						
f_{RF}	frequency range		50	–	1100	MHz
$V_{RF(rms)}$	input voltage level (RMS value)	50 to 100 MHz	150	–	200	mV
		100 to 1100 MHz	50	–	150	mV
R_I	input resistance	at 1 GHz	–	200	–	Ω
		at 100 MHz	–	600	–	Ω
C_I	input capacitance	note 1	–	2.0	–	pF
R_{RF}	division ratios		2048	–	262143	–
Oscillator and reference divider (pins OSCIN and OSCOUT)						
f_{OSC}	oscillator frequency range		3	–	16	MHz
$V_{OSC(RMS)}$	input level sine wave (RMS value)		0.15	–	V_{CC}/2.8	V
$V_{OSC(p-p)}$	input level square wave (peak-to-peak value)		0.45	–	V_{CC}	V
t_{OSC_mk}	input mark width	see Fig.8	10	–	–	ns
t_{OSC_sp}	input space width		31	–	–	ns
Z_{OSC}	output impedance at pin OSCOUT		–	–	2	kΩ
R_{ref}	reference division ratio	see Table 1	128	–	1920	
1/8 crystal frequency (open collector output) (pin FX8)						
I_{OL}	LOW level output current	$V_{OL} \geq 0.6$ V	1.0	–	–	mA
Phase comparator (pin PCD)						
f_{PCD}	frequency range		5	–	100	kHz
I_{PCD}	output current	V_{PCD} = 2.5 V				
		bit IPCD = 1	0.9	1.2	1.4	mA
		bit IPCD = 0	0.45	0.6	0.75	mA
I_{PCDL}	output leakage current		−5	±1	+5	nA
V_{PCD}	output voltage		0.4	–	V_{CP}−0.5	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Serial clock and serial data input (pins SCL and SDA)						
f_{CLK}	clock frequency		0	–	100	kHz
V_{IH}	HIGH level input voltage		3	–	–	V
V_{IL}	LOW level input voltage		–	–	1.5	V
I_{IH}	HIGH level input current		–	3	10	μA
I_{IL}	LOW level input current		−10	−5	–	μA
C_I	input capacitance		–	–	10	pF
I_{sink}	SDA sink current	V_{OL} = 0.4 V	3	–	–	mA
Slave address select input (pin SAA) and Hardware power-down input (pin HPDN)						
V_{IH}	HIGH level input voltage		3	–	–	V
V_{IL}	LOW level input voltage		–	–	0.4	V
I_{IH}	HIGH level input current		–	–	0.1	μA
I_{IL}	LOW level input current		−10	–	–	μA
VCO output switches (pins VCOA and VCOB) and synthesizer alarm (pin SYA); note 2						
I_{OL}	LOW level sink current	$V_{OL} \geq 0.4$ V	400	–	–	μA

Notes to the characteristics

1. C_I is in parallel with R_I
2. Pin VCOA is forced to logic 0 during out-of-lock condition



The current I_{PCD} is averaged over a reference period of 24 μs.

Fig.4 Gain of phase detector and charge pump.

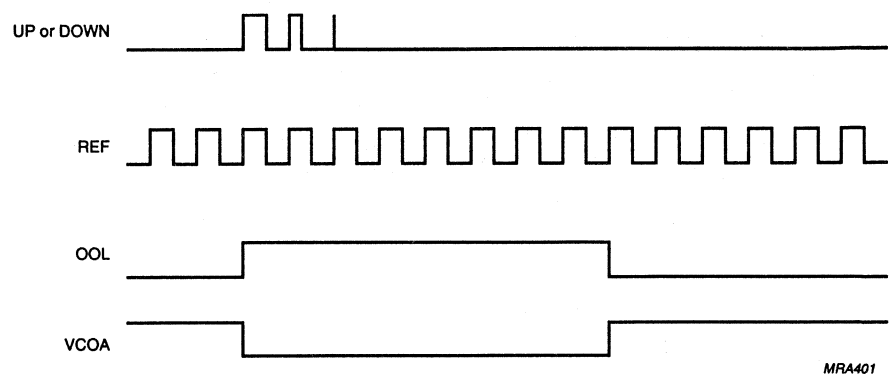


Fig.5 Out-of-lock function.

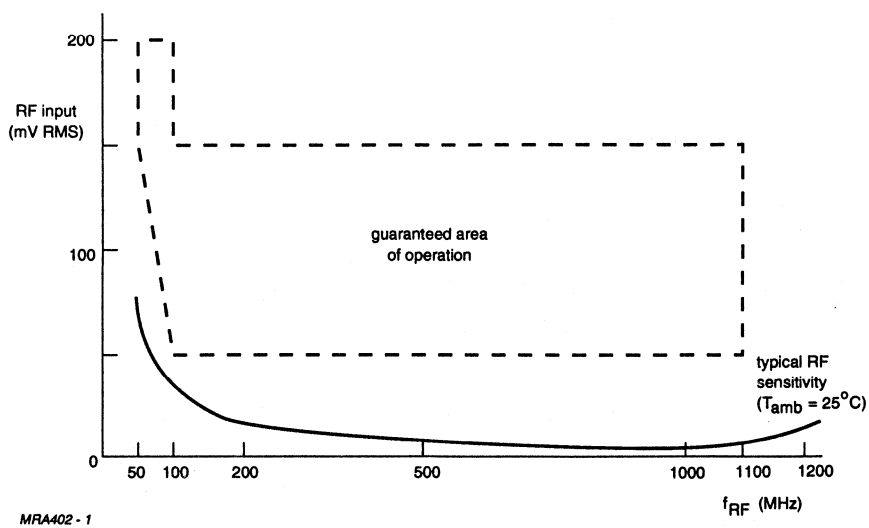


Fig.6 RF input high frequency sensitivity.

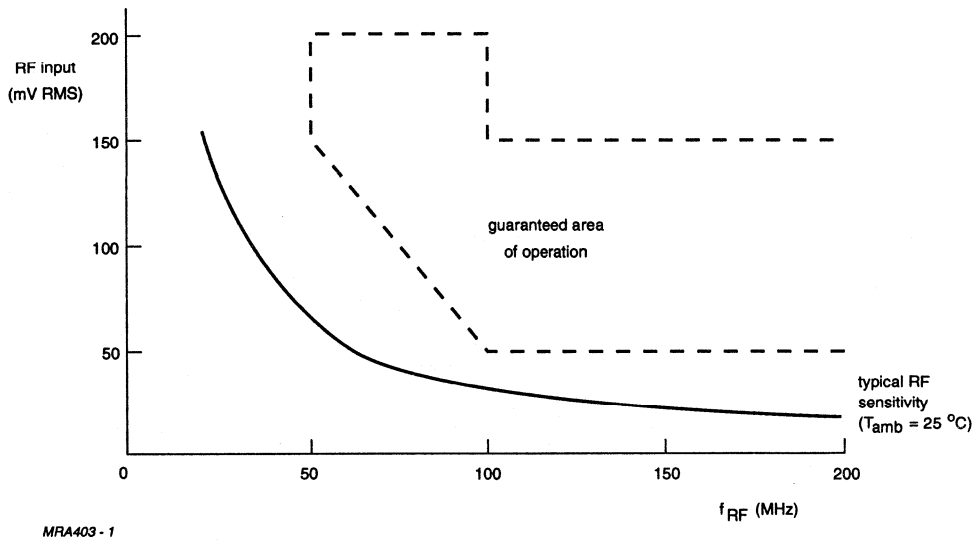


Fig.7 RF input low frequency sensitivity.

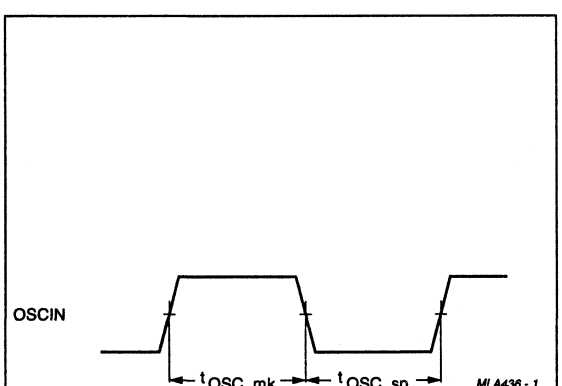
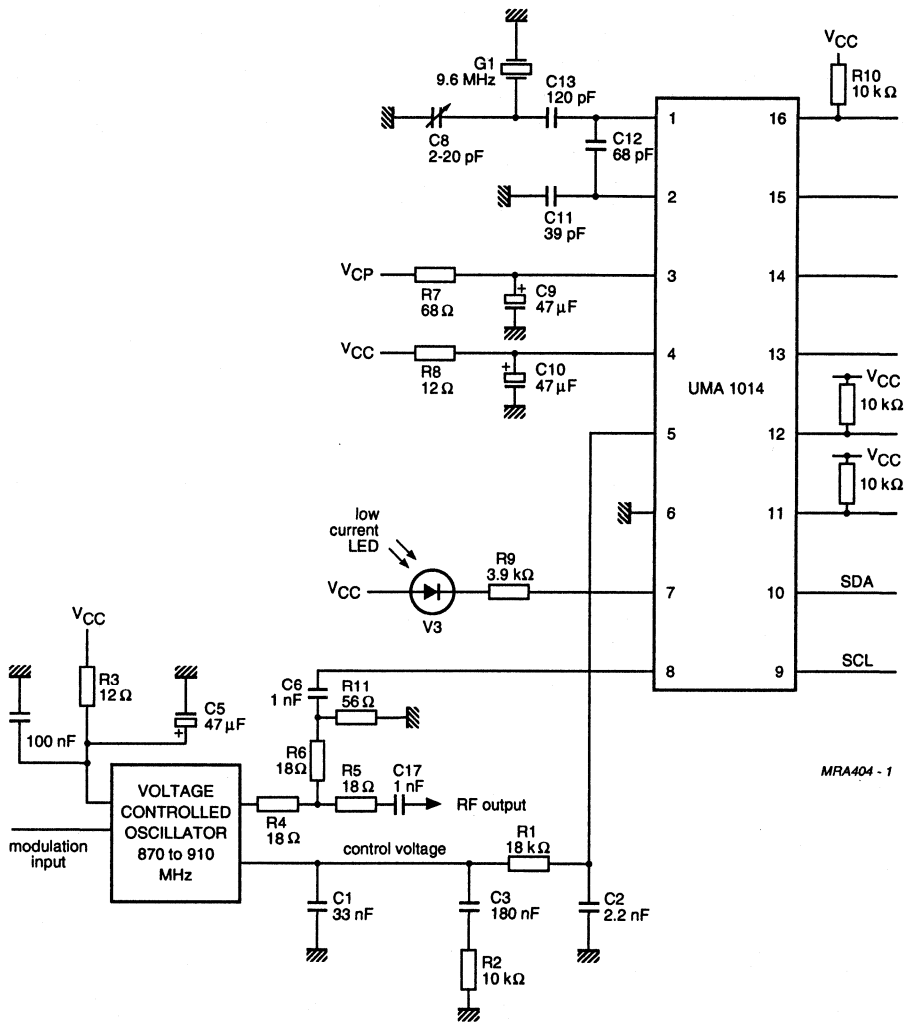


Fig.8 Oscillator input timing.



ETACS application for:

V_{co} sensitivity = 11 MHz/V.

Channel spacing = 12.5 kHz.

Fig.9 Typical cellular mobile radio application.

Low-power dual frequency synthesizer for radio communications

UMA1015M

FEATURES

- Two fully programmable RF dividers up to 1.1 GHz
- Fully programmable reference dividers up to 35 MHz
- Different reference frequency for each synthesizer (selectable)
- Three-line serial bus interface
- Phase comparator gain adjustable via external resistor
- Out-of-lock indication
- On-chip voltage doubler
- Low current from 3 V supply
- Separate power-down mode for each synthesizer
- Up to 4 open-drain output ports

APPLICATIONS

- Cordless telephones
- Hand-held mobile radio

GENERAL DESCRIPTION

The UMA1015M is a low-power dual frequency synthesizer for radio communications which operates in the 400 to 1100 MHz frequency range. Each synthesizer consists of a fully programmable main divider, a phase and frequency detector and a charge pump. There is a fully programmable reference divider common to both synthesizers which operates up to 35 MHz. The IC is programmed via a 3-wire serial bus which operates up to 10 MHz. The charge pump currents (gains) are fixed by an external resistance at pin ISET. The BiCMOS device is designed to operate from 2.7 (3 Ni-Cd cells) to 5.5 V at low current. The charge pump supply can be supplied from an external source or from an on-chip voltage doubler. Each synthesizer can be powered down independently to save current either by hardwire inputs or via the serial bus.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage		2.7	–	5.5	V
V_{CC}	charge pump supply	external supply; doubler disabled	2.7	–	5.5	V
$V_{CC(VD)}$	charge pump supply from voltage doubler	doubler enabled	–	$2V_{DD}-1$	5.5	V
$I_{DD} + I_{CC}$	operating supply current	both synthesizers ON; doubler disabled	–	10	–	mA
$I_{DD(PD)} + I_{CC(PD)}$	current in power-down per supply	doubler disabled	–	0.01	–	mA
$I_{DD(PD)}$	current in power-down from supply V_{DD}	doubler enabled	–	0.05	–	mA
RF_{INA}, RF_{INB}	RF input frequency for each synthesizer		400	–	1100	MHz
f_{XTAL}	crystal reference input frequency		3	–	35	MHz
f_{REF}	phase comparator frequency		–	12.5	–	kHz
T_{amb}	operating ambient temperature		–20	–	+70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
UMA1015M	20	SSOP20	plastic	SOT266A

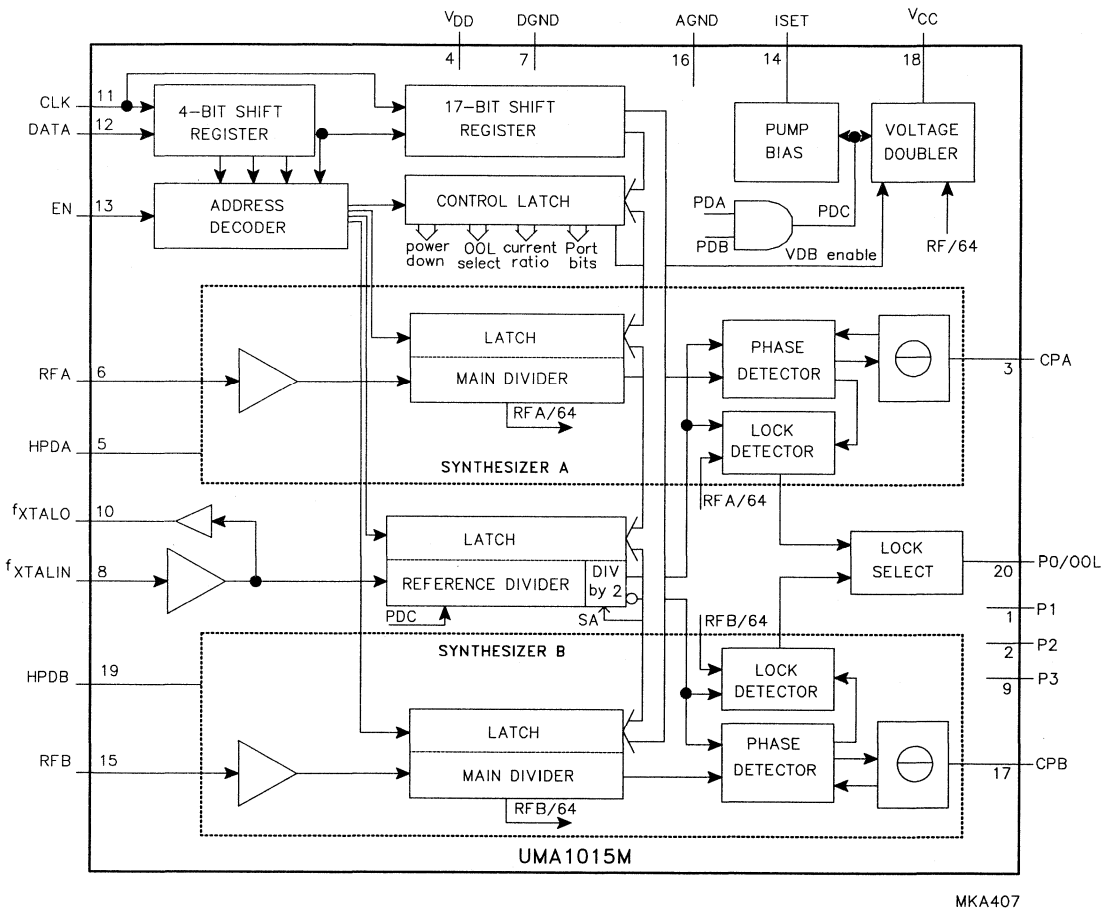


Fig.1 Block diagram.

Low-power dual frequency synthesizer for radio communications

UMA1015M

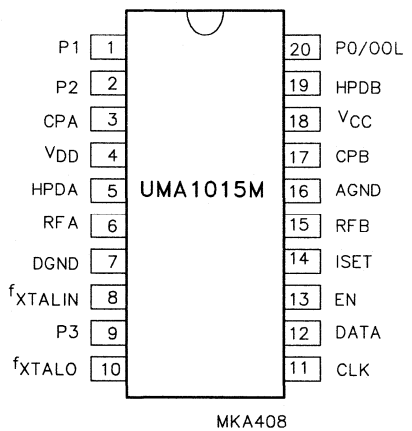


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
P1	1	output Port 1
P2	2	output Port 2
CPA	3	charge pump output synthesizer A
V_{DD}	4	digital supply 2.7 to 5.5 V
HPDA	5	hardware power-down synthesizer A
RFA	6	RF input synthesizer A
DGND	7	digital ground
f_{XTALIN}	8	common reference frequency input from TCXO
P3	9	output Port 3
f_{XTALO}	10	buffered output of f_{XTALIN}
CLK	11	programming bus clock input
DATA	12	programming bus data input
EN	13	programming bus enable input (active LOW)
ISET	14	regulator pin to set charge pump currents
RFB	15	RF input synthesizer B
AGND	16	analog ground for charge pumps
CPB	17	charge pump output synthesizer B
V_{CC}	18	analog supply to charge pumps; external or voltage doubler output 2.7 to 5.5 V
HPDB	19	hardware power-down synthesizer B
P0/OOL	20	output Port 0/out-of-lock output

Frequency synthesizer for radio communication equipment

UMA1016xT

FEATURES

- RF input frequencies to 1 GHz
- Fully programmable RF divider
- Three-line serial bus interface
- On-chip 3 to 16 MHz crystal oscillator
- Mask programmable +2 to +31 reference divider ratio
- Up to 1 MHz channel spacing
- Crystal frequency buffered output
- Dual register architecture for fast Tx/Rx switching in TDD single synthesizer systems
- Phase detector compensated for supply and temperature variations
- Power-down mode

APPLICATIONS

- 900 MHz cordless telephones
- Portable battery-powered radio equipment

GENERAL DESCRIPTION

The UMA1016xT is a low power synthesizer for radio communications. Manufactured in bipolar technology, it is designed for a 70 to 1000 kHz channel spacing in the 500 to 1000 MHz band. The channel is programmed via a 3-wire serial bus. The internal dual register architecture allows a single synthesizer to be used in TDD systems. Fast switching between transmit and receive frequencies is achieved without the need for bus overhead. It also incorporates a sensitive, low power RF divider and a dead-zone-eliminated 3-state phase comparator. A power-down mode enables the circuit to be idled.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CC}	supply voltage		4.5	–	5.5	V
V_{DD}	supply voltage		4.5	–	5.5	V
$I_{CC} + I_{DD}$	supply current		–	10	–	mA
$I_{cc\text{-}pd}$	I_{CC} in power-down		–	0.8	–	mA
f_{ref}	reference frequency		70	250	1000	kHz
RF_I	RF input frequency		500	–	1000	MHz
T_{amb}	operating ambient temperature range		–20	–	+70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
UMA1016AT	16	SO	plastic	SOT109A
UMA1016xT	16	SO	plastic	SOT109A

Notes to the Ordering Information

1. UMA1016AT has a Reference Division Factor of 27.
2. UMA1016xT is a customized version.

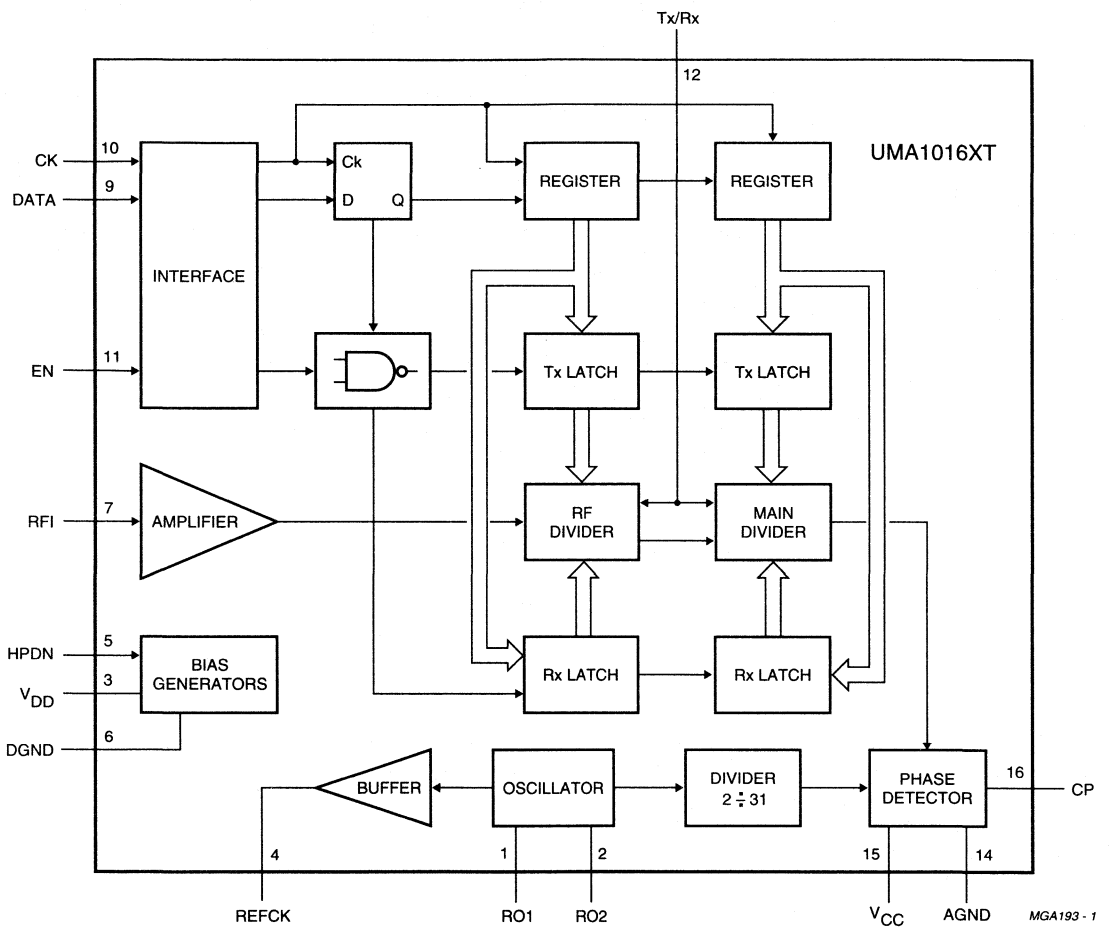


Fig.1 Block diagram.

PINNING

PIN	DESIGNATION	DESCRIPTION
1	RO1	oscillator input or TCXO input
2	RO2	oscillator output to crystal circuit
3	V_{DD}	5 V supply to digital section
4	REFCK	reference crystal frequency buffered output
5	HPDN	Hardware Power-Down Not; IC operates when pin is HIGH
6	DGND	digital ground
7	RFI	1 GHz RF signal input
8	i.c.	internally connected
9	DATA	serial data line input
10	CK	serial clock line input
11	$\overline{EN}$	programming bus enable input (active LOW)
12	TX/$\overline{RX}$	transmit (high)/receive (low) mode select input
13	i.c.	internally connected
14	AGND	analog ground
15	V_{CC}	5 V supply to charge pump circuit
16	CP	charge pump output

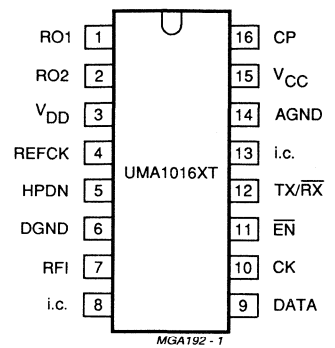


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

General

The UMA1016xT is a low power synthesizer for radio communications in the range 500 to 1000 MHz. It includes an oscillator circuit, reference divider, RF divider, 3-state phase and frequency comparator, charge pump and main control circuit for the transfer of serial data into two internal registers.

V_{DD} supplies power to the digital circuits while V_{CC} powers the charge pump. V_{DD} and V_{CC} are nominally 5 V but will operate in the range 4.5 V to 5.5 V.

Reduced noise coupling is facilitated by separate digital and analog ground pins which must always be externally connected to the same DC potential to prevent the flow of large currents across the die.

The synthesizer is placed in idle mode during power-down but the oscillator and buffer remain operative and may be used as a clock for system timing.

Main Divider

The main divider is a fully programmable pulse-swallow type. Following a sensitive (50 mV, −13 dBm) input amplifier, the RF signal is applied to a 13-bit divider (MD13,...MD1). The division ratio is provided via the serial bus to two 13-bit latches, corresponding to transmit and receive frequencies. The serial programming register is written to under processor control, independently of divider operation. This removes difficulty if using a low data bus transmission speed. The new ratio is transferred to the appropriate latch when the programming enable signal (EN) returns HIGH.

The last register bit (PB0) is used to determine whether the new value is loaded into the transmit (PB0 = 1) or receive (PB0 = 0) frequency latch. To avoid spurious phase changes, the divider incorporates the new ratio only at the end of the on-going reference period. The minimum division ratio is 512. One reference cycle is required to update a new ratio. Internal power-on occurs rapidly.

Oscillator

External capacitive feedback is applied to the common collector Colpitts oscillator which has high voltage supply rejection and negligible temperature drift. It is designed to function as an input buffer without the need for external components when a TCXO or other clock is used. A separate output buffer, which remains active during power-down (HPDN taken LOW), provides a TTL-compatible signal to drive external logic circuits (REFCK).

Reference Divider

The reference divider has a fixed divider ratio set by metal masking between 2 and 31. For example, a 4 MHz crystal connected to the oscillator and a ÷16 ratio allows a channel spacing of 250 kHz. Other frequencies and ratios are possible.

Phase Comparator

The phase comparator combines a phase and frequency detector and charge pump (Fig. 3). The charge pump current is internally fixed and determined for fast switching. It is compensated against power supply and temperature variation.

The detector is assembled from dual D-type flipflops which, together with feedback, remove the "dead" zone. Upon the detection of a phase error, either UP or DO go HIGH. This gates the appropriate current generator to source or sink 1.75 mA at the output pin. When no phase error is detected, CP becomes 3-state. The tuning voltage of the VCO is established from the sum of the current pulses into the loop filter.

A simple passive loop filter may be used to offer high performance without requiring an operational-amp. The phase comparator function is summarized in Table 2.

Main Control Interface

The programming control interface permits access to two internal latches, denoted Tx and Rx. The serial input bits on DATA, entered MSB first, are converted to a parallel word and stored in the appropriate latch under the control of the last entered register bit (PB0). When this is set HIGH, data serially fed to the register is loaded into the transmit (Tx) latch; when PB0 is LOW, the data is transferred to the receive latch (Rx).

The data sent to the synthesizer is loaded in bursts framed by the signal EN. Programming clock edges, together with their appropriate data bits, are ignored until EN becomes active (LOW). The internal latches are updated with the latest programming data when EN returns inactive (HIGH). Only the last 15 bits serially clocked into the device are retained within the programming register. One extra shift register bit (PB7) can be internally added via metal masking to allow direct software compatibility with a 7-bit swallow counter and a 64/65 dual-modulus prescaler. No check is made on the number of clock pulses received during the time that programming is enabled. EN going HIGH while CLOCK is still

LOW generates an active clock edge causing a shift of the data bits.

Data programmed into the register is lost during power-down (HPDN taken LOW). The maximum serial bus clock speed is specified as 5 MHz. Minimum speed is limited by the clock edge rise and fall times to ensure that no data transparency condition can exist.

Independent of any serial programming activity, the RF divider chain uses the data previously stored within the selected latch to determine the synthesized channel frequency. The Tx/Rx signal controls which latch is read to preload the counter bits at each division cycle. When new data is updated into the device, it is used during the cycle following latch selection by the Tx/Rx control line.

If the Tx/Rx line is tied LOW, only data loaded into the Rx latch is used. In this event the serial data stream clocked into the synthesizer must terminate with an "0". The logic diagram for the first bits of the programming interface is shown below. The other bits are processed in a similar manner by a further 9 stages of the shift register-latches-multiplexer.

The signals supplied to the circuit are described by the timing diagram. The table of values has been specified for maximum bus speed. Under slow clocking conditions, rise and fall times must not be excessively slow.

Table 1 Main divider division ratio

MAIN COUNTER							
MD1	MD2	../..	MD7	MD8	../..	MD12	MD13
LSB							MSB

Table 2 Operation of phase comparator

SYMBOL	$F_{ref} < F_{var}$	$F_{ref} > F_{var}$	$F_{ref} = F_{var}$
UP	0	1	0
DO	1	0	0
I_{pcd}	−1.75 mA	+1.75 mA	< ± 5 nA

Table 3 Register and latch bit allocations

FIRST	REGISTER AND LATCH BIT ALLOCATIONS													LAST IN
pb14	pb13	pb12	pb11	pb10	pb9	pb8	pb7	pb6	pb5	pb4	pb3	pb2	pb1	pb0
md13	md12	md11	md10	md9	md8	md7	X	md6	md5	md4	md3	md2	md1	address

Note

pb7; see section MAIN CONTROL INTERFACE.

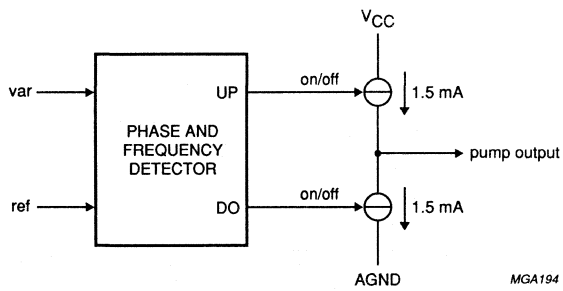


Fig.3 Phase comparator block diagram.

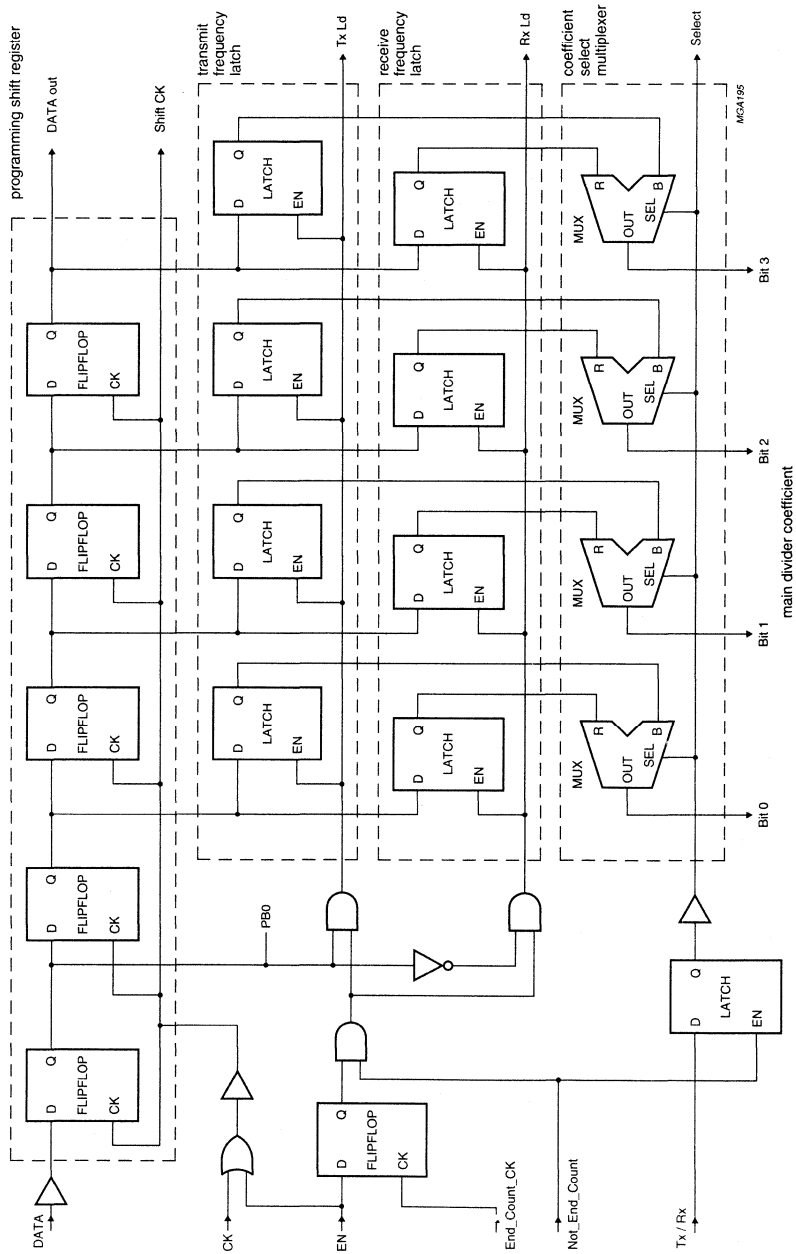


Fig.4 Simplified interface logic diagram.

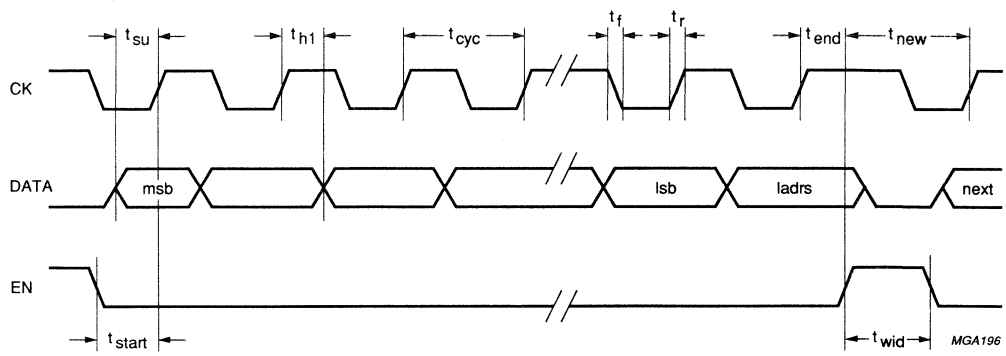


Fig.5 Logic interface signals.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage range		−0.2	–	7	V
V_{CCA}	analog supply voltage range		−0.2	–	7	V
V_i	input voltage range	to ground	0	–	V_{DD}	V
T_{stg}	storage temperature range		−55	–	125	°C
T_{amb}	operating ambient temperature range		−10	–	70	°C

Handling

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

TIMING CHARACTERISTICS

V_{DD}, V_{CC} = 5 V; T_{amb} = −20 to 70 °C unless otherwise specified.
Typical values measured at V_{CC}, V_{DD} = 5 V, T_{amb} = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Serial programming clock (pin 10)						
f_{ck}	clock frequency		0.01	4	5	MHz
t_r	rise time		–	5	50	ns
t_f	fall time		–	5	50	ns
t_{cyc}	clock period		0.2	–	–	ns
Enable programming (pin 11)						
t_{start}	delay to rising clock edge		30	–	–	ns
t_{end}	delay from last clock edge		0	–	–	ns
t_{width}	minimum inactive pulse width		200	–	–	ns
t_{new}	delay from EN inactive to new data		300	–	–	ns
Register serial input data (pin 9)						
t_{su}	input data to CK set-up time		10	–	–	ns
t_{HD}	input data to CK hold time		10	–	–	ns

Note to the Timing Characteristics

Minimum and maximum values are for maximum clock speed.

CHARACTERISTICS

V_{DD} and V_{CC} = 5 V; T_{amb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power supply						
V_{DDD}	digital voltage supply range		4.5	5	5.5	V
V_{CCA}	analog voltage supply range		4.5	5	5.5	V
I_d	digital supply current	V_{DD} = 5.5 V; REFCK off	–	–	10.8	mA
I_c	analog supply current	V_{CC} = 5.5 V; pump off	–	–	2.1	mA
I_{pd}	digital idle supply current	power-down mode	–	0.8	1.5	mA
RF divider input (RFI)						
f_{vco}	VCO frequency range		500	–	1000	MHz
V_{rf}	input signal voltage level (RMS)		50	–	300	mV
R_{rf}	input resistance	RF = 1 GHz	–	350	–	Ω
C_{rf}	input capacitance	indicative; not tested	–	1.5	–	pF
N	main divider division ratio		512	–	8191	
Oscillator and reference divider (RO1, RO2)						
f_{ref}	oscillator frequency range	REFCK used	3	–	16	MHz
V_{osc}	sinusoidal input level at pin 1 (RMS value)		0.1	–	0.5	V
C_{o1}	parasitic capacitance at pin 1	indicative; not tested	–	5	–	pF
Z_{os}	output impedance at pin 2	indicative; not tested	–	2	–	kΩ
C_{o2}	output capacitance	indicative; not tested	–	5	–	pF
Phase comparator and charge pump output (CP)						
F_{cp}	phase detector frequency range		70	250	1000	kHz
$-I_{cp}$	charge pump source current	V_{cc} = 4.5 to 5.5 V	−2.2	−1.75	−1.3	mA
$+I_{cp}$	charge pump sink current	V_{cc} = 4.5 to 5.5 V	1.3	1.75	2.2	mA
I_{leak}	charge pump off leakage current		−10	–	+10	nA
V_{cp}	charge pump voltage compliance range	I_{cp} within specified range	0.5	–	V_{CC} − 0.5	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Interface logic input signal levels (HPDN, EN, DATA, CK, Tx/Rx)						
V_{IH}	input logic HIGH level	all inputs	3	–	V_{DD} + 0.3	V
V_{IPD}	input logic LOW level	HPDN	3-0.3	–	0.6	V
V_{IL}	input logic LOW level	except HPDN	−0.3	–	1	V
I_{BIAS}	input bias current	logic 1	–	–	2	µA
I_{IL}	input bias current	logic 0	−2	–	–	µA
C_I	pin input capacitance	indicative; not tested	–	3	–	pF
Oscillator buffered logic output signal (REFCK)						
V_{oh}	driven output voltage; HIGH	V_{DD} = 5 V	3.5	–	V_{DD} − 0.5	V
V_{ol}	driven output voltage; LOW		0	–	0.4	V
I_{OL}	output sink current	V_{CL} = 0.4 V	−0.4	–	–	mA
t_r	ref clock output rising edge	C_I = 25 pF	–	50	–	ns
t_f	ref clock output falling edge	C_L = 25 pF	–	50	–	ns

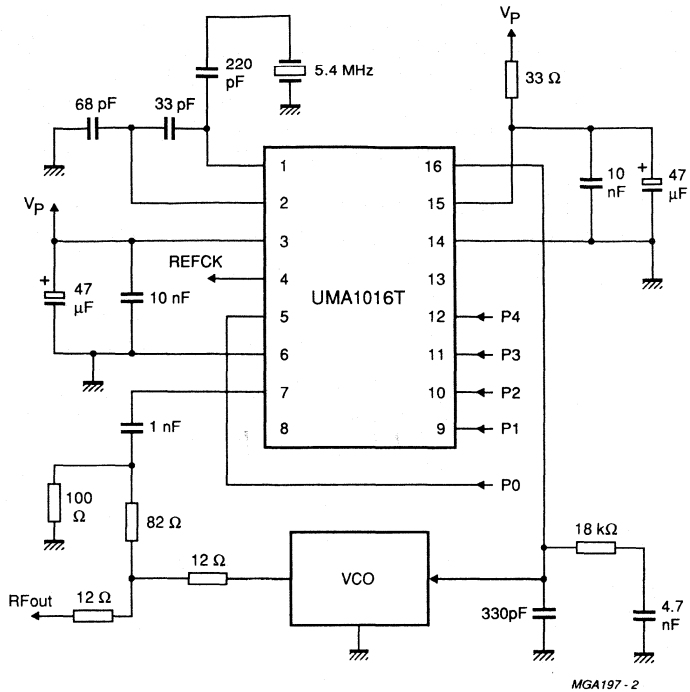


Fig.6 Application diagram.

APPLICATION INFORMATION

In a typical single-synthesizer application, the circuit is connected as shown in Fig. 6. Both analog and digital supplies are decoupled to ground with HF and LF filter capacitors. Correct oscillator operation requires capacitors both to ground and to provide feedback across the amplifier. Five signals are shown fed from a microcontroller to provide serial programming, control TDD frequency selection and initiate the power-down mode. Other system logic may also be clocked by a crystal frequency output from the synthesizer.

A passive 2nd-order loop filter giving a 3rd-order system response is shown in Fig. 6. Indicated values are intended for rapid frequency switching (500 µs), 200 kHz channel spacing (reference +27) and breakthrough levels below –60 dB. The VCO output shows a power splitter supplying both the synthesizer RF input and drive buffer for other system components (RF amplifier in transmit mode, input mixer in receive mode). The minimizing of loop filter node leakage currents requires careful board layout.

Low-voltage dual frequency synthesizer for radiotelephones

UMA1018M

FEATURES

- Low current from 3 V supply
- Fully programmable RF divider
- Three-line serial bus interface
- Second synthesizer to control first IF or offset loop frequency
- Independent fully programmable reference dividers for each loop driven from external crystal
- Dual-phase detector outputs to allow fast frequency switching
- Integrated digital-to-analog converter
- Dual power-down modes.

APPLICATIONS

- 900 MHz mobile telephones
- Portable battery-powered radio equipment.

GENERAL DESCRIPTION

The BICMOS device integrates prescalers, programmable dividers, and phase comparators to implement two phase-locked loops. It is designed to operate from 3 Ni-Cd cells in pocket phones with low current as well as nominal 5 V supplies. The principal synthesizer operates on VCO input frequencies above 1.2 GHz, the auxiliary synthesizer operates to 200 MHz. The auxiliary loop is intended for first IF or transmit offset loop frequency setting. Each synthesizer has a fully programmable reference divider. All divider ratios are supplied via a three-line serial programming bus.

Separate power and ground pins are provided to the analog and digital circuits. The ground leads shoud be externally shorted together otherwise large currents may flow across the die and damage it.

The principal synthesizer phase detector uses two charge pumps; one provides normal loop feedback, the other is only active during a fast mode to speed-up switching. The auxiliary loop has a separate phase detector. All charge pump currents (gain) are fixed by an external resistance at pin ISET. Only passive loop filters are used; the charge pumps function within a wide voltage compliance range to improve the overall system performance. An on-chip 8-bit DAC allows adjustment of an external function, such as temperature compensation of a crystal oscillator in GSM systems.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive digital supply voltage	2.7	–	5.5	V
V_{CC}	positive charge pump supply	2.7	–	5.5	V
$I_{CC} + I_{DD}$	operating supply current principle and auxiliary synthesizers on	–	8	–	mA
$I_{CC(PD)} + I_{DD(PD)}$	supply current with auxiliary synthesizer in power-down	–	6	–	mA
$I_{CC(PD)}$	supply current in power-down per supply	–	10	–	µA
RF_{IN}	principle input frequency	500	–	1200	MHz
AF_{IN}	auxiliary input frequency	50	–	200	MHz
f_{XTAL}	crystal reference input frequency	3	–	35	MHz
f_{REFP}	principle phase comparator frequency	10	200	2000	kHz
f_{REFA}	auxiliary phase comparator frequency	10	–	1000	kHz
T_{amb}	operating ambient temperature	–20	–	+70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
UMA1018M	20	SSOP20	plastic	SOT266A

Low-voltage dual frequency synthesizer for radiotelephones

UMA1018M

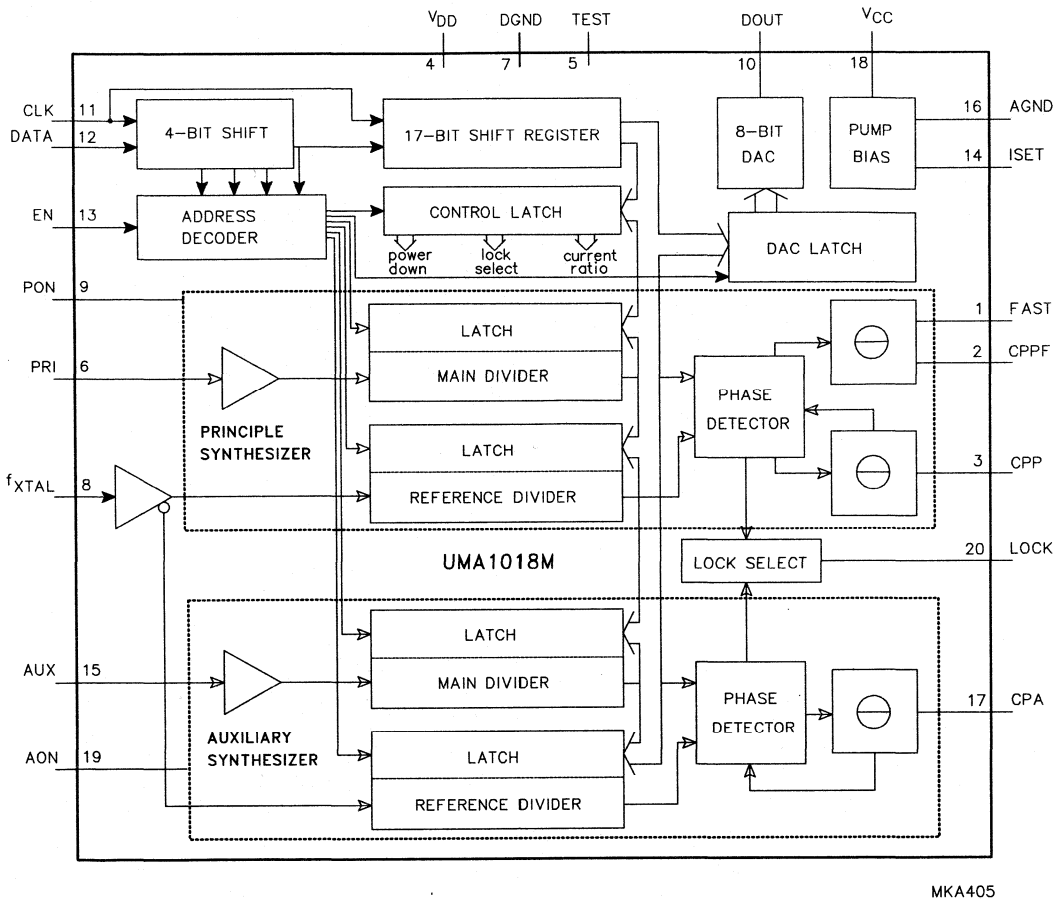


Fig.1 Block diagram.

Low-voltage dual frequency synthesizer for radiotelephones

UMA1018M

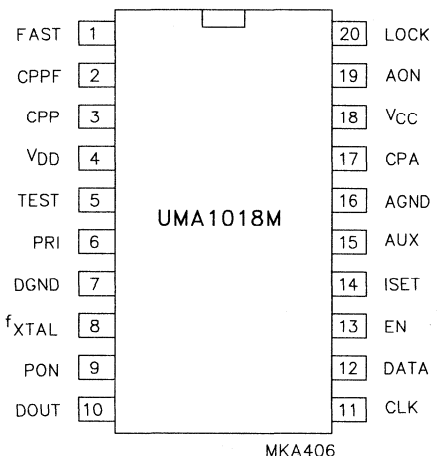


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
FAST	1	control input to speed up main synthesizer
CPPF	2	principle synthesizer speed-up charge pump output
CPP	3	principle synthesizer normal charge pump output
V_{DD}	4	digital section 2.7 to 5.5 V power supply
TEST	5	control input to switch to test mode (must be connected to ground)
PRI	6	1 GHz principle synthesizer RF divider input
DGND	7	digital ground
f_{XTAL}	8	common reference frequency input from crystal oscillator
PON	9	principle synthesizer power-on input
DOUT	10	8-bit digital-to-analog convertor output
CLK	11	serial clock line input
DATA	12	serial data line input
EN	13	programming bus enable input (active LOW)
ISET	14	regulator pin to set the charge pump currents
AUX	15	auxiliary synthesizer frequency input
AGND	16	analog ground
CPA	17	auxiliary synthesizer charge pump output
V_{CC}	18	2.5 to 5.5 V supply to charge pump and DAC circuits
AON	19	auxiliary synthesizer power-on input
LOCK	20	in-lock detect output (main PLL) and test mode output

Data processor for cellular radio (DPROC)

UMF1000T

FEATURES

- Single chip solution to all the data handling and supervisory functions
- Configuration to both AMPS and TACS
- I²C serial bus control
- All analog interface and filtering functions fully implemented on chip
- Error handling in hardware reduces software requirements
- Robust SAT decoding and transponding circuitry
- Low current consumption
- Small physical size
- Minimum external peripheral components required.

GENERAL DESCRIPTION

The UMF1000T is a low power CMOS LSI device incorporating the data tranceiving, data processing, and SAT functions (including on-chip filtering) for an AMPS or TACS hand-held portable cellular radio telephone.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage (pin 28)	4.5	5.0	5.5	V
I_{DD}	supply current (pin 28) normal operation with external clock	–	2.5	–	mA
T_{amb}	operating ambient temperature range	−40	–	+85	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
UMF1000T	28	SO28	plastic	SOT136A

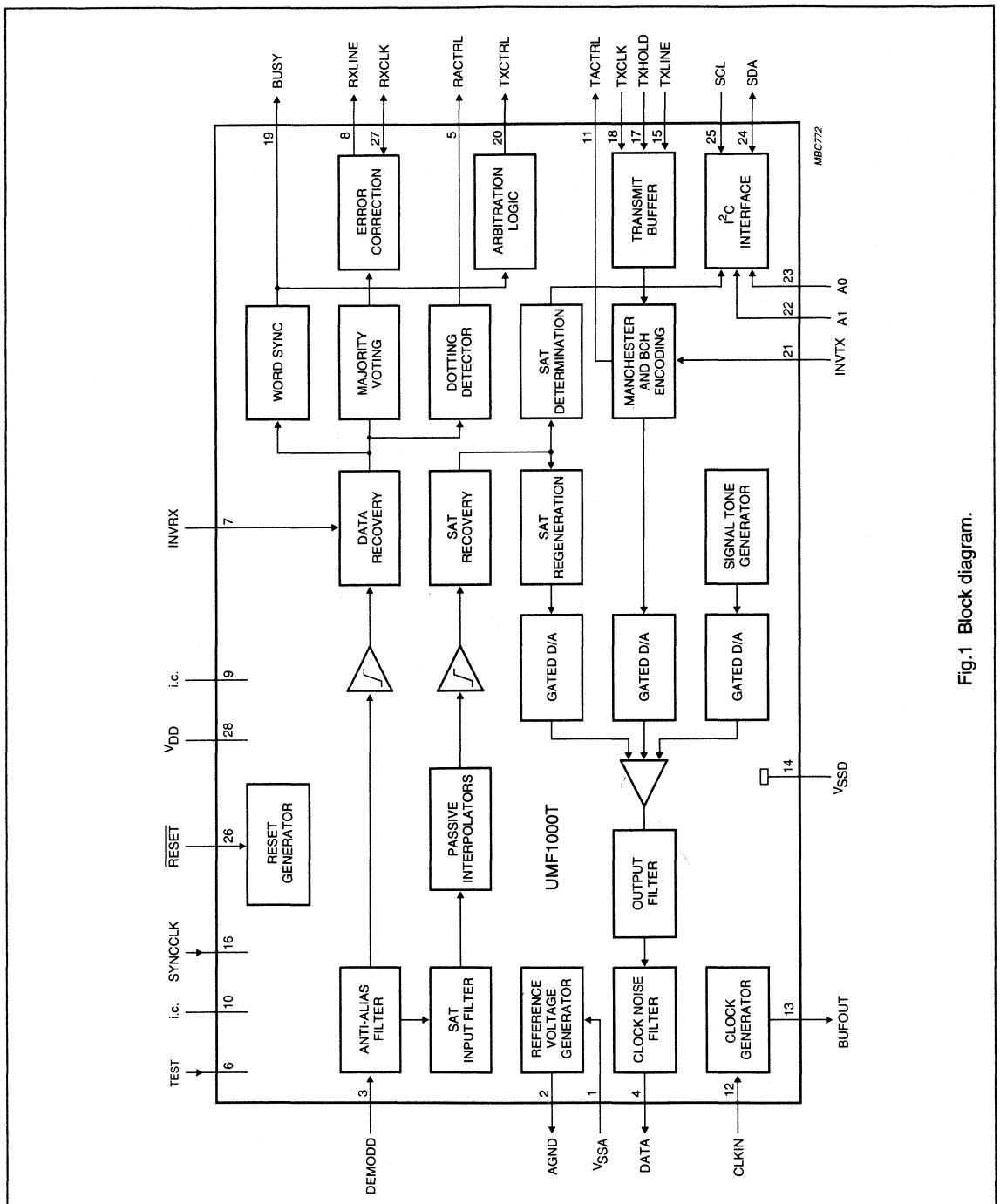


Fig.1 Block diagram.

Data processor for cellular radio (DPROC) UMF1000T

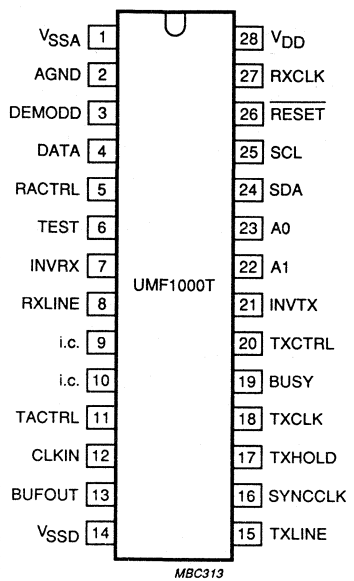


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{SSA}	1	analog negative supply (0 V)
AGND	2	$(V_{DD} - V_{SSA})/2$ analog reference ground
DEMODD	3	received data signal input
DATA	4	transmitted data signal output
RACTRL	5	received audio control output
TEST	6	SCAN control input – used for power-on reset
INVRX	7	inverts sense of received data stream
RXLINE	8	received data signal output
i.c	9	internally connected; must be left open-circuit
i.c	10	internally connected; must be left open-circuit
TACTRL	11	transmitter audio control output
CLKIN	12	1.2 MHz external master clock input
BUFOUT	13	buffered output of internal clock oscillator
V_{SSD}	14	digital ground
TXLINE	15	transmitted data signal
SYNCCLK	16	SCAN CLOCK control input – used for power-on reset
TXHOLD	17	holds off transmission of data
TXCLK	18	transmitted data clock input
BUSY	19	reverse control channel status output
TXCTRL	20	transmitter control output
INVTX	21	inverts sense of transmitted data stream
A1	22	address input 1 – used for power-on reset (I^2C-bus)
A0	23	address input 0 (I^2C-bus)
SDA	24	serial data input/output (I^2C-bus)
SCL	25	serial clock input (I^2C-bus)
$\overline{RESET}$	26	master reset input
RXCLK	27	received data clock input
V_{DD}	28	positive supply voltage (+5 V)

CHARACTERISTICS

V_{DD} = 5 V ±10%; T_{amb} = −40 to +85 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	positive supply voltage		4.5	5.0	5.5	V
I_{DD}	supply current	normal operation; note 1	–	2.5	–	mA
Digital inputs (note 2)						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	$V_{DD}+0.3$	V
C_I	input capacitance		–	–	6	pF
Digital outputs (note 2)						
V_{OL}	LOW level output voltage	I_{sink} = 1 mA	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_{source} = 1 mA	$V_{DD}-0.4$	–	–	V
Open-drain outputs (note 3)						
V_{OL}	LOW level output voltage	I_{sink} = 2 mA	–	–	0.4	V
Open-drain SDA						
V_{OL}	LOW level output voltage	I_{sink} = 3 mA	–	–	0.4	V

Notes to the characteristics

1. 1.2 MHz clock on CLKIN, SYNCCLK HIGH, outputs unloaded analog part operating.
2. All digital inputs and outputs of DPROC are compatible with standard CMOS devices and the following general characteristics apply.
3. Open-drain outputs have no internal pull-up resistors.

FUNCTIONAL DESCRIPTION

General

The UMF1000T (DPROC) is a single-chip CMOS device which handles the data and supervisory functions of an AMPS or TACS subscriber set.

These functions are:

- Data reception and transmission
- Control and voice channel exchanges
- Error detection, correction, decoding and encoding
- Supervisory Audio Tone decoding and transponding
- Signalling Tone generation.

In an AMPS or TACS cellular telephone system, mobile stations communicate with a base over full duplex RF channels. A call is initially set up using one out of a number of dedicated control channels. This establishes a duplex voice connection using a pair of voice channels. Any further transmission of control data occurs on these voice channels by briefly blanking the audio and simultaneously transmitting the data. The data burst is brief and barely noticeable by the user. A data rate of 10 kbits/s is used in the AMPS system and 8 kbits/s in TACS. The signalling formats for both Forward Channels (base to mobile) and Reverse Channels (mobile to base) are shown in Fig.3.

A function known as Supervisory Audio Tone (SAT), a set of 3 audio tones (5970, 6000 and 6030 Hz), is used to indicate the presence of the mobile on the designated voice channel. This signal, which is analogous to the On-Hook signal on land lines, is sent out to the mobile by the base station on the Forward Voice Channel. The signal must be accurately recovered and transponded back to the base station to complete the 'loop'. At the base station this signal is used to ascertain the overall quality of the communication link.

Another voice channel associated signal is Signalling Tone (ST). This tone (8 kHz TACS, 10 kHz AMPS) is generated by the mobile and is sent in conjunction with SAT on the Reverse Voice Channel to serve as an acknowledgement signal to a number of system orders.

The key requirements of a hand-held portable cellular set are:

- Small physical size
- Minimum number of interconnections (serial bus)
- Low power consumption
- Low cost.

The DPROC is a member of our Cellular Radio chip set, based on the I²C-bus, which meets these requirements. A cellular radio system schematic using the chip set is shown in Fig.4.

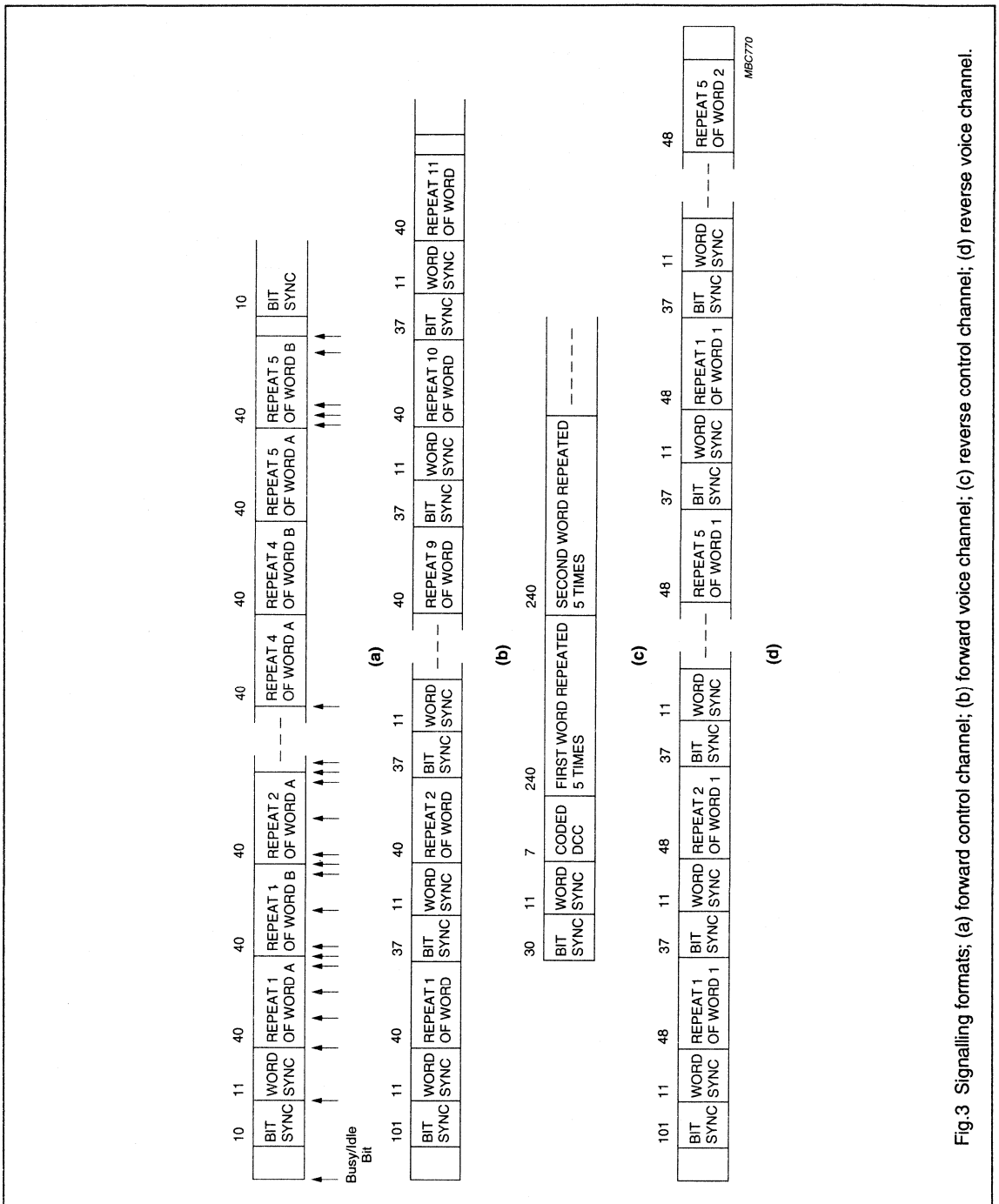


Fig.3 Signalling formats; (a) forward control channel; (b) forward voice channel; (c) reverse control channel; (d) reverse voice channel.

Data processor for cellular radio (DPROC)

UMF1000T

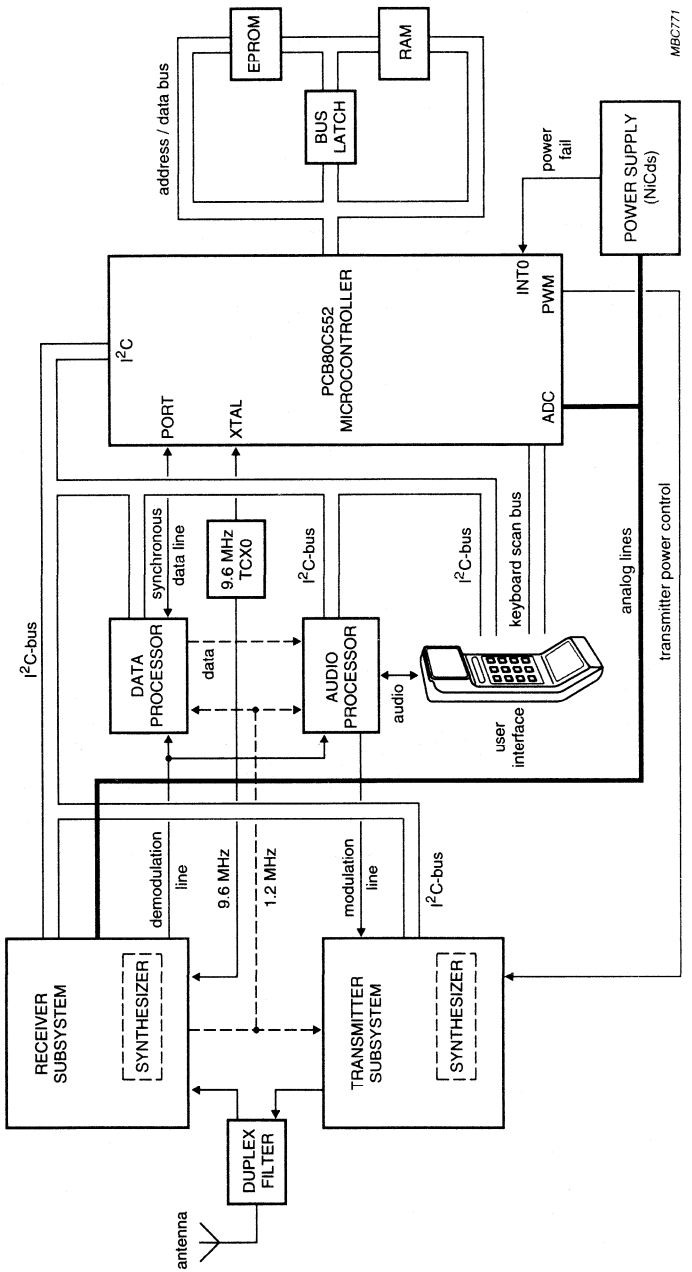


Fig.4 Cellular radio system schematic.

EXTERNAL PIN DESCRIPTION

Supply (V_{DD}; V_{SSA}; V_{SSD}; AGND)

Both V_{SSA} and V_{SSD} must be connected to common ground.

SYMBOL	DESCRIPTION
V_{DD}	positive supply voltage for digital and analog circuitry (±5 V +10%)
V_{SSA}	negative supply voltage for analog circuitry (0 V)
V_{SSD}	digital ground (0 V)
AGND	internally generated reference ground based by internal analog circuitry; voltage level $(V_{DD}-V_{SSA})/2$ ±2%

System clock (CLKIN; BUFOUT)

CLKIN is a digital input for the externally generated 1.2 MHz master clock. This signal should be accurate to 100 x 10^{-6} and have a worst case of 60 : 40 mark-space ratio. BUFOUT is the buffered output of the clock oscillator and provides the option of generating the clock signal on chip by connecting a 1.2 MHz crystal between BUFOUT and CLKIN.

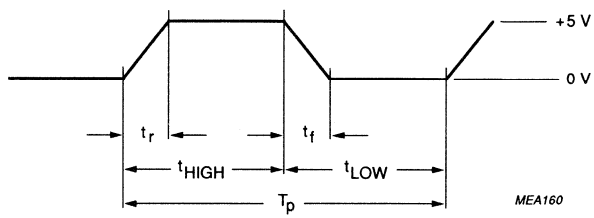


Fig.5 System clock timing diagram.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
T_p	clock period time	833.25	833.33	833.42	ns
t_{HIGH}	HIGH time	40%	50%	60%	T_p
t_{LOW}	LOW time	–	T_p-t_{HIGH}	–	
t_r	rise time	–	50	–	ns
t_f	fall time	–	50	–	ns

I²C serial data link (SDA; SCL)

SDA is the bi-directional data line; SCL the clock input from an I²C master. These constitute a typical I²C link and conform to standard characteristics as defined in the I²C-bus specification.

- Data rate: up to 100 kbits/s

Slave Address Select (A0; A1)

Selection of the device slave address is achieved by connecting A0 to either V_{SSD} or V_{DD} and connecting A1 to either pin 16 and pin 6 or to V_{DD}. The slave address is defined in accordance with the I²C specifications as shown in Fig.6.

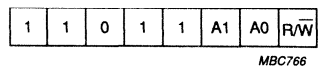


Fig.6 Device slave address.

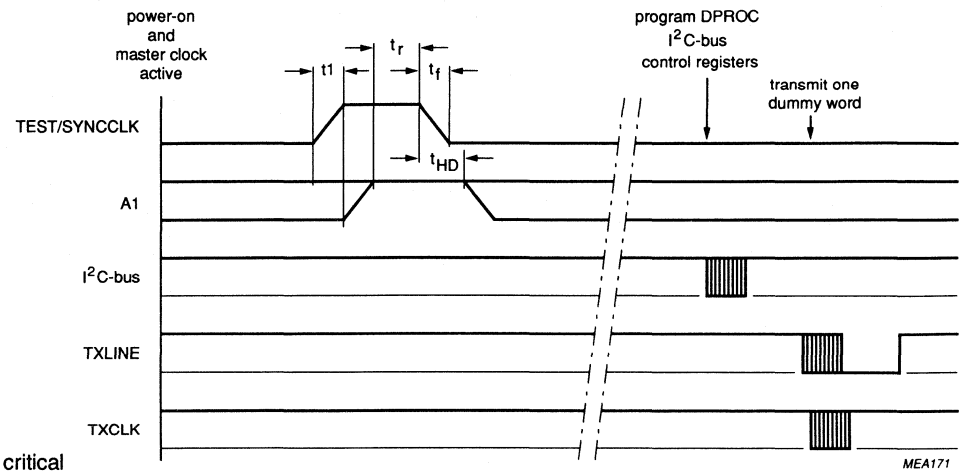
Power-up state

DPROC will not respond reliably to any inputs (including $\overline{\text{RESET}}$) until 100 µs after the power supply has settled within the specified tolerance. The analog sections of the device will have stabilized within 5 ms. No power-on reset is provided, therefore before the device can enter normal operation TEST and SYNCCLK must be pulsed HIGH. The reset pulse on these pins must have a minimum period of 250 µs and the fall time of the negative going edge must be faster than 1 µs. Pin A1 must remain HIGH during this reset period therefore if the A1 bit of the I²C address is required to be logic 0. A1 may be connected to TEST and SYNCCLK. If it is required to be at logic 1 then A1 may be permanently connected to V_{DD}. If it is required that A0 = logic 1, then a normal master reset (pin 26) sequence must follow the power-on reset sequence to get the internal registers in the defined state.

After the power-on reset a dummy transmission should be made to initiate internal DPROC counters. This transmission should be made with arbitration (ABREN) disabled and the RF transmitter stage switched OFF. Figure 7 shows the power-on reset sequence.

Master reset ($\overline{\text{RESET}}$)

$\overline{\text{RESET}}$ is an asynchronous active LOW master reset input, with a minimum active pulse width of 2 µs which may be used to reset certain logic within DPROC to a predefined state as illustrated in Tables 1 and 2. Alternatively, DPROC may be set into a known initial state be setting the I²C control register as required. The internal reset sequence after a negative pulse on $\overline{\text{RESET}}$ takes 250 µs.



Where:

t1 = time not critical

t_r = reset time = 250 µs max.

t_f = pulse fall time = 1 µs max.

t_{HD} = A1 hold time = 0 µs min.

Note

The RF transmitter is OFF during reset sequence.

Fig.7 Power-on reset programming sequence.

Table 1 Predefined state of the digital output pins

OUTPUT	STATE
RXLINE	HIGH
TXCTRL	HIGH
TACTRL	HIGH
RACTRL	HIGH
BUSY	HIGH

Table 2 Predefined state of I²C registers

REGISTER	BIT							
	7	6	5	4	3	2	1	0
control	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
SATD	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
TST	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW

Data Transfer Link (RXLINE; TXLINE; TXHOLD; TXCLK and RXCLK)

RXLINE, TXLINE, TXCLK and RXCLK provide a dedicated serial data link for the transfer of system data messages between DPROC and the system controller at variable rates of up to 200 kbits/s.
TXHOLD allows the system controller to preload the DPROC transmit register with one word without the data being transmitted. DPROC then starts transmitting the instant TXHOLD is driven LOW.

- RXCLK: clock input from system controller
- RXLINE: data output from DPROC to system controller
- TXCLK: clock input from system controller
- TXLINE: open drain data bi-directional line to the system controller
- TXHOLD: (HIGH) holds off transmission of data
- Data rate: up to 200 kbits/s

Note

A minimum mean data transfer rate for the received data of 2.1 kbits/s (AMPS) and 1.7 kbits/s (TACS) is required to ensure contiguity of message words.

The format for received and transmitted data words is shown in Fig.15(a) and Fig.15(b) respectively. The receive and transmit data timing is illustrated in Fig.16(a) and Fig.16(b) respectively.

Transmitter Control (TXCTRL)

TXCTRL is an open-drain output used to disable the transmitter during a Reverse Control Channel access failure.

- output level HIGH: RF enable
- output level LOW: RF disable

Transmitter Audio Enable (TACTRL)

TACTRL is an open-drain digital output signal used to blank the audio path and enable the data path to the modulator during data bursts on the Reverse Voice Channel.

- output level HIGH: audio enabled
- output level LOW: audio muted

Receiver Audio Enable (RACTRL)

RACTRL is an open-drain digital output used to blank the audio path to the earpiece when a sequence of dotting and word sync is detected.

RACTRL and TACTRL functions can be combined using one line.

- output level HIGH: audio enabled
- output level LOW: audio muted

Reverse Control Channel Status (BUSY)

BUSY is a digital output giving the status of the Reverse Control Channel. This is determined by a majority decision on the result of the last 3 consecutive Busy/Idle bits and has the following logic levels:

- output level HIGH: channel busy
- output level LOW: channel idle

On a voice channel BUSY indicates channel idle.

Invert Receive Data (INVRX)

Enables an additional inverter in the receive data path. This allows RF demodulators with high or low local oscillators to be used. The TACS and AMPS specifications define a NRZ encoded logic 1 as a LOW-to-HIGH transition in the centre of a data bit period. The polarity of the demodulated data stream into DPROC depends on the receiver local oscillator.

- input HIGH: data inverted
- input LOW: data normal

Invert Transmit Data (INVTX)

Enables an additional inverter in the transmit data path. This allows RF modulators with high or low local oscillators to be used. The TACS and AMPS specifications define a NRZ encoded logic 1 as a LOW-to-HIGH transition in the centre of a data bit period. The polarity of the modulated data stream depends on the transmitter local oscillator.

- input HIGH: data inverted
- input LOW: data normal

Transmitted Data Output (DATA)

Data is an analog output which provides Manchester encoded and filtered data signal SAT and signalling tone. This signal should normally be AC coupled into the Audio/Data summer.

- DC level: analog ground (AGND)
- signal level: 2 V (p-p) for signalling tone; signal level with filtered data signal
- signal tolerance: 2% + supply voltage variation (ΔV_{DD})
- minimum load capacitance: 10 kΩ
- maximum load capacitance: 2 nF
- maximum output impedance: 50 Ω

Received Data Input (DEMODD)

Demodd inputs analog data and SAT signals from the RF demodulator. This pin should normally be AC coupled.

- DC level: analog ground (AGND)
- maximum data level: 1 V (p-p)
- nominal data level: 250 mV (p-p)
- minimum data level: 200 mV (p-p)
- minimum SAT level: 50 mV (p-p)
- input impedance: min. 1 MΩ

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

System configuration

A device generating a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves'.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

Timing specifications

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig.12.

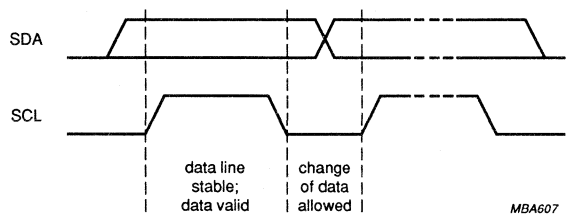


Fig.8 Bit transfer.

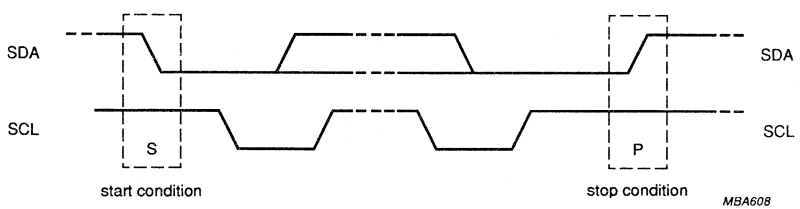


Fig.9 Definition of start and stop conditions.

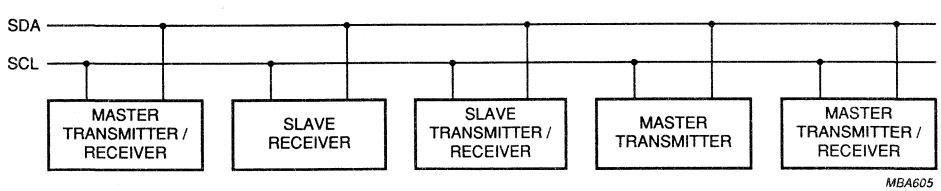


Fig.10 System configuration.

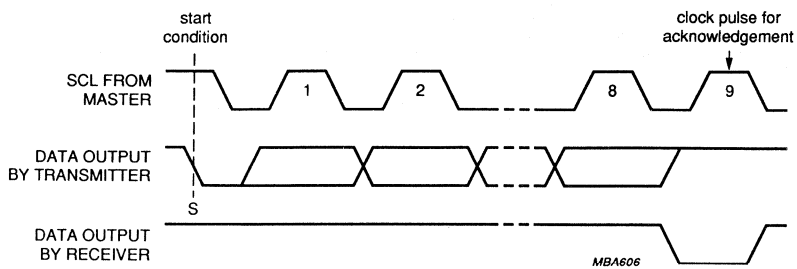


Fig.11 Acknowledgement on the I²C-bus.

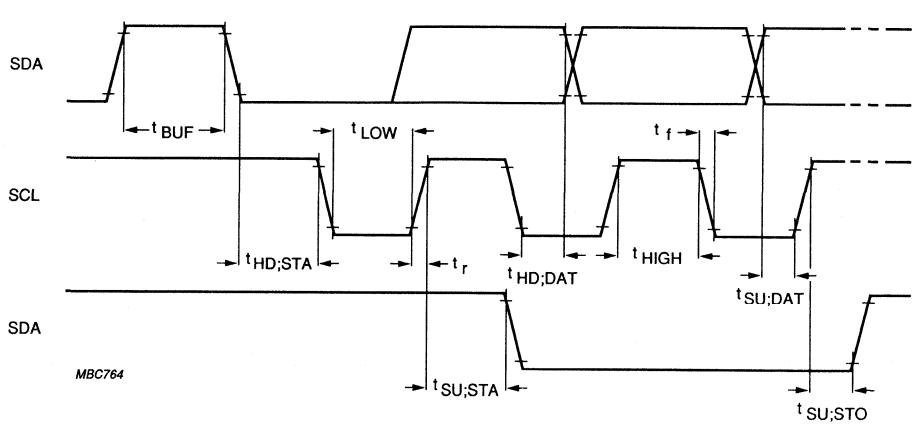
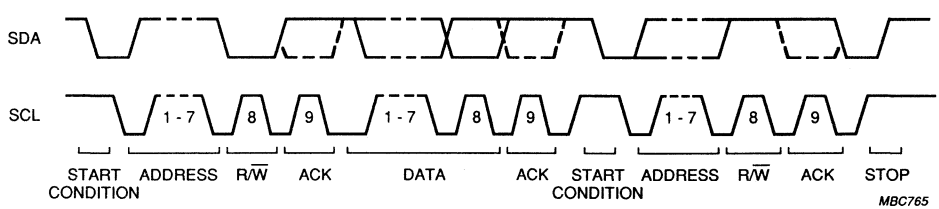


Fig.12 Timing.

Where:

All the values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{DD} to V_{SS}.

SYMBOL	TIMING	DESCRIPTION
t_{BUF}	$t \geq t_{LOW(min)}$	the minimum time the bus must be free before a new transmission can start
$t_{HD;\ STA}$	$t \geq t_{HIGH(min)}$	start condition hold time
$t_{LOW(min)}$	4.7 µs	clock LOW period
$t_{HIGH(min)}$	4 µs	clock HIGH period
$t_{SU;\ STA}$	$t \geq t_{LOW(min)}$	start condition set-up time, only valid for repeated start code
$t_{HD;\ DAT}$	$t \geq 0$ µs	data hold time
$t_{SU;\ DAT}$	$t \geq 250$ ns	data set-up time
t_r	$t \leq 1$ µs	rise time of both the SDA and SCL line
t_f	$t \leq 300$ ns	fall time of both the SDA and SCL line
$t_{SU;\ STO}$	$t \geq t_{LOW(min)}$	stop condition set-up time



Where:

Clock $t_{LOW(min)}$: 4.7 µs

Clock $t_{HIGH(min)}$: 4 µs

The dashed line is the acknowledgement of the receiver

Maximum number of bytes: unrestricted

Premature termination of transfer: allowed by generation of STOP condition

Acknowledge clock bit: must be provided by the master.

Fig.13 Complete data transfer.

I²C REGISTERS

General

The I²C register block resides internally within the I²C interface block and contains various items of status and control information which are transferred to and from DPROC via the I²C-bus. The block is organized into four 8-bit registers:

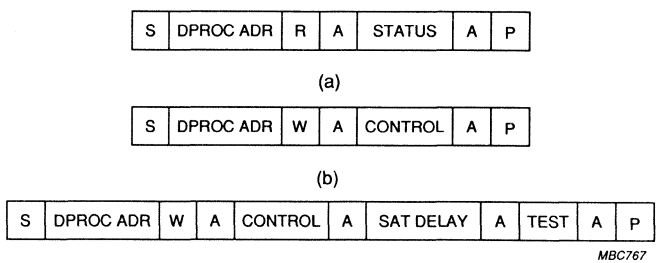
- Status Register: contain read only items
- Control Register: contain write only items
- SAT Programmable Phase Shift Register: contain write only items
- TEST Register

Note

In normal operation the SAT delay register and the TEST register require programming only after a device reset.

Table 3 Register map

REGISTER	BIT							
	7	6	5	4	3	2	1	0
status	–	–	WYNSC	BUSY	TXABRT	TXIP	MSCC1	MSCC0
control	–	SERV	STS	TXRST	ABREN	FVC	STEN	SATEN
SATD	<----------SAT delay data---------->							



Where:

S: START condition

W: read/write bit (logic 0 = write)

R: read/write bit (logic 1 = read)

A: acknowledge bit

P: STOP condition

DPROC ADR: slave address of DPROC

TEST: must be programmed to logic 0 for normal operation.

Fig.14 I²C data format; (a) read from DPROC status register; (b) write to DPROC control register; (c) write to all DPROC registers.

Status Register

This is read only register containing DPROC status information.

MEASURED SAT COLOUR CODE (MSCC1; MSCC0)

MSCC1 and MSCC0 provide information about the current measured SAT colour code in accordance with Table 4.

Table 4 Measured SAT Colour Code

MSCC1	MSCC0	SAT frequency (Hz)
0	0	5970
0	1	6000
1	0	6030
1	1	no valid SAT

TRANSMISSION IN PROGRESS (TXIP)

TXIP indicates whether DPROC is currently accessing the Reverse Control or Voice Channels.

- logic 1: data transmission in progress
- logic 0: transmission not in progress

TRANSMISSION ABORT STATUS (TXABRT)

TXABRT indicates that a Reverse Control Channel Access Attempt has been aborted by DPROC without successful message transmission.

- logic 1: transmission attempt aborted
- logic 0: no access collision detected

REVERSE CONTROL CHANNEL STATUS (BUSY)

BUSY gives the status of the Reverse Control Channel. This is determined by a majority decision on the result of the last 3 consecutive Busy/Idle bits on the Forward Control Channel.

- logic 1: channel busy
- logic 0: channel idle

On a voice channel the BUSY bit defaults to the set state.

Note

This signal is also routed to the BUSY output pin.

WORD SYNCHRONIZATION INDICATOR (WSYNC)

WSYNC indicates whether DPROC has acquired frame synchronization according to the Forward Control Channel format.

- logic 1: frame synchronization acquired
- logic 0: no frame synchronization

Control Register

This is a write only register containing DPROC control information.

SAT Path Enable (SATEN)

SATEN enables the SAT transponded signal to be output on external pin DATA.

- logic 1: SAT tone enabled
- logic 0: SAT tone inhibited

Signalling Tone (ST) Path Enable (STEN)

STEN enables the Signalling Tone to be output on external pin DATA.

- logic 1: ST enabled
- logic 0: ST inhibited

Channel Format Select (FVC)

FVC selects the required channel format.

- logic 1: voice channel format
- logic 0: control channel format

Transmission Abort Permission (ABREN)

ABREN indicates whether DPROC has permission to abort data transmission and disable RF on the Reverse Control Channel following the detection of a channel access attempt collision.

- logic 1: RF disable allowed
- logic 0: RF disable inhibited

Message Transmission Abort (TXRST)

TXRST terminates a message being transmitted on the reverse channel. It is a monostable signal which when activated causes a reset of the message transmission circuitry and causes TXABRT and TXIP I²C signals to be reset.

This signal does not clear the DPROC transmit register; therefore if a word has been loaded into DPROC after a TXABRT has occured the control line TXHOLD should be held LOW to allow the word to be cleared from the DPROC input register.

- logic 1: reset active
- logic 0: reset inactive

System Type Select (STS)

STS selects required system format.

- logic 1: AMPS
- logic 0: TACS

Note

Toggling this signal also resets the receive logic in DPROC.

Serving System Select (SERV)

SERV selects which of the serving system data streams (A or B) is accepted.

- logic 1: system A selected
- logic 0: system B selected

SAT Programmable Delay Register (SATD)

SATD programs the value of phase shift which is applied to the SAT tones in the SAT Regeneration Block. This value will be determined and programmed into the System Controller during manufacture. The recovered SAT is delayed in time by approximately 0.8 µs x value in the register which corresponds to approximately 1.8 degrees x value in the register. The total phase shift is limited to 360 degrees.

The ability to adjust SAT phase angle is not necessary in current AMPS and TACS systems. Therefore this register should normally be in AMPS and TACS, this function is not necessary and should programmed to zero.

DIGITAL CIRCUIT BLOCKS

General

The majority of the digital circuitry within the DPROC device is identical for both AMPS and TACS. The device has little additional redundancy to implement both systems. The functions of these blocks are described in the following sections and relate to those shown in Fig.1.

Data Recovery

The Data Recovery Block receives wideband Manchester encoded data in sampled and sliced form from the Strobed Comparator Block, on which it performs the following functions:

- clock recovery
- Manchester decoding
- data regeneration

The Clock Recovery Block extracts an 8 or 10 kHz (TACS or AMPS) phase-locked clock signal from the Manchester encoded data stream. This is implemented using a digital-phase-locked-loop (PLL) which has an adjustable 'bandwidth' to provide both fast acquisition and low jitter.

Manchester decoding is performed by exclusive ORing the recovered Manchester encoded data with the recovered clock.

The NRZ data regeneration is performed by a digital integrate and dump circuit. This consists of an up/down counter that counts 1.2 MHz cycles during the data period. The sense of the count is determined by the result of the Manchester Decoder output.

The number of counts is sampled at the end of a data period. If this number exceeds a threshold the data is latched as a 1 otherwise it is latched as a 0.

SAT Processing

The Supervisory Audio Tone processing consists of the following functions:

- SAT recovery
- SAT determination
- SAT regeneration

SAT RECOVERY

The SAT Recovery Block receives a filtered and sliced SAT signal which must be recovered before being routed to the Determination and Regeneration Blocks.
The recovery is performed using a digital phase-locked-loop.

SAT DETERMINATION

The SAT Determination Block indicates which, if any, of the valid SAT tones is detected from the recovered SAT. The AMPS and TACS specifications require that a determination is made at least every 250 ms. Determination involves counting the number of cycles of the regenerated SAT in this time period. This count is then compared to a set of four known counts which define the boundaries between the SAT frequencies and the SAT not valid events. The result is then coded into the I²C status registers MSCC0 and MSCC1 as shown in Table 5.

SAT REGENERATION

The SAT Regeneration Block generates a digital SAT stream from the recovered SAT stream for transponding back to the base station. The AMPS and TACS specifications require the SAT to be transponded with a maximum phase shift of 20 degrees between the point the modulated RF signal enters the mobile from the base station, and the point the modulated RF leaves the mobile. A variable phase compensation circuit is provided in DPROC to shift the recovered SAT through 0 to 360 degrees before being passed to the output summing network. The degree of phase shift is determined during manufacture of the set and the required additional phase shift is stored in non-volatile RAM and programmed via I²C at each power-on cycle. The phase correction is performed by a counter delay method using signals which are phase locked to the recovered SAT.

Dotting Detector

The Dotting Detector Block determines whether a data inversion (dotting) pattern has been received on the Forward Voice Channel. The detection of 32 bits of data inversion indicates that the Clock Recovery Block has acquired bit synchronization and that the narrow bandwidth mode on the clock recovery phase-locked-loop is selected. This signal is also used to indicate that a data burst is expected and activates the audio mute RACTRL, after a Word Synchronization Block has been received, for the duration of the burst.

Table 5 Status registers MSCC0, MSCC1; decoded SAT frequencies

REGISTER		SAT frequency band (Hz ±2 Hz)	decoded SAT (Hz)
MSCC0	MSCC1		
1	1	max. 5956	not valid
0	0	5956 to 5986	5970
0	1	5986 to 6014	6000
1	0	6014 to 6046	6030
1	1	min. 6046	not valid

Word Synchronization Detector

The Word Synchronization Block performs the following functions:

- Frame Synchronization
- Reverse Control Channel status (B/I determination)
- Valid Serving System determination

These functions are associated solely with the Forward Control Channel and have no meaning on the Forward Voice Channel.

Information in a data stream is identified by its position with respect to a unique synchronization word. This synchronization word is an 11-bit Barker code which has a low probability of simulation in an error environment, and can be easily detected. Data received is only considered valid at times when DPROC has achieved frame synchronization. In this condition the block leaves its search mode and enters its lock mode. This is indicated by bit WSYNC being set HIGH. In order to achieve this two consecutive synchronization words separated by 463 bits must be detected. Once in lock mode, the synchronization word detector is examined every 463 bits and only loses frame synchronization after 5 consecutive unsuccessful attempts at detecting the synchronization word have been made. At this point bit WSYNC is cleared and the device is returned to its search mode. On the Forward Voice Channel detection of the synchronization word indicates that the following 40 bits are valid data. Information detailing the status of the Reverse Control Channel is given by the Busy/Idle bits. These occur at intervals of 11 bits within the frame, the first occurring immediately following the synchronization word. The status of the channel is determined by a majority decision on the last three consecutive Busy/Idle bits.

Majority Voting Block

The Majority Voting Block performs the following functions:

- identifying position and validity of frames in the received data stream
- extracting five repeats of each word from a valid frame
- performing a bit-wise majority decision on the five repeats of the data word.

The validity of the frames is determined by setting a counter in operation which times out and resets the circuitry after 920 or 463 bit periods from detecting valid word synchronization. The time out period selected depends on whether DPROC is monitoring the Forward Voice or Control Channel respectively.

Up to five repeats of the message word are searched for and extracted by DPROC. On the forward Voice Channel DPROC will extract the first five words that occur for which a correct synchronization word is found. These words can occur in any position in the frame. A serial majority vote is performed as the fifth word is being extracted.

Error Correction Block

The Error Correction Block performs the following functions:

- extraction of a valid message from the Majority-Voted Word
- computation of the S1 and S3 syndromes
- correction of up to one error in the word
- communication of received data to the System Controller via the Received Data Serial Link.

Interpretation of parity of a received word is obtained from knowledge of the syndromes of the word. The syndromes are calculated using feedback shift registers with two characteristic equations:

$1 + X + X^6$ and $1 + X + X^2 + X^4 + X^6$

Once the syndromes of a received word are known, it is possible to determine if a correctable error is present. DPROC only corrects up to one error although the code used has a Hamming distance of five. The occurence of two or more errors is signalled by setting the BCH error flag, which is communicated to the System Controller via the Received Data Serial Link.

Received Data Serial Link

The Received Data Serial Link transfers data and control information from DPROC to the System Controller. The data is transferred on RXLINE under control of a clock signal RXCLK, generated by the System Controller. The system controller is informed of the arrival of a decoded data word in the DPROC output register by RXLINE being driven LOW. If the system controller chooses to ignore the received data or only partially clock the data out, the DPROC will reset the receive buffer for the next word after the period RWIN (see Fig.16).

Data Format

Each Received Data word consists of 4 bytes. The word format is shown in Fig.15(a). The sense and function of the fields is shown in Table 6.

Link Protocol

The Received Data protocol is described by the timing diagram Fig.16(a) and has the following parameters:

- maximum receive window (RWIN)

  Control Channel (TACS) = 47 ms

  Control Channel (AMPS) = 37 ms
- minimum clock period ($t_{CLK(min)}$) = 2 µs
- minimum clock hold-off (t_{WAIT}) = 100 µs

Transmit Data Serial Interface

The Transmit Data Serial Link performs reception of data from the System Controller to DPROC over a dedicated line TXLINE. The transfer of data is synchronous with a clock signal TXCLK, generated by the System Controller.

Data Format

Each Transmit Data word consists of 5 bytes. The word format is shown in Fig.15(b). The sense and function of the fields is shown in Table 7.

Link Protocol

Messages are normally up to 5 words in length on the Reverse Control Channel and up to 2 words in length on the Reverse Voice Channel. However, DPROC will transmit messages of any word length. These must be transmitted on the data stream without interruption. To avoid the need for large buffer areas, a flexible protocol is used to allow DPROC to control the transfer of data words. DPROC has an on-chip buffer which can hold one complete word of a message. While new words are being loaded into DPROC, within the time period Buffer clear to end of TWIN, DPROC will maintain uninterrupted data transmission. The System Controller can abort the transmission of a message at any point activating the I²C signal TXRST. This signal causes the interface to return to its power-up state and resets TXIP and TXABRT (see Table 3). On completion of these tasks TXRST will return to its inactive state. The Transmit Data Protocol is described by the timing diagram shown in Fig.16(b) and has the following parameters:

- maximum transmit window (TWIN)

  voice channel (TACS) = 60 ms

  voice channel (AMPS) = 48 ms

  control channel (TACS) = 29 ms

  control channel (AMPS) = 23 ms
- minimum clock period ($t_{CLK(min)}$) = 2 µs

Table 6 Received Data word

BIT	TITLE	SENSE	FUNCTION
31	start	LOW	identifies start of word
30	BCH error	active HIGH	indicates that an uncorrected BCH error is associated with the word
29 to 2	received data	binary data	received data word
1	RXLINE error	LOW	if detected as HIGH indicates that a transmission error has occured on the microprocessor to DPROC serial link
0	stop	HIGH	identifies end of the word

Table 7 Transmit data word

BIT	TITLE	SENSE	FUNCTION
39	start	LOW	identifies start of word
38, 37	DCC	binary data	digital colour code
36 to 1	transmit data	binary data	transmit data word
0	stop	HIGH	identifies end of the word

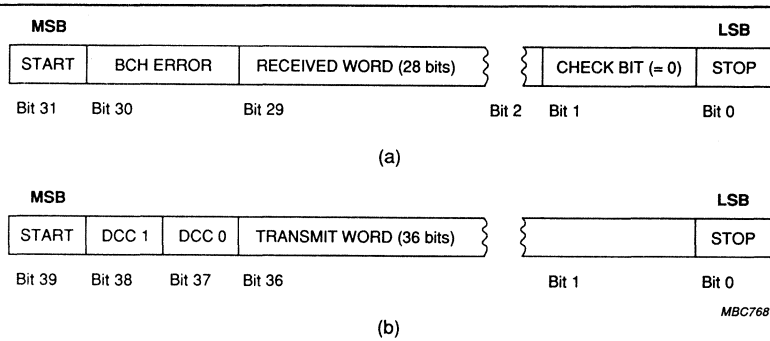
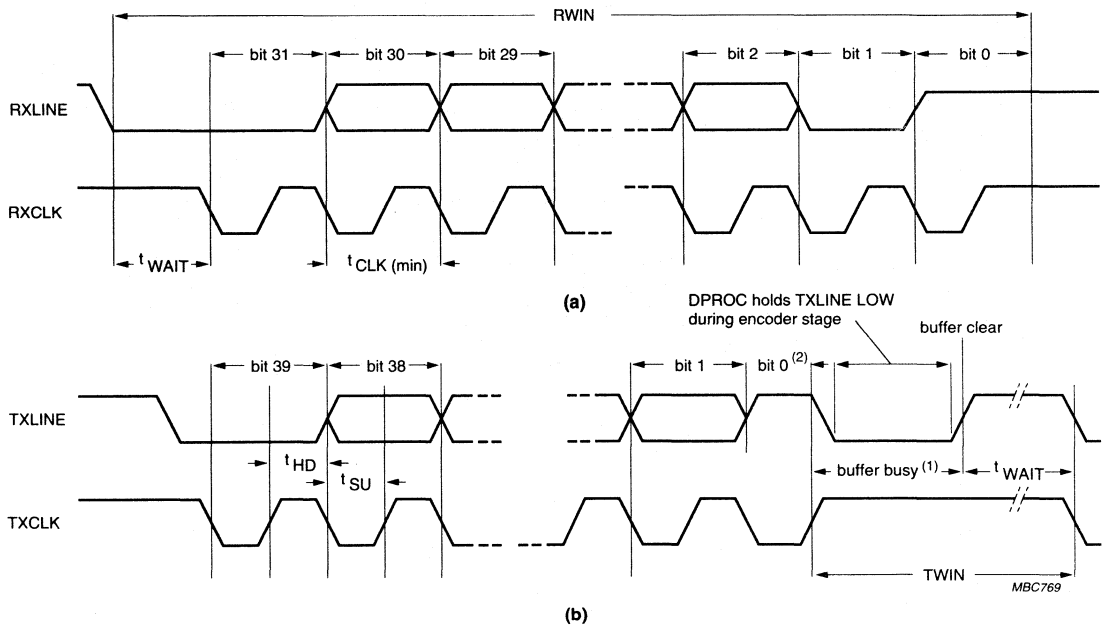


Fig.15 Data word formats; (a) received data word; (b) transmit data word.



Where:

t_{HD} = 100 ns minimum

t_{SU} = 0 ns minimum

t_{WAIT} = 0 ns minimum

(1) The buffer busy time depends on whether the first or subsequent words are being loaded.

(2) The system controller should monitor the TXLINE during bit 0, if the status of TXLINE does not change from a HIGH to a LOW on the rising edge of TXCLK, then a framing error has occured. This can be caused by glitches on the clock line or if an arbitration error occured while the DPROC transmit register was being loaded. The system controller should recover the situation by holding TXLINE HIGH and supplying clocks on TXCLK until TXLINE goes LOW. Then the situation should be treated as a normal channel arbitration failure as described in **Reverse Control Channel Access Arbitration** - Abort Procedure.

Fig.16 Data timing diagrams; (a) DPROC to microcontroller link; receive data timing; (b) microcontroller to DPROC link; transmit data timing.

BCH and Manchester Encoding Block

The functions performed by this circuit block include:

- reception of data from the System Controller
- parity generation
- message construction
- Manchester encoding

Each 36-bit Information Word sent on the Reverse Voice and Control Channels is coded into a 48-bit code word. The code word consists of the 36-bit word followed by 12 parity bits. These parity bits are formed by clocking the information word into a 12-bit feedback shift register with characteristic equation:

$$1 + X^3 + X^4 + X^5 + X^8 + X^{10} + X^{12}$$

The BCH Encoder Block constructs the Reverse Voice and Control Channel data streams from the information it receives from the System Controller.
The streams are formed out of the four possible field types:

- Dotting (data inversions)
- 11-bit Synchronization Word
- Digital Colour Code
- 48-bit code word

The 2 bits of DCC received from the System Controller are coded into a 7-bit word as shown in Table 8.

The data sense for Manchester Encoding has a NRZ logic 1 encoded as a 0-to-1 transition and a NRZ logic 0 encoded as a 1-to-0 transition.

Reverse Control Channel Access Arbitration

The AMPS and TACS specifications require a method of arbitration on the Reverse Control Channel to prevent two mobiles from transmitting on the same channel at the same time. This function is performed by DPROC monitoring the Busy/Idle stream sent on the Forward Control Channel.

The AMPS and TACS specifications state that once the mobile has commenced transmitting on the Reverse Control Channel it must monitor the Busy/Idle stream. If this stream becomes active outside a predetermined 'window', measured from the start of the transmission of the message, the mobile must terminate its transmission and disable the transmitter immediately.

In the Cellular Radio chip-set there are two levels of control of the RF transmitter; the first is absolute control by the System Controller, the second is conditional by other devices in the set. In DPROC the conditional control of the transmitter is performed via the output TXCTRL. This line is effectively wired ANDed together, using open-drain outputs, with other devices which may wish to control the transmitter. When these devices do not wish to disable the transmitter their output is in a HIGH impedance state.

An exception to this procedure occurs when the Serving System instructs the mobile not to monitor the Busy/Idle bits. In this event the arbitration logic can be disabled by clearing I²C register bit ABREN.

The flow of events during a Control Channel Access attempt is as follows:

INITIAL STATE

- transmitter power off via I²C
- DPROC transmit circuitry in power-up state
- TXCTRL line HIGH

ACCESS ATTEMPT PROCEDURE

1. System Controller decides to send message (see **Note to the Access Attempt Procedure**).
2. System Controller drives TXCTRL LOW directly.
3. System Controller switches transmitter power-on and waits for power-up for the transmitter module (RF transmitter is still disabled by TXCTRL).
4. System Controller sets TXRST via I²C to DPROC.
5. System Controller sets ABREN via I²C (if required) allowing DPROC to control the transmitter.
6. System Controller determines status of Reverse Control Channel by monitoring the Busy/Idle bit. If busy, waits a random time then tries again.
7. System Controller releases TXCTRL allowing it to be pulled HIGH enabling the transmitter output.
8. System Controller transfers the first word of the message to DPROC via serial link (see **Note to the Access Attempt Procedure**).
9. DPROC sets I²C signal TXIP and starts sending message while monitoring Busy/Idle status.
10. If channel becomes busy before 56 bits and ABREN is set then perform Abort Procedure.
11. If channel remains idle after 104 bits and ABREN is set then perform Abort Procedure.
12. System controller loads the subsequent words of the message into DPROC when the buffer becomes clear (Fig.16b).

13. On completion of entire message DRPCO clears TXIP and 25 ms later the System Controller disables transmitter via I²C.
14. System Controller finally sends TXRST to prepare DPROC for next transmission.

Note to the Access Attempt Procedure

At stage 1 the system controller may choose to preload DPROC with the first word of the message and hold it from transmission until stage 7 using the TXHOLD line. This gives a lower time overhead between detecting an IDLE channel and commencing the transmission. To use this feature TXHOLD must be driven HIGH before the last bit of data has been transferred into DPROC. Figure 17 illustrates the DPROC data transmission timing.

ABORT PROCEDURE (SEE FIG.18)

1. DPROC immediately disables transmitter output by driving TXCTRL LOW.
2. DPROC sets TXABRT.
3. System Controller detects failure by monitoring TXCTRL and TXABRT.
4. System Controller disables transmitter via RF power amplifier.
5. System Controller sends TXRST to prepare DPROC for next transmission.

Note to the Abort Procedure

If a message is loaded into DPROC after a TXABRT has occured this word will remain in the DPROC transmit register and will not be cleared to TXRST.
If this situation arises the method of clearing the buffer ready for a second access attempt is to leave TXHOLD LOW and then send a TXRST prior to setting up a new transmission after TXLINE goes HIGH; this will clear any residual data in the buffer.

Signal Tone Generation (ST)

The 8 or 10 kHz (TACS or AMPS) tone generated from the Manchester Encoding Block is used as the Signalling Tone stream.

ANALOG CIRCUIT BLOCKS

General

The analog signal processing functions on DPROC are implemented using switched-capacitor techniques. The main filtering functions are operated at 300 kHz, and these circuits are 'interfaced' to the continuous time and sampled digital domains by distributed RC active filters, passive interpolators and comparators.

The distributed RC sections, the Anti-Alias Filter and the Clock Noise Filter, are non-critical and are designed to tolerate process spreads. The critical filtering in the SAT Filter and the Output Filter, is performed by 300 kHz switched-capacitor circuitry. The Passive Interpolators increase the sampling rate from 300 kHz to 1.2 MHz. The sampled analog signals from the Passive Interpolators are converted to sampled 2-state digital signals by the Strobed Comparators. The Gated Digital-to-Analog converters and Analog Summer blocks perform resynchronization and sub-sampling of the digitally generated DPROC output signals, and conversion to the sampled analog domain.

These analog section of the device are shown in Fig.1.

Reference Voltage Generator

The Reference Voltage Generator generates the analog ground reference voltage (AGND) used internally within the DPROC device. To minimize noise AGND must be externally decoupled to V_{SSA} as shown in Fig.19.

Anti-Alias Filter

The Anti-Alias Filter is placed before the SAT sampling block to prevent any unwanted signals or high-frequency noise present on the DEMODD pin being aliased into the pass-band by the sampling action of the switched-capacitor filter. To achieve this the Anti-Alias Filter is a continuous time-distributed RC-active low-pass filter.

Table 8 Digital Colour Code; 7-bit word

DCC1	DCC0	Coded DCC						
0	0	0	0	0	0	0	0	0
0	1	0	0	1	1	1	1	1
1	0	1	1	0	0	0	1	1
1	1	1	1	1	1	1	0	0
		DCC1			DCC0		DCC1.EXOR.DCC0	

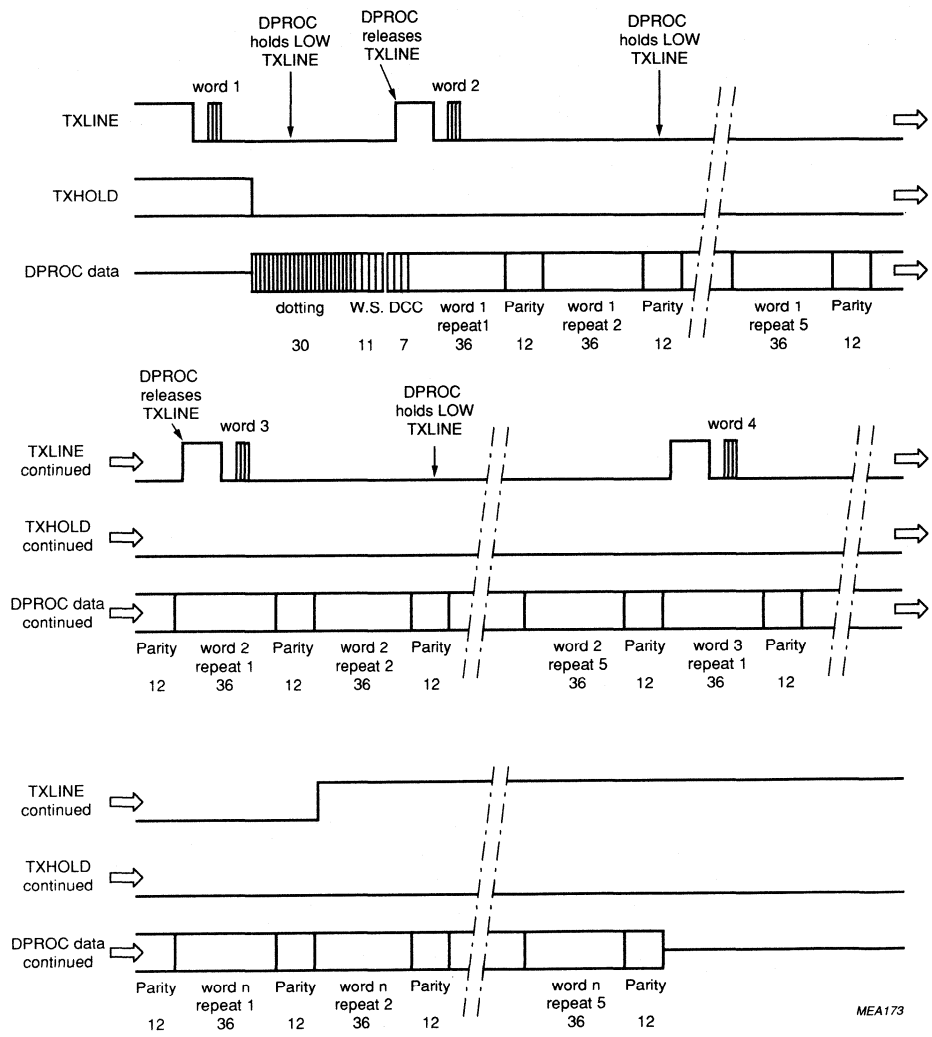


Fig.17 DPROC data transmission timing/microcontroller interface.

SAT Input Filter

The SAT Input Filter is a switched-capacitor filter which provides band-pass filtering of the SAT signals from the DEMODD pin to improve the SAT signal-to-noise ratio prior to recovery and transponding.

Passive Interpolator

The function of the Passive Interpolator is to increase the sampling rate at the output of the switched-capacitor filters. This reduces the coarseness of the zero-crossing information which would otherwise cause unacceptable isochronous distortion in the recovered signal.

Strobed Comparators

The Strobed Comparators form the analog-to-digital interface for the received data and SAT signals from the DEMODD pin. These comparators act as limiting amplifiers which convert the filtered sampled analog signals into 2-state sampled digital signals containing only the zero-crossing information from the analog signal.

Gated Digital-to-Analog and Analog Summer

The Gated Digital-to-Analog converters and Analog Summer form the interface between the digital and analog circuitry on the transmit path of DPROC. It is at this point that the three sampled digital signals, containing SAT, ST and encoded digital data, are combined to form a composite signal.
The data streams are enabled by the I²C signals STEN, SATEN and the internal signal DATAEN respectively (DATAEN disables SAT and ST when data is being transmitted). The digital-to-analog conversion and sub-sampling operation is performed by the Gated Digital-to-Analog converters and Analog Summer. The relative signal weights applied in the summer (with respect to the data path) are shown in Table 9.

Output Filter

The Output Filter is a switched-capacitor filter which performs band-limiting of the DPROC output signals in accordance with the AMPS and TACS specifications. The required below band roll-off is achieved via external AC coupling from the DATA pin.

Clock Noise Filter

The filter is a non-critical continuous time-distributed RC-active low-pass filter used to remove any switching transient residues from the output signal.

Table 9 Relative signal weights

SIGNAL	RELATIVE OUTPUT LEVEL AMPS AND TACS
ST	1.0
SAT	0.25
DATA	1.0

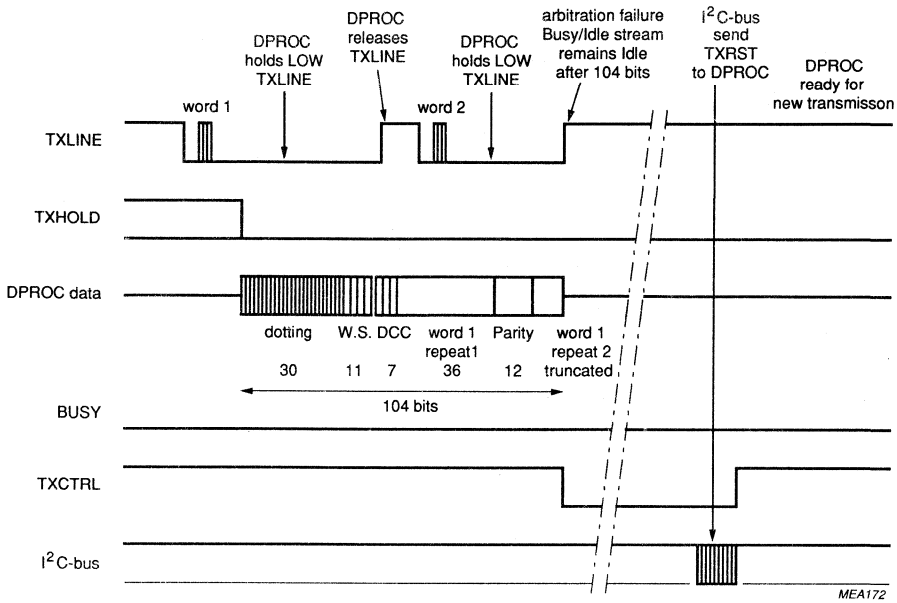


Fig.18 DPROC data transmission timing/microcontroller interface during arbitration failure.

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 358 10011.

APPLICATION INFORMATION

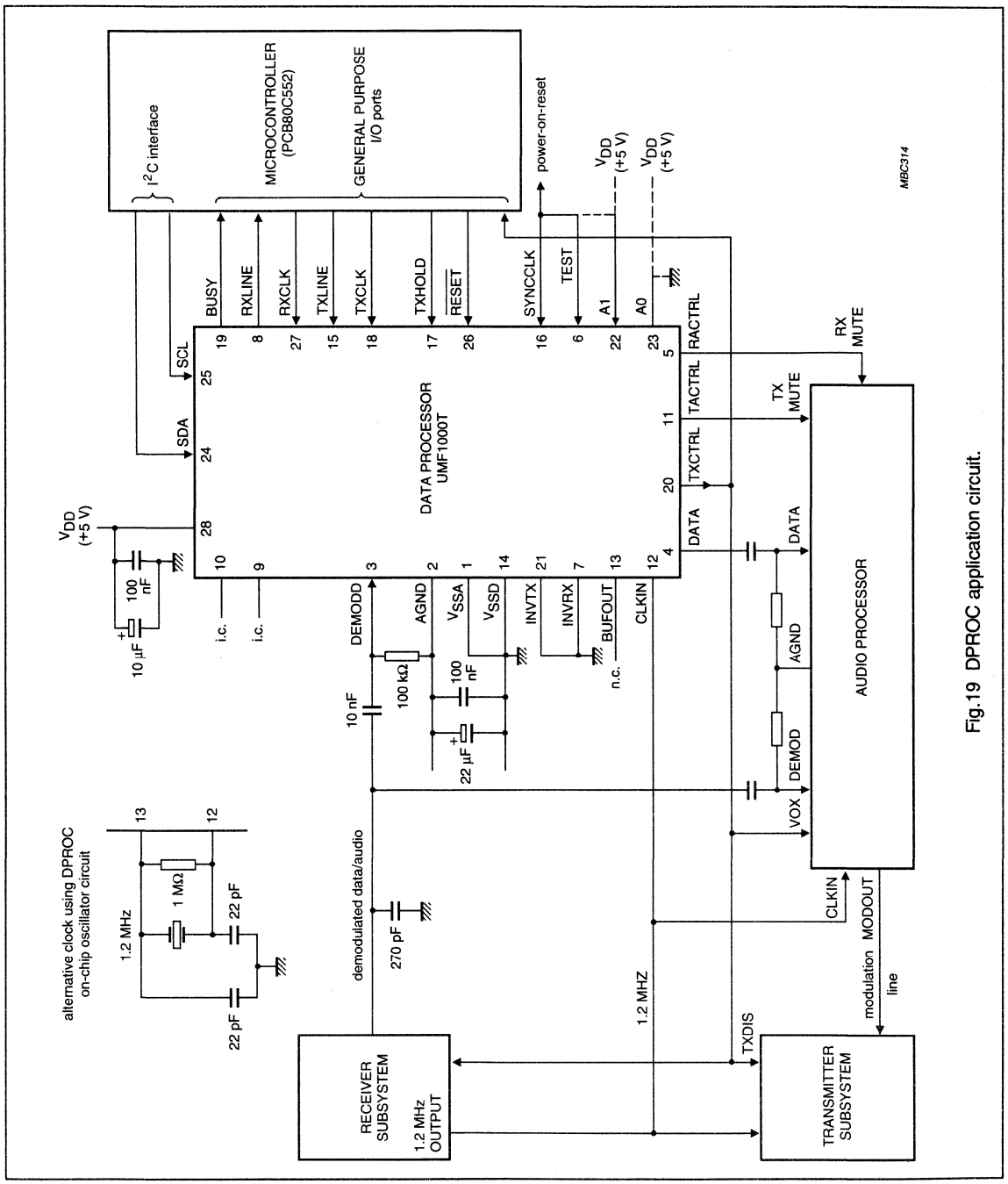


Fig.19 DPROC application circuit.

Data sheet	
status	Preliminary specification
date of issue	October 1990

VN2406L

N-channel enhancement mode vertical D-MOS transistor

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK SC07 OR DATA SHEET

FEATURES

- Very low $R_{DS(on)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching.
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope and designed for use as a line current interrupter in telephone sets and for applications in relay, high-speed and line transformer drivers.

PIN CONFIGURATION

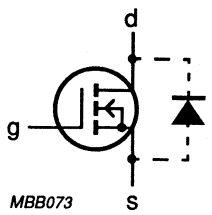


Fig.1 Symbol.

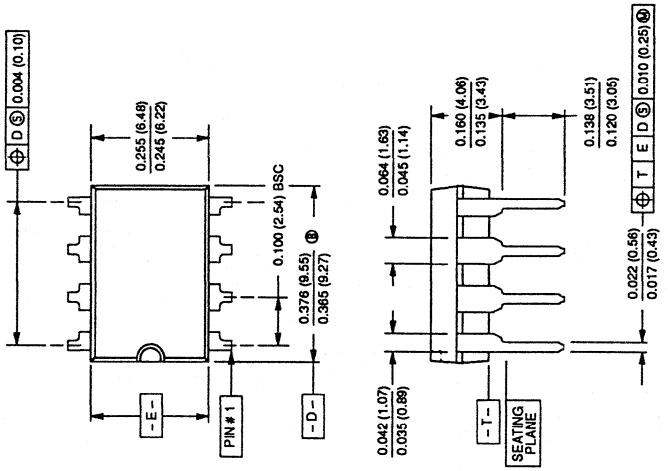
PINNING - TO-92 variant

PIN	DESCRIPTION
1	drain
2	gate
3	source

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	240	V
I_D	drain current	210	mA
$R_{DS(on)}$	drain-source on-resistance	6	Ω
$V_{GS(th)}$	gate-source threshold voltage	2	V

PACKAGE INFORMATION

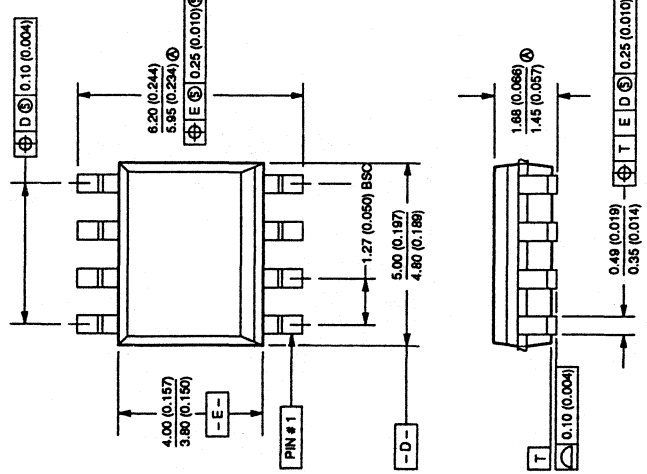


NOTES

1. Controlling dimension: Inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC Specification MS-001-AB for standard Dual In-Line (DIP) package 0.300 inch row spacing (plastic) 8 leads (Issue B, 7/85).
3. Dimension and tolerancing per ANSI Y14, 5M – 1982.
4. "T", "D", and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with Pin #1 and continue counterclockwise to Pin #8 when viewed from the top.

853–0404B 07236

Fig.1 8-pin (300 mils wide) plastic dual in-line (N) package (DWG 0404B).

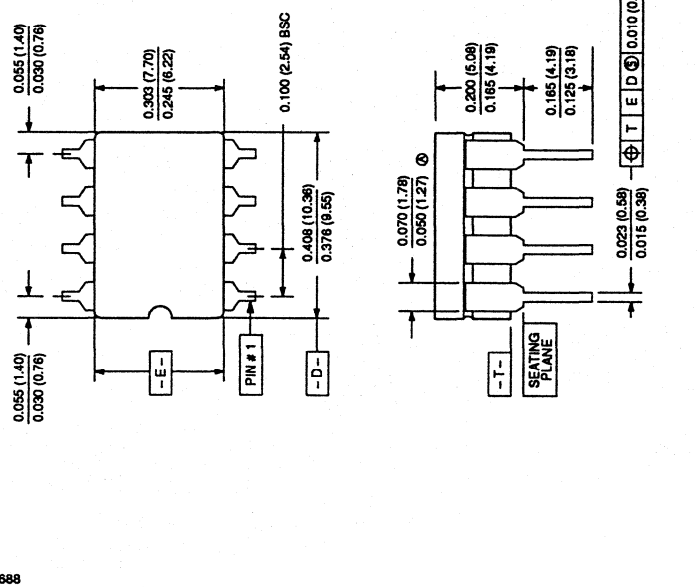


853-0174C 04697

NOTES

1. Package dimensions conform to JEDEC Specification MS-012-AA for standard Small Outline (SO) package, 8 leads, 3.75mm (0.150") body width (Issue A, June 1985).
2. Controlling dimensions are mm. Inch dimensions in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982.
4. "D" and "E" are reference datums on the molded body and do not include mold flash/protrusions. Mold flash/protrusions at "D" shall not exceed 0.15mm (0.006") per side. Inter-lead flash/protrusions at "E" shall not exceed 0.25mm (0.010") per side.
5. The lead width above the seating plane shall not exceed a maximum value of 0.61mm (0.024").
6. Pin numbers start with Pin #1 and continue counterclockwise to Pin #8 when viewed from top.
7. Signetics ordering code for a product packages in a plastic Small Outline (SO) package is the suffix D after the product number.

Fig.2 8-pin (157 mils wide) plastic SO (Small Outline) dual in-line (D) package (DWG 0174C).



NOTES:

1. Controlling dimension: Inches. Millimeters are shown in parentheses.
2. Dimension and toleranding per ANSI Y14. 5M-1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with Pin #1 and continue counterclockwise to Pin #8 when viewed from the top.

853-0580A 006688

Fig.3 8-pin (300 mils wide) ceramic dual in-line (F) package (DWG 0580A).

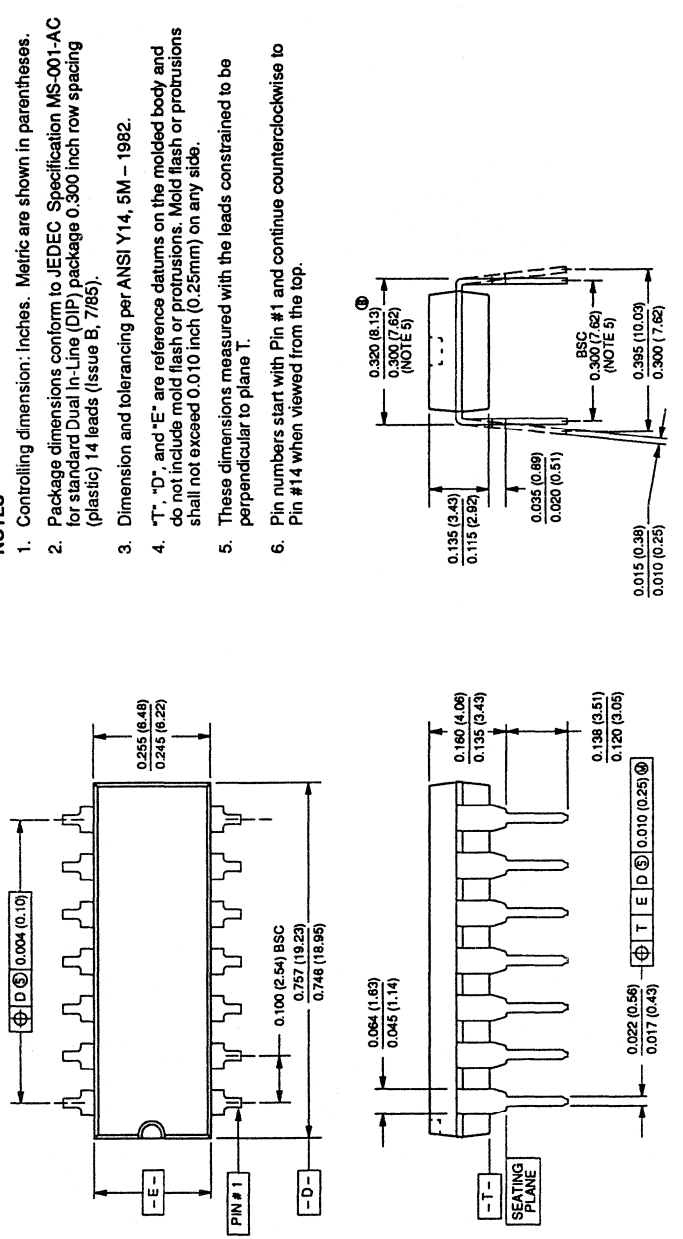


Fig.4 14-pin (300 mils wide) plastic dual in-line (N) package (DWG 0405B).

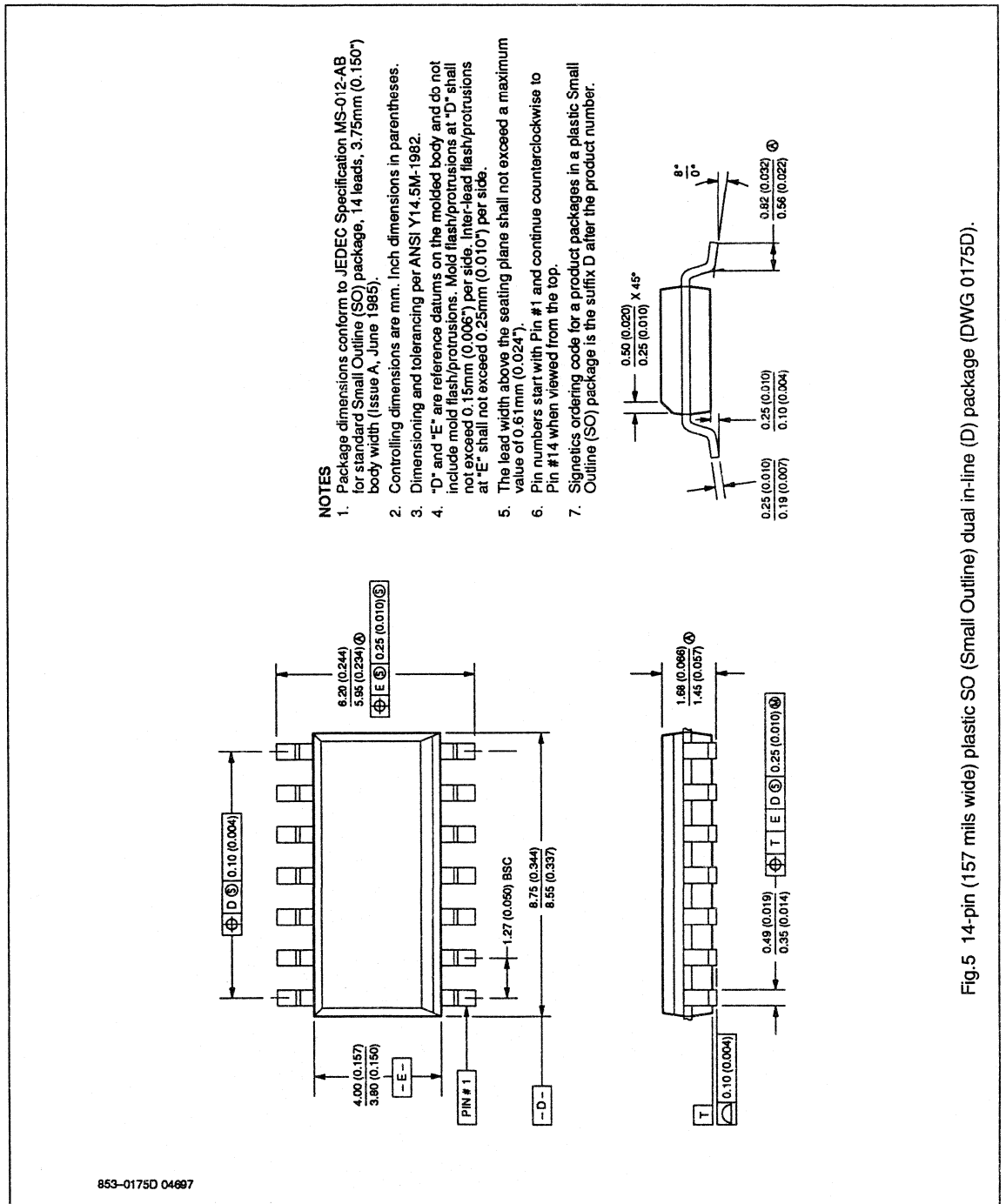
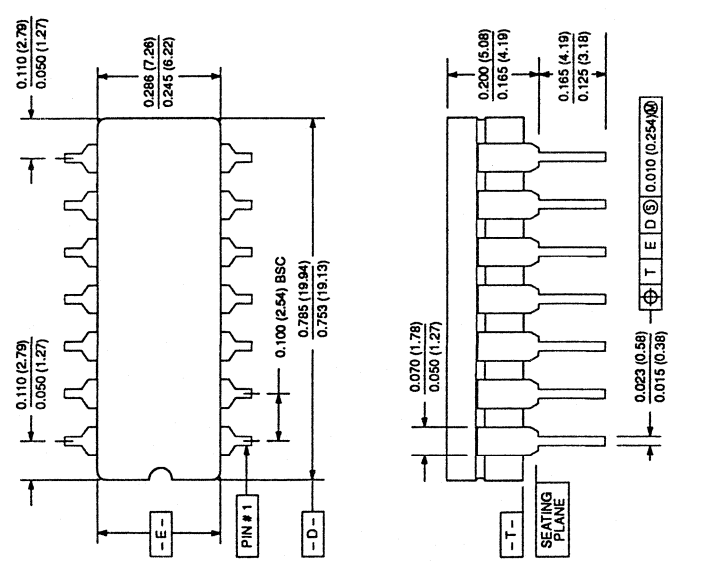


Fig.5 14-pin (157 mils wide) plastic SO (Small Outline) dual in-line (D) package (DWG 0175D).



NOTES:

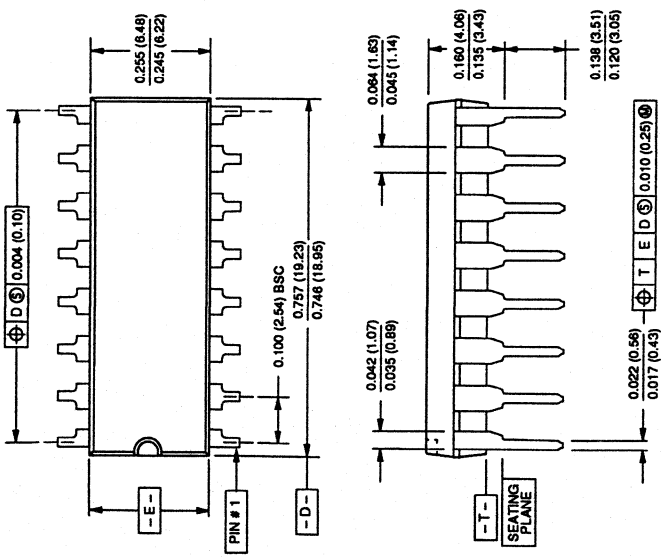
1. Controlling dimension: Inches. Millimeters are shown in parentheses.
2. Dimension and tolerancing per ANSI Y14.5M-1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with Pin #1 and continue counterclockwise to Pin #14 when viewed from the top.

853-0581B 06688

Fig.6 14-pin (300 mils wide) ceramic dual in-line (F) package (DWG 0581B).

NOTES

1. Controlling dimension: Inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC Specification MS-001-AA for standard Dual In-Line (DIP) package 0.300 inch row spacing (plastic) 16 leads (Issue B, 7/85).
3. Dimension and tolerancing per ANSI Y14, 5M – 1982.
4. "T", "D", and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with Pin #1 and continue counterclockwise to Pin #16 when viewed from the top.



853-0406C 02880

Fig.7 16-pin (300 mils wide) plastic dual in-line (N) package (DWG 0406C).

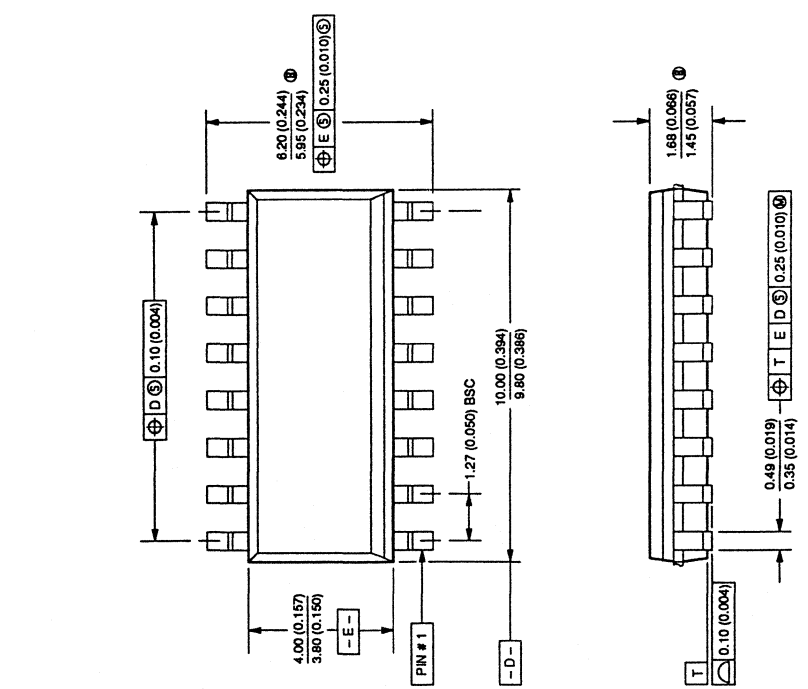


Fig.8 16-pin (157 mils wide) plastic SO (Small Outline) dual in-line package (DWG 0005D).

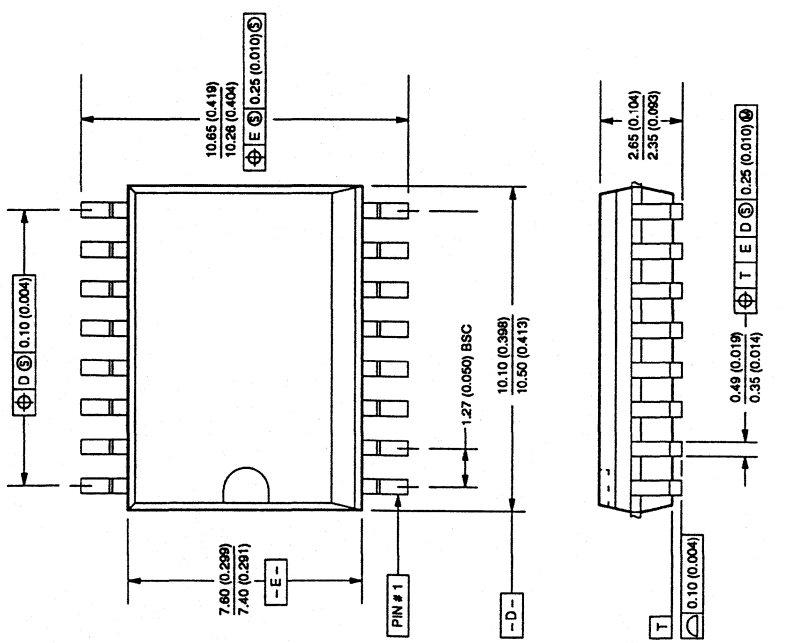


Fig.9 16-pin (300 mils wide) plastic SOL (Small Outline Large) dual in-line (D) package (DWG 0171B).

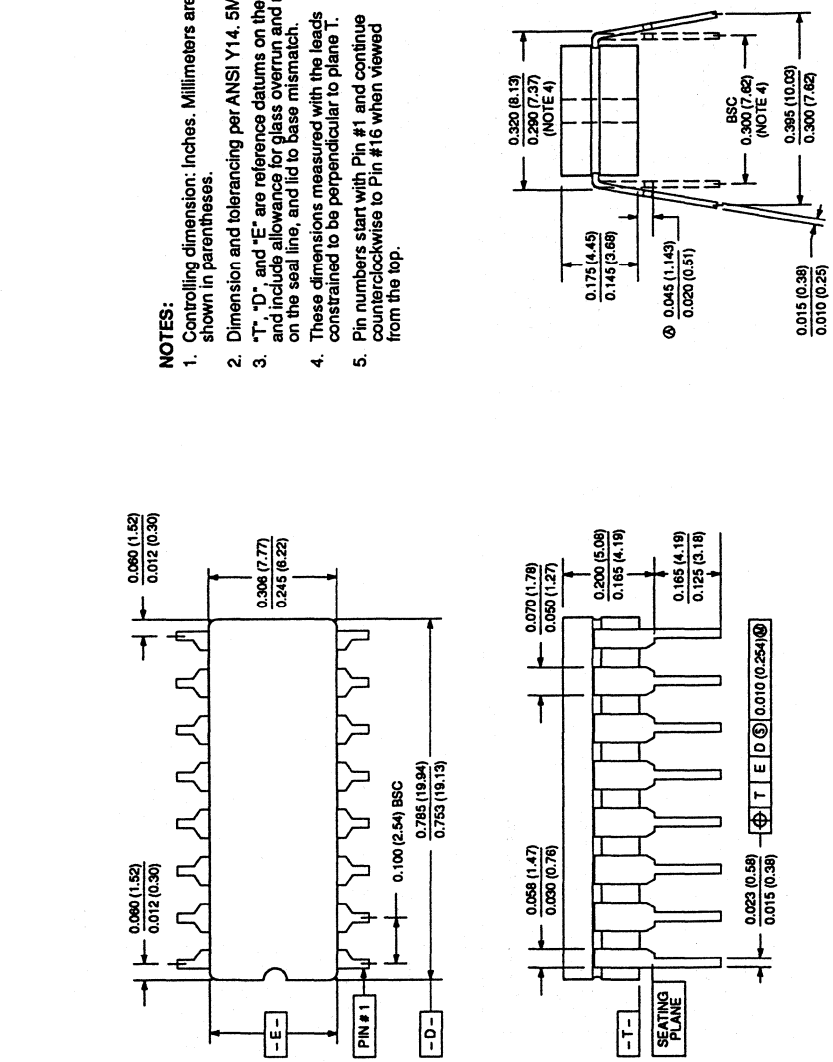


Fig.10 16-pin (300 mils wide) ceramic dual in-line (F) package (DWG 0582B).

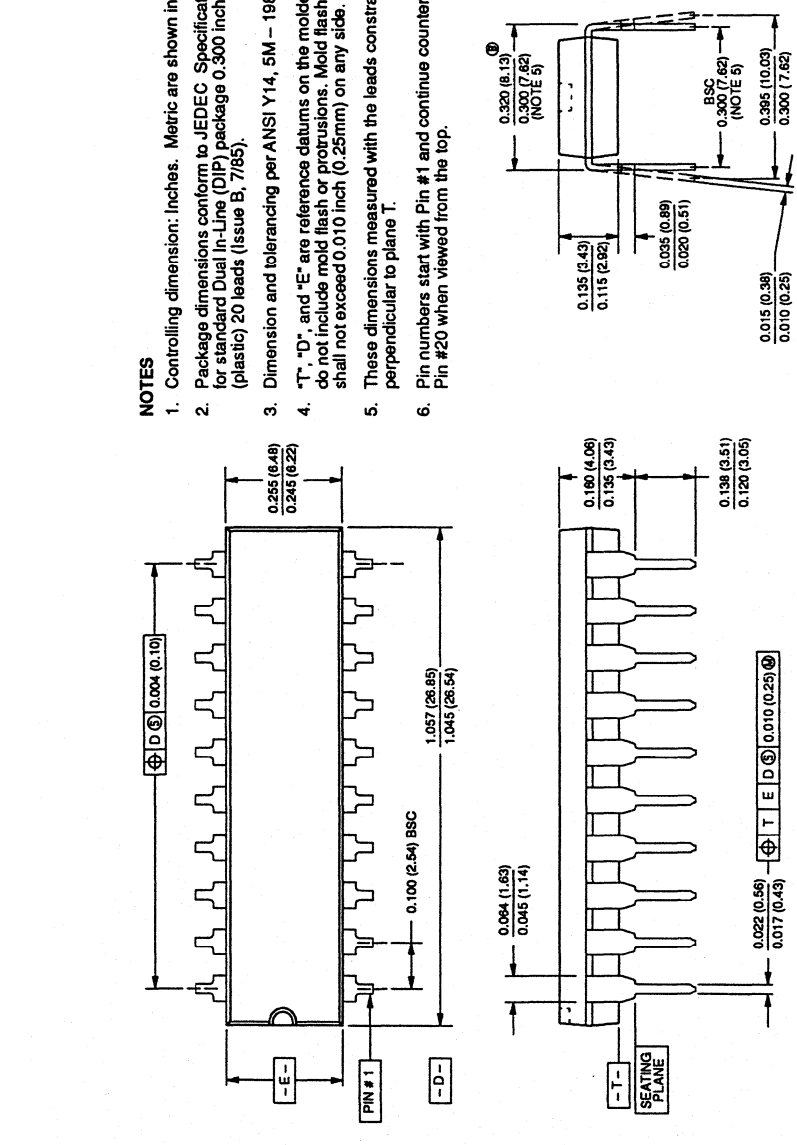


Fig.11 20-pin plastic dual in-line (N) package (DWG 0408B).

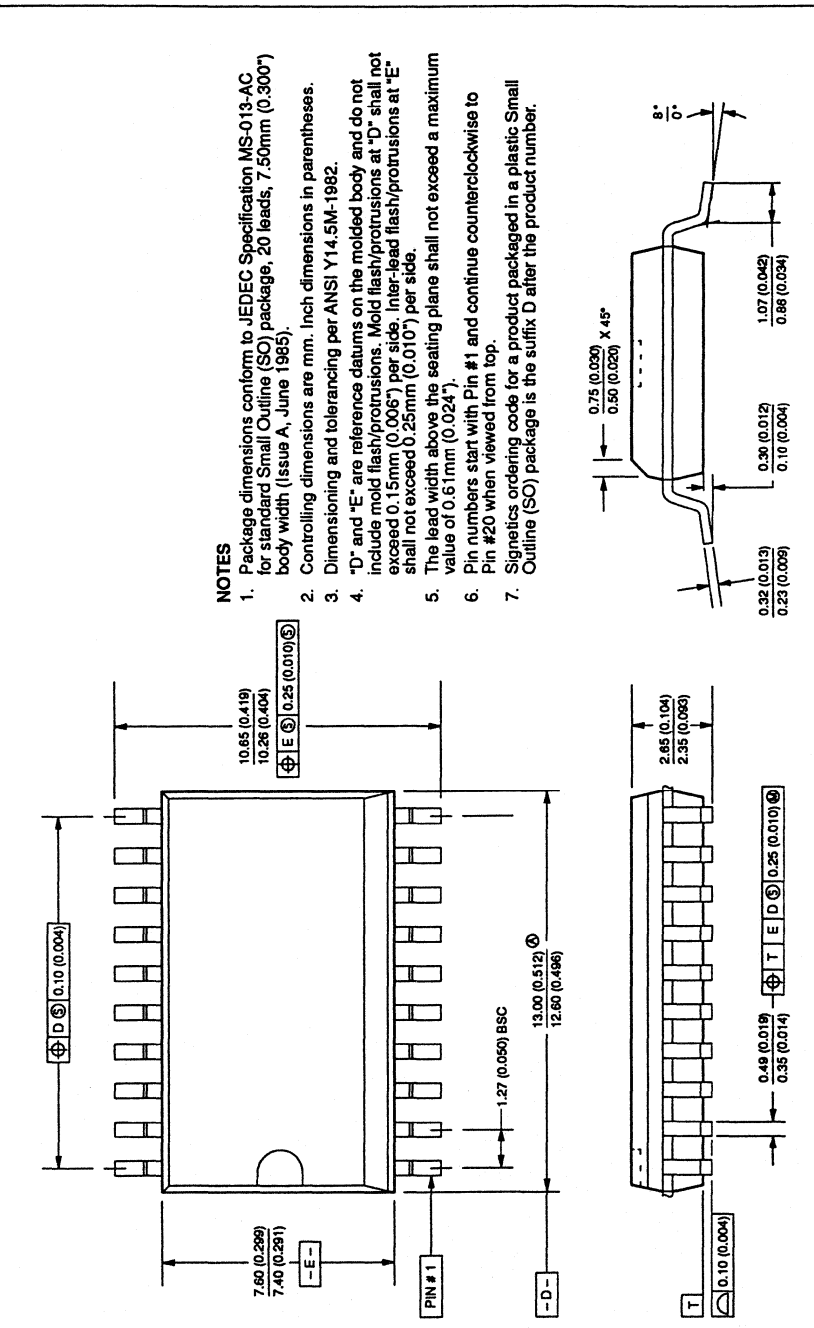


Fig.12 20-pin (300 mils wide) plastic SOL (Small Outline Large) dual in-line (D) package (DWG 0172D).

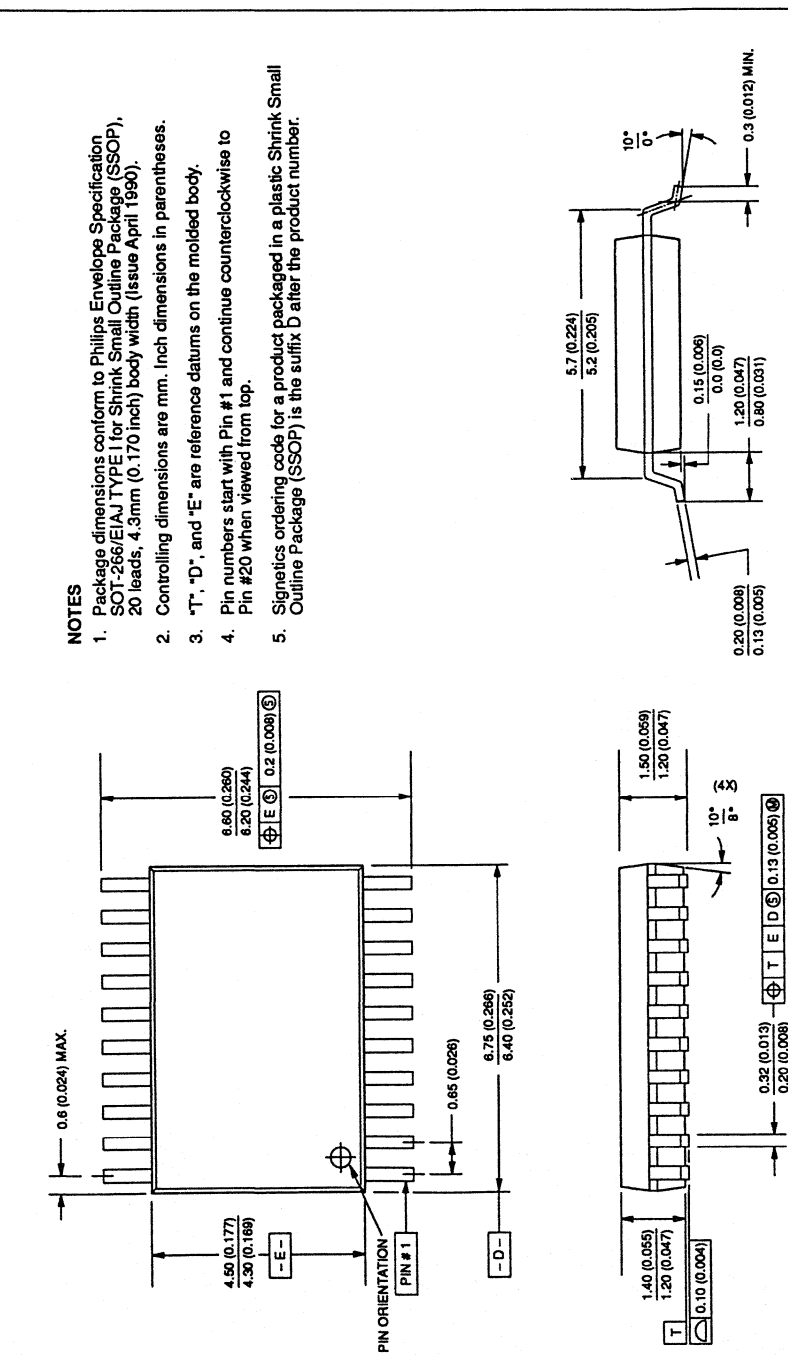


Fig.13 20-pin (170 mils wide) plastic SSOP (Shrink Small Outline Package) dual in-line (DK) package (DWG 1563).

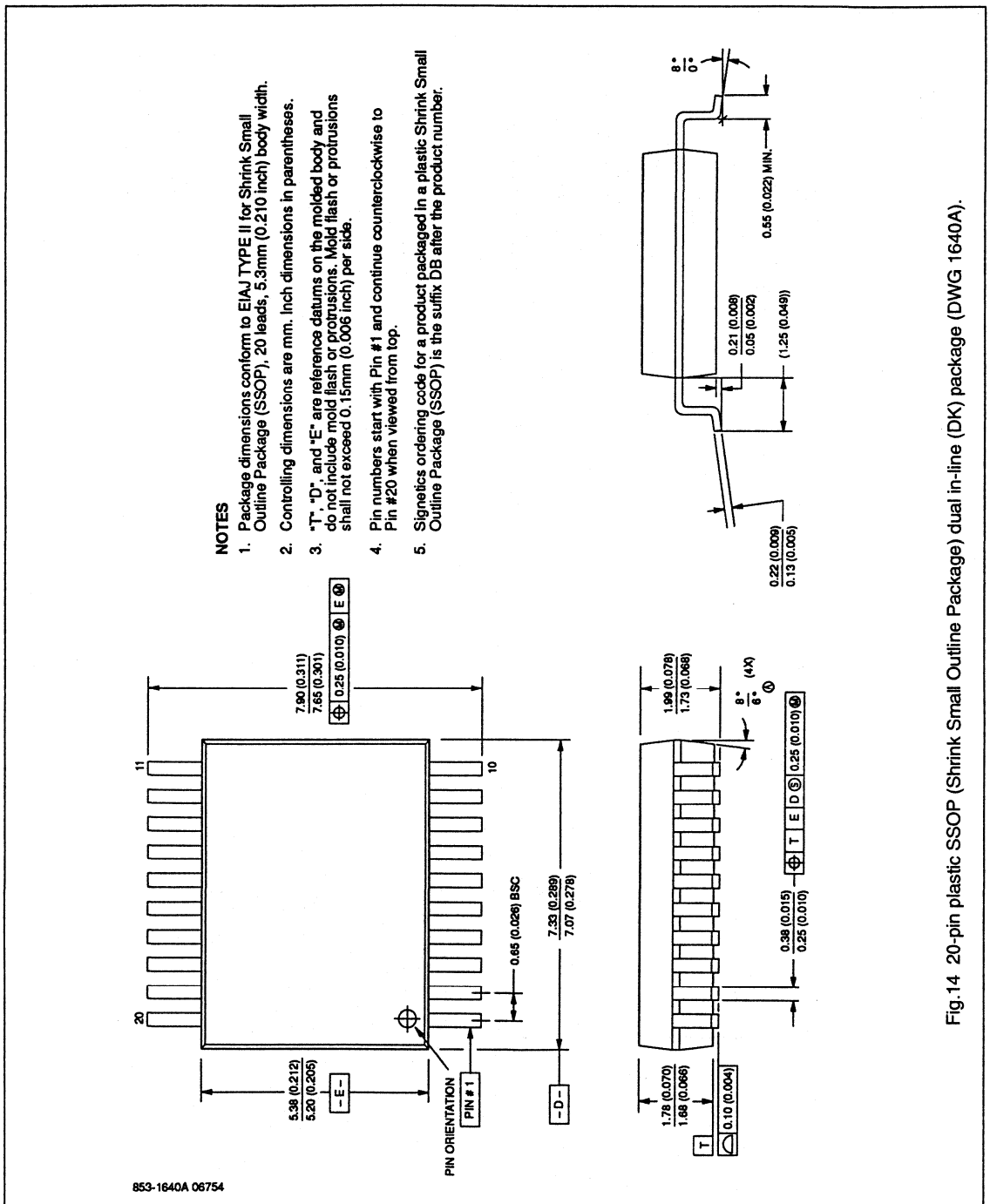


Fig.14 20-pin plastic SSOP (Shrink Small Outline Package) dual in-line (DK) package (DWG 1640A).

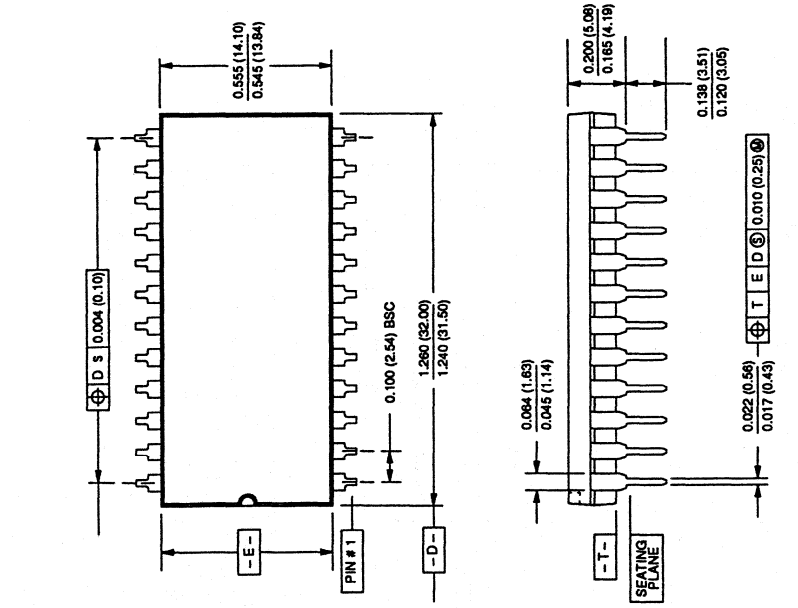


Fig.15 24-pin (600 mils wide) plastic dual in-line (N) package (DWG 0412A).

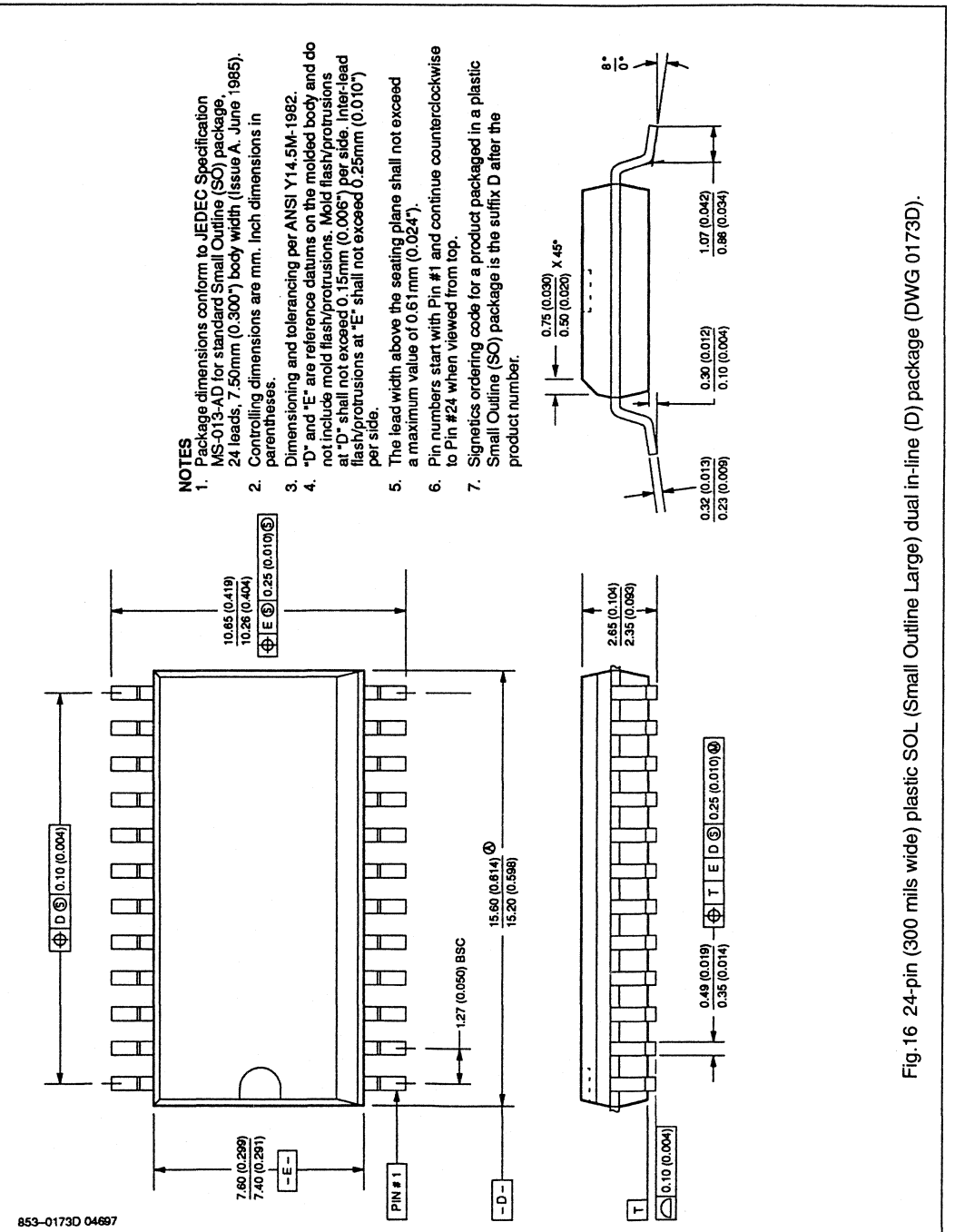


Fig.16 24-pin (300 mils wide) plastic SOL (Small Outline Large) dual in-line (D) package (DWG 0173D).

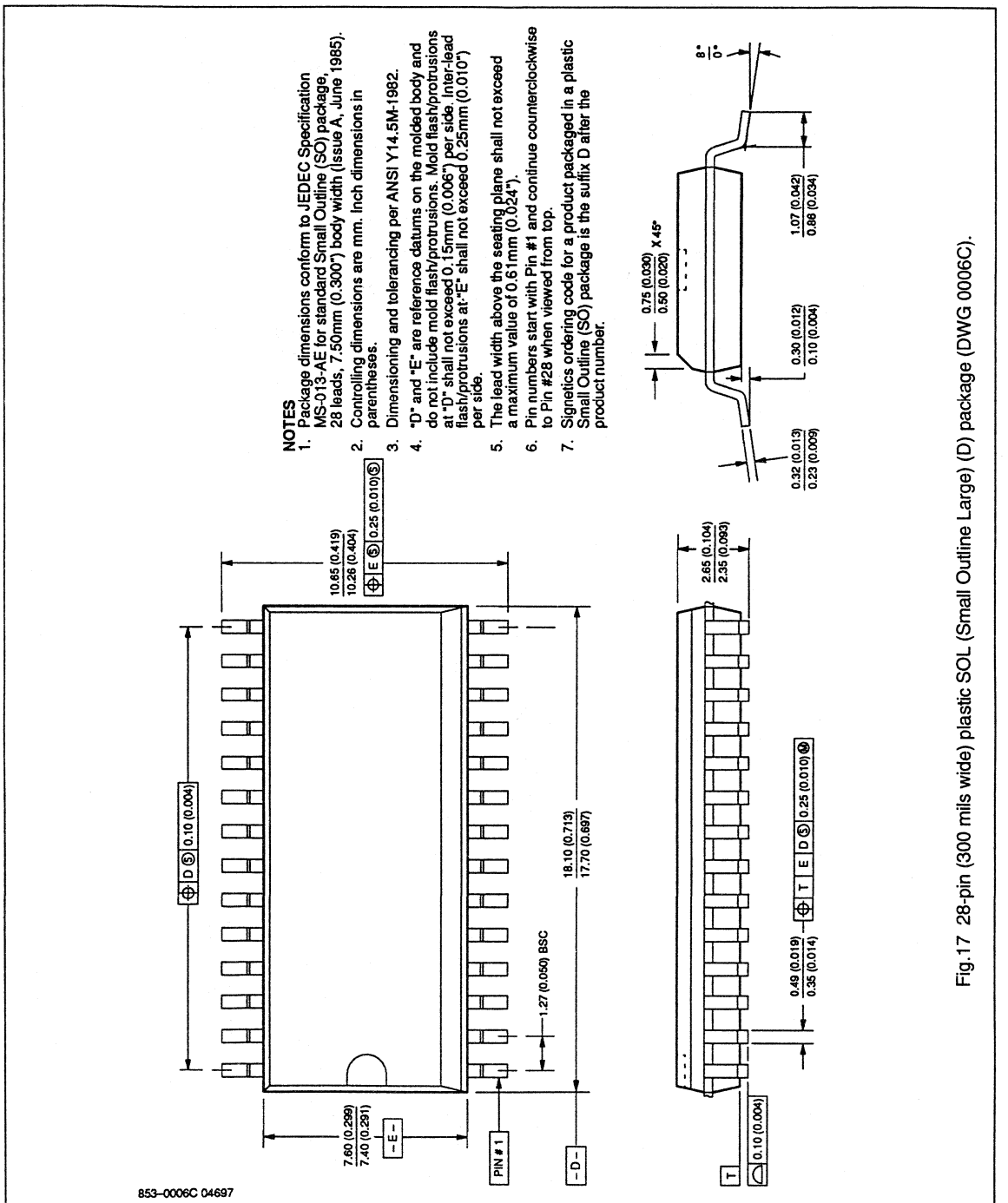


Fig.17 28-pin (300 mils wide) plastic SOL (Small Outline Large) (D) package (DWG 0006C).

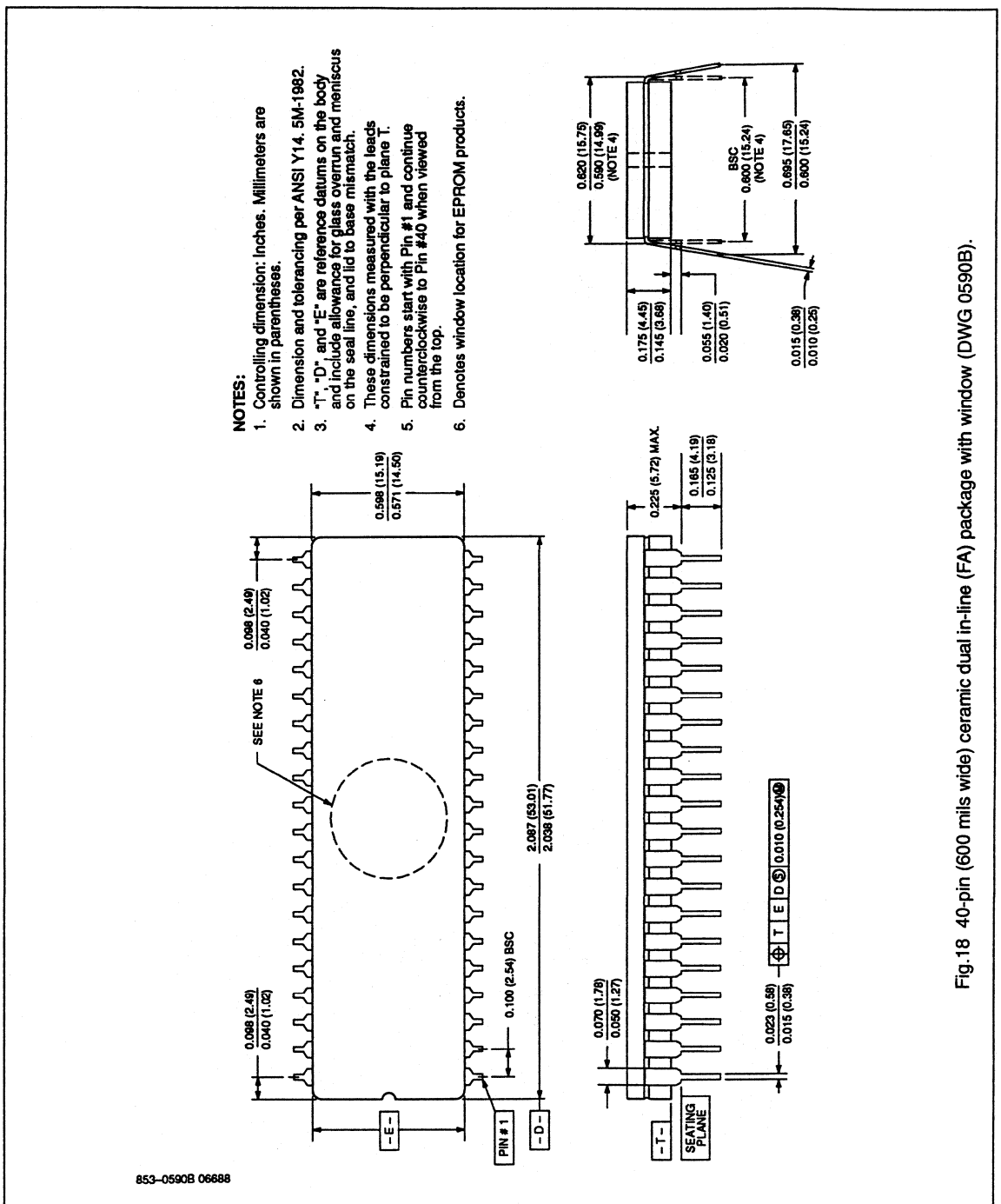


Fig.18 40-pin (600 mils wide) ceramic dual in-line (FA) package with window (DWG 0590B).

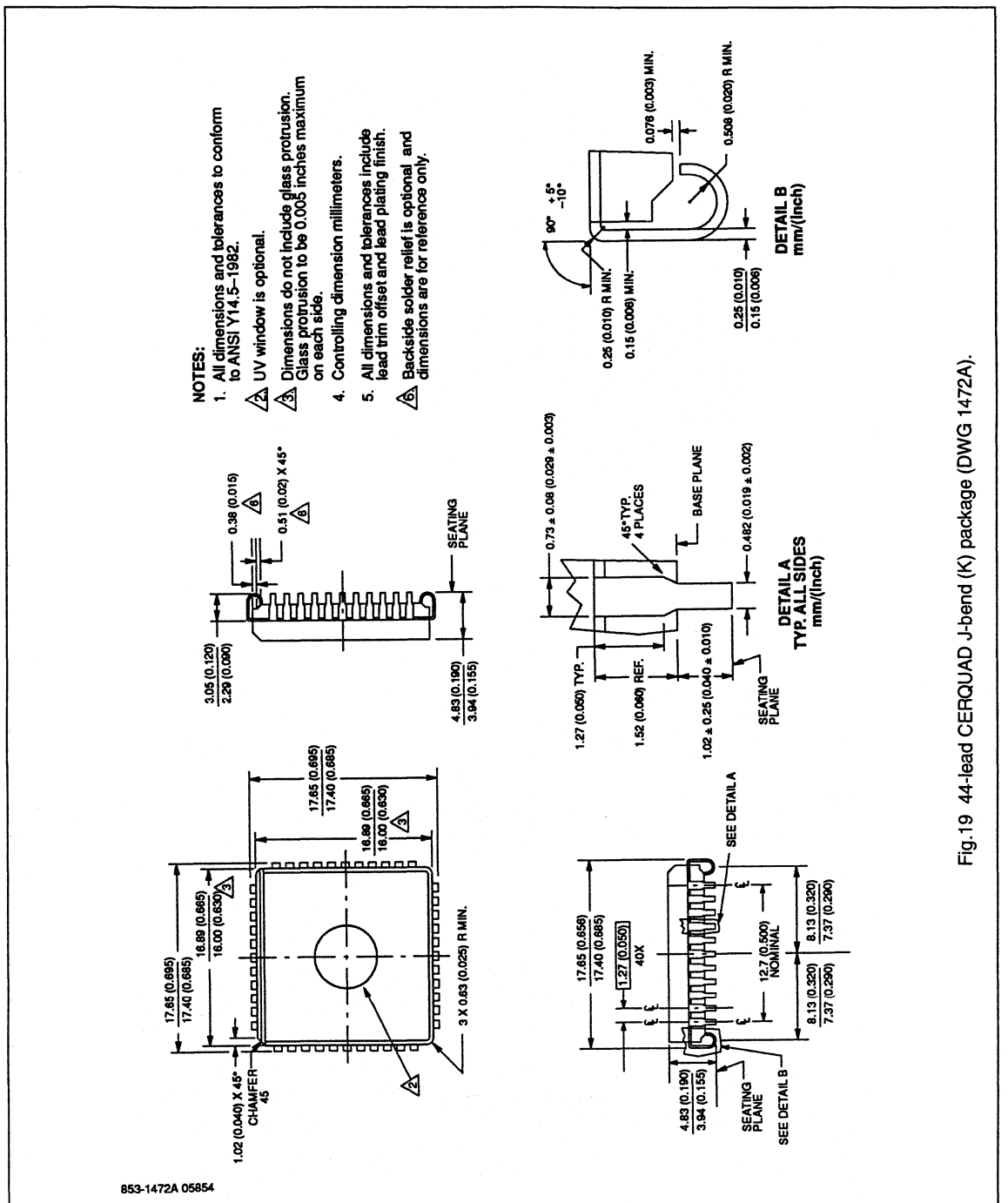


Fig.19 44-lead CERQUAD J-bend (K) package (DWG 1472A).

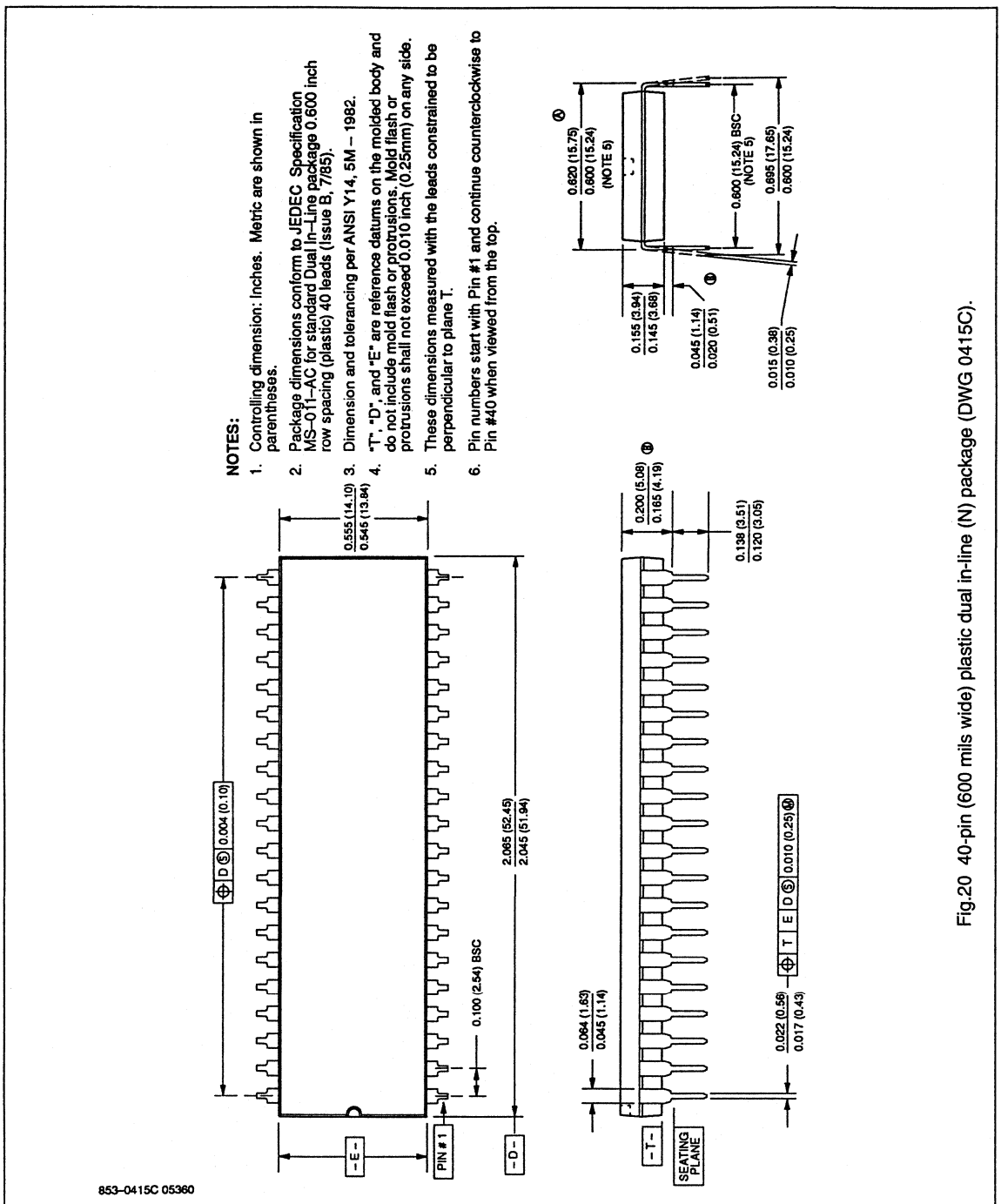


Fig.20 40-pin (600 mils wide) plastic dual in-line (N) package (DWG 0415C).

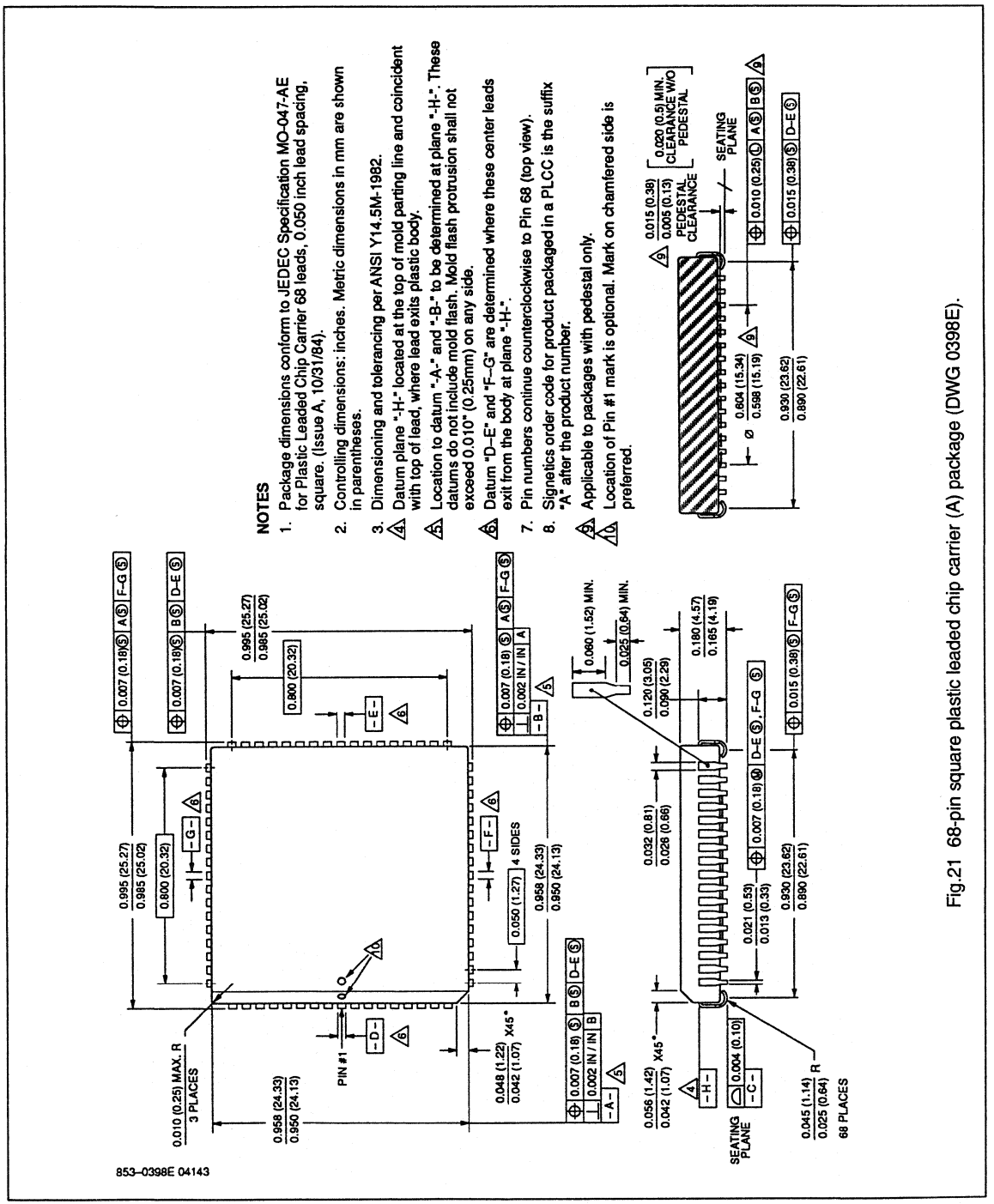


Fig.21 68-pin square plastic leaded chip carrier (A) package (DWG 0398E).

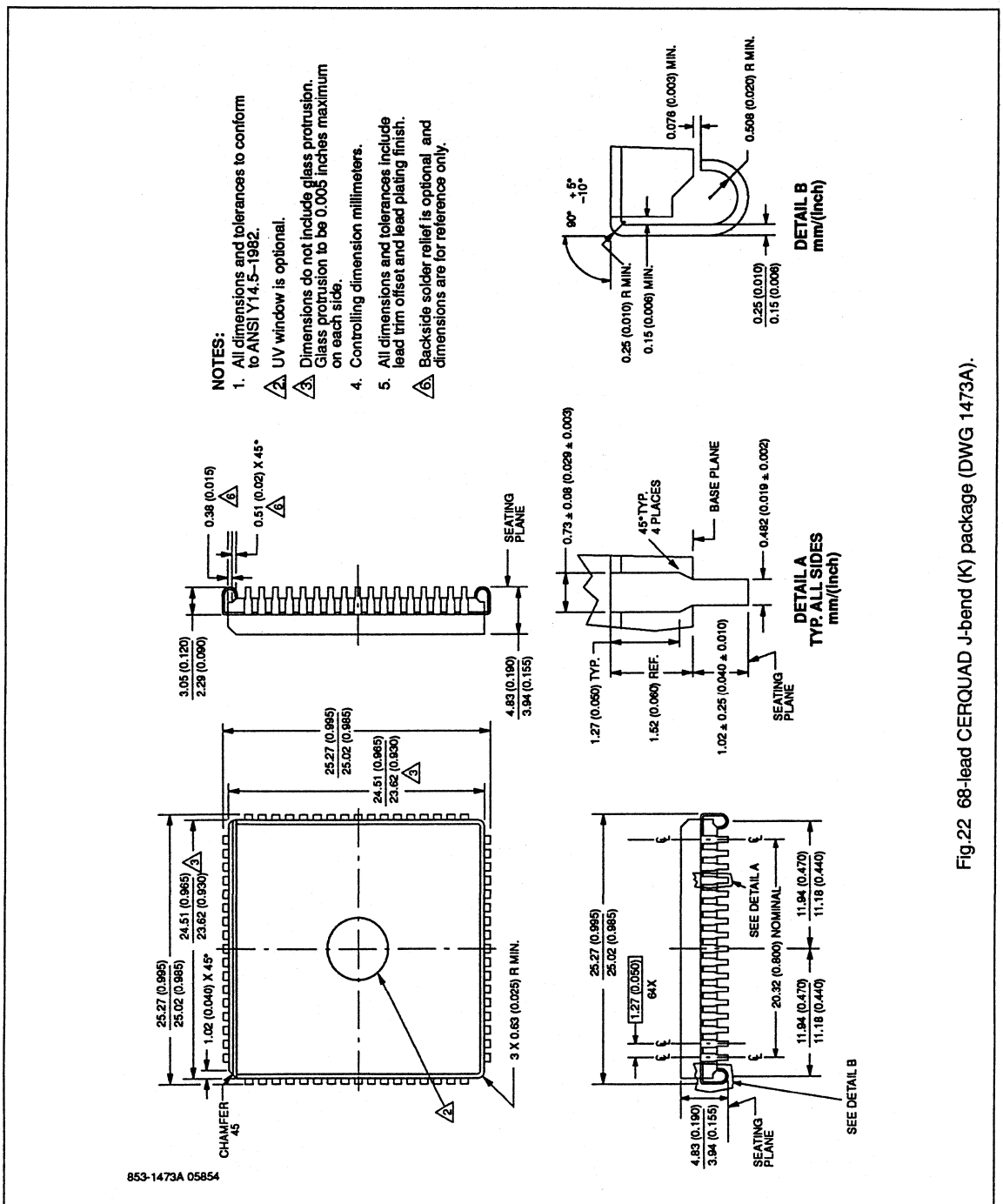
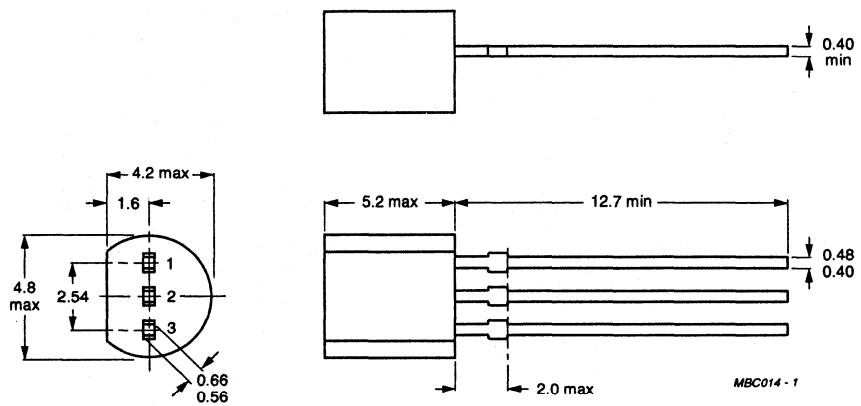
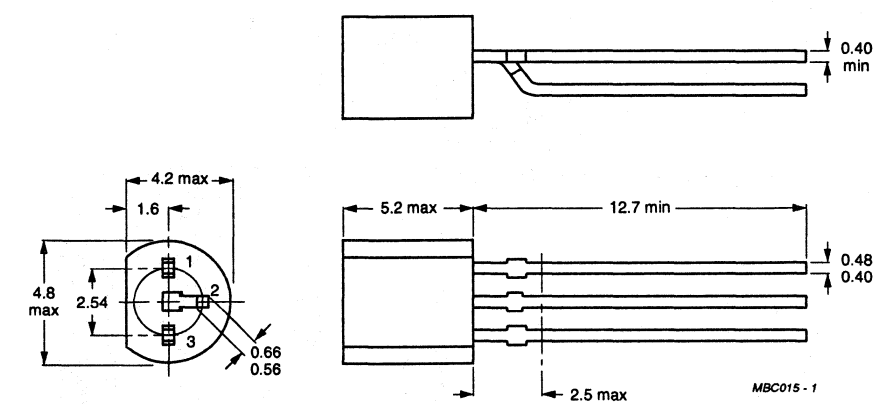


Fig.22 68-lead CERQUAD J-bend (K) package (DWG 1473A).



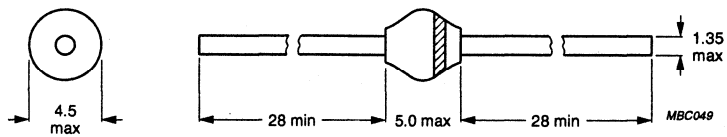
Dimensions in mm.

Fig.23 TO-92 VARIANT (VN2406L series).



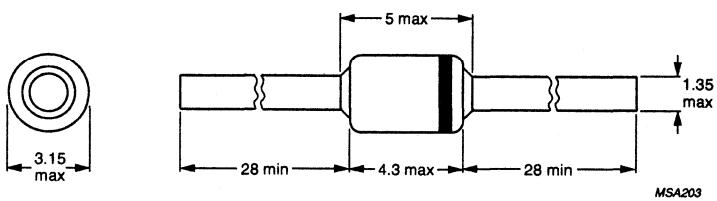
Dimensions in mm.

Fig.24 TO-92 VARIANT (BS107 BS108 BS170 BSN254/A BSP254/A BSS89 BSS92 BST74A BST76A series).



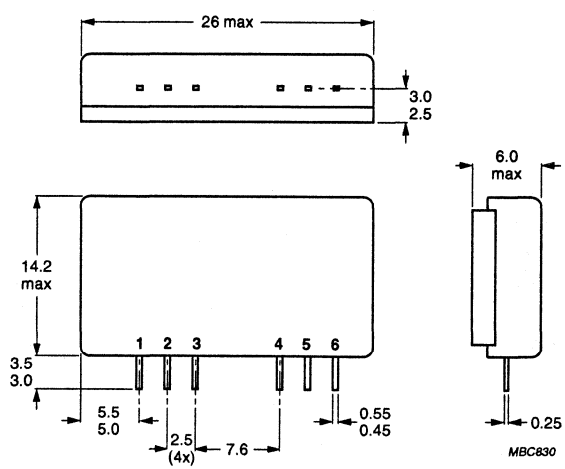
Dimensions in mm.

Fig.25 BZW03 and BZW14 series (SOD64).



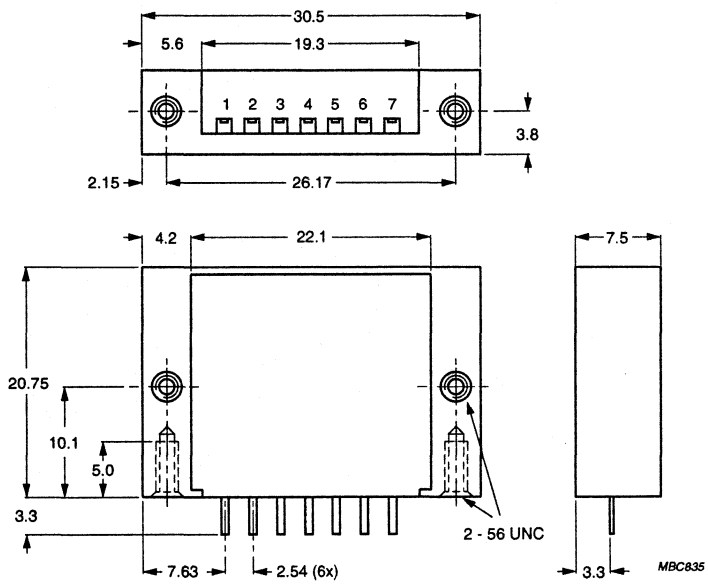
Dimensions in mm.

Fig.26 BR211 series (SOD84).



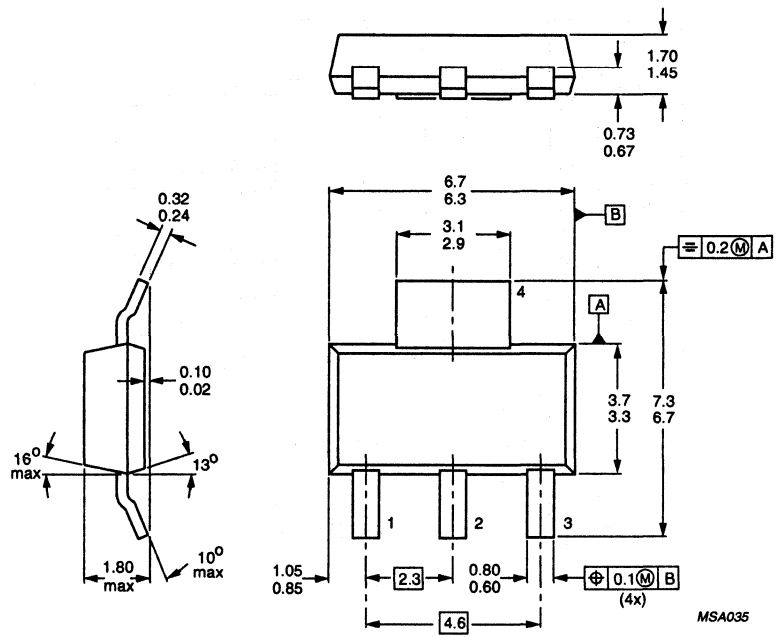
Dimensions in mm.

Fig.27 BGY46A BGY46B BGY47A series (SOT181).



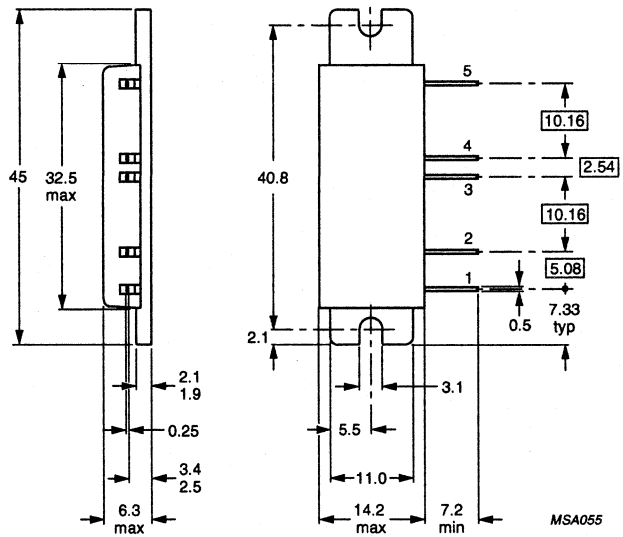
Dimensions in mm.

Fig.28 BGY95A/B BGY96A/B series (SOT200).



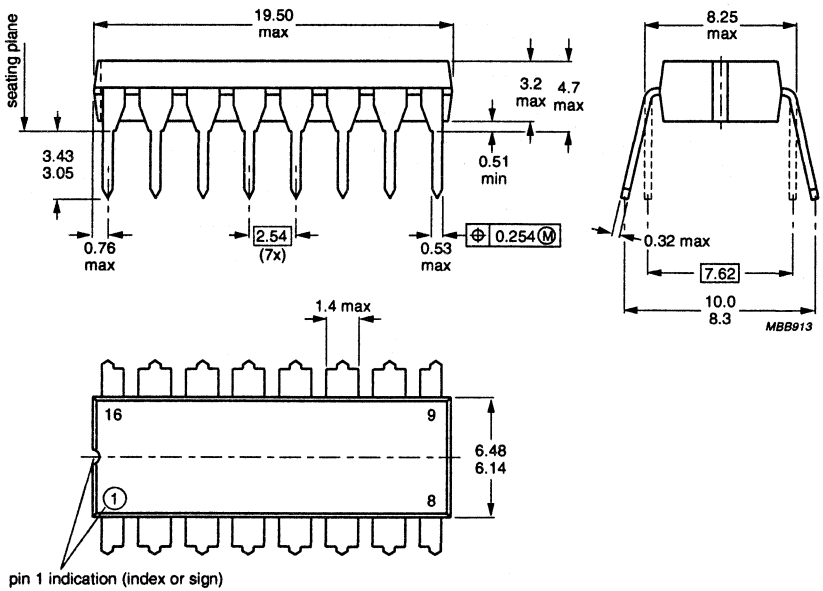
Dimensions in mm.

Fig.29 BSP126 BSP225 BSP89 BSP92 series (SOT223).



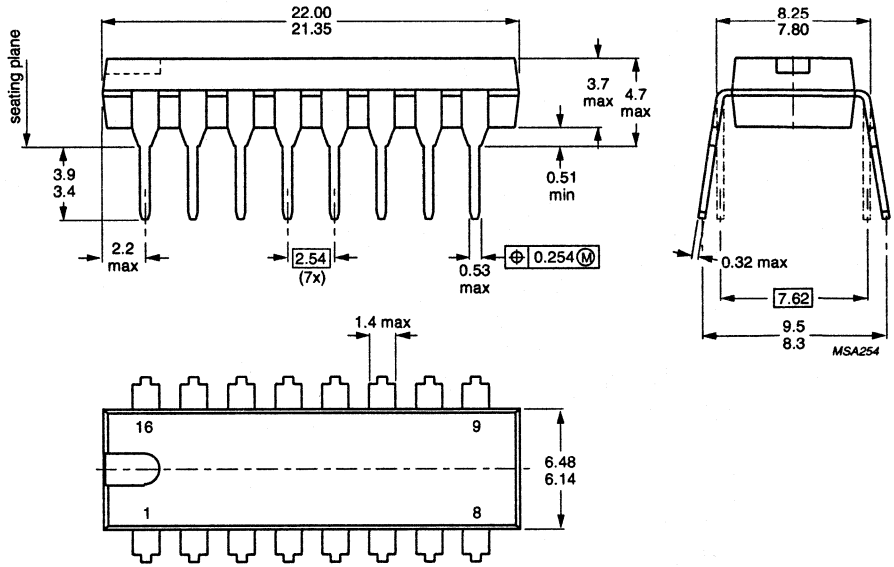
Dimensions in mm.

Fig.30 BGY110D/E/F/G series (SOT246).



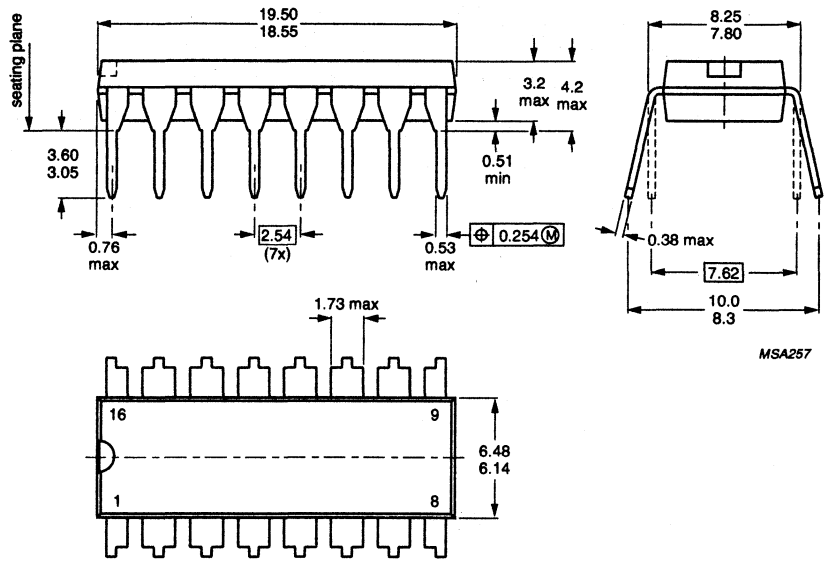
Dimensions in mm.

Fig.31 16-lead dual in-line; plastic (SOT38Z).



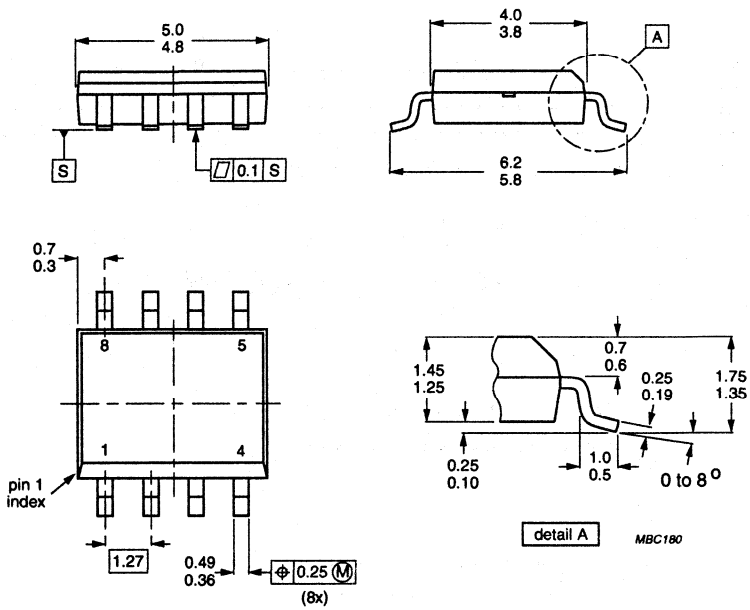
Dimensions in mm.

Fig.32 16-lead dual in-line; plastic (SOT38 GE GG).



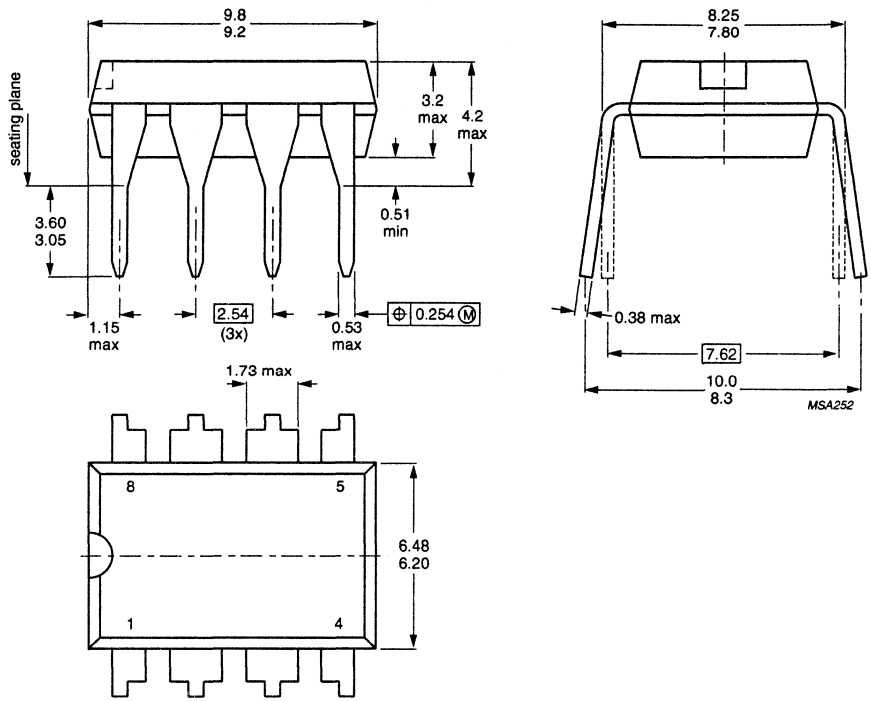
Dimensions in mm.

Fig.33 16-lead dual in-line; plastic (SOT38 DF).



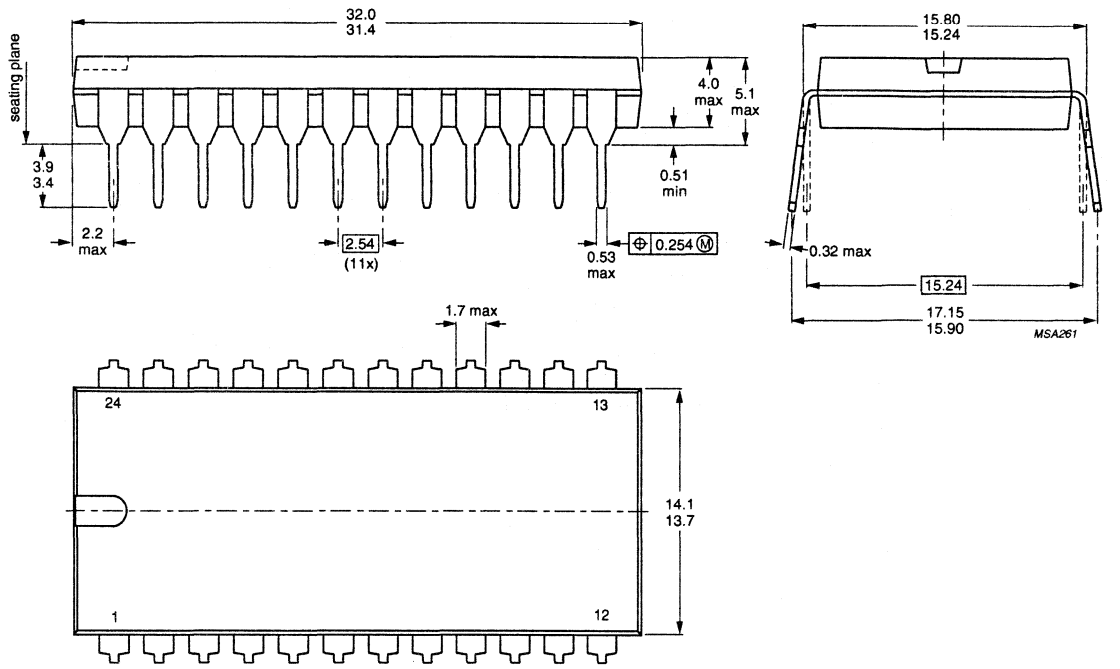
Dimensions in mm.

Fig.34 8-lead mini-pack; plastic (SO8; SOT96A).



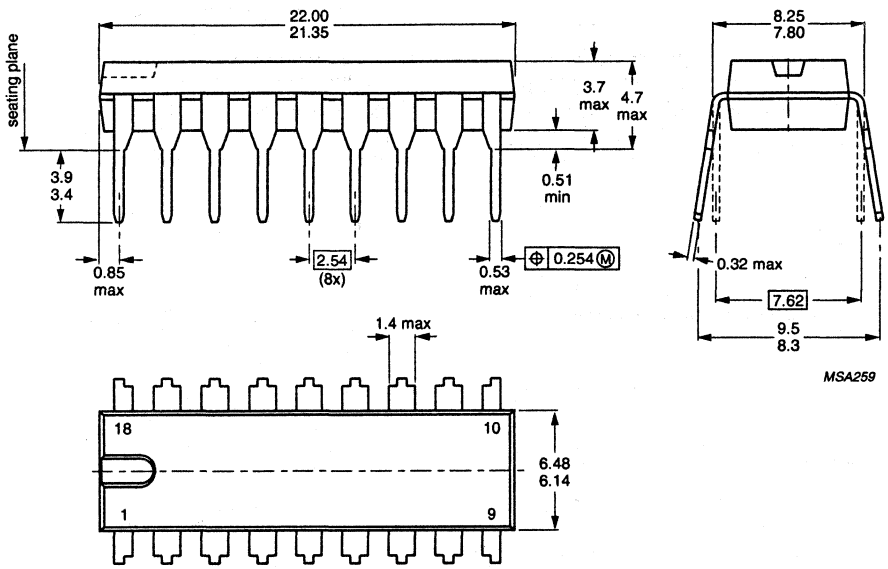
Dimensions in mm.

Fig.35 8-lead dual in-line; plastic (SOT97).



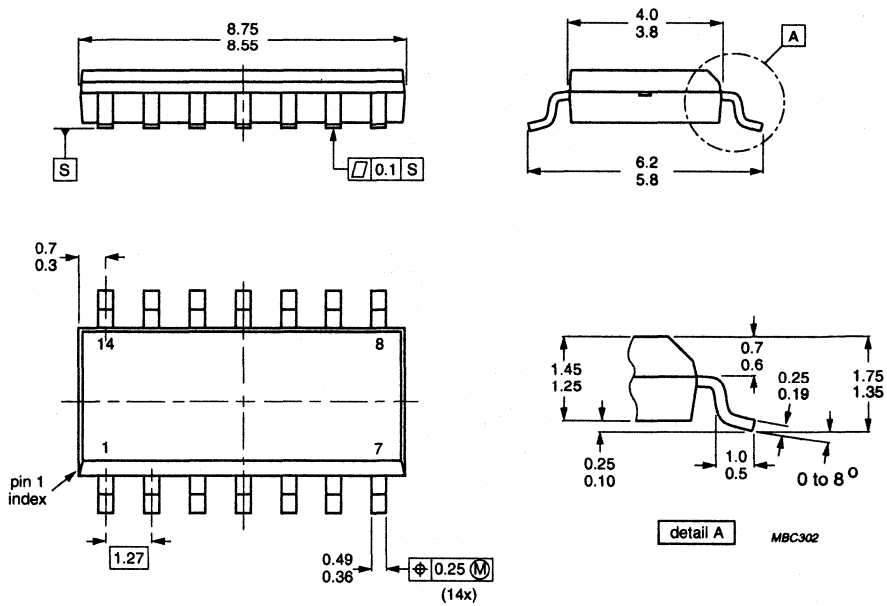
Dimensions in mm.

Fig.36 24-lead dual in-line; plastic (SOT101LG).



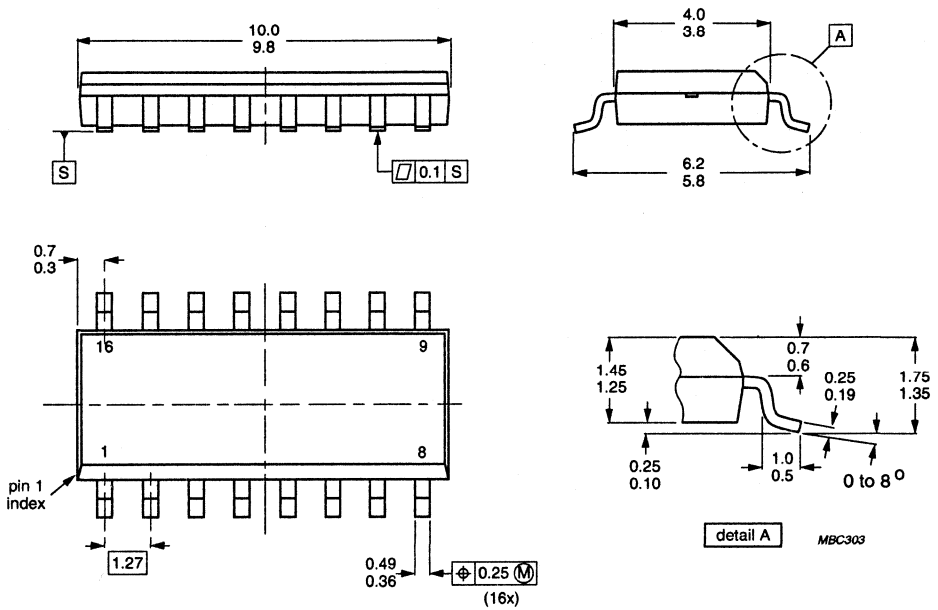
Dimensions in mm.

Fig.37 18-lead dual in-line; plastic (SOT102G).



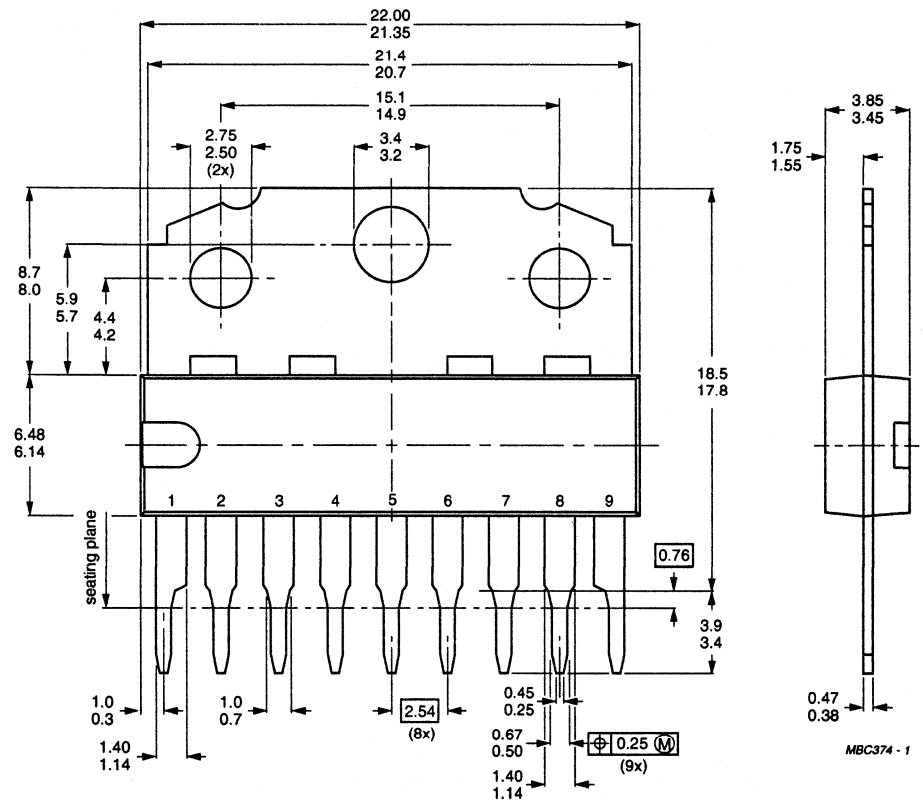
Dimensions in mm.

Fig.38 14-lead mini-pack; plastic (SO14; SOT108A).



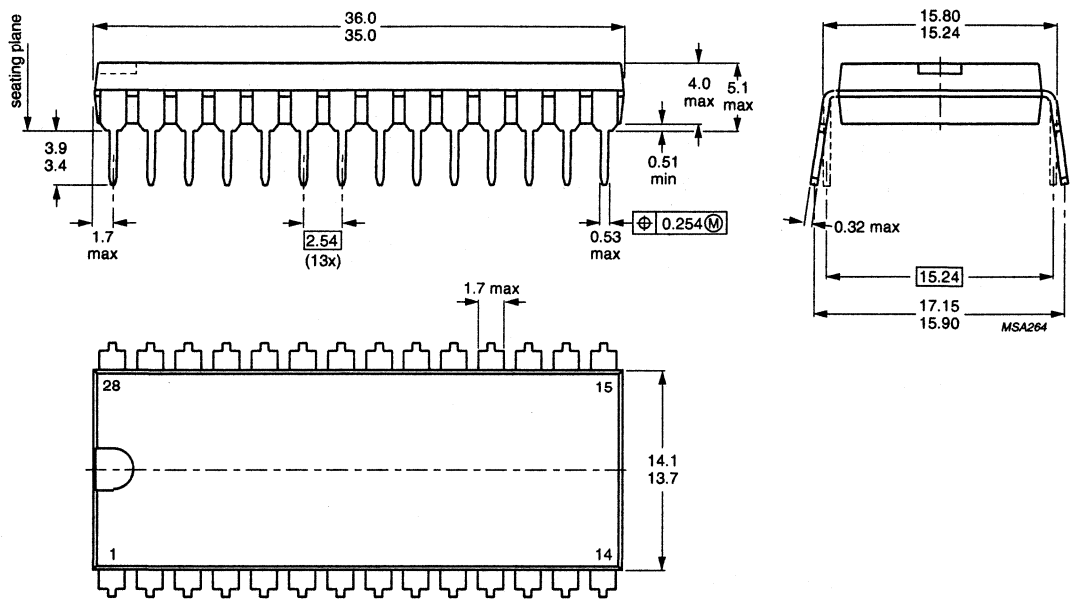
Dimensions in mm.

Fig.39 16-lead mini-pack; plastic (SO16; SOT109A).



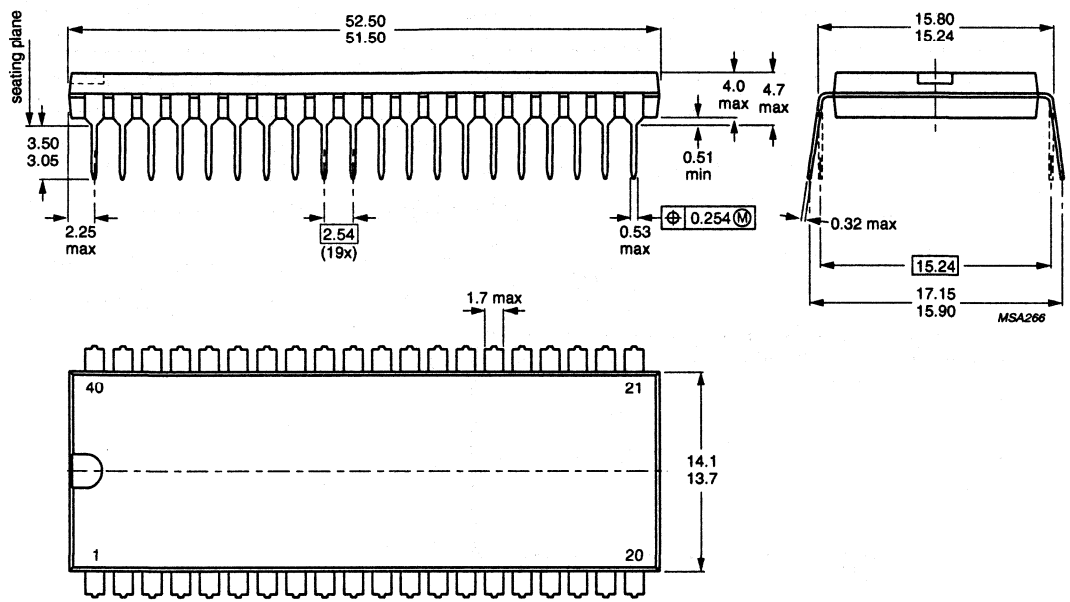
Dimensions in mm.

Fig.40 9-lead single in-line; plastic (SOT110B).



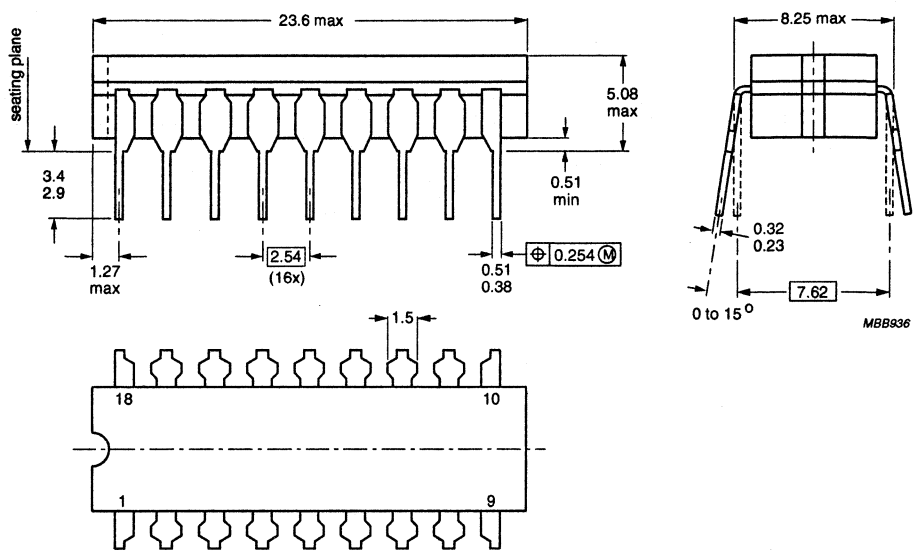
Dimensions in mm.

Fig.41 28-lead dual in-line; plastic (SOT117N).



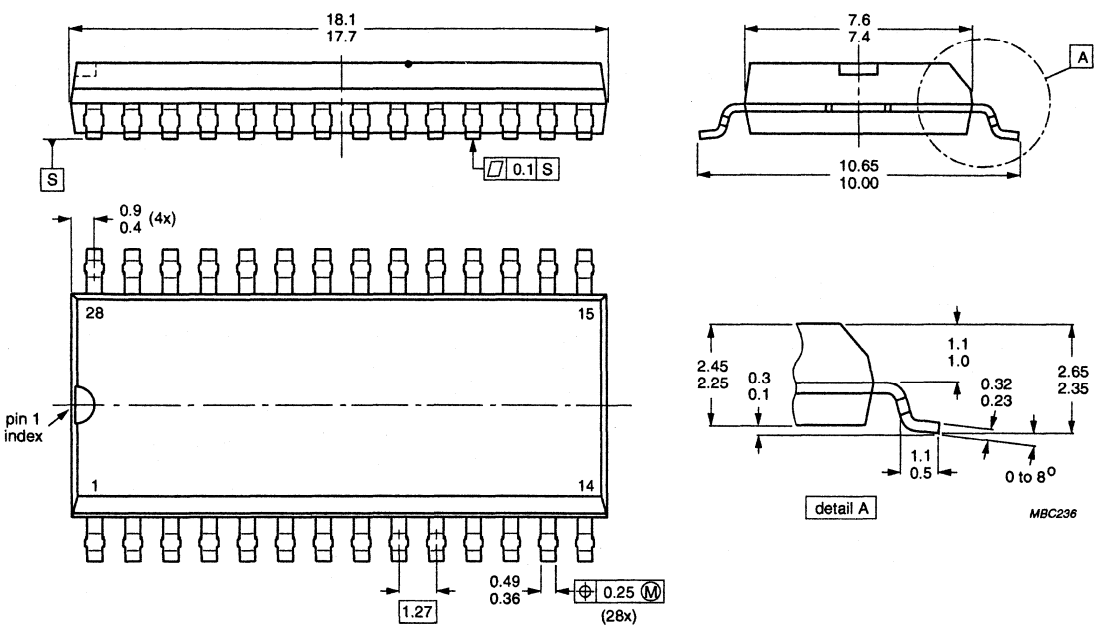
Dimensions in mm.

Fig.42 40-lead dual in-line; plastic (SOT129).



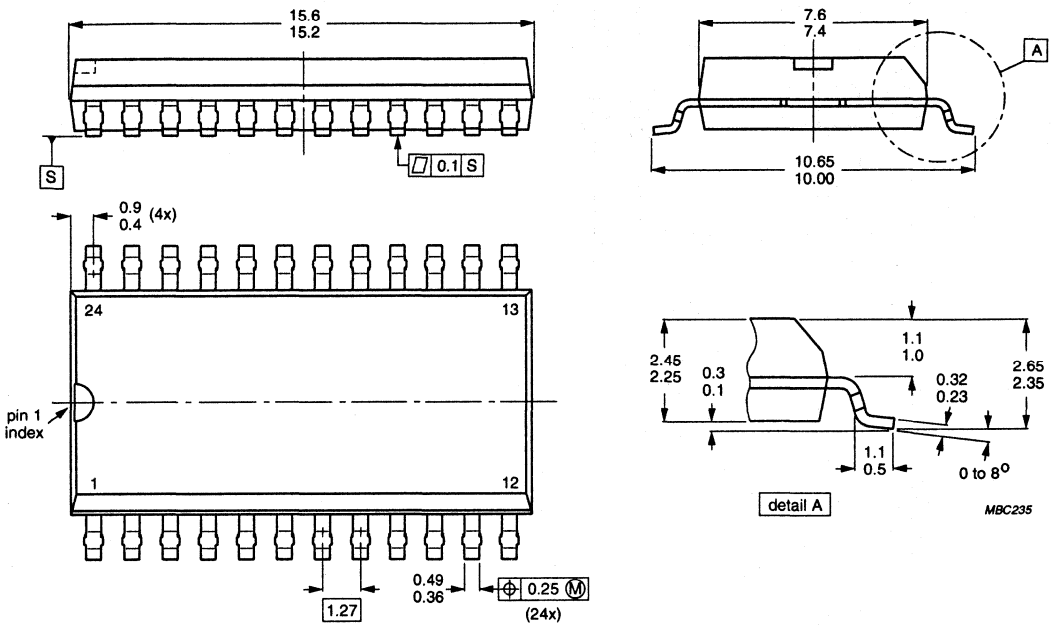
Dimensions in mm.

Fig.43 18-lead dual in-line; ceramic (cerdip) (SOT133B).



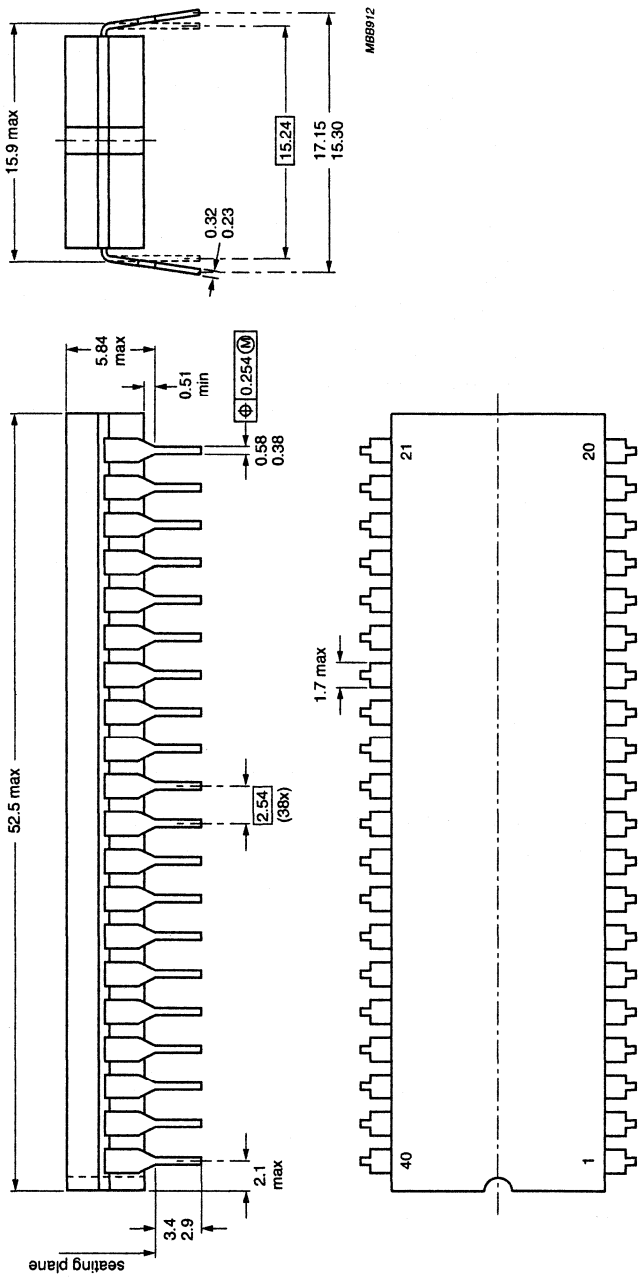
Dimensions in mm.

Fig.44 28-lead mini-pack; plastic (SO-28; SOT136A).



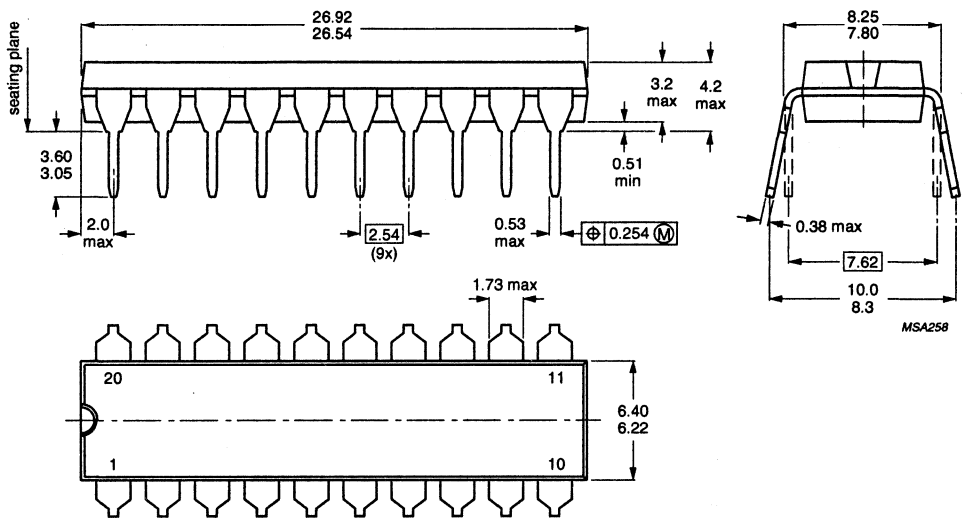
Dimensions in mm.

Fig.45 24-lead mini-pack; plastic (SO-24; SOT137A).



Dimensions in mm.

Fig.46 40-lead dual in-line; ceramic (cerdip) (SOT145).



Dimensions in mm.

Fig.47 20-lead dual in-line; plastic (SOT146).

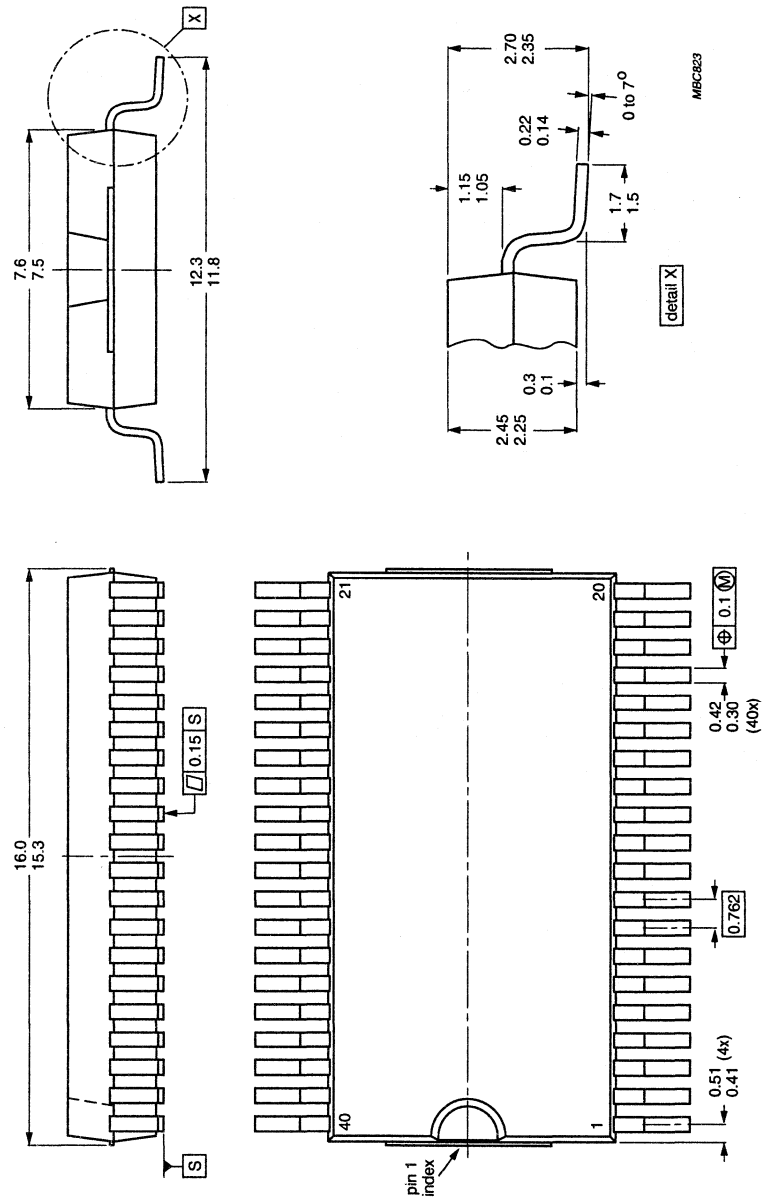
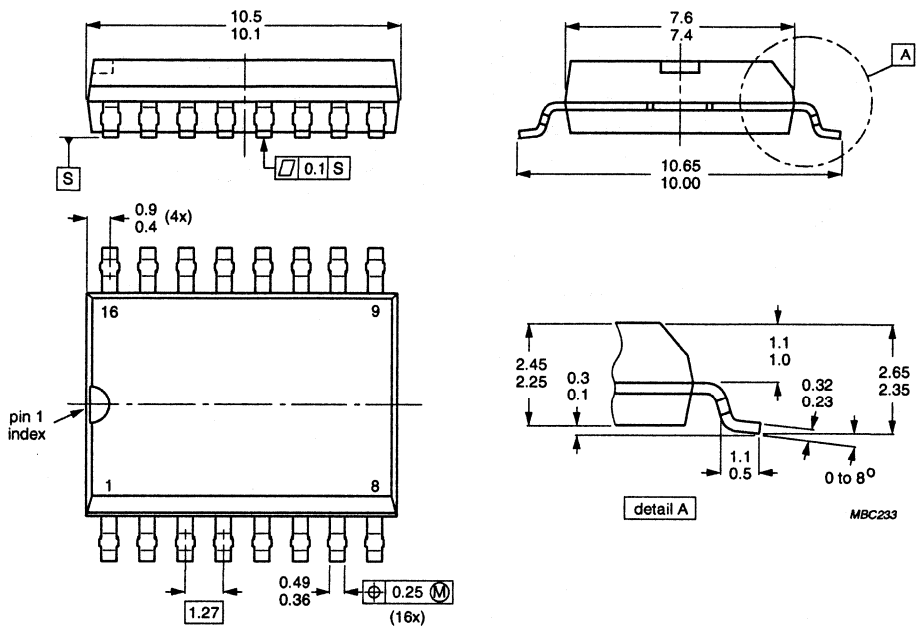


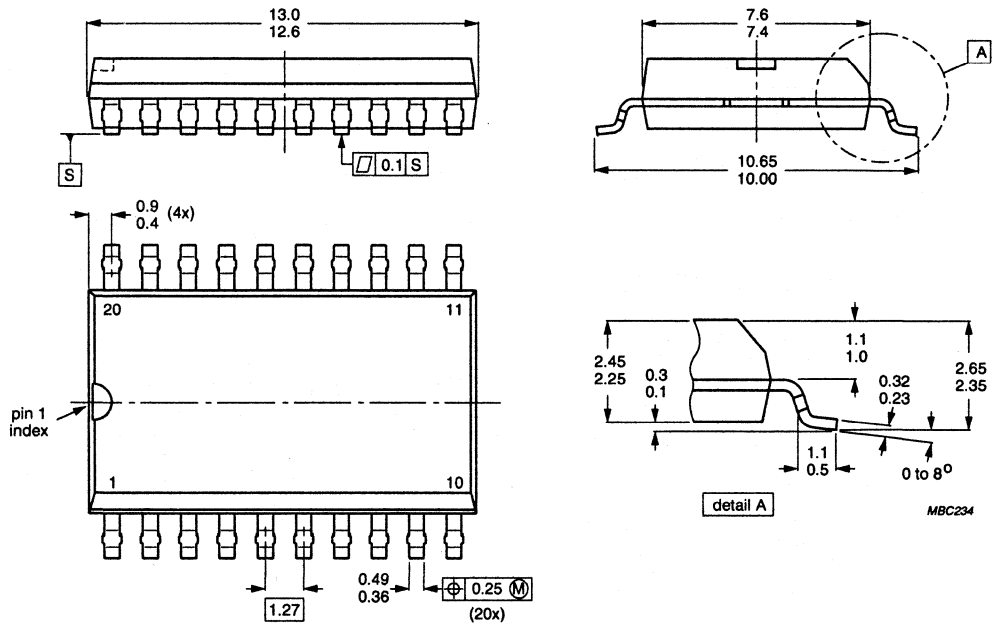
Fig.48 40-lead mini-pack; plastic (VSO40; SOT158A).

Dimensions in mm.



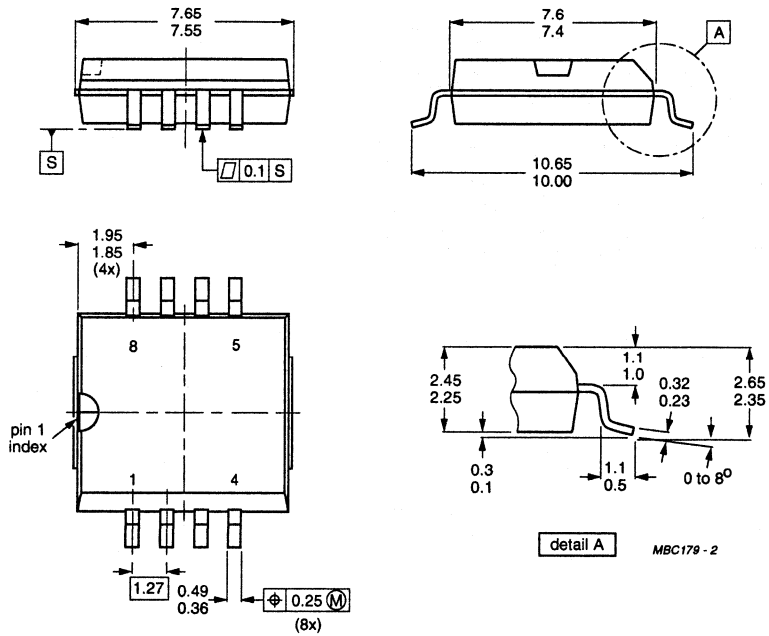
Dimensions in mm.

Fig.49 16-lead mini-pack; (SO16L; SOT162A).



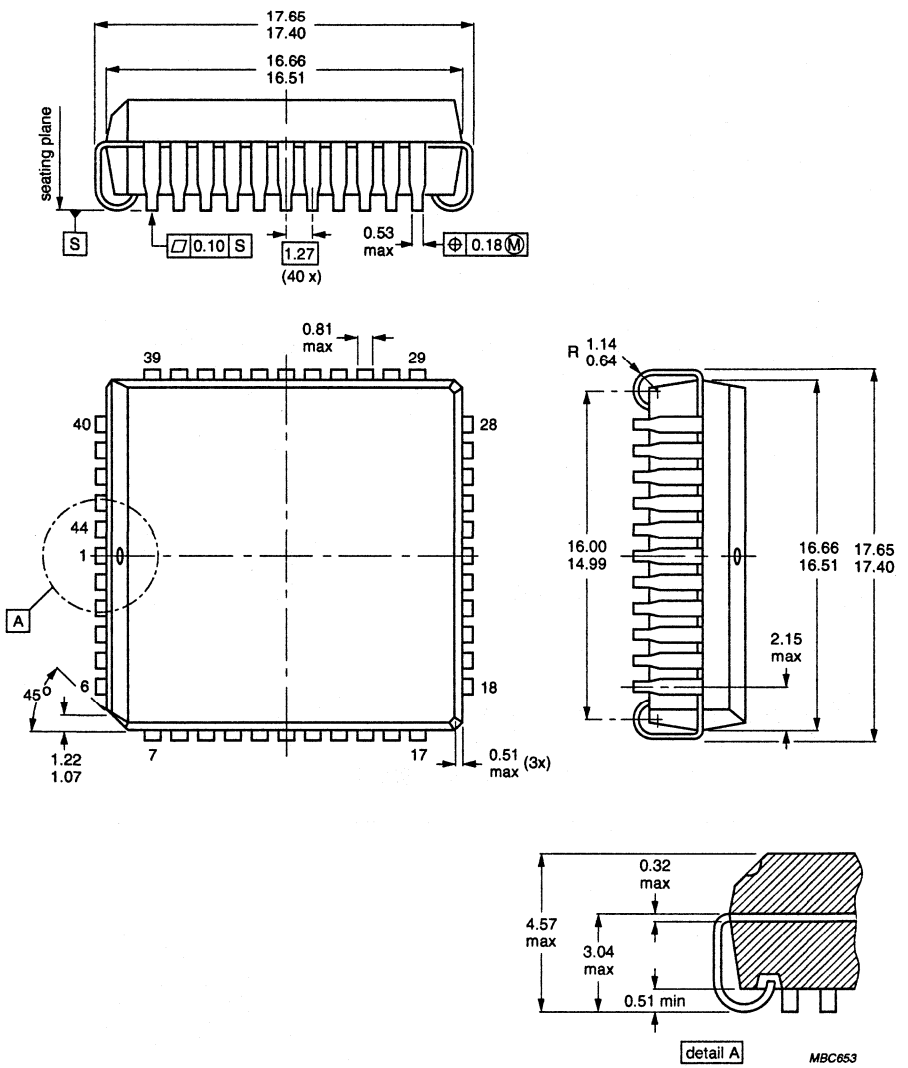
Dimensions in mm.

Fig.50 20-lead mini-pack; plastic (SO20L; SOT163A).



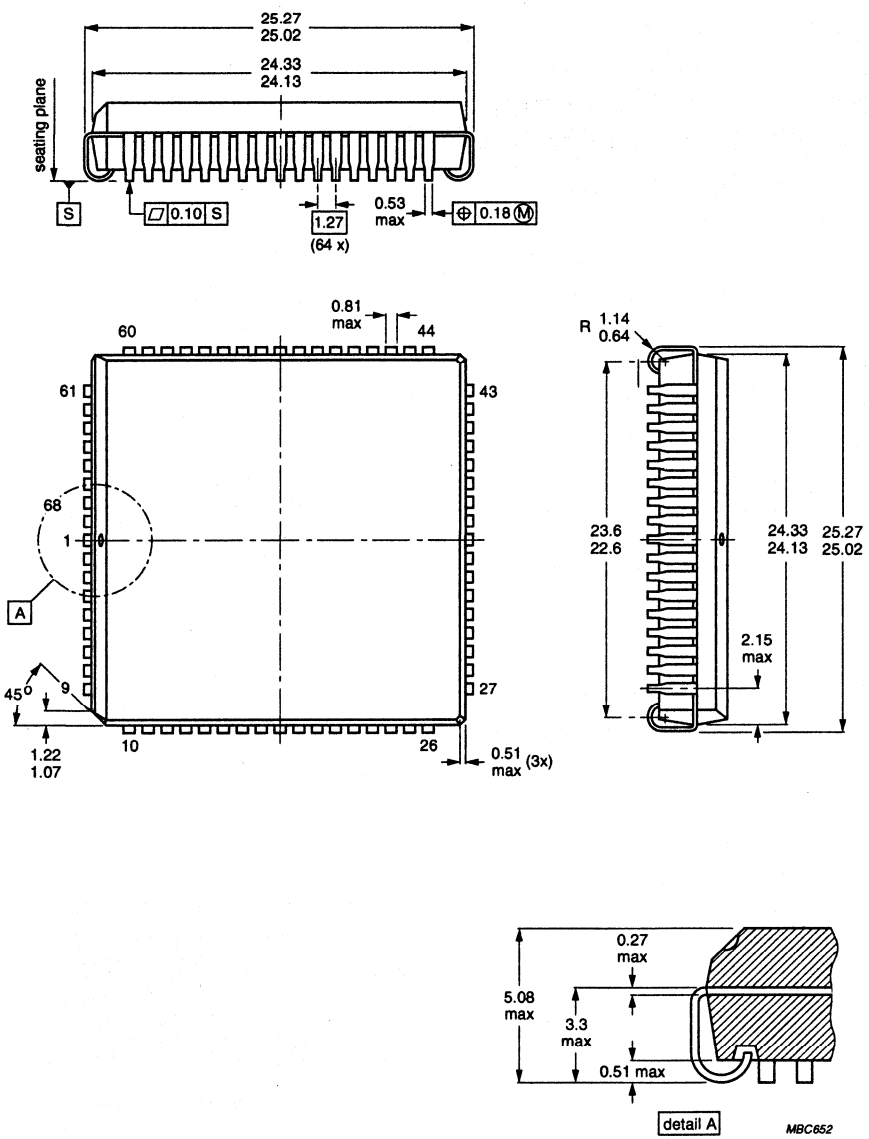
Dimensions in mm.

Fig.51 8-lead mini-pack; plastic (SO8L; SOT176C).



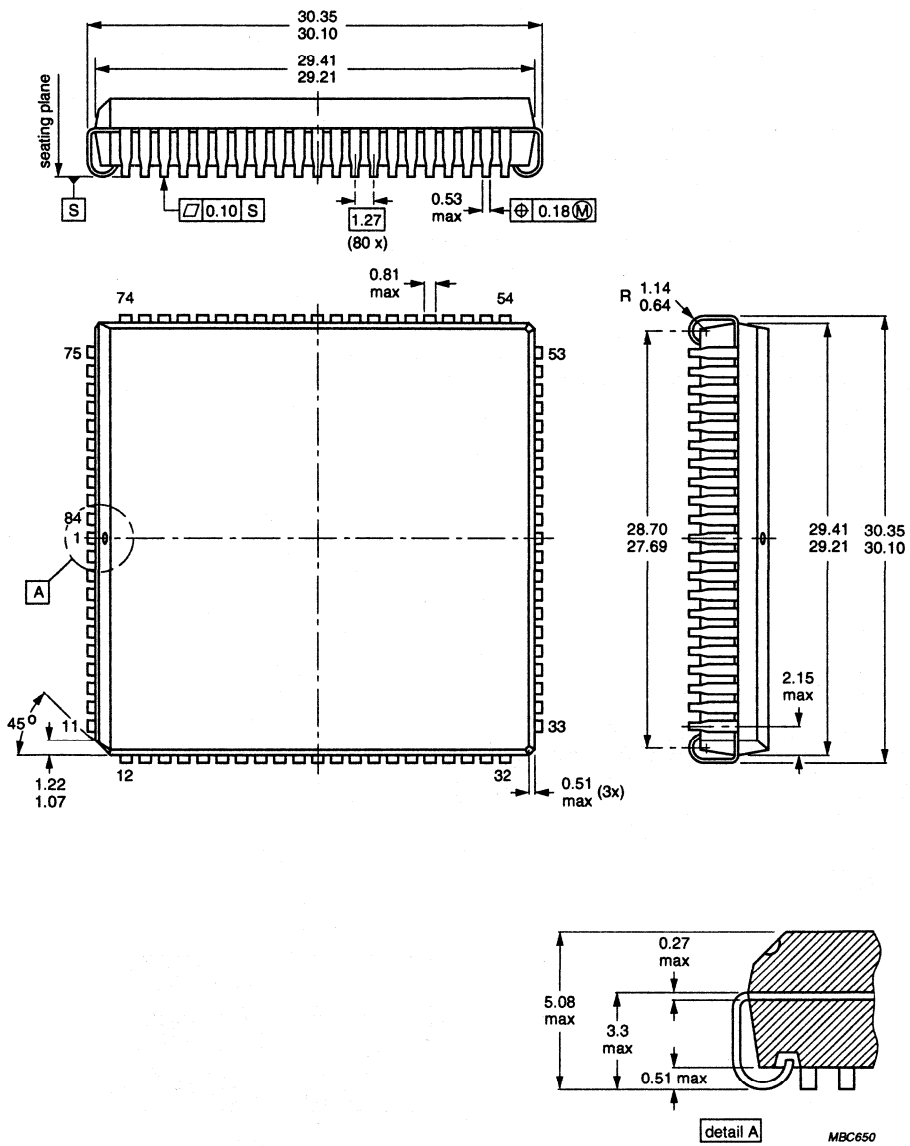
Dimensions in mm.

Fig.52 44-lead plastic leaded chip carrier (PLCC) (SOT187CG).



Dimensions in mm.

Fig.53 68-lead plastic leaded chip carrier (PLCC) (SOT188CG).



Dimensions in mm.

Fig.54 84-lead plastic leaded chip carrier (PLCC) (SOT189AG).

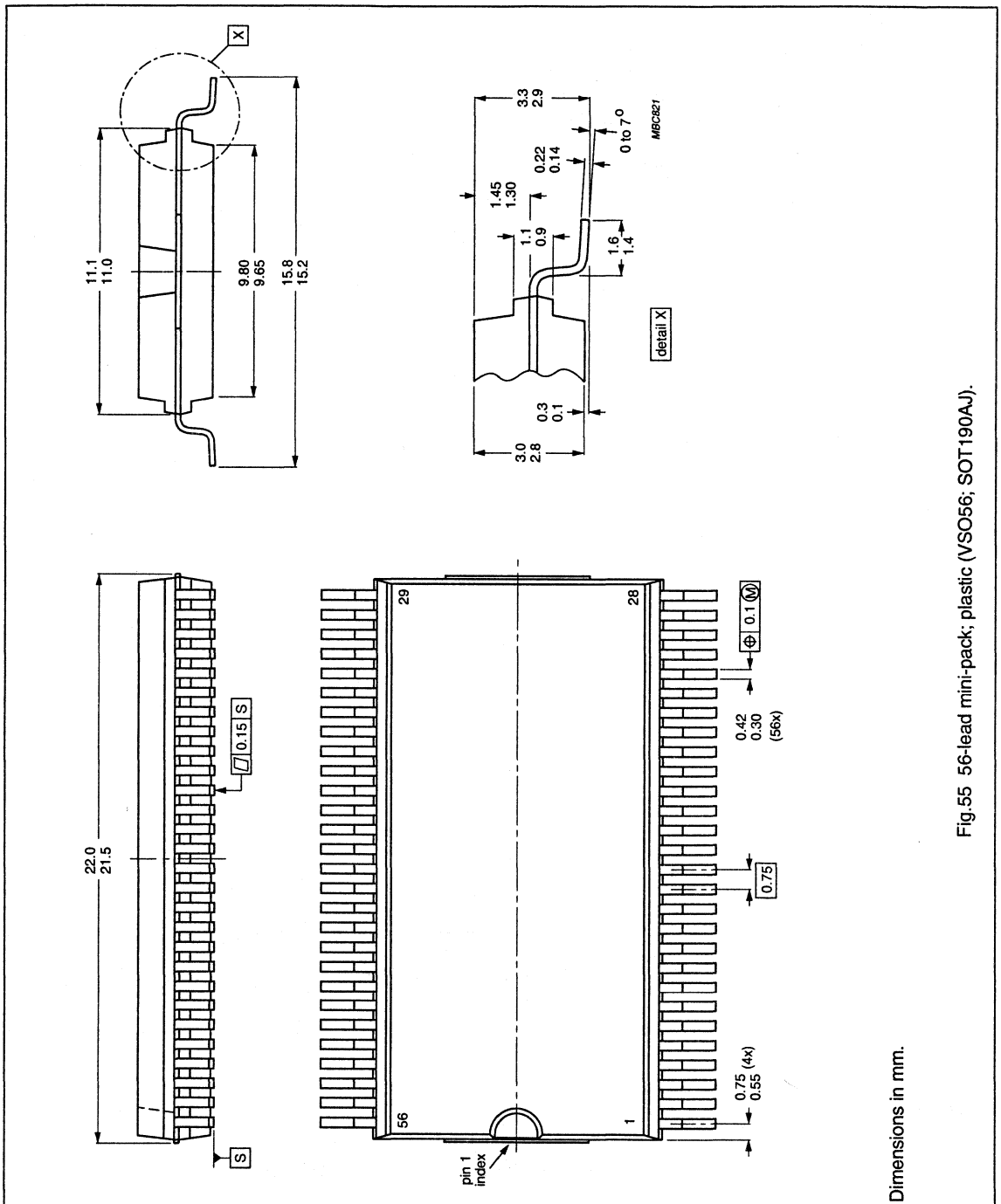
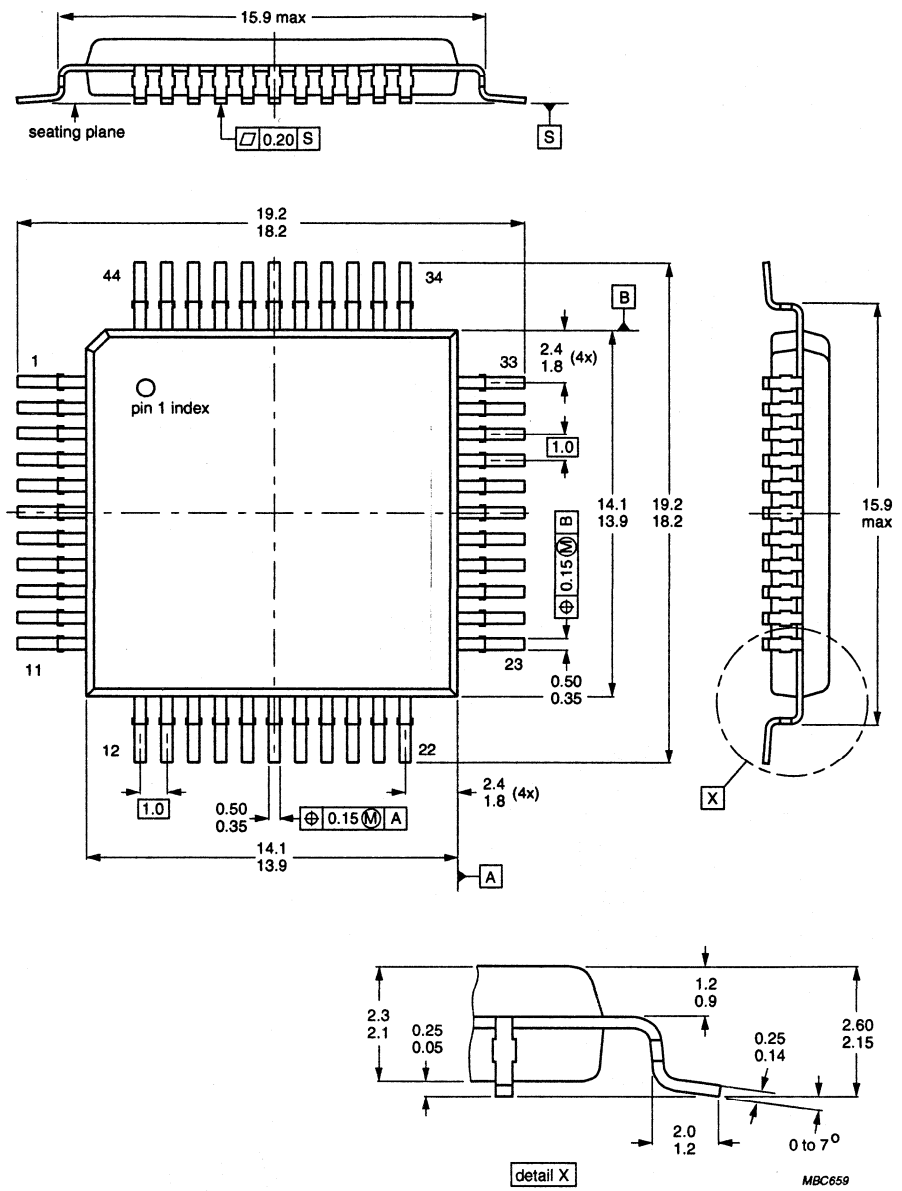


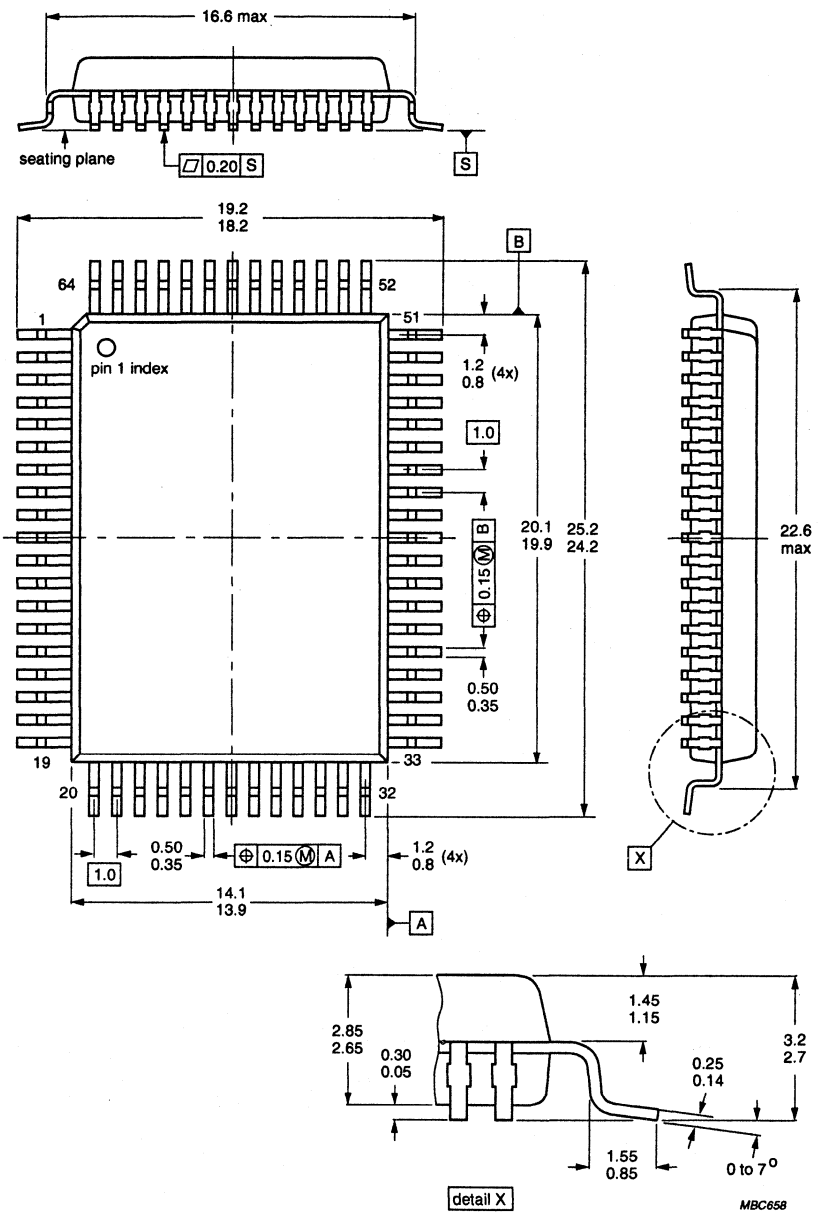
Fig.55 56-lead mini-pack; plastic (VSO56; SOT190AJ).

Dimensions in mm.



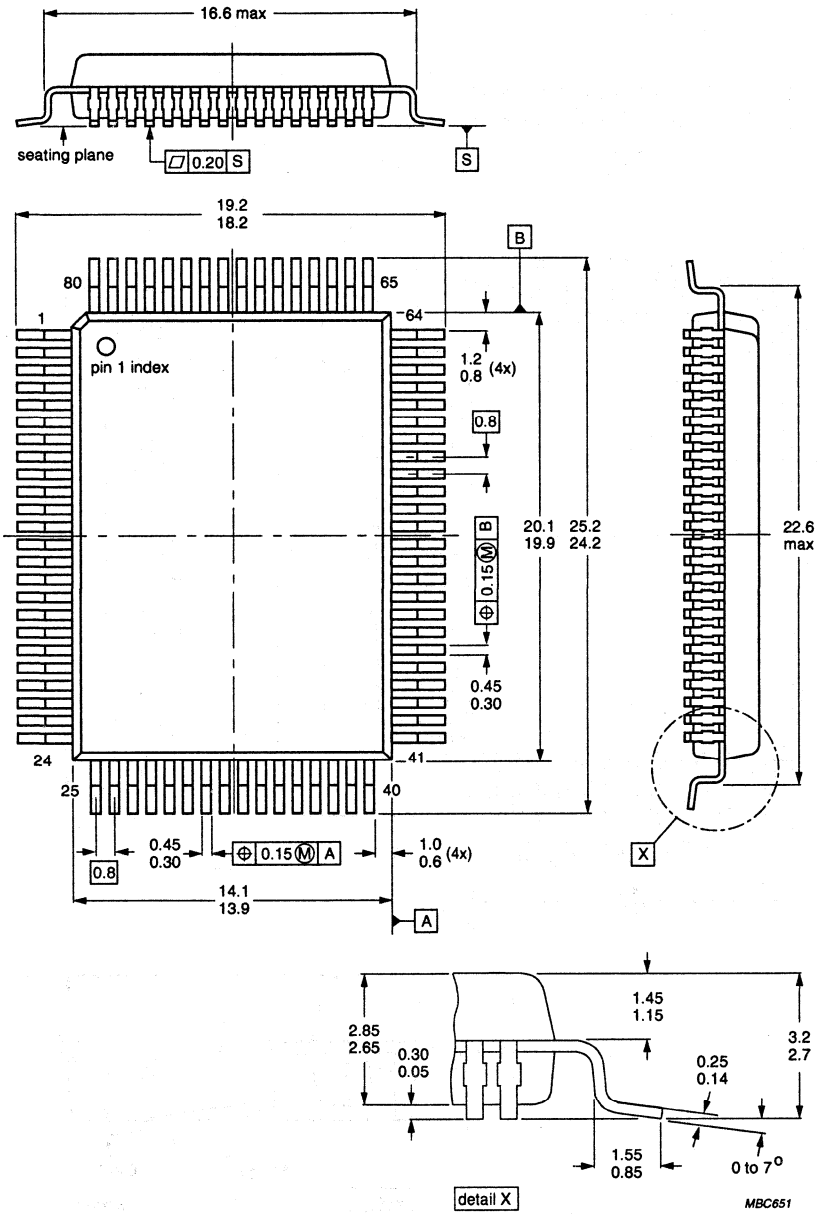
Dimensions in mm.

Fig.56 44-lead quad flat-pack 14 mm square; plastic (SOT205AG).



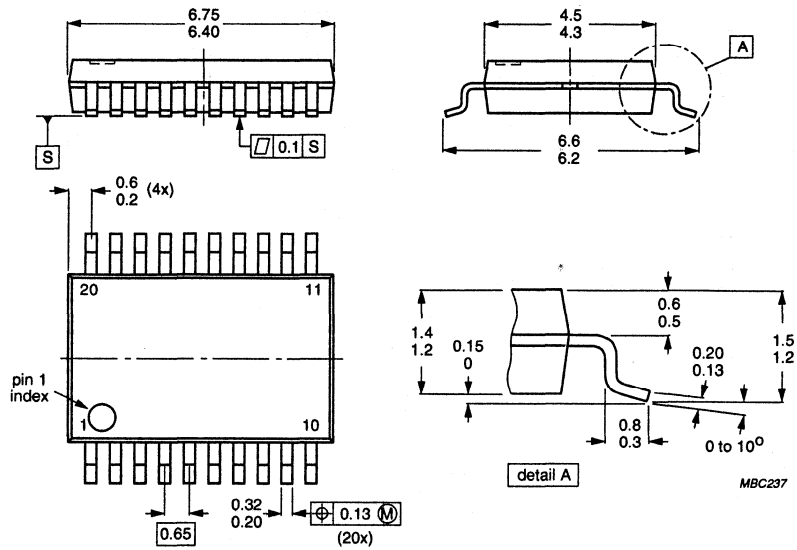
Dimensions in mm.

Fig.57 64-lead quad flat-pack rectangular; plastic (SOT208A).



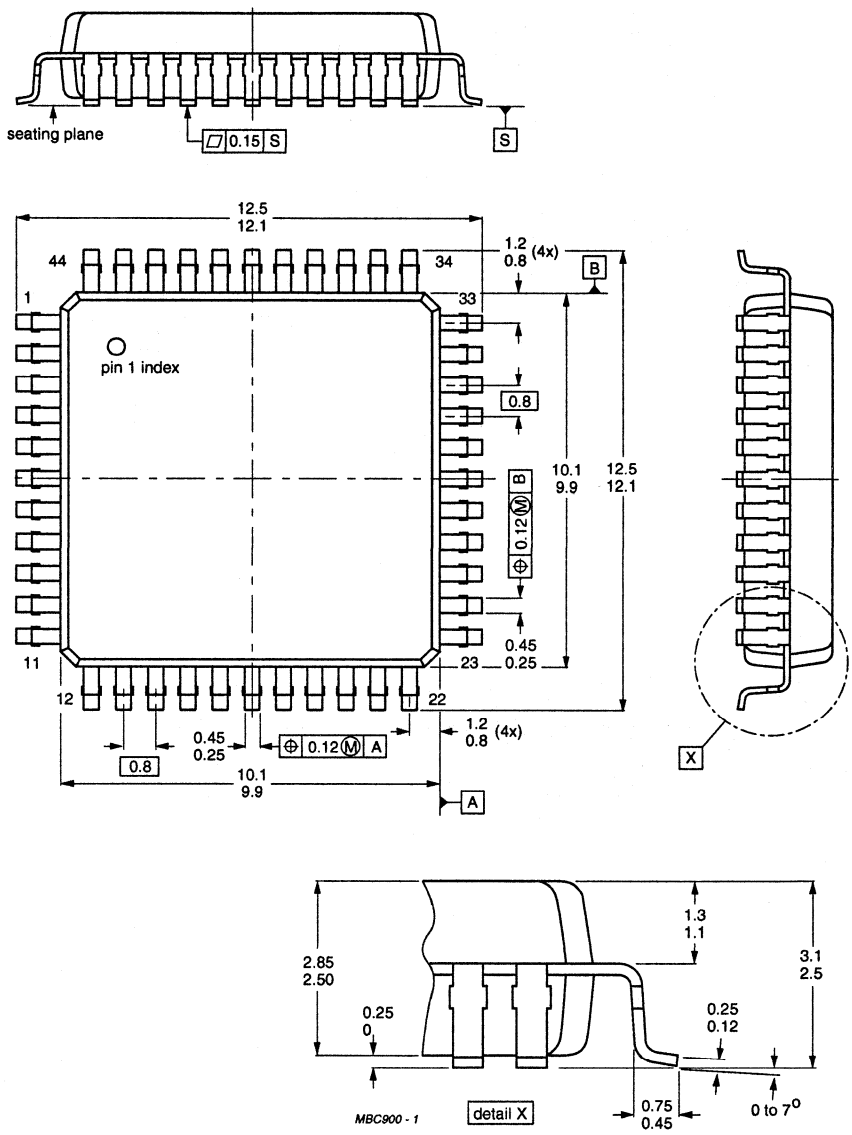
Dimensions in mm.

Fig.58 80-lead quad flat-pack; plastic (SOT219).



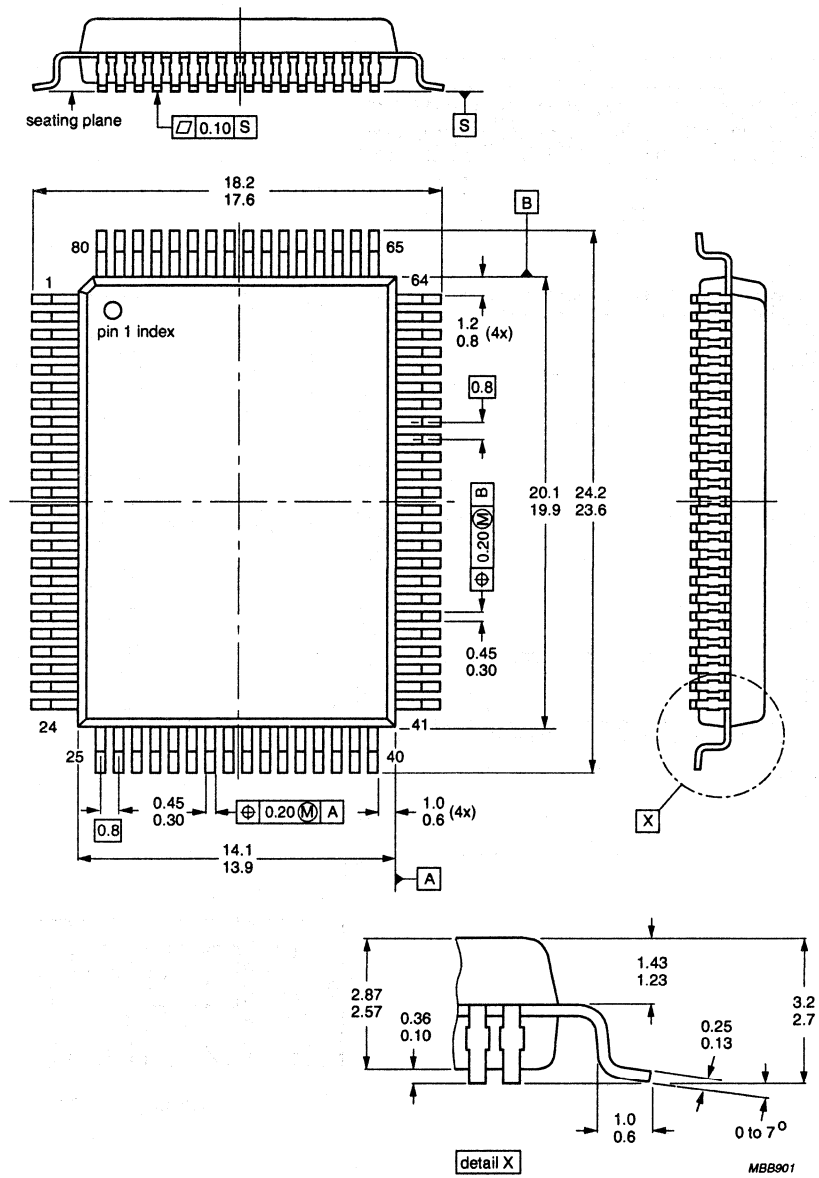
Dimensions in mm.

Fig.59 20-lead shrink dual in-line; plastic (SSOP20; SOT266A).



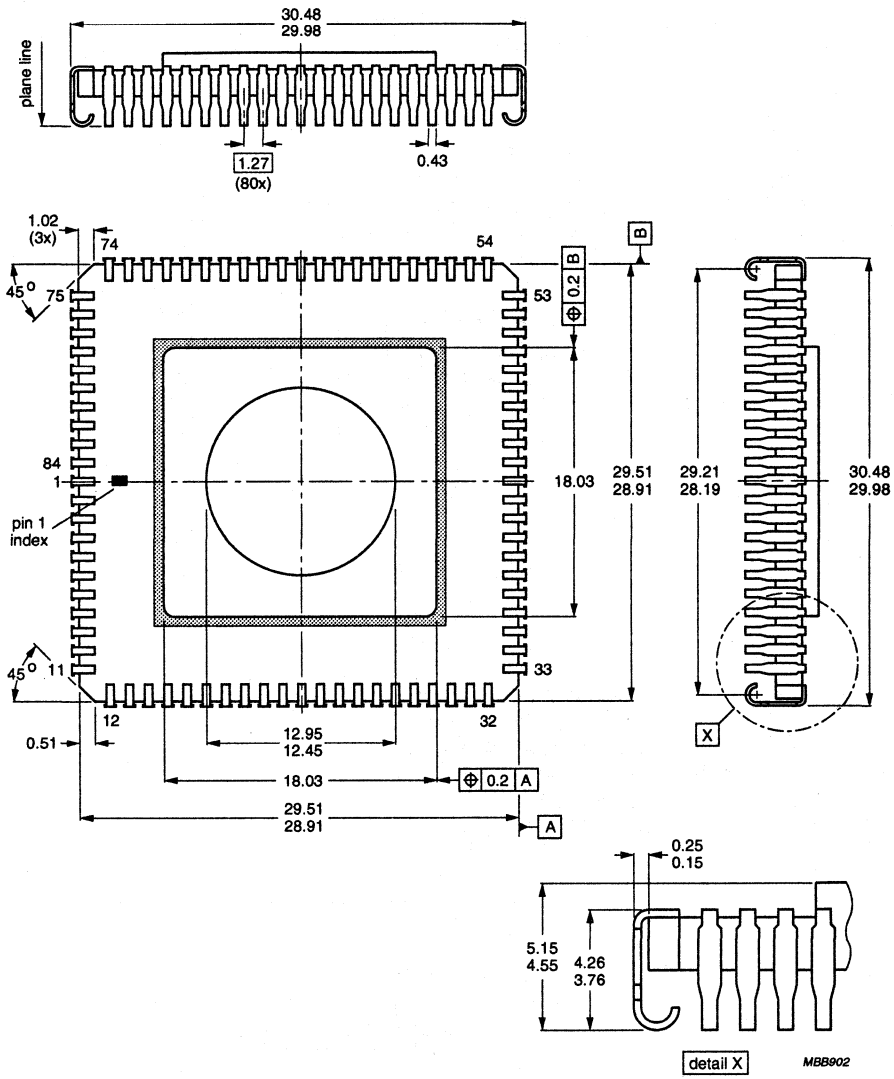
Dimensions in mm.

Fig.60 44-lead quad flat-pack 10 mm square; plastic (QFP44S10; SOT311A).



Dimensions in mm.

Fig.61 80-lead quad flat-pack; plastic (QFP80; SOT318).



Dimensions in mm.

Fig.62 80-lead ceramic quad K-pack (N0331B).

SOLDERING

Plastic mini-packs, PLCC and QFP

BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

SOLDERING

Plastic dual in-line packages

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C, it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

SOLDERING

Tab modules

FLUXING

Use a flux that does not have to be removed, or a water-soluble flux.

SOLDERING

The reflow soldering method using a pulse-heated tool is usually suitable. Limit the soldering operation to 3 s at 250 °C at the leads.

CLEANING

Avoid cleaning if possible. If cleaning is necessary, use cold or hot water. A detergent may be added to the water. Finally rinse with de-ionized water.

Do **not** use ultrasonic cleaning methods as these may damage the inner or outer leads.

Do **not** use solvents.

DATA HANDBOOK SYSTEM

Data handbook system

DATA HANDBOOK SYSTEM

Philips Semiconductors data handbooks contain all pertinent data available at the time of publication and each is revised and reissued regularly.

Loose data sheets are sent to subscribers to keep them up-to-date on additions or alterations made during the lifetime of a data handbook.

Catalogues are available for selected product ranges (some catalogues are also on floppy discs).

Our data handbook titles are listed here.

Integrated circuits

Book	*Title*
IC01	Semiconductors for Radio and Audio Systems
IC02	Semiconductors for Television and Video Systems
IC03	Semiconductors for Telecom Systems
IC04	CMOS HE4000B Logic Family
IC05	Advanced Low-power Schottky (ALS) Logic Series
IC06	High-speed CMOS Logic Family
IC08	100K ECL Logic Family
IC10	Memories
IC11	General-purpose/Linear ICs
IC12	Display Drivers and Microcontroller Peripherals (planned)
IC13	Programmable Logic Devices (PLD)
IC14	8048-based 8-bit Microcontrollers
IC15	FAST TTL Logic Series
IC16	ICs for Clocks and Watches
IC18	Semiconductors for In-car Electronics and General Industrial Applications (planned)
IC19	Semiconductors for Datacom: LANs, UARTs, Multi-protocol Controllers and Fibre Optics
IC20	8051-based 8-bit Microcontrollers
IC21	68000-based 16-bit Microcontrollers (planned)
IC22	ICs for Multi-media Systems
IC23	QUBIC Advanced BiCMOS Interface Logic ABT, MULTIBYTE™
IC24	Low Voltage CMOS Logic

Discrete semiconductors

Book	*Title*
SC01	Diodes
SC02	Power Diodes
SC03	Thyristors and Triacs
SC04	Small-signal Transistors
SC05	Low-frequency Power Transistors and Hybrid IC Power Modules
SC06	High-voltage and Switching NPN Power Transistors
SC07	Small-signal Field-effect Transistors
SC08a	RF Power Bipolar Transistors
SC08b	RF Power MOS Transistors
SC09	RF Power Modules
SC10	Surface Mounted Semiconductors
SC13	PowerMOS Transistors
SC14	RF Wideband Transistors, Video Transistors and Modules
SC15	Microwave Transistors
SC16	Wideband Hybrid IC Modules
SC17	Semiconductor Sensors

Professional components

PC01	High-power Klystrons and Accessories
PC06	Circulators and Isolators

MORE INFORMATION FROM PHILIPS SEMICONDUCTORS?

For more information about Philips Semiconductors data handbooks, catalogues and subscriptions contact your nearest Philips Semiconductors national organization, select from the **address list on the back cover of this handbook**. Product specialists are at your service and enquiries are answered promptly.

Data handbook system

OVERVIEW OF PHILIPS COMPONENTS DATA HANDBOOKS

Our sister product division, Philips Components, also has a comprehensive data handbook system to support their products. Their data handbook titles are listed here.

Display components

Book	*Title*
DC01	Colour Display Components Colour TV Picture Tubes and Assemblies Colour Monitor Tube Assemblies
DC02	Monochrome Monitor Tubes and Deflection Units
DC03	Television Tuners, Coaxial Aerial Input Assemblies
DC05	Flyback Transformers, Mains Transformers and General-purpose FXC Assemblies

Liquid crystal displays

LCD01	Liquid Crystal Displays and Driver ICs for LCDs

Magnetic products

MA01	Soft Ferrites
MA03	Piezoelectric Ceramics Specialty Ferrites

Passive components

PA01	Electrolytic Capacitors
PA02	Varistors, Thermistors and Sensors
PA03	Potentiometers and Switches
PA04	Variable Capacitors
PA05	Film Capacitors
PA06	Ceramic Capacitors
PA07	Quartz Crystals for Special and Industrial Applications
PA08	Fixed Resistors
PA10	Quartz Crystals for Automotive and Standard Applications
PA11	Quartz Oscillators

Professional components

PC04	Photo Multipliers
PC05	Plumbicon Camera Tubes and Accessories
PC07	Vidicon and Newvicon Camera Tubes and Deflection Units
PC08	Image Intensifiers
PC09	Dry-reed Switches
PC12	Electron Multipliers

MORE INFORMATION FROM PHILIPS COMPONENTS?

For more information contact your nearest Philips Components national organization shown in the following list.

Argentina: BUENOS AIRES, Tel. (541)541 4261, Fax. (541)786 7635.
Australia: NORTH RYDE, Tel. (02)805 4455, Fax. (02)805 4466.
Austria: WIEN, Tel. (01)60101 1820, Fax. (01)60101 1210.
Belgium: BRUXELLES, Tel. (02)741 8211, Fax. (02)735 8667.
Brazil: SÃO PAULO, Tel. (011)829 1166, Fax. (011)829 1849.
Canada: SCARBOROUGH, Tel. (416)292 5161, Fax. (416)754 6248.
Chile: SANTIAGO, Tel. (02)773 816, Fax. (02)5602 735 3594.
China (Peoples Republic of): SHANGHAI, Tel. (021)3264140, Fax. (021)3202160.
Colombia: BOGOTA, Tel. (01)249 7624, Fax. (01)261 0139.
Denmark: COPENHAGEN, Tel. (032)883 333, Fax. (031)571 949.
Finland: ESPOO, Tel. (9)0-50261, Fax. (9)0-520971.
France: ISSY-LES-MOULINEAUX, Tel. (01)4093 8000, Fax. (01)4093 8127.
Germany: HAMBURG, Tel. (040)3296-0, Fax. (040)3296 216.
Greece: TAVROS, Tel. (01)489 4339/(01)489 4911, Fax. (01)481 5180.
Hong Kong: KWAI CHUNG, Tel. (852)724 5121, Fax. (852)480 6960.
India: BOMBAY, Tel. (022)493 8541, Fax. (022)494 1595.
Indonesia: JAKARTA, Tel. (021)5201122, Fax. (021)5205189.
Ireland: DUBLIN, Tel. (01)693 355, Fax. (01)640 210.
Italy: MILANO, Tel. (02)6752.1, Fax. (02)6752 3300.
Japan: TOKIO, Tel. (03)3740 5143, Fax. (03)3740 5035.
Korea (Republic of): SEOUL, Tel. (02)794-5011, Fax. (02)798-8022.
Malaysia: KUALA LUMPUR, Tel. (03)757 5511, Fax. (03)757 4880.
Mexico: CHI HUA HUA, Tel. (016)18-67-01/(016)18-67-02, Fax. (016)778 0551.
Netherlands: EINDHOVEN, Tel. (040)7 83749, Fax. (040)7 88399.
New Zealand: AUCKLAND, Tel. (09)849-4160, Fax. (09)849-7811.
Norway: OSLO, Tel. (02)74 8000, Fax. (02)74 8341.
Pakistan: KARACHI, Tel.(021)577 032, Fax. (021)569 1832.
Peru: LIMA, Tel. (014)350 059, Fax. (014)468 949.
Philippines: MANILA, Tel. (02)810-0161, Fax. (02)817-3474.
Portugal: LISBOA, Tel. (01)388 3121, Fax. (01)388 3208.
Singapore: SINGAPORE, Tel. (65)350 2000, Fax. (65)355 1758.
South Africa: JOHANNESBURG, Tel. (011)470-5434, Fax. (011)470-5494.
Spain: BARCELONA, Tel. (03)301 6312, Fax. (03)301 4243.
Sweden: STOCKHOLM, Tel. (0)8-782 1000, Fax. (0)8-782 9002.
Switzerland: ZÜRICH, Tel. (01)488 2211, Fax. (01)481 7730.
Taiwan: TAIPEI, Tel. (2)509 7666, Fax. (2)500 5912.
Thailand: BANGKOK, Tel. (2)399-3280 to 9, (2)398-2083, Fax. (2)398-2080.
Turkey: ISTANBUL, Tel. (01)279 2770, Fax. (01)269 3094.
United Kingdom: LONDON, Tel. (071)580 6633, Fax. (071)636 0394.
United States: RIVIERA BEACH, Tel.(800)447-3762/(407)881 3200, Fax. (407)881 3300.
Uruguay: MONTEVIDEO, Tel. (02)704 044, Fax. (02)920 601.
Venezuela: CARACAS, Tel. (02)241 7509, Fax. (02)951 7339.
For all other countries apply to: **Philips Components,**
Marketing Communications, Building BAE,
P.O. Box 218, 5600 MD, EINDHOVEN, The Netherlands
Telex 35000 phtcnl, Fax. +31-40-724547.

NOTES

Philips Semiconductors – a worldwide company

Argentina IEROD, Av. Juràmento 1991 - 14.B, (1428) BUENOS AIRES, Tel. (541)541 4261/541 4106, Fax. (541)786 7635

Australia 34 Waterloo Road, NORTH RYDE, NSW 2113, Tel. (02)805 4455, Fax. (02)805 4466

Austria Triester Str. 64, 1101 WIEN, Tel. (01)60 101-1236, Fax. (01)60 101-1210

Belgium 80 Rue Des Deux Gares, B-1070 BRUXELLES, Tel. (02)525 6111, Fax. (02)525 7246

Brazil Rua do Rocia 220 - 5th floor, CEP:04552-000-SÃO PAULO-SP, Brazil. P.O. Box 7383-CEP:01051. Tel. (011)829-1166, Fax. (011)829-1849

Canada INTEGRATED CIRCUITS: Tel. (800)234-7381, Fax. (708)296-8556 DISCRETE SEMICONDUCTORS: 601 Milner Ave, SCARBOROUGH, ONTARIO, M1B 1M8, Tel. (0416)292 5161 ext. 2336, Fax. (0416)292 4477

Chile Av. Santa Maria 0760, SANTIAGO, Tel. (02)773 816, Fax. (02)777 6730

Colombia Carrera 21 No. 56-17, BOGOTA, D.E., P.O. Box 77621, Tel. (01)249 7624, Fax. (01)217 4549

Denmark Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S, Tel. (032)88 2636, Fax. (031)57 1949

Finland Sinikalliontie 3, SF-02630 ESPOO, Tel. (9)0-50261, Fax. (9)0-520971

France 117 Quai du Président Roosevelt, 92134 ISSY-LES-MOULINEAUX Cedex, Tel. (01)4093 8000, Fax. (01)4093 8127

Germany Burchardstrasse 19, D-2 HAMBURG 1, Tel. (040)3296-0, Fax. (040)3296 213

Greece No. 15, 25th March Street, GR 17778 TAVROS, Tel. (01)4894 339/4894 911, Fax. (01)4814 240

Hong Kong 15/F Philips Ind. Bldg., 24-28 Kung Yip St., KWAI CHUNG, Tel. (0)4245 121, Fax. (0)4806 960

India PEICO ELECTRONICS & ELECTRICALS Ltd., Components Dept., Shivsagar Estate, Block 'A', Dr. Annie Besant Rd., Worli, BOMBAY-400 018, Tel. (022)4938 541, Fax. (022)4941 595

Indonesia Philips House, Jalan H.R. Rasuna Said Kav. 3-4, P.O. Box 4252, JAKARTA 12950, Tel. (021)5201 122, Fax. (021)5205 189

Ireland Newstead, Clonskeagh, DUBLIN 14, Tel. (01)640 000, Fax. (01)640 200

Italy V. Le F. Testi, 327, 20162-MILANO, Tel. (02)6752.1, Fax. (02)6752.3350

Japan Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKIO 108, Tel. (03)3740 5101, Fax. (03)3740 0570

Korea (Republic of) Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL, Tel. (02)794-5011, Fax. (02)798-8022

Malaysia No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR, Tel. (03)7755 1088, Fax. (03)757 4880

Mexico Philips Components, 6D Founder Blvd., EL PASO, TX 79906, Tel. 9-5(800)234-7381, Fax. (708)296-8556

Netherlands Postbus 90050, 5600 PB EINDHOVEN, Tel. (040)78 37 49, Fax. (040)78 83 99

New Zealand 2 Wagener Place, C.P.O. Box 1041, AUCKLAND, Tel. (09)849-4160, Fax. (09)849-7811

Norway Box 1, Manglerud 0612, OSLO, Tel. (02)74 8000, Fax. (02)74 8341

Pakistan Philips Markaz, M.A. Jinnah Rd., KARACHI-3, Tel. (021)577 039, Fax. (021)569 1832

Peru Carretera Central 6.500, LIMA 3, Apartado 5612, Tel. (014)350 059, Fax. (014)468 999/468 949

Philippines PHILIPS SEMICONDUCTORS PHILIPPINES Inc, 106 Valero St. Salcedo Village, P.O. Box 911, MAKATI, Metro MANILA, Tel. (02)810 0161, Fax. (02)817 3474

Portugal Av. Eng. Duarte Pacheco 6, 1009 LISBOA Codex, Tel. (01)683 121, Fax. (01)658 013

Singapore Lorong 1, Toa Payoh, SINGAPORE 1231, Tel. (65)350 2000, Fax. (65)251 6500

South Africa 195-215 Main Road, Martindale, P.O. Box 7430, JOHANNESBURG 2000, Tel. (011)470-5433, Fax. (011)470-5494

Spain Balmes 22, 08007 BARCELONA, Tel. (03)301 6312, Fax. (03)301 4243

Sweden Tegeluddsvägen 1, S-11584 STOCKHOLM, Tel. (0)8-782 1000, Fax. (0)8-782 9002

Switzerland Allmendstrasse 140-142, CH-8027 ZÜRICH, Tel. (01)488 2211, Fax. (01)482 8595

Taiwan 69, Min Sheng East Road, Sec 3, P.O. Box 22978, TAIPEI, Tel. (2)509 7666, Fax. (2)500 5899

Thailand PHILIPS ELECTRONICS (THAILAND) Ltd., 60/14 MOO 11, Bangna - Trad Road Km. 3 Prakanong, BANGKOK 10260, Tel. (2)399-3280 to 9, (2)398-2083, Fax. (2)398-2080

Turkey Talatpasa Cad. No. 5, 80640 LEVENT/ISTANBUL, Tel. (01)279 2770, Fax. (01)269 3094

United Kingdom Philips Semiconductors Limited, P.O. Box 65, Philips House, Torrington Place, LONDON, WC1E 7HD, Tel. (071)436 41 44, Fax. (071)323 03 42

United States INTEGRATED CIRCUITS: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409, Tel. (800)234-7381, Fax. (708)296-8556 DISCRETE SEMICONDUCTORS: 2001 West Blue Heron Blvd., P.O. Box 10330, RIVIERA BEACH, FLORIDA 33404, Tel. (800)447-3762 and (407)881-3200, Fax. (407)881-3300

Uruguay Coronel Mora 433, MONTEVIDEO, Tel. (02)70-4044, Fax. (02)92 0601

Venezuela Calle 6, Ed. Las Tres Jotas, CARACAS, 1074A, App. Post. 78117, Tel. (02)241-7509, Fax. (02)241 4518

For all other countries apply to: Philips Semiconductors, International Marketing and Sales, Building BAF-1, P.O. Box 218, 5600 MD, EINDHOVEN, The Netherlands, Telex 35000 phtcnl, Fax. +31-40-724825

SCD16

Printed in The Netherlands Date of release: 03-'93 9398 652 36011

Philips Semiconductors

PHILIPS

PHILIPS